Full-Bridge Single-Inductor-Based Buck–Boost Inverters

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***Abstract*—The output voltage of renewable energy sources is influenced by environmental conditions. To compensate for the variations of voltage, a buck–boost power conditioning system can be used. This article presents a full-bridge single-inductor-based buck–boost inverter. Its output voltage can be greater or lower than the input voltage depending on the controllable duty ratio. This inverter features bidirectional and reactive power flow operations with no high-frequency common-mode voltage. The unique feature of the proposed inverter is using a single inductor in the power train, which enhances the power density. Moreover, only two switches can operate at high frequency. This enables the inverter to be made with the high efficiency and simple circuit configuration. Based on the proposed full-bridge inverter, a novel cascaded buck–boost inverter is also presented. It retains all the benefits of the proposed full-bridge inverter. The theoretical analysis of the proposed full-bridge inverter is first explained in detail. It is then extended to a cascaded inverter. Thereafter, the practical effectiveness of the proposed inverters is verified with the experimental tests by implementing the hardware prototypes of 110 V_{rms}, 60 Hz, and 500 W for full-bridge single-inductor-based buck–boost inverter, and 220 V_{rms}, 60 Hz, and 1000 W for the cascaded inverter.**

***Index Terms*—Buck–boost inverter, efficiency, full-bridge, power density, single inductor.**

I. Introduction

MANY renewable energy sources (RESs) require power inverters when they are connected to the grid. In general, they can be classified as the voltage source inverter (VSI) or current source inverter (CSI) [1]–[3]. The full-bridge VSI is shown in Fig. 1(a). It is a step-down inverter with the output peak voltage, which is always lower than the input voltage. The full-bridge CSI is shown in Fig. 1(b). It is a step-up inverter with the output peak voltage, which is always higher than the input voltage.

The output voltage of RESs is greatly influenced by environmental conditions. Thus, to compensate for the variations of voltage, the inverter system must make the buck–boost operation. To deal with this, a boost dc–dc converter is cascaded with a VSI, as shown in Fig. 2. It provides a boost function, and the VSI provides a buck function. Similarly, buck dc–dc converter is cascaded with a CSI, as shown in Fig. 3, where the buck dc–dc converter provides a buck operation, and the CSI provides a boost operation. However, they require multiple inductors and capacitors in two high-frequency stages, and they might have the high-frequency common-mode voltage. Also, the inverting and noninverting buck–boost dc–dc converters cascaded with an unfolding circuit [4], [6] are shown in Figs. 4 and 5, respectively. The dc–dc converter generates a rectified dc voltage, and the unfolding circuit converts it to a sinusoidal output voltage [4]–[6]. The unfolding circuit operates at line-frequency, and therefore, it results in negligible switching loss. However, they are the unity power factor inverters. Also, they cause zero-crossing distortion while requiring multiple inductors. In [6] and [7], the modified inverters are proposed by removing the capacitor $C_{\rm dc}$ and the

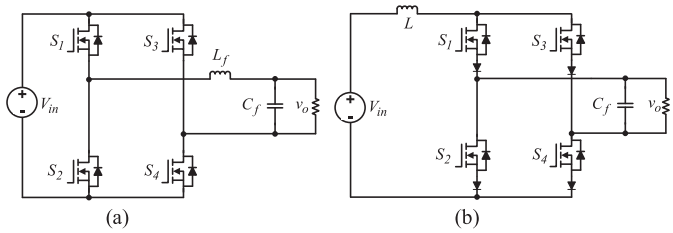

Fig. 1. Full-bridge inverters. (a) Single-phase VSI. (b) Single-phase CSI.

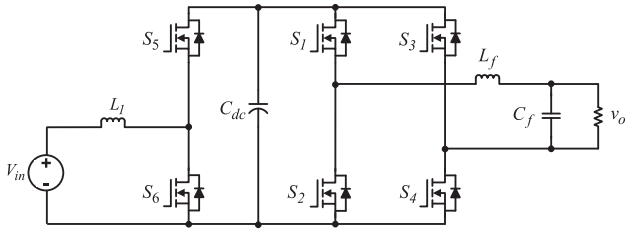

Fig. 2. Boost dc–dc converter cascaded with a VSI.

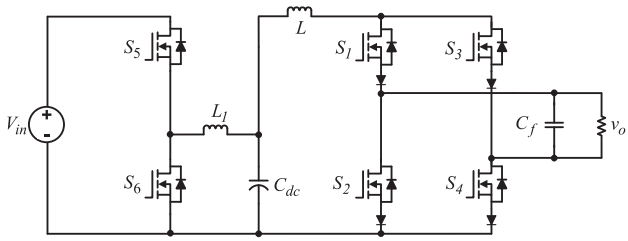

Fig. 3. Buck dc–dc converter cascaded with a CSI.

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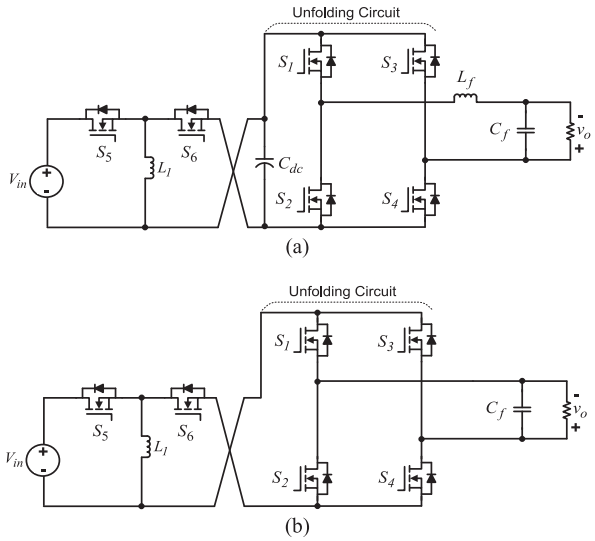

Fig. 4. Unity power factor inverting buck–boost dc–dc converter cascaded with an unfolding circuit. (a) Conventional [4]. (b) Presented in [7].

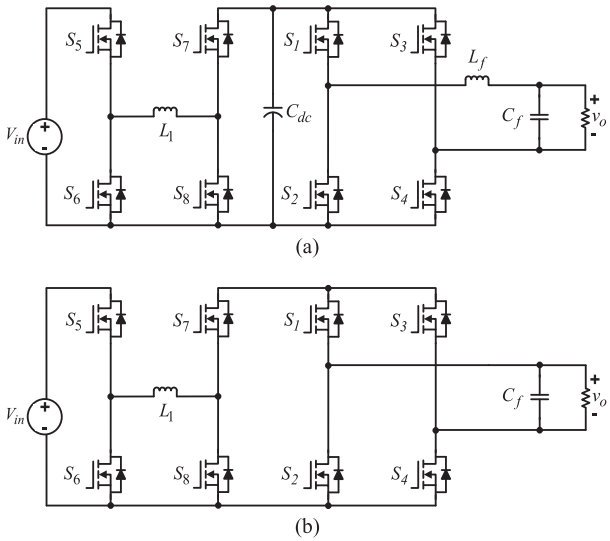

Fig. 5. Unity power factor noninverting buck–boost dc–dc converter cascaded with an unfolding circuit. (a) Conventional [4]. (b) Presented in [7].

output filter inductor L_f in Figs. 4(a) and 5(a), as shown in Figs. 4(b) and 5(b). However, they are the unity power factor inverters. Also, they can cause zero-crossing distortion in light load.

The differential boost inverter combined with two boost dc–dc converters [8], [9] provides a buck–boost operation in a single stage. However, it still requires multiple inductors and capacitors. The Z-source inverter implemented with impedance network and the full-bridge circuit provides a buck–boost operation in a quasi-single stage [10], [11]. It has no shoot-through issues while providing high efficiency and reliability. However, it requires more passive components, which three inductors and two energy storing capacitors. The dual-buck type of inverters in [12]–[14] provide buck–boost operation in a single stage. Like the Z-source inverter, they have no shoot-through issues, and

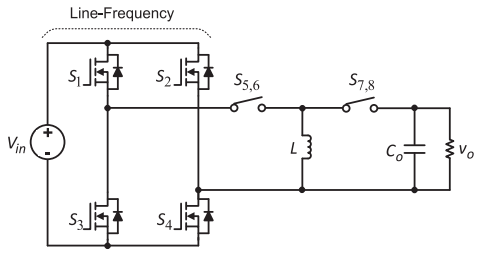

Fig. 6. Proposed full-bridge single-inductor-based buck–boost inverter with reactive power flow capability.

they can be designed by switches without any careful consideration of their reverse recovery characteristics. However, they still require many passive components. The inverters in [15]–[18] are designed with two unidirectional inverting or noninverting buck–boost converters. However, they always provide the unity power factor without controlling the reactive power. Also, even though they provide a buck–boost operation in a single stage, they require two voltage sources [15]–[19] and more passive components.

This article proposes the new full-bridge single-inductor-based buck–boost inverter, as shown in Fig. 6. It provides a buck–boost dc–ac operation in a single stage. In particular, it has only a single inductor. This enables to improve the power density and decrease the control complexity. Moreover, the proposed buck–boost inverter is bidirectional, and it can control the reactive power. In addition, it has no high-frequency common-mode voltage [20], [21]. Also, because it has only two switches working at high frequency at a time, the switching loss can be reduced. The detailed analysis of proposed inverter is given in Section II.

The proposed inverter is then extended into a new type of cascaded buck–boost inverter for the integration of various energy sources, as shown in Fig. 7. It generates a high output voltage with low input voltage. It retains all the benefits of the proposed full-bridge inverter, such as single inductor, only two high-frequency switches, no high-frequency common-mode voltage, and reactive power flow support.

II. Circuit Topology and Operation Analysis

A. Circuit Topology

As shown in the circuit topology of Fig. 6, it consists of four unidirectional switches $S_1 - S_4$, two bidirectional switches $S_{5,6}$ and $S_{7,8}$, one inductor L, and one output filtering capacitor C_o. Note that the bidirectional switches can be implemented in several ways, as shown in Fig. 8. In this study, $S_{5,6}$ and $S_{7,8}$ are implemented by the common source back-to-back metal–oxide–semiconductor field-effect transistors (mosfets), as shown in Fig. 9.

B. Modulation Strategy

The modulation strategy of the proposed buck–boost inverter is shown in Fig. 10. It is known that the switches S_1, S_2, S_3, and S_4 operate at line frequency. Thus, their switching losses

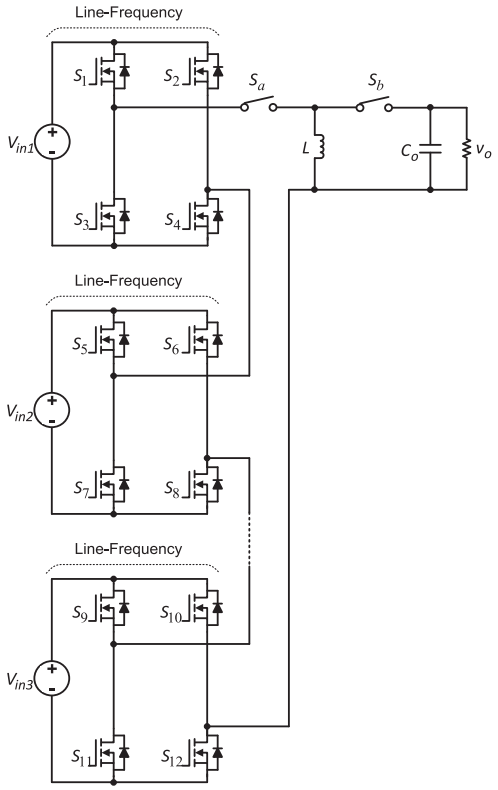

Fig. 7. Proposed cascaded single-inductor-based buck–boost inverter.

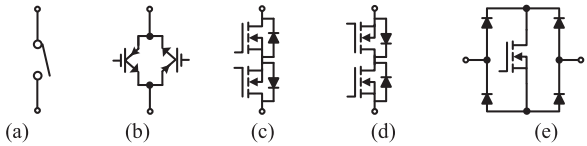

Fig. 8. Implementation of bidirectional switch. (a) Symbol. (b) Antiparallel connected reverse current blocking insulated gate bipolar transistors (IGBTs). (c) Common source back-to-back MOSFETs. (d) Common drain back-to-back MOSFETs. (e) Diode bridge.

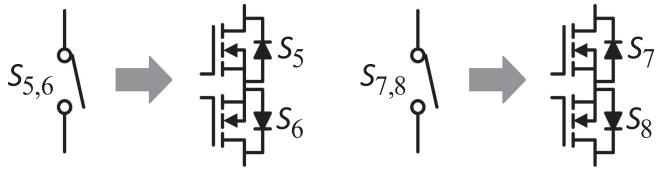

Fig. 9. Implementation of bidirectional switches used in this study.

are negligible. The other switches $S_{5,6}$ and $S_{7,8}$ operate at high frequency only for half-cycle of the output voltage.

From Fig. 10, for $v_o > 0$, S_2, S_3, S_5, and S_7 are ON. In contrast, S_1 and S_4 are OFF. On the other hand, S_6 and S_8 are switching complementarily with the dead time. Similarly, for $v_o < 0$, S_1, S_4, S_6, and S_8 are ON. S_2 and S_3 are OFF. S_5 and S_7 are switching complementarily with the dead time. The equivalent circuits of the proposed inverter for $v_o > 0$ and $v_o < 0$ are shown in Figs. 11 and 12, respectively.

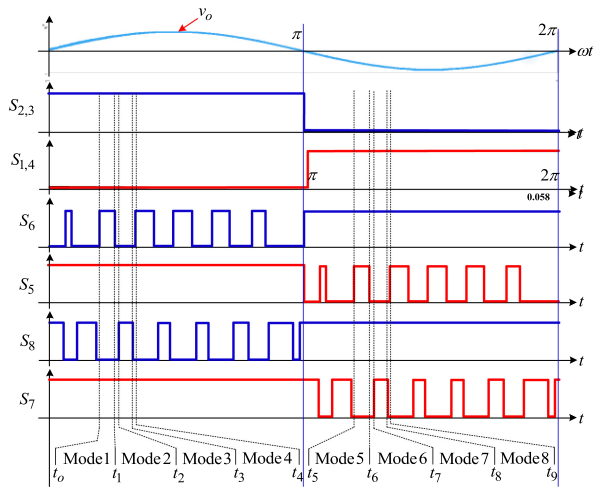

Fig. 10. Modulation strategy of the proposed full-bridge inverter.

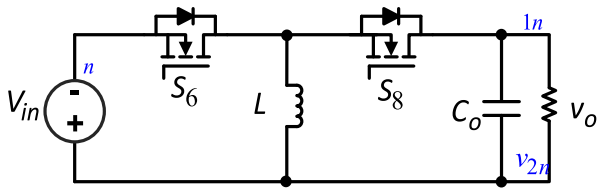

Fig. 11. Equivalent circuit of the proposed inverter for positive half-cycle of v_o.

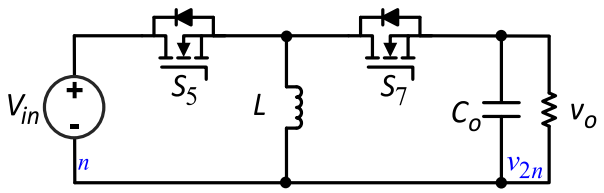

Fig. 12. Equivalent circuit of the proposed inverter for negative half-cycle of v_o.

C. Operation Modes

The proposed inverter has eight operating modes. The operating modes 1–4 are for $v_o > 0$ and modes 5–8 are for $v_o < 0$.

1) Mode-1: This mode is shown in Fig. 13(a). The switch S_6 is ON, and S_8 is OFF. The inductor current i_L rises linearly with the slope of V_{in}/L

$$\begin{cases} v_L = V_{\text{in}} \\ i_{C_o} = -i_0 \end{cases} \tag{1}$$

where i_o is the output current and i_{C_o} is the capacitor current.

2) Mode-2: This mode is shown in Fig. 13(b). Switches S_6 and S_8 are OFF. i_L decreases linearly with the slope of $-v_o/L$ through S_7 and the body diode of S_8

$$\begin{cases} v_L = -v_0 \\ i_{C_o} = i_L - i_o\,. \end{cases} \tag{2}$$

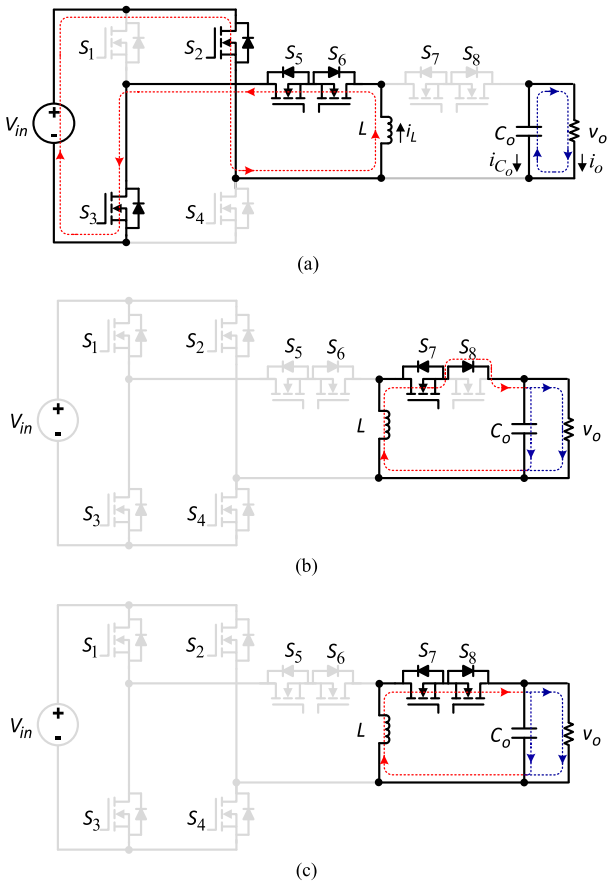

Fig. 13. Operating modes of the proposed full-bridge inverter for the positive half-cycle of the output voltage. (a) Mode-1. (b) Mode-2 and mode-4. (c) Mode-3.

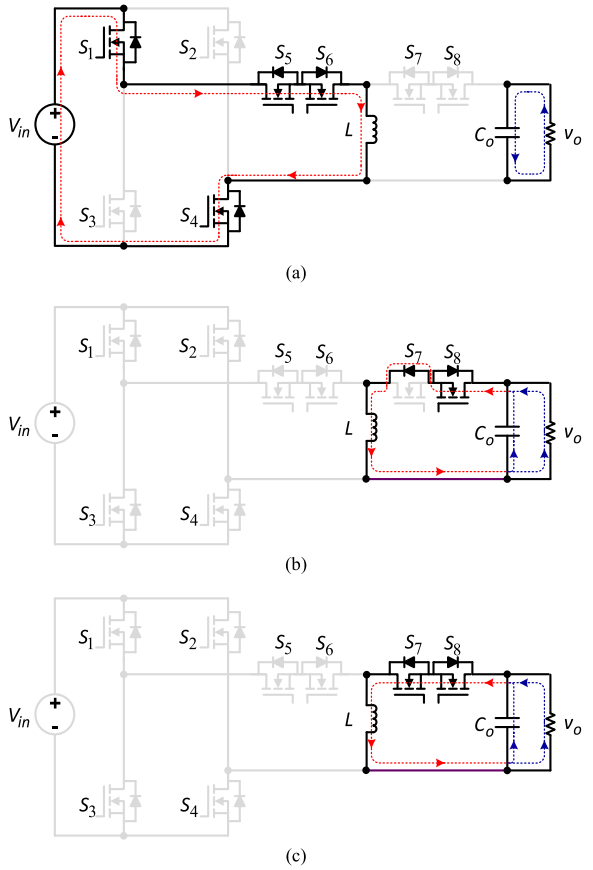

Fig. 14. Operating modes of the proposed full-bridge inverter for the negative half-cycle of the output voltage. (a) Mode-5. (b) Mode-6 and mode-8. (3) Mode-7.

3) Mode-3: This mode is shown in Fig. 13(c). S_6 is OFF and S_8 is ON. v_L is still equal to $-v_o$. And, i_L continues to decrease with the slope of $-v_o/L$ through S_7 and S_8. v_L and i_{C_o} are the same as in (2).
4) Mode-4: This mode is the same as mode-2.
5) Mode-5: This mode is shown in Fig. 14(a). S_5 is ON and S_7 is OFF. v_L becomes equal to $-V_{\text{in}}$, and i_L increases linearly with the slope of V_{in}/L

$$\begin{cases} v_{\text{L}} = -V_{\text{in}} \\ i_{C_o} = i_0. \end{cases} \tag{3}$$

6) Mode-6: This mode is shown in Fig. 14(b). S_5 and S_7 are OFF. The value of v_L is v_o, and i_L decreases linearly with the slope of v_o/L through S_8 and the body diode of S_7

$$\begin{cases} v_L = v_0 \\ i_{C_o} = -i_L + i_o. \end{cases} \tag{4}$$

7) Mode-7: This mode is shown in Fig. 14(c). S_5 is OFF and S_7 is ON. v_L is still equal to v_o, and i_L continues to decrease with the slope v_o/L through S_7 and S_8. v_L and i_{C_o} are the same as in (2).
8) Mode-8: This mode is the same as mode-6.

D. Control Signal Generation

Assume that V_o is the peak value of the output voltage v_o, $d_{S6}(t)$ is the duty ratio of switch S_6 for $v_o > 0$, and $d_{S5}(t)$ is the duty ratio of switch S_5 for $v_o < 0$. Using the volt–sec balance condition on the inductor and (1) and (2), we obtain

$$V_o \sin(\omega t) = \frac{d_{S6}(t)}{1 - d_{S6}(t)} V_{\text{in}}, \qquad 0 \le \omega t < \pi. \tag{5}$$

Similarly, by using the volt–sec balance condition on the inductor and (3) and (4), we obtain

$$V_o \sin(\omega t - \pi) = \frac{d_{S5}(t)}{1 - d_{S5}(t)} V_{\text{in}}, \qquad \pi \le \omega t \le 2\pi. \tag{6}$$

From (5), $d_{S6}(t)$ can be obtained as

$$d_{S6}(t) = \frac{V_o \sin(\omega t)}{V_o \sin(\omega t) + V_{\text{in}}}, \quad 0 \le \omega t < \pi. \tag{7}$$

From (6), $d_{S5}(t)$ can be obtained as

$$d_{S5}(t) = \frac{V_o \sin(\omega t - \pi)}{V_o \sin(\omega t - \pi) + V_{\text{in}}}, \quad \pi \le \omega t \le 2\pi. \tag{8}$$

The maximum voltage gain G of the inverter in a line-frequency cycle is the ratio of peak output voltage to input

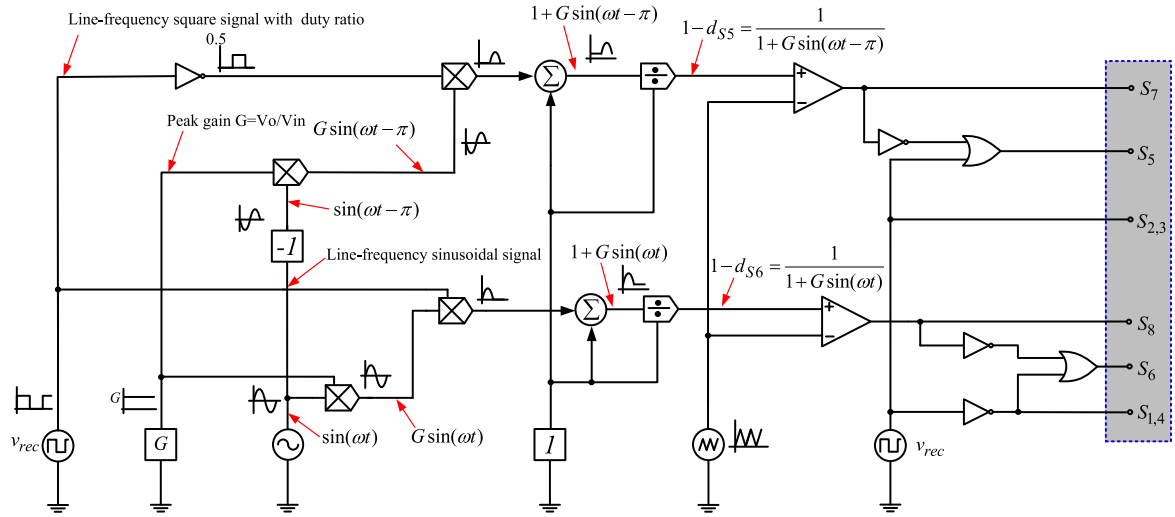

Fig. 15. Block diagram of the control signal generation.

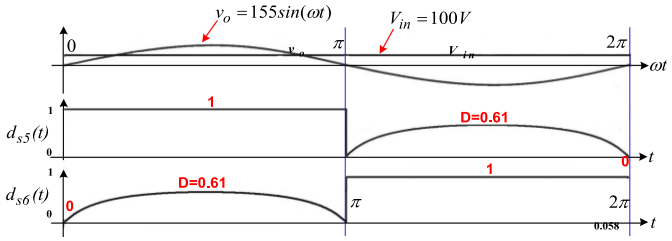

Fig. 16. Design example of duty ratios.

voltage

$$G = \frac{V_o}{V_{\text{in}}}. \tag{9}$$

By putting (9) in (7) and (8) we obtain

$$d_{S6}(t) = \frac{G\sin(\omega t)}{G\sin(\omega t)+1},\ 0 \le \omega t < \pi \tag{10}$$

$$d_{S5}(t) = \frac{G\sin(\omega t-\pi)}{G\sin(\omega t-\pi)+1},\ \pi \le \omega t \le 2\pi. \tag{11}$$

The maximum duty ratio D in a line-frequency cycle occurs at the positive or negative peak of v_o. Thus, D can be obtained as in (12) for $\sin(\omega t) = 1$ in (7), and $\sin(\omega t - \pi) = 1$ in (8)

$$D = \frac{G}{G+1}. \tag{12}$$

Fig. 15 is the block diagram for the signal generation using (10) and (11). For $V_{\text{in}} = 100$ V and $v_o = 155\ \sin(\omega t)$, duty ratios $d_{S5}(t)$ and $d_{S6}(t)$ are shown in Fig. 16. As shown for $v_o > 0$, $d_{S6}(t)$ varies from 0 at $v_o = 0$, to a maximum value $D = 0.61$ at $v_o = 155$ V. And as v_o decreases from peak value to zero, $d_{S6}(t)$ decreases from 0.61 to 0. For $v_o < 0$, $d_{S5}(t)$ varies from 0 at $v_o = 0$ V, to a maximum value $D = 0.61$ at $v_o = -155$ V. And as v_o decreases from negative peak value to zero, $d_{S5}(t)$ decreases from 0.61 to 0.

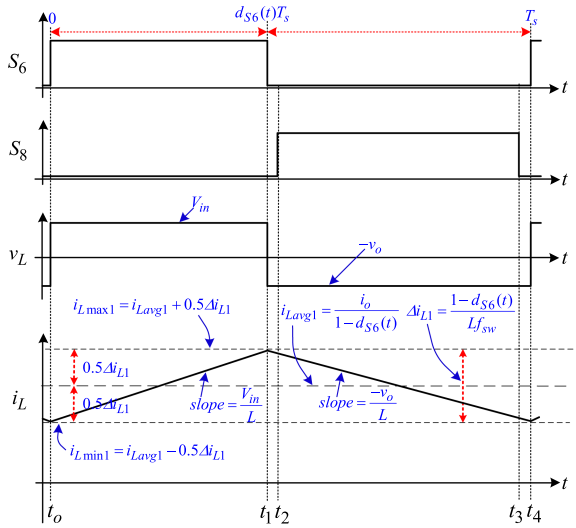

Fig. 17. Inductor voltage and current waveforms for $v_o > 0$.

E. Inductor Current

The fundamental waveforms are shown in Figs. 17 and 18. Using (1)–(4), and the amp–sec balance condition on the output capacitor C_o, we obtain the average inductor currents as

$$\begin{cases} i_{\text{Lavg1}} = \frac{i_o}{1-d_{S6}(t)}, & v_o > 0 \\ i_{\text{Lavg2}} = -\frac{i_o}{1-d_{S5}(t)}, & v_o < 0. \end{cases} \tag{13}$$

Similarly, from (1)–(4) we obtain the inductor current ripple as

$$\begin{cases} \Delta i_{L1} = \frac{1-d_{S6}(t)}{Lf_{sw}} v_o, & v_o > 0 \\ \Delta i_{L2} = -\frac{1-d_{S5}(t)}{Lf_{sw}} v_o, & v_o < 0 \end{cases} \tag{14}$$

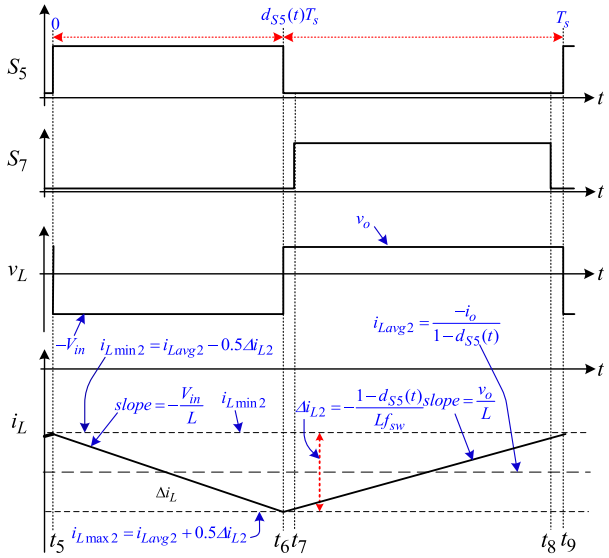

Fig. 18. Inductor voltage and current waveforms for $v_o < 0$.

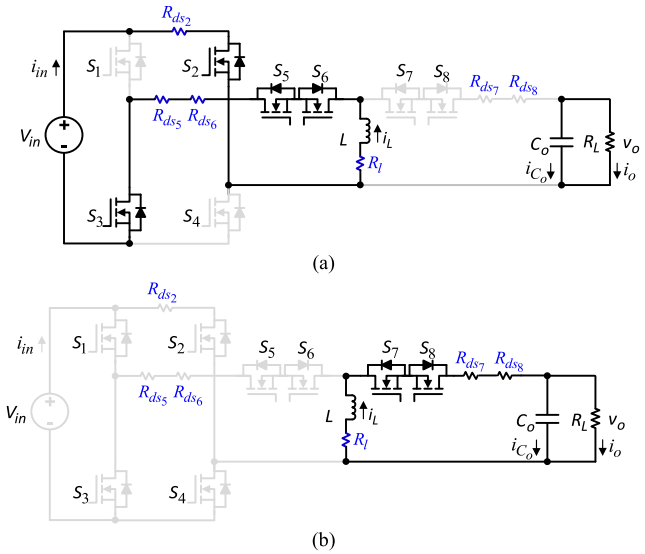

Fig. 19. Equivalent circuits of the proposed full-bridge inverter with parasitic resistances for $v_o > 0$. (a) $d_{S6}T_s$. (b) $(1-d_{S6})T_s$.

where f_{sw} is the switching frequency. The maximum and minimum values of inductor current can be calculated as

$$\begin{cases} i_{L\max 1} = i_{Lavg1} + \frac{\Delta i_{L1}}{2}, & v_o > 0 \\ i_{L\max 2} = i_{Lavg2} + \frac{\Delta i_{L2}}{2}, & v_o < 0 \end{cases} \tag{15}$$

$$\begin{cases} i_{L\min 1} = i_{Lavg1} - \frac{\Delta i_{L1}}{2}, & v_o > 0 \\ i_{L\min 2} = i_{Lavg2} - \frac{\Delta i_{L2}}{2}, & v_o < 0. \end{cases} \tag{16}$$

Then, the instantaneous inductor current for $v_o > 0$ is given as follows.

1) Mode-1, $t_o \le t \le t_1$: From Fig. 17 i_L is

$$i_L = i_{L\min 1} + \frac{V_{\text{in}}}{L} t\,. \tag{17}$$

Using (13)–(15) and (17) gives

$$i_L = \frac{i_o}{1-d_{S6}(t)} - \frac{1-d_{S6}(t)}{2Lf_{sw}} v_o + \frac{V_{\text{in}}}{L} t. \tag{18}$$

2) Mode-2, $t_1 < t \le t_2$: From Fig. 17 i_L is

$$i_L = i_{L\max 1} - \frac{(t-t_1)}{L} v_o. \tag{19}$$

Substituting $t_1 = d_{S6}(t)T_s$, and using (13)–(15) and (19) gives

$$i_L = \frac{i_o}{1-d_{S6}(t)} + \frac{1-d_{S6}(t)}{2Lf_{sw}} v_o - \frac{t-d_{S6}(t)T_s}{L} v_o. \tag{20}$$

3) Mode-3, $t_2 < t \le t_3$: i_L is the same as in (20).

4) Mode-4, $t_3 < t \le t_4$: i_L is the same as in (20).

The instantaneous inductor current for $v_o < 0$ is given as follows.

5) Mode-5, $t_5 \le t \le t_6$: From Fig. 18, i_L is

$$i_L = i_{L\min 2} - \frac{V_{\text{in}}}{L} t. \tag{21}$$

Using (16) in (21), we obtain

$$i_L = \frac{-i_o}{1-d_{S5}(t)} + \frac{1-d_{S5}(t)}{2Lf_{sw}} v_o - \frac{V_{\text{in}}}{L} t. \tag{22}$$

6) Mode-6, $t_6 < t \le t_7$: From Fig. 18, i_L is

$$i_L = i_{L\max 2} + \frac{(t-t_6)}{L} v_o. \tag{23}$$

Substituting $t_6 = d_{S5}(t)T_s$, and using (15) gives

$$i_L = \frac{-i_o}{1-d_{S5}(t)} - \frac{1-d_{S5}(t)}{2Lf_{sw}} v_o + \frac{t-d_{S5}(t)T_s}{L} v_o. \tag{24}$$

7) Mode-7, $t_7 < t \le t_8$: i_L is the same as in (24).

8) Mode-8, $t_8 < t \le t_9$: i_L is the same as in (24).

III. Design of Parameters

The analysis for the positive and negative half-cycles of the output voltage is the same; therefore, only the analysis for the positive half-cycle is presented. Equivalent circuits of the proposed full-bridge inverter with parasitic resistances are shown in Fig. 19. R_{ds_2}, R_{ds_5}, R_{ds_6}, R_{ds_7}, R_{ds_8}, and R_l are the parasitic resistances of S_2, S_5, S_6, S_7, S_8, and L, respectively, and R_L is the load resistance. From Fig. 19(a), we obtain

$$L\frac{di_L(t)}{dt} = V_{\text{in}} - i_L\left(R_{ds_2} + R_{ds_3} + R_{ds_5} + R_{ds_6} + R_l\right). \tag{25}$$

From Fig. 19(b), we obtain

$$L\frac{di_L(t)}{dt} = -v_o - i_L\left(R_{ds_7} + R_{ds_8}\right) \tag{26}$$

$$d_{S6}(t)T_s \times V_{\text{in}} - i_L\left(R_{ds_2} + R_{ds_3} + R_{ds_5} + R_{ds_6} + R_l\right) = \left(1-d_{S6}(t)\right)T_s \times v_o + i_L\left(R_{ds_7} + R_{ds_8}\right) \tag{27}$$

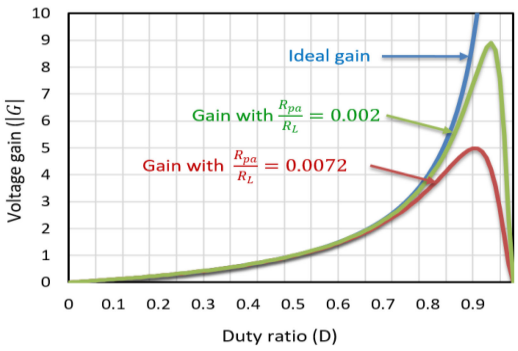

Fig. 20. Voltage gain of proposed buck–boost inverter.

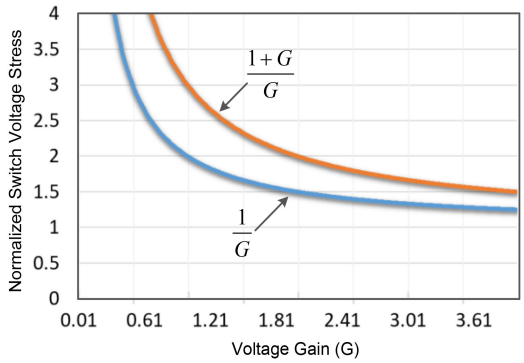

Fig. 21. Voltage stress of switches of the proposed buck–boost inverter.

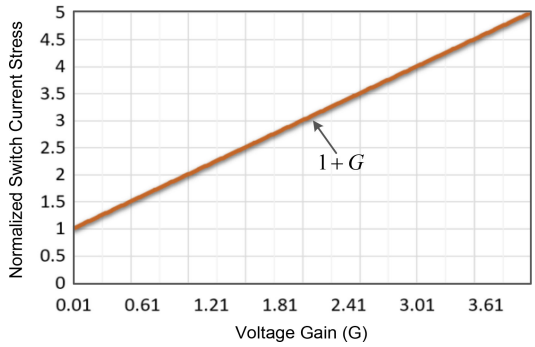

Fig. 22. Current stress of switches of the proposed buck–boost inverter.

$$\frac{v_o}{V_{\text{in}}} = \frac{d_{S6}(t)}{1-d_{S6}(t)}\left[\frac{d_{S6}(t)}{R_L(1-d_{S6}(t))^2}\left[2R_{ds}+R_l+\frac{2R_{ds}}{d_{S6}(t)}\right]+1\right]^{-1}. \tag{29}$$

Using (25) and (26), and the volt–sec balance condition on the inductor, we obtain (27). By using (13) in (27), we derive (28). By assuming the same drain–source conduction resistances for all the switches (R_{ds}), (28) can be expressed as (29). With the new parameter $R_{pa}(= 2R_{ds} + R_l + \frac{2R_{ds}}{d_{S6}})$, (29) is rewritten as

$$\frac{v_o}{V_{\text{in}}} = \frac{d_{S6}}{1-d_{S6}}\left[\frac{d_{S6}}{(1-d_{S6})^2}\left[\frac{R_{pa}}{R_L}\right]+1\right]^{-1}. \tag{30}$$

Finally, the peak voltage gain from (30) is given as

$$\frac{V_o}{V_{\text{in}}} = \frac{D}{1-D}\left[\frac{D}{(1-D)^2}\left[\frac{R_{pa}}{R_L}\right]+1\right]^{-1}. \tag{31}$$

Then, the voltage gains of the proposed buck–boost inverter with and without parasitic resistances are shown in Fig. 20. Note that its practical value can be improved by decreasing the parasitic resistances of circuit components.

The voltage stress of switches normalized to V_o in terms of G is expressed as (32). Similarly, the current stress of switches normalized to the peak output current I_o in terms of G are obtained as (33). Thereafter, the relationships between the voltage and current stress of switches and G are shown in Figs. 21 and 22, respectively

$$\frac{V_{\text{stress }(S1-S4)}}{V_0} = \frac{1}{G} \quad \frac{V_{\text{stress }(S5-S8)}}{V_0} = \frac{(1+G)}{G} \tag{32}$$

$$\frac{I_{\text{stress }(S1-S8)}}{I_0} = 1+G. \tag{33}$$

Finally, the following two equations are used to determine the proper values of inductor and capacitor, respectively

$$L = \frac{(1-D)\,V_o}{\Delta I_L f_{sw}} \tag{34}$$

$$C = \frac{I_o D}{\Delta v_c f_{sw}} \tag{35}$$

where Δi_L is the inductor current ripple and Δv_c is the capacitor voltage ripple.

IV. Common-Mode Voltages

The total common mode of the proposed full-bridge can be expressed as [4], [22]

$$v_{tCM} = \frac{v_{1N}+v_{2N}}{2} - \left(\frac{v_{1N}-v_{2N}}{2}\right) = v_{2N}. \tag{36}$$

The terms v_{1N} and v_{2N} are the voltages at the output terminals of the proposed inverter with respect to the neutral of the input voltage, as shown in Figs. 11 and 12.

From Fig. 11, for $v_0 > 0$, $v_{2N} = V_{\text{in}}$. Substituting this value in (36), we obtain

$$v_{tCM} = V_{\text{in}}. \tag{37}$$

$$\frac{v_o}{V_{\text{in}}} = \frac{d_{S6}(t)}{1-d_{S6}(t)}\left[\left[\frac{d_{S6}(t)\left(R_{ds_2}+R_{ds_3}+R_{ds_5}+R_{ds_6}+R_l\right)+\left(1-d_{S6}(t)\right)\left(R_{ds_7}+R_{ds_8}\right)}{R_L(1-d_{S6}(t))^2}\right]+1\right]^{-1} \tag{28}$$

TABLE I
COMPARISON OF THE PROPOSED AND CONVENTIONAL FULL-BRIDGE INVERTERS

	Proposed inverter	H-bridge inverter + boost dc-dc converter	Boost inverter + buck dc-dc converter	Inverting buck-boost dc-dc converter + unfolding inverter	Non-inverting buck-boost dc-dc converter + unfolding inverter
Number of intermediate dc-link capacitor?	0	1	1	1	1
Number of inductors?	1	2	2	2	2
Reactive power flow?	Yes	Yes	Yes	No	No
No of switches?	8, [6, if diode-bridge is used]	6	6	6	8
Line-frequency switches?	4	0	0	4	4
Switches at high-frequency at a time?	2	4 (buck mode) 6 (boost mode)	6 (buck mode) 4 (boost mode)	2	2
High-frequency common-mode voltage?	No	No	No	No	No

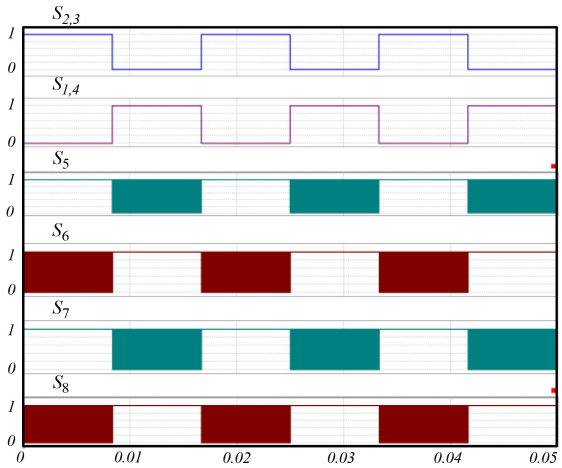

Fig. 23. Switching signals of switches in the proposed inverter.

From Fig. 12, for $v_0 < 0$, $v_{2N} = 0$. Substituting this value in (36), we obtain

$$v_{tCM} = 0. \tag{38}$$

It is found from (37) and (38) that the total common-mode voltage of the proposed inverter is V_{in} for $v_0 > 0$, and 0 for $v_0 < 0$. Thus, the proposed inverter has no high-frequency common-mode voltage.

The comparison of the proposed and conventional full-bridge buck–boost inverters is given in Table I.

In order to verify the effectiveness of the proposed full-bridge single-inductor-based buck–boost inverter with the output power of 500 W, switching frequency of 30 kHz, and line frequency of 60 Hz, the simulation study is first carried out by using the power simulation (PSIM) software.

The switching signals of switches in the proposed inverter are shown in Fig. 23. It is observed that the switching signals $S_1 - S_4$ are the line-frequency signals. Those of $S_5 - S_8$ are the high-frequency signals only for one half-cycle of the output voltage. Thus, only two switches operate at a time at high frequency. Also, the switches S_6 and S_8 generate the positive half-cycle of output ac voltage from the input dc voltage. In contrast, the switches S_5 and S_7 generate the negative half-cycle of output ac voltage.

When the proposed inverter operates in a boost mode, where V_{in} and V_o are 85 and 155 V, respectively, the simulation results for V_{in}, v_o, i_L, i_o, and the drain–source voltages, v_{DS_1}, v_{DS_3}, v_{DS_5}, and v_{DS_6} (of switches S_1, S_3, S_5, and S_6, respectively) are shown in Fig. 24. On the other hand, when the proposed inverter operates in a buck mode, where V_{in} and V_o are 200 and 155 V, respectively, the results are shown in Fig. 25. They show similar responses to those in Fig. 24. In particular, it is known from the results in Figs. 24 and 25 that the proposed inverter operates successfully both as a step-up and step-down inverter.

V. EXTENSION TO CASCADED BUCK–BOOST INVERTER

Based on the proposed buck–boost inverter in Fig. 6, a cascaded buck–boost inverter is developed as shown in Fig. 7, which can be used for the integration of various renewable energy sources. As shown, only one inductor is required and two switches S_a and S_b are high frequency. All the other switches are line frequency. Unlike the traditional inverter, the proposed inverter has no intermediate dc link capacitors. The peak output voltage of the proposed cascaded buck–boost inverter can be obtained as

$$V_o = \frac{nD\sum_{i=1}^{n} V_i}{1-D}. \tag{39}$$

As shown, a very high output voltage can be obtained with low input voltages. Fig. 26 shows the simulated results of the proposed inverter for the specifications given in Table III. As shown, a high output voltage of 311 V is obtained with a low input voltage of 50 V. All the other waveforms are similar to that of the proposed full-bridge inverter.

VI. EXPERIMENTAL RESULTS

In order to show the practical effectiveness and performance of the proposed inverters, the hardware prototypes of 500 and 1000 W are implemented and tested. The hardware prototypes of full-bridge single-inductor-based buck–boost inverter and proposed cascaded inverter are shown in Figs. 27 and 28.

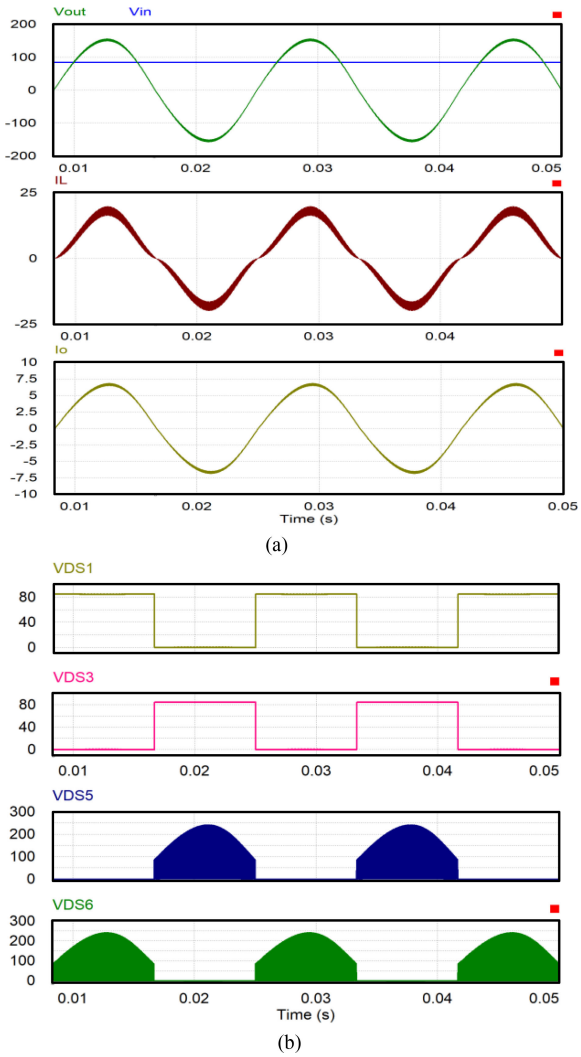

Fig. 24. Simulation results in a boost operation. (a) Input and output voltages, inductor and output currents. (b) Drain–source voltages of switches.

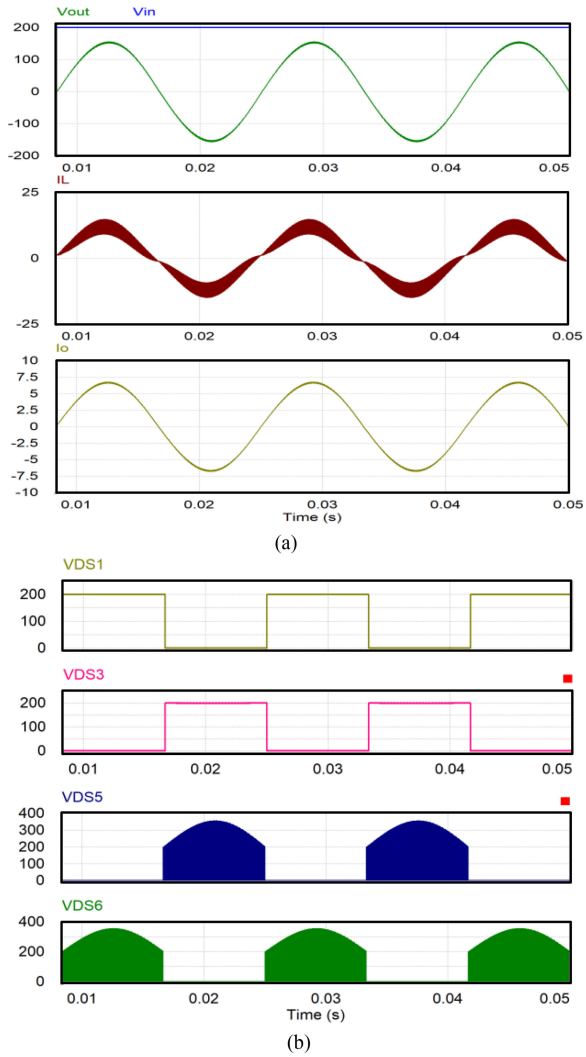

Fig. 25. Simulation results in a buck operation. (a) Input and output voltages, inductor and output currents. (b) Drain–source voltages of switches.

TABLE II
PARAMETERS FOR THE PROPOSED SINGLE-PHASE INVERTER

Parameters	Value / Number
Input voltage, V_{in}	$85-200$ V
Output voltage, $V_{o.pk}$	155 V
Output power, P_o	500 W
Switching frequency, f_{sw}	30 kHz
Inductor, L	0.3 mH
Capacitor, C	6.8 μF
MOSFET, S_1-S_8	47N60CFD

TABLE III
PARAMETERS FOR THE PROPOSED CASCADED INVERTER

Parameters	Value / Number
Input voltage, V_{in}	50 V
Output voltage, $V_{o.pk}$	311 V
Output power, P_o	1000 W
Switching frequency, f_{sw}	30 kHz
Inductor, L	0.3 mH
Capacitor, C	6.8 μF
MOSFET, S_a, S_b	47N60CFD
MOSFET, S_1-S_{12}	IRFP150NPBF

The design specifications for both inverters are given in Tables II and III.

In single-phase buck–boost inverter, when V_{in} is 85 V and v_o is $155\sin(\omega t)$V, the experimental results for V_{in}, v_o, i_o, and i_L in a boost operation are shown in Fig. 29(a). Also, the real measurements of drain–source voltages v_{DS_5}, v_{DS_2}, v_{DS_1}, and v_{DS_6} of switches S_5, S_2, S_1, and S_6, respectively, are shown in Fig. 29(b). Similarly, the practical waveforms of drain–source voltages v_{DS_5}, v_{DS_6}, v_{DS_8}, and v_{DS_7} of switches S_5, S_6, S_8, and S_7, respectively, are shown in Fig. 29(c).

When V_{in} is 200 V and V_o is 155 V, the experimental results are shown in Fig. 30. They show similar responses to those in Fig. 29, except for the buck operation. In particular, it is clearly observed that S_1 and S_2 are working at line frequency, and the switches S_5, S_6, S_7, and S_8 are working at high frequency

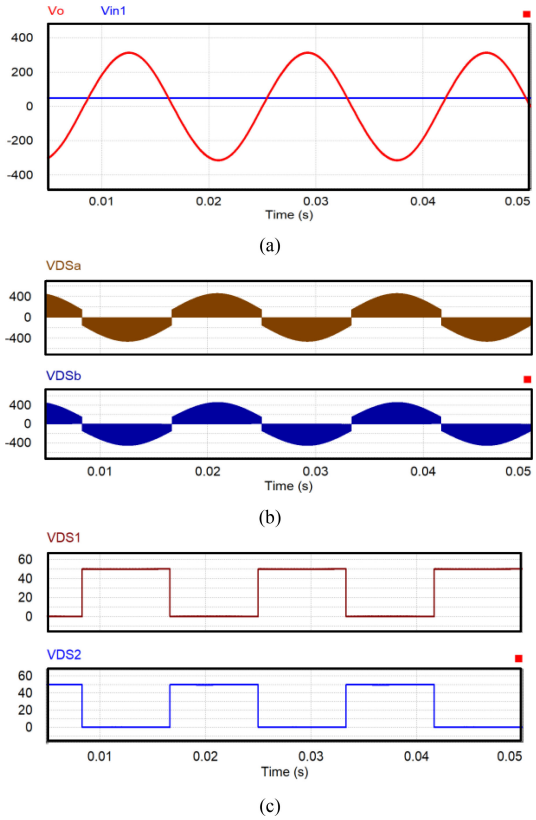

Fig. 26. Simulation results of the proposed cascaded inverter.

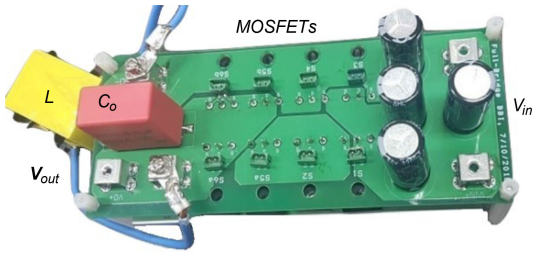

Fig. 27. Hardware prototype of the proposed single-phase inverter.

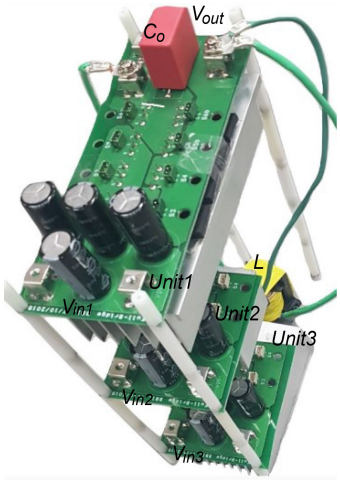

Fig. 28. Hardware prototype of the proposed cascaded inverter.

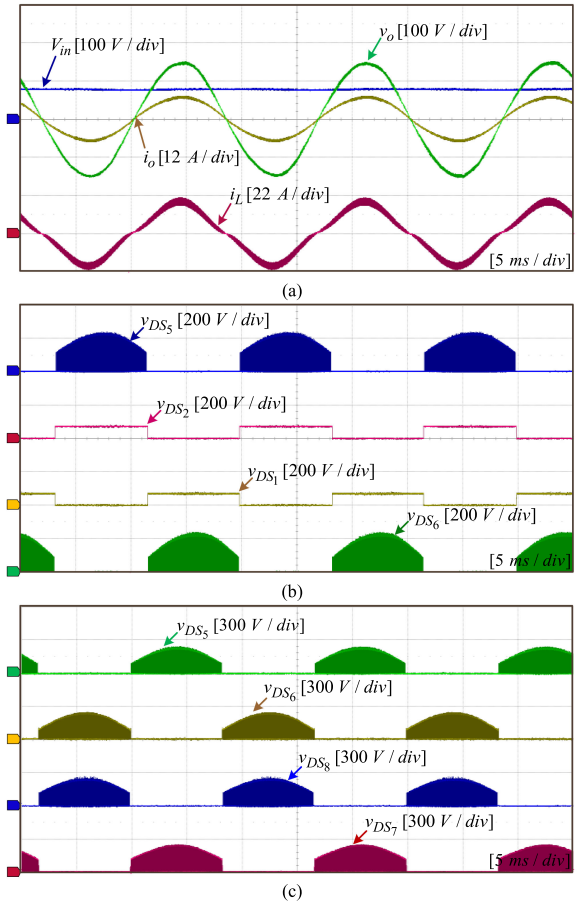

Fig. 29. Experimental results in a boost operation. (a) Input and output voltages, output current and inductor current. (b) Drain–source voltages of switches v_{DS_5}, v_{DS_2}, v_{DS_1}, and v_{DS_6}. (c) Drain–source voltages of switches v_{DS_5}, v_{DS_6}, v_{DS_8}, and v_{DS_7}.

only for half-cycle of output voltage. Moreover, the experimental results in Figs. 29 and 30 show good agreement with the simulation results in Figs. 24 and 25. In summary, they verify that the proposed full-bridge single-inductor-based buck–boost inverter can be used as both a step-up and step-down inverter. In particular, it can operate in a wide range of input voltages. Also, when the proposed inverter operates with a partially inductive load, the experimental results are shown in Fig. 31. In other words, the load consists of the inductor of 50 mH and resistor of 24 Ω. It is clearly observed that the proposed inverter still operates well while providing the reactive power.

In cascaded inverter, when V_{in} is 50 V and $v_o$is 311 $\sin(\omega t)$ V, the experimental results for V_{in} and v_o are shown in Fig. 32(a). The practical waveforms of drain–source voltages v_{DS_1} and v_{DS_2} of switches S_1 and S_2 are shown in Fig. 32(b). Similarly, the drain–source voltages v_{DS_a} and v_{DS_b} of switches S_a and S_b are shown in Fig. 32(c).

Finally, the measured efficiency of the proposed full-bridge inverter in all operating ranges is shown in Fig. 33. The efficiency is measured using Yokogawa-1800 power analyzer. It is known that the efficiency in buck modes is higher than in boost modes. In particular, the maximum efficiency of 96.8% is obtained when

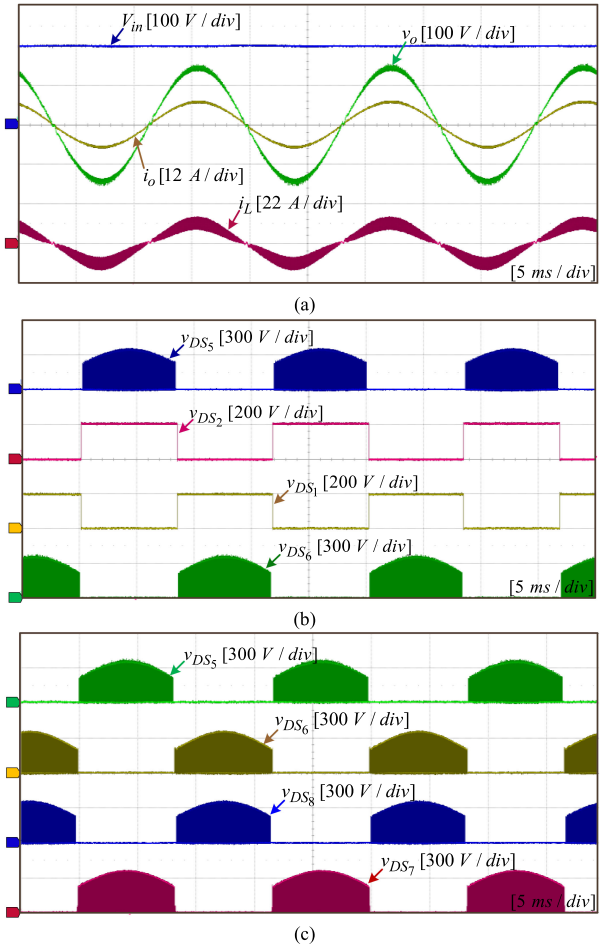

Fig. 30. Experimental results in a buck operation. (a) Input and output voltages, output current and inductor current. (b) Drain–source voltages of switches v_{DS_5}, v_{DS_2}, v_{DS_1}, and v_{DS_6}. (c) Drain–source voltages of switches v_{DS_5}, v_{DS_6}, v_{DS_8}, and v_{DS_7}.

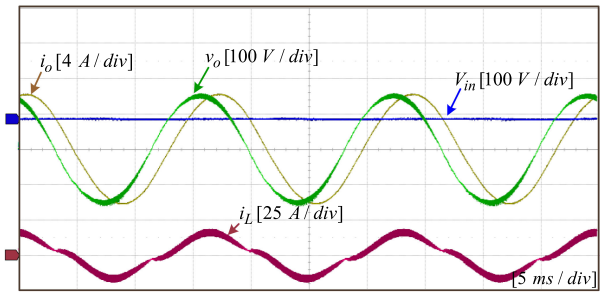

Fig. 31. Experimental results when the proposed inverter operates with a partially inductive load.

the value of V_{in} is 200 V. This is because the inductor current causes conduction loss, and its value in a boost mode is higher than that in a buck mode. Also, the total harmonic distortions (THDs) of output voltage in all operating ranges are shown in Fig. 34. The current flowing through L increases as the input voltage decreases. This affects the harmonic distortion of output voltage, and it increases its THD. Its high value can be reduced by decreasing the inductance of the inductor.

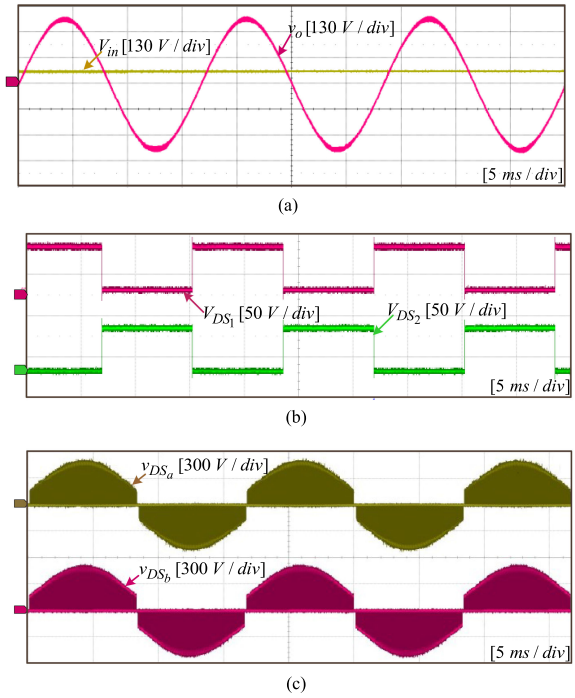

Fig. 32. Experimental results of the proposed cascaded inverter. (a) Input and output voltages. (b) Drain–source voltages of switches v_{DS_1} and v_{DS_2}. (c) Drain–source voltages of switches v_{DS_a} and v_{DS_b}.

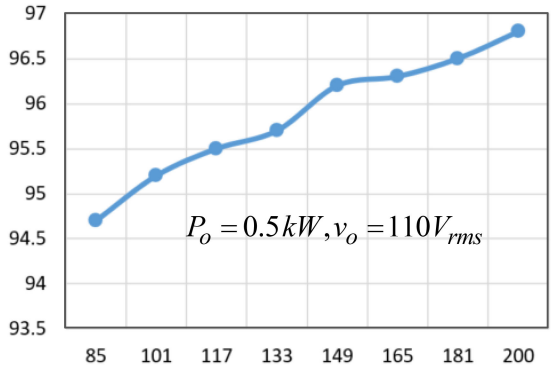

Fig. 33. Experimental result: efficiency.

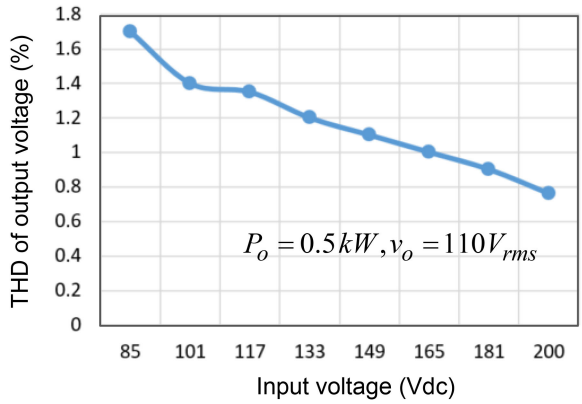

Fig. 34. Experimental result: THD of output voltage.

VII. Conclusion

A new single-inductor-based full-bridge buck–boost inverter and cascaded inverter are proposed. The detailed circuit analysis with its equivalent circuits is presented. Also, the modulation strategy for its proper operation is developed and discussed.

A 500 W, 110 $V_{\rm rms}$ and 1000 W, 220 $V_{\rm rms}$ experimental prototype was fabricated, and experimental studies were performed at 30 kHz to verify the practical effectiveness of the proposed full-bridge single-inductor-based buck–boost inverter and proposed cascaded inverter. Peak efficiency 96.8% was reported. The proposed single-phase buck–boost inverter generated an output voltage 155 V_{pk} for input voltages 85 and 200 V, which verified the step-up and step-down operations of the proposed inverter. The proposed cascaded inverter generated an output voltage $311V_{pk}$ for an input voltage 50 V.

The proposed inverters provide reactive power, which is verified through the operation with a partially inductive load consisting of inductance 50 mH and resistance 24 Ω. The unique feature of the proposed inverters is that it requires only a single inductor, and only two switches are operated at a time at high switching frequency. As the result, the power density and efficiency of the inverter can be improved while decreasing its control complexity.

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