Extensible Z-Source Inverter Architecture: Modular Construction and Analysis

Xinping Ding, *Member, IEEE*, Yangyang Hao, Kai Li, Haibin Li, Zhengyi Wei, and Weimin Wu, *Member, IEEE*

***Abstract*—Z-source inverter (ZSI) can overcome some drawbacks of classical current- and voltage-source inverter, which have features such as high reliability and buck–boost capability of single-stage inverter. This article proposes an extensible ZSI architecture, abbreviated as EZSI. The proposed architecture provides high voltage gain at a small shoot-through duty ratio, which improves the output waveform quality. It inherits the advantages of continuous input current and low dc-link voltage overshoot of quasi-ZSI. The EZSI can be constructed with modularization, using low voltage components to construct a high-power single-stage inverter. A modular analysis method of EZSI is proposed, which divides the high-dimensional state equation of inverter into several independent low-dimensional state equations and simplifies the research of EZSI. A typical EZSI ($n = 2$) L-mSSCL validates the correctness and feasibility of the proposed theory. Compared with the conventional high boost ZSIs, the proposed EZSI ($n = 2$) L-mSSCL has advantages in the aspects of boost capacity, component stress, and inverter efficiency. The operating principle, characters design rules, and power dissipation of the components is analyzed in detail. A 1-kW prototype is used for experimental validation. The theoretical analysis results match with the experimental results.**

***Index Terms*—Buck–boost, impedance-source inverter, single-stage inverter, Z-source inverters (ZSIs), Z-source network.**

I. Introduction

FOR the last few decades, the impedance-source inverter (Z-source inverter, ZSI) has been attracting significant attention. Such type of inverter can achieves buck–boost capability with a single-stage power conversion. The unique feature increases the immunity of the inverters to electromagnetic noise, which may cause uncontrolled shoot-through (or open-circuit) that destroys the traditional voltage-source inverter and current-source inverters, respectively. Furthermore, in a ZSI, both switches in a leg can be turned ON simultaneously to eliminate dead-time and to improve the quality of the output profile. With rapid development of distributed power generation systems, research achievements have made on the topic of ZSI [1]–[30]. Researchers have studied modeling and control [2]–[14], predictive control [15]–[18], high voltage-gain inverters [19]–[21], [28]–[30], photovoltaic grid-connected system, and electric car driving system [22]–[27].

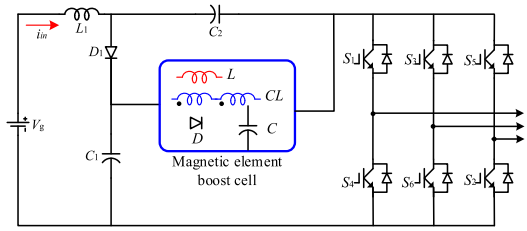

Fig. 1. ZSI network with MEBCs.

High voltage-gain inverters are widely used in distributed generation grid-connected systems, such as photovoltaic and fuel cell system. A ZSI with high voltage gain has certain advantages in grid-connected systems. Several dc–dc boost theories were successfully used in ZSI, resulting in excellent performance [31]–[44]. Among them, technologies based on "magnetic element" such as coupled-inductor [34]–[39], switched-inductor [40], [41], and switched coupled-inductor [42], [43] performed the best. These elements are collectively known as "magnetic element boost cell (MEBC)."

The "MEBC" is embedded into the quasi-ZSI (qZSI) to get high voltage gain, as shown in Fig. 1. The resulting inverters provide continuous input current, strong boost capabilities, and low dc-link voltage overshoot. Hence, such inverters are suitable for use in distributed power generation systems [20], [41], [44], [46]. Ahmed *et al.* [41] present an SCL MEBC, and obtain a high voltage gain, low dc-link voltage spike, and continuous input current of the SCL qZSI. An mSSCL and CWMV cell has been presented in [20] and [48], which improves the boost factor with coupled inductor and bootstrap capacitor. However, the existing research is based on sporadic and independent individual inverters and no systematic research on inverters has been performed from holistic and modular points of view. Thus, existing research results suffer from low scalability and complicated inverter analysis and design.

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This article proposes an extensible Z-source inverter (EZSI) architecture. A modular inverter architecture is used for arbitrarily regulate output ac voltage of the inverter, which makes the proposal of new inverters more convenient and flexible. The modular analysis method simplifies the analysis process of ZSIs and improves the accuracy of circuit analysis. The advantages of such inverters are as follows.

1) Inverter proposal is diverse and flexible, and can be applied to different application fields.
2) Dimensionality reduction. The proposed architecture can divide the high-dimensional equation of state into several independent low-dimensional equations of state and simplify the analysis process of the inverter.
3) Extensibility and integration. The construction of inverter based on integration is beneficial to the standardization of inverter in mass production. This kind of inverter uses low voltage and small current component to complete the inversion function of high voltage and large current, which reduces the cost of the prototype.
4) The inverter has continuous input current, low dc-link voltage overshoot across the inverter bridge, and its efficiency is improved thanks to low current/voltage stress and recycling the leakage inductance energy.

The rest of this article is organized as follows. Section II presents the configuration of the proposed EZSI. The steady-state analysis of the EZSI is presented in Section III. In Section IV, the voltage and current stress on components of EZSI (n) is proposed. In Section V, a typical EZSI I ($n = 2$) L-mSSCL is presented to verify the features of the proposed theory. Section VI proposes the experimental results. Finally, Section VII concludes this article.

II. EZSI Architecture

Fig. 1 shows the generic qZSI, which consists of the qZSI framework and MEBC. The quasi-Z-source framework provides continuous input current, low dc-link voltage overshoot, and boost capability. In addition, the MEBC mainly enhances the ability of boosting, which is shown in Fig. 2.

MEBC is composed of magnetic elements (inductors and transformers), capacitors, and diodes, which realizes the storage and release of energy during a switching cycle. MEBC can be divided into two types, Z-source network and non-Z-source network, according to whether the magnetic element has a flywheel path when the ZSI is in the traditional zero state. We summarized and classified the existing MEBCs, and the specific cells are shown in Fig. 2(a) and (b).

A. Proposed EZSI Architecture

Fig. 3 shows the proposed EZSI architectures, abbreviated as EZSI (n). An EZSI architecture is divided into two types according to the circuit structure, namely, EZSI I (n) and EZSI II (n).

Fig. 3(a) shows the extensible ZSI with continuous input current, represented as EZSI I (n). The extensible ZSI with

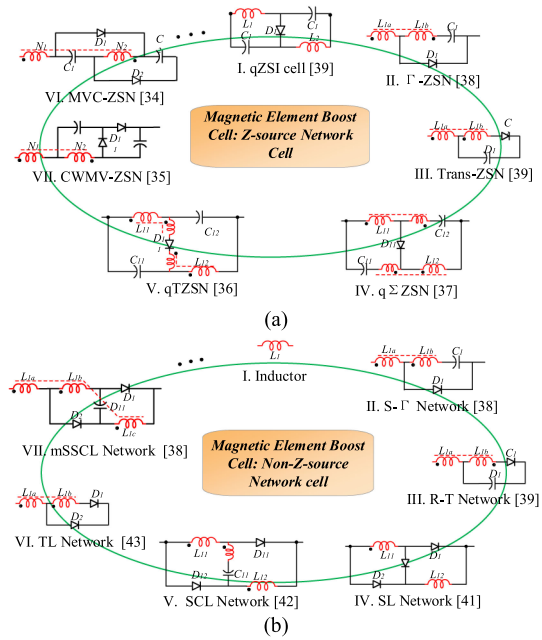


Fig. 2. MEBCs. (a) Z-source network. (b) Non-Z-source network.

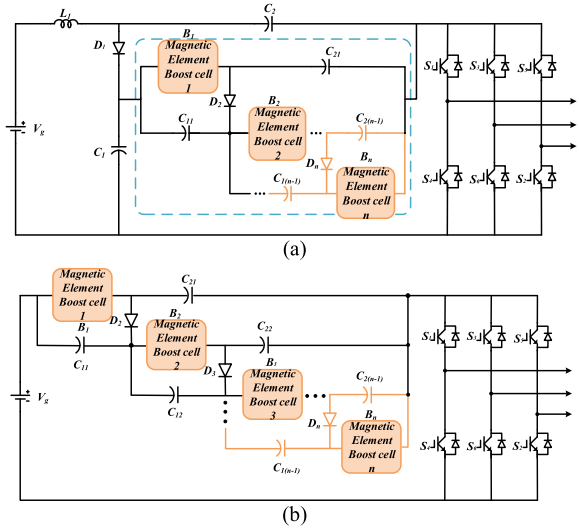


Fig. 3. Structure of the EZSI architecture. (a) Architecture I with continuous input current, (b) Architecture II with discontinuous input current.

discontinuous input current is shown in Fig. 3(b), which is abbreviated as EZSI II (n). An EZSI consists of a qZSI framework and several embedded MEBCs.

The construction of high voltage-gain single-stage inverter with the idea of system integration is beneficial to the popularization of this kind of inverter and has obvious advantages in reducing cost and increasing circuit flexibility. The derivation and modular analysis of the EZSI is shown in Fig. 4. We construct and analyze the inverter according to the "MEBC→ Basic modular circuit→ MEBC based qZSI→ EZSI" process.

This type inverter can be named as EZSI I/II (n) MEBC1-…MEBCn. For example, EZSI I ($n = 2$) qZSN-SCL.

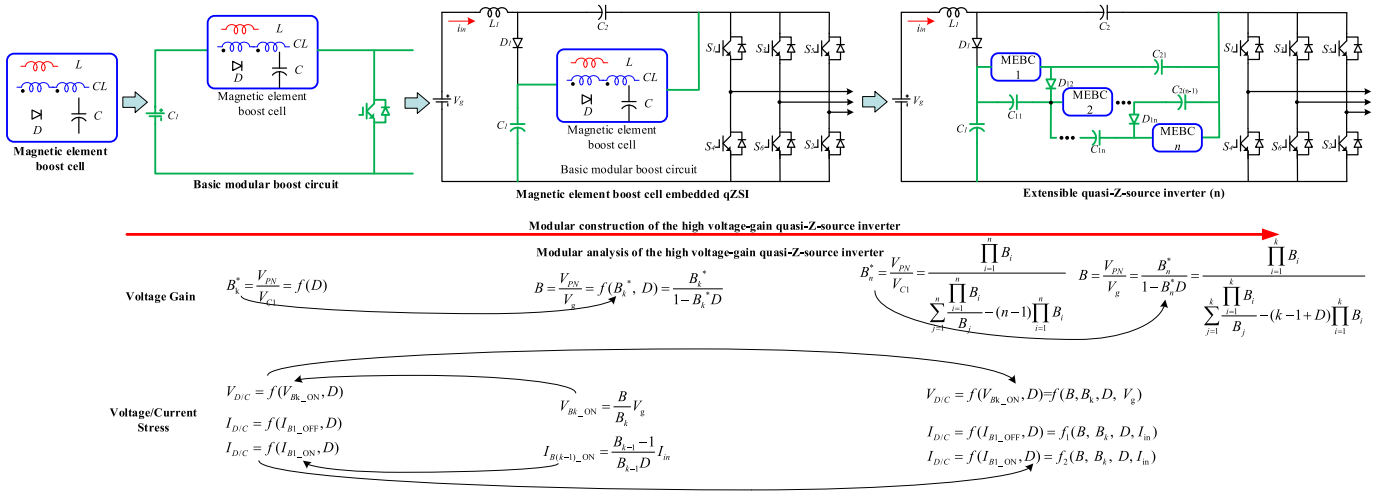


Fig. 4. Derivation and modular analysis of the EZSI.

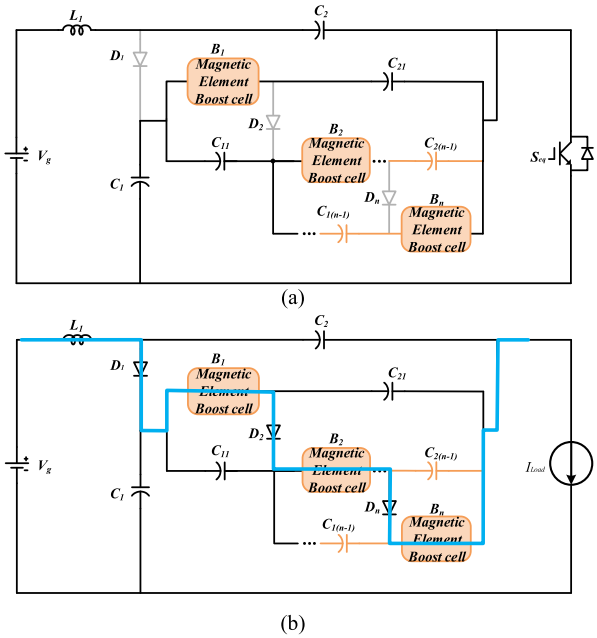


Fig. 5. Operating modes of the proposed EZSI II (n). (a) Shoot-through state. (b) Nonshoot-through state.

Similar to the traditional ZSIs, the EZSI architecture has an extra shoot-through mode besides the six active states and two traditional zero states.

1) Shoot-through mode: Initiated by turning ON the switches simultaneously from at least a phase leg of the VSI H-bridge; the equivalent circuit is shown in Fig. 5(a). The MEBCs are connected in parallel and charged by capacitors C_1, $C_{1(k-1)}$, and $C_{2(k-1)}$. And the input inductor L1 is charged by input source V_g and capacitor C_2.
2) Nonshoot-through mode: In this mode, the VSI operates in the active states or the traditional zero states. The output of the EZSI (n) can be equivalent to a constant current source load. The MEBCs are connected in series to supply to the load together with the input source V_g, and charge the capacitors C_1, $C_{1(k-1)}$, and $C_{2(k-1)}$ at the same time.

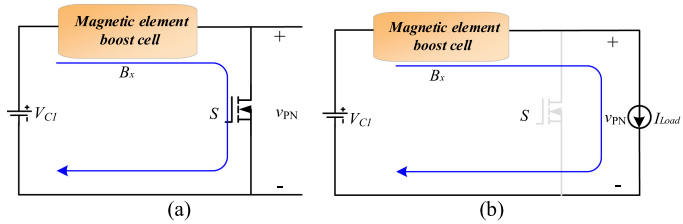


Fig. 6. Structure of basic modular boost circuit and its operating modes. (a) Shoot-through state. (b) Nonshoot-through state.

It can be seen from Fig. 5 that the MEBCs are connected in parallel to reduce the current stress of components at shoot-through interval, while they are connected in series to reduce the voltage stress at nonshoot-through interval.

B. Modular Analysis of EZSIs

The key to the modular construction and analysis of EZSI is that the "basic modular boost circuits" have the same operating modes to ZSI: shoot-through state and nonshoot-through state.

Fig. 6 shows the basic modular boost circuit used in the proposed qZSI architecture, which consists of the MEBC and a switch. During the shoot-through state, energy is transferred from the voltage source V_{C1} to the MEBC, while the MEBC provides energy to the load together with the input capacitor C_1 at the nonshoot-through state. Thus, when the specific MEBC, such as switched inductor, is embedded into the basic modular boost circuit, the voltage boost factor B of the circuit can be obtained. The detail switched inductor embedded basic modular boost circuit and its voltage boost factor is shown in Fig. 7 and (1), respectively

$$B_x = \frac{V_{\mathrm{PN}}}{V_{C1}} = f(D) = \frac{1+D}{1-D} \tag{1}$$

where B_x is the converter boost factor of the xth basic modular boost circuit, V_{PN} and V_{C1} are the peak dc-link voltage and capacitor voltage of C_1, respectively, and D is the shoot-through duty ratio.

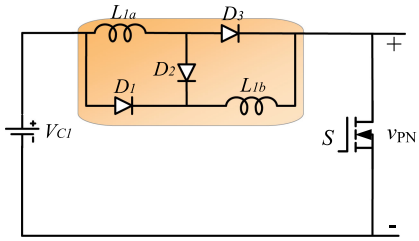


Fig. 7. Switched-inductor embedded basic modular boost circuit.

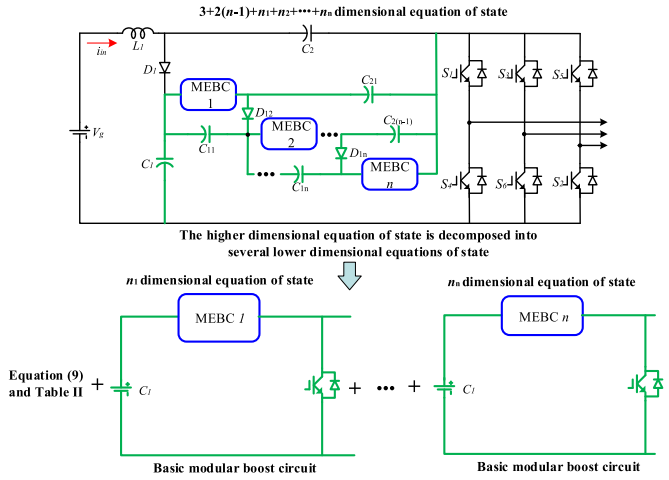


Fig. 8. Dimension reduction of the EZSI's equation of state.

The proposed EZSI consists of basic modular boost circuits and can be analyzed by their boost factors $B_1, B_2, \ldots B_n$.

Fig. 8 shows the dimension reduction of the inverter's equation of state with the proposed modular analysis. We can simplify the $(3 + 2(n\text{ -}1) + n_1 + \ldots n_n)$-dimensional equation of state into several low-dimensional equations of state, including an n_1-dimensional equation, …and n_n-dimensional equation.

III. Steady-State Analysis of EZSI

The proposed EZSI is composed of several basic modular boost circuits, as shown in Figs. 9–12. Hence, the analysis of proposed EZSI can be simplified into the study of different basic modular boost circuits.

A. EZSI I

We choose the EZSI I as a typical example to study EZSI in detail. Fig. 9 shows the derivation of the arbitrary EZSI architecture I, which is composed of qZSI architecture and embedded equivalent EZSI II (n). The overall inverter analysis can also be decomposed into two parts: qZSI framework and equivalent EZSI II (n).

B. qZSI Framework

The qZSI framework contains the basic modular boost circuit, as shown in Fig. 6, which has been marked in green in Fig. 10.

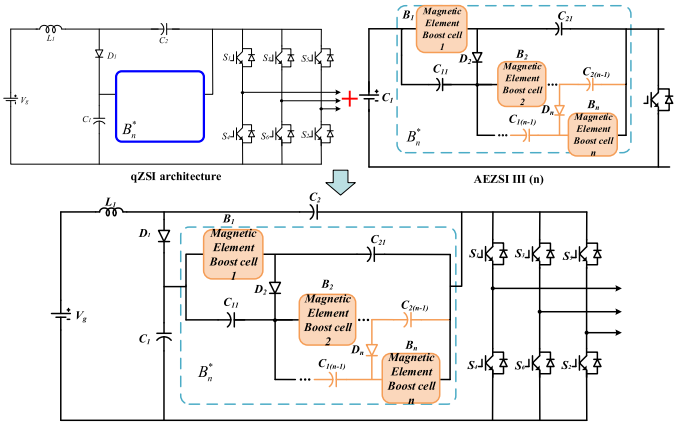


Fig. 9. Derivation of the extensible ZSI I.

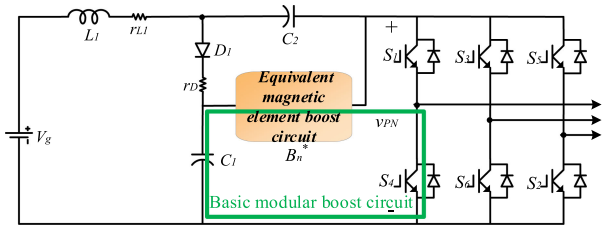


Fig. 10. Generic structure of qZSI framework.

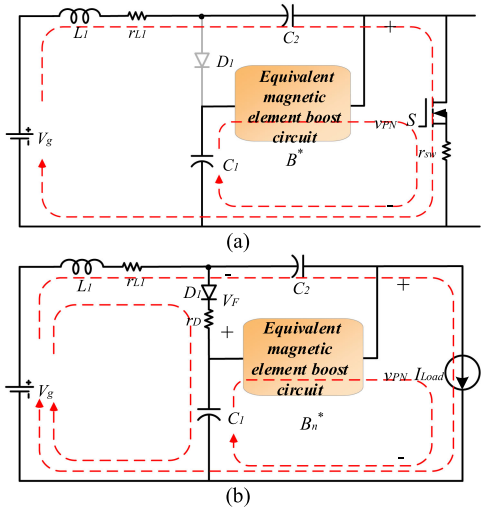


Fig. 11. Operating modes of qZSI framework. (a) Shoot-through state. (b) Nonshoot-through state.

As per the existing ZSI, the qZSI framework has two operating modes: shoot-through state and nonshoot-through state.

During the shoot-through state, as Fig. 11(a) shows, one has

$$V_g - V_{L1} + V_{C2} - r_L I_{in} - r_{DS} I_{sh} = 0 \tag{2}$$

where r_{L1} and r_{DS} are the parasitic resistances of the inductor and switch, respectively, and I_{sh} is the average current of the switches at shoot-through state.

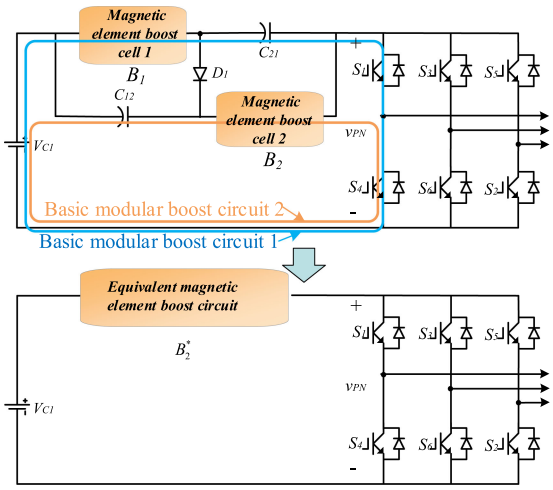


Fig. 12. Structure of EZSI II ($n = 2$).

The governing equations in nonshoot-through state can be expressed as

$$\begin{cases} V_g - V_{L1} - V_{C1} - r_{\mathrm{L}} I_{\mathrm{in}} - V_{\mathrm{F}} = 0 \\ V_g - V_{L1} + V_{C2} - V_{\mathrm{PN}} - r_{\mathrm{L}} I_{\mathrm{in}} = 0 \\ B_n^* V_{C1} - V_{\mathrm{PN}} = 0 \end{cases} \tag{3}$$

where B^* is the boost factor of the equivalent basic modular boost circuit, V_{PN}, and V_{C1} are the peak dc-link voltage and capacitor voltage of C_1, respectively, D is the shoot-through duty ratio, I_{in} is the input inductor current, and V_{F} is the forward voltage of the diode.

Applying the volt–second balance to inductor L_1, we obtain

$$\begin{aligned} &D\left(V_{\mathrm{g}} + V_{C2} - r_{\mathrm{L}} I_{\mathrm{in}} - r_{\mathrm{DS}} I_{\mathrm{sh}}\right) \\ &\quad + (1-D)\left(V_g - V_{C1} - r_{\mathrm{L}} I_{\mathrm{in}} - V_{\mathrm{F}}\right) = 0 \\ &D\left(V_{\mathrm{g}} + V_{C2} - r_{\mathrm{L}} I_{\mathrm{in}} - r_{\mathrm{DS}} I_{\mathrm{sh}}\right) \\ &\quad + (1-D)\left(V_g + V_{C2} - V_{\mathrm{PN}} - r_{\mathrm{L}} I_{\mathrm{in}}\right) = 0. \end{aligned} \tag{4}$$

The equation for V_{PN}, V_{C1}, and V_{C2} can be written as

$$\begin{aligned} V_{\mathrm{PN}} &= \frac{B_n^*(V_{\mathrm{g}} - D r_{DS} I_{\mathrm{sh}} - V_{\mathrm{F}} - r_{\mathrm{L}} I_{\mathrm{in}})}{1 - B_n^* D} \\ V_{\mathrm{C1}} &= \frac{V_{\mathrm{g}} - V_{\mathrm{F}} - r_{\mathrm{L}} I_{\mathrm{in}} - D r_{DS} I_{\mathrm{sh}}}{1 - B_n^* D} \\ V_{\mathrm{C2}} &= \frac{(B_n^* - 1) V_{\mathrm{g}} - D(B_n^* - 1) r_{\mathrm{SW}} I_{\mathrm{sh}} - B_n^*(1-D) V_{\mathrm{F}} - (B_n^* - 1) r_{\mathrm{L}} I_{\mathrm{in}}}{1 - B_n^* D}. \end{aligned} \tag{5}$$

The dc component of the input current and shoot-through current of switches is

$$\begin{aligned} I_{\mathrm{in}} &= B_{\mathrm{ideal}} \frac{V_{\mathrm{PN}}}{R}, \\ I_{\mathrm{sh}} &= \frac{B_n^* - 1}{B_n^* D} I_{\mathrm{in}} + I_{\mathrm{in}} = \frac{B_n^*(1+D) - 1}{B_n^* D} I_{\mathrm{in}}. \end{aligned} \tag{6}$$

On substituting (4) into (2), we obtain

$$V_{\mathrm{PN}} = \frac{B_{\mathrm{n,ideal}}^* \cdot B_n^* R(V_{\mathrm{g}} - V_{\mathrm{F}})}{B_{\mathrm{n,ideal}}^*(B_{\mathrm{ideal}} \cdot B_n^*(r_{\mathrm{L}} + (1+D) r_{DS}) - (B_n^* D - 1) R) - B_{\mathrm{ideal}} \cdot B_n^* r_{DS}} \tag{7}$$

$$\begin{aligned} B &= \frac{V_{\mathrm{PN}}}{V_{\mathrm{g}}} \\ &= \frac{B_{\mathrm{n,ideal}}^* \cdot B_n^* R(V_{\mathrm{g}} - V_{\mathrm{F}})}{(B_{\mathrm{n,ideal}}^*(B \cdot B_n^*(r_{\mathrm{L}} + (1+D) r_{DS}) - (B_n^* D - 1) R) - B \cdot B_n^* r_{DS}) V_{\mathrm{g}}}. \end{aligned} \tag{8}$$

Ignoring the parasitic parameters, the ideal boost factor of the quasi-Z-source architecture can be simplified to

$$B_{\mathrm{ideal}} = \frac{B_n^*}{1 - B_n^* D}. \tag{9}$$

The boost factor B of EZSI I is a function of the shoot-through duty cycle D and the boost factor B_n^* of the basic modular boost circuit. In other words, the boost factor B of the EZSI I can be obtained by finding B_n^* of the EZSI II (n).

C. EZSI I (n)

1) EZSI II ($n = 2$): Fig. 12 shows the structure of EZSI II ($n = 2$), which also has two operating modes. The EZSI II ($n = 2$) consists of two basic modular boost circuits, which are marked with blue and orange lines, respectively. From Fig. 12, we have

$$\begin{aligned} V_{\mathrm{PN}} &= B_1(V_{C1} + V_{C21}) = B_2(V_{\mathrm{C1}} + V_{C12}) \\ &= V_{C12} + V_{C21} + V_{C1}. \end{aligned} \tag{10}$$

With this equation, the relation between V_{PN} and V_{C1} can be expressed as

$$B_{2,\mathrm{ideal}}^* = B_{1,2} = \frac{V_{PN}}{V_{\mathrm{C1}}} = \frac{B_1 B_2}{B_1 + B_2 - B_1 B_2} \tag{11}$$

where B_1 and B_2 are the boost factor of the first and second basic modular boost circuit, respectively, and $B_{1,2}$ is the equivalent boost factor for MEBC1 and MEBC2. From (11), the boost factor of the EZSI II ($n = 2$) can be obtained by the boost factors B_1 and B_2.

2) EZSI II (n): In Fig. 3(b), considering the diode threshold voltage V_{F}, the peak dc-link voltage in nonshoot-through state is

$$\begin{aligned} &B_1(V_{C1} + V_{C21}) = V_{\mathrm{PN}} \\ &B_2(V_{C1} + V_{C11} + V_{C22}) = V_{\mathrm{PN}} \\ &B_3(V_{C1} + V_{C11} + V_{C12} + V_{C23}) = V_{\mathrm{PN}} \\ &\qquad \cdots\cdots \\ &B_{n-1}(V_{C1} + V_{C11} + V_{C12} + \cdots + V_{C1n-2} + V_{C2n-1}) = V_{\mathrm{PN}} \\ &B_n(V_{C1} + V_{C11} + V_{C12} + \cdots + V_{C1n-1}) = V_{\mathrm{PN}}. \end{aligned} \tag{12}$$

It also can be expressed as

$$\begin{aligned} &V_{C1} + V_{C11} + V_{C21} + V_F = V_{\mathrm{PN}} \\ &V_{C1} + V_{C11} + V_{C12} + V_{C22} + V_F = V_{\mathrm{PN}} \\ &V_{C1} + V_{C11} + V_{C12} + V_{C13} + V_{C23} + V_F = V_{\mathrm{PN}} \\ &\qquad \cdots\cdots \\ &V_{C1} + V_{C11} + V_{C12} + \cdots + V_{C1n-2} + V_{C2n-2} + V_F = V_{\mathrm{PN}} \\ &V_{\bar{C}1} + V_{C11} + V_{C12} + \cdots + V_{C1n-1} + V_{C2n-1} = V_{\mathrm{PN}}. \end{aligned} \tag{13}$$

With (12) and (13), the peak dc-link voltage is simplified as

$$V_{\mathrm{PN}} = \frac{\prod_{i=1}^{n} B_i V_{C1} - ((n-1)\prod_{i=1}^{n} B_i) V_F}{\sum_{j=1}^{n} \frac{\prod_{i=1}^{n} B_i}{B_j} - (n-1)\prod_{i=1}^{n} B_i}. \tag{14}$$

Solving (14) for $B_n{}^*$, one has

$$B_n^* = \frac{\prod_{i=1}^{n} B_i}{\sum_{j=1}^{n} \frac{\prod_{i=1}^{n} B_i}{B_j} - (n-1)\prod_{i=1}^{n} B_i} \left(1 - \frac{(n-1)V_{\mathrm{F}}}{\frac{V_{\mathrm{g}}}{1-B_n^* D}}\right)$$
$$= B_{\mathrm{n,ideal}}^* \left(1 - \frac{(n-1)V_F}{\frac{V_{\mathrm{g}}}{1-B_n^* D}}\right). \quad (15)$$

The boost factor of the EZSI II (n) with the diode threshold voltage becomes

$$B_n^* = \frac{B_{\mathrm{n,ideal}}^*(V_{\mathrm{g}} - (n-1)V_F)}{B_{\mathrm{n,ideal}}^* D(n-1)V_F + V_{\mathrm{g}}}. \quad (16)$$

The ideal value of $B_n{}^*$ is

$$B_{n,\mathrm{ideal}}^* = \frac{\prod_{i=1}^{n} B_i}{\sum_{j=1}^{n} \frac{\prod_{i=1}^{n} B_i}{B_j} - (n-1)\prod_{i=1}^{n} B_i} \quad (17)$$

where B_i and B_j are the converter boost factors of the *i*th and *j*th basic modular boost circuit, respectively, and B_n^* is the total boost factor of the *n* basic modular boost circuits.

D. *Boost Factor* B*, Stages* n*, and MEBCs*

The extended stage *n* is related to the specific MEBC cell and is limited by the boost factor *B* of the inverter architecture. We know that the boost factor of the ZSI architecture can be reduced to a general form $B = B_n^*/(1 - B_n^* D)$, where $(1 - B_n^* D) > 0$. The appropriate value range of the shoot-through duty cycle is $0.1 < D < 0.2$, so the stage *n* and the boost factor of each MEBC satisfy the following relation:

$$n = 2, \frac{B_1 B_2}{B_1 + B_2 - B_1 B_2} < 6 \quad (18)$$

$$n = 3, \frac{B_1 B_2 B_3}{B_1 B_2 + B_1 B_3 + B_2 B_3 - 2B_1 B_2 B_3} < 6. \quad (19)$$

Fig. 13 shows the limiting conditions for inverter voltage gain *B*, stage *n*, and voltage gain B_{x} of each cell. The shaded area is an optional area for the MEBC voltage gain B_{x}. We can select the appropriate MEBCs according to the voltage gain, as shown in Fig. 13, and obtain the EZSI that meets the application requirements.

IV. Voltage and Current Stress Analysis

The voltage and current stress on components of the proposed extensible ZSI architecture can be analyzed and studied using the boost factor of "basic modular boost circuit" B_x and shoot-through duty ratio *D*, which simplifies the difficulty and complexity of the specific inverter analysis.

A. *Voltage Stress Analysis*

In Fig. 9, the voltage stresses of the capacitors C_1 and C_2 are

$$V_{C1} = \frac{V_{\mathrm{PN}}}{B_n^*} = \frac{B}{B_n^*} V_g = \frac{1}{1/B_n^* - D} V_g$$
$$V_{C2} = V_{\mathrm{PN}} - \frac{1}{B_n^*} V_{\mathrm{PN}} = (B - \frac{B}{B_n^*}) V_g. \quad (20)$$

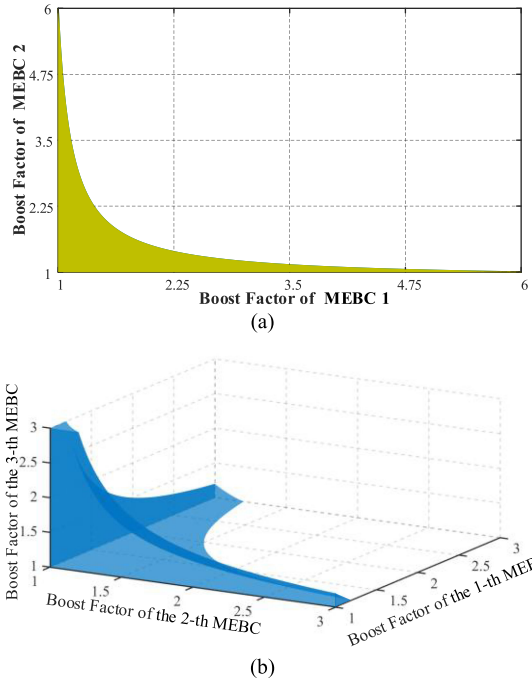


Fig. 13. Constraint relation between voltage gain of inverter and boost factor of each MEBC. (a) Stage $n = 2$. (b) Stage $n = 3$.

From (20), we can conclude that the voltage stress across capacitor C_1 or C_2 is the function of B_n^*, *D*, and V_{g}, that is, $V_{\mathrm{C1,C2}} = f(B_n^*, D, V_{\mathrm{g}})$.

In order to deduce the voltage stresses across capacitors C_{1k} and C_{2k}, we present the voltage equations in shoot-through state, as shown in Fig. 5(a)

$$\begin{aligned}
&B_1(V_{C1} + V_{C21}) = V_{\mathrm{PN}} \\
&B_2(V_{C1} + V_{C11} + V_{C22}) = V_{\mathrm{PN}} \\
&B_3(V_{C1} + V_{C11} + V_{C12} + V_{C23}) = V_{\mathrm{PN}} \\
&\cdots\cdots \\
&B_k(V_{C1} + V_{C11} + V_{C12} + \cdots + V_{C1(k-1)} + V_{C2k}) = V_{\mathrm{PN}}
\end{aligned} \quad (21)$$

where B_k is the boost factor of the *k*-th basic modular boost circuit, *k* is a positive integer, and $k = 1,2,\ldots n\text{-}1$.

From Fig. 5(b), we therefore write

$$V_{C1(k-1)} + V_{C2(k-1)} = V_{C2(k-2)}. \quad (22)$$

Substituting (21) into (22), one has

$$B_k(V_{PN} + V_{C2k} - V_{C2(k-1)}) = V_{\mathrm{PN}}$$
$$V_{C2k} - V_{C2(k-1)} = \frac{V_{\mathrm{PN}}}{B_k} - V_{\mathrm{PN}}. \quad (23)$$

With (22) and (23), the *k*th capacitor voltage V_{C1k} is

$$V_{C1k} = \left(B - \frac{B}{B_k}\right) V_g. \quad (24)$$

One can rewrite (21) as a system of equations

$$V_{C2k} - V_{C2(k-1)} = \frac{V_{\mathrm{PN}}}{B_k} - V_{\mathrm{PN}}$$

$$V_{C2(k-1)} - V_{C2(k-2)} = \frac{V_{\rm PN}}{B_{k-1}} - V_{\rm PN}$$
$$\cdots = \cdots$$
$$V_{C22} - V_{C21} = \frac{V_{\rm PN}}{B_2} - V_{\rm PN}$$
$$V_{C21} - V_{C2} = \frac{V_{\rm PN}}{B_1} - V_{\rm PN}. \tag{25}$$

The left- and right-hand sides of (25) are added, respectively, and one obtains

$$V_{C2k} - V_{C2} = \frac{V_{\rm PN}}{B_k} + \frac{V_{\rm PN}}{B_{k-1}} + \frac{V_{\rm PN}}{B_{k-2}} + \cdots + \frac{V_{\rm PN}}{B_2} + \frac{V_{\rm PN}}{B_1} - kV_{\rm PN}. \tag{26}$$

Therefore, the kth capacitor voltage $V_{\rm C2k}$ is

$$\begin{aligned} V_{C2k} &= \tfrac{V_{\rm PN}}{B_k} + \tfrac{V_{\rm PN}}{B_{k-1}} + \tfrac{V_{\rm PN}}{B_{k-2}} + \cdots + \tfrac{V_{\rm PN}}{B_2} + \tfrac{V_{\rm PN}}{B_1} - kV_{\rm PN} \\ &\quad + V_{\rm PN} - \tfrac{1}{B_n^*}V_{\rm PN} \\ &= V_{\rm PN}\big(\big(\tfrac{1}{B_k} + \tfrac{1}{B_{k-1}} + \tfrac{1}{B_{k-2}} + \cdots + \tfrac{1}{B_2} + \tfrac{1}{B_1}\big) \\ &\quad - k + 1 - \tfrac{1}{B_n^*}\big) \\ &= V_{\rm PN}\Bigg(\Bigg(\frac{\sum_{j=1}^{k}\frac{\prod_{i=1}^{k} B_i}{B_j} - (k-1)\prod_{i=1}^{k} B_i}{\prod_{i=1}^{k} B_i} \\ &\quad + k - 1 - k + 1 - \tfrac{1}{B_n^*}\Bigg)\Bigg) \\ &= V_{\rm g}\big(\tfrac{B}{B_k^*} - \tfrac{B}{B_n^*}\big), k \le n-1, \text{ and } k \text{ is a positive integer.} \end{aligned} \tag{27}$$

The voltage and current stresses on the components in magnetic element boost circuit (MEBC) can be calculated by the voltage and current of the MEBC. The voltage and current stresses across the kth MEBC is defined as $V_{\rm Bk\text{-}ON}/I_{\rm Bk\text{-}ON}$ and $V_{\rm Bk\text{-}OFF}/I_{\rm Bk\text{-}OFF}$, respectively. The labeling of voltage and current is shown in Fig. 14.

From Fig. 14, we have

$$\begin{aligned} V_{Bk\_\rm ON} &= V_{C1} + V_{C11} + V_{C12} + \cdots + V_{C1(k-1)} + V_{C2k} \\ &= V_{C1} + V_{C11} + V_{C12} + \cdots + V_{C1(k-1)} + V_{C2(k-1)} \\ &\quad - V_{C2(k-1)} + V_{C2k} \\ &= V_{PN} - V_{C2(k-1)} + V_{C2k} = \frac{B}{B_k}V_g \end{aligned} \tag{28}$$

$$\begin{aligned} V_{Bk\_\rm OFF} &= V_{C2k} - V_{C2(k-1)} = \big(\tfrac{B}{B_k^*} - \tfrac{B}{B_n^*}\big)V_g - \big(\tfrac{B}{B_{k-1}^*} - \tfrac{B}{B_n^*}\big)V_g \\ &= \big(\tfrac{B}{B_k^*} - \tfrac{B}{B_{k-1}^*}\big)V_g = \big(\tfrac{B}{B_k} - B\big)V_g. \end{aligned} \tag{29}$$

The voltage stress across the kth MEBC $V_{\rm Bk\text{-}ON/OFF}$ is the hub connecting the voltage stress on components inside MEBC and the input source $V_{\rm g}$. A detailed analysis is shown in Section IV-C.

B. Current Stress Analysis

This section mainly studies the current stress of capacitors, diodes, and MEBCs.

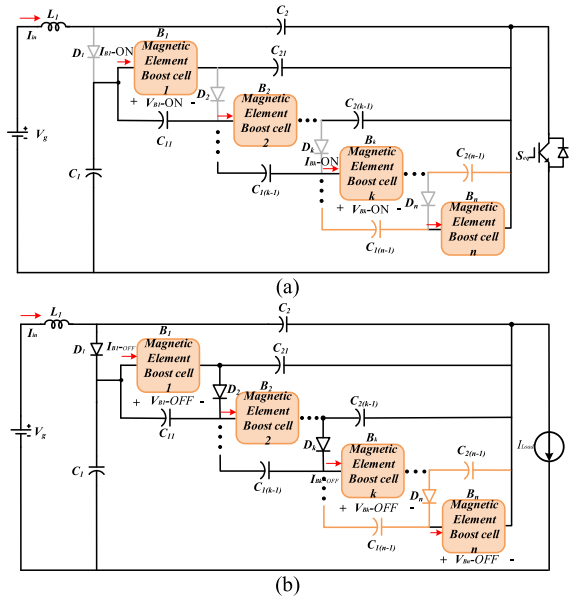


Fig. 14. Schematic diagram of voltage and current stresses of MEBCs. (a) Shoot-through state. (b) Nonshoot-through state.

All diodes are conducting in a nonshoot-through state, and the current stress across the kth diode can be expressed as

$$I_{Dk} = \frac{1}{1-D}I_{\rm in}. \tag{30}$$

The average current of MEBC is equal to $I_{\rm in}$, and considering the MEBC stores as much energy as it releases in one switching cycle, we have

$$\begin{aligned} &DI_{B(k-1)\_\rm ON} + (1-D)I_{B(k-1)\_\rm OFF} = I_{\rm in} \\ &DT_sV_{B(k-1)\_\rm ON}I_{B(k-1)\_\rm ON} \\ &\quad + (1-D)T_sV_{B(k-1)\_\rm OFF}I_{B(k-1)\_\rm OFF} = 0. \end{aligned} \tag{31}$$

On solving for $I_{\rm B(k\text{-}1)}$, one has

$$I_{B(k-1)\_\rm ON} = \frac{B_{k-1}-1}{B_{k-1}D}I_{\rm in}, I_{B(k-1)\_\rm OFF} = \frac{1}{B_{k-1}(1-D)}I_{\rm in} \tag{32}$$

where $I_{\rm B(k\text{-}1)\text{-}ON}$ and $I_{\rm B(k\text{-}1)\text{-}OFF}$ represent the currents flowing into the kth MEBC in shoot-through state and nonshoot-through state, respectively.

The maximum capacitor current occurs in the shoot-through state, and the current relation can be obtained from Fig. 14(a)

$$\begin{aligned} &I_{C11\_\rm ON} = I_{C1\_\rm ON} - I_{B1\_\rm ON} \\ &I_{C12\_\rm ON} = I_{C1\_\rm ON} - I_{B1\_\rm ON} - I_{B2\_\rm ON} \\ &\cdots\cdots \\ &I_{C1k\_\rm ON} = I_{C1\_\rm ON} - I_{B1\_\rm ON} - I_{B2\_\rm ON} - \cdots - I_{Bk\_\rm ON}. \end{aligned} \tag{33}$$

TABLE I
VOLTAGE/CURRENT STRESS OF EZSI II (N = K) IN Fig. 3

Type	EZSI (n=k)
Voltage stress	$V_{C1k}=(B-\frac{B}{B_k})V_g$, $V_{C2k}=(\frac{B}{B_k^*}-\frac{B}{B_n^*})V_g$
	$V_{Dk}=BV_g$, $V_{Bk\_ON}=\frac{B}{B_k}V_g$
Current stress	$I_{Dk}=\frac{1}{1-D}I_{in}$, $I_{B(k-1)\_ON}=\frac{B_{k-1}-1}{B_{k-1}D}I_{in}$
	$I_{C1k\_ON}=\frac{1}{D}(\frac{1}{B_k^*}-\frac{1}{B_n^*})I_{in}$, $I_{C2k\_ON}=\frac{B_k-1}{B_kD}I_{in}$

Substituting (31) into (32) and solving for I_{C1k}

$$\begin{aligned}
I_{C11_ON} &= \tfrac{1}{D}\left(\tfrac{1}{B_1}-\tfrac{1}{B_n^*}\right)I_{in}\\
I_{C12_ON} &= \tfrac{1}{D}\left(\tfrac{1}{B_1}+\tfrac{1}{B_2}-\tfrac{1}{B_n^*}-1\right)I_{in}\\
&\cdots\cdots\\
I_{C1k_ON} &= \tfrac{1}{D}\left(\tfrac{1}{B_1}+\tfrac{1}{B_2}+\cdots+\tfrac{1}{B_k}-\tfrac{1}{B_n^*}-(k-1)\right)I_{in}\\
&= \left(\tfrac{1}{B_k^*D}-\tfrac{1}{B_n^*D}\right)I_{in}.
\end{aligned} \tag{34}$$

With the same manner, I_{C2k} is written as

$$I_{C2k\_ON}=\frac{B_k-1}{B_kD}I_{in}. \tag{35}$$

Based on the above analysis, the voltage and current stresses of capacitors, diodes and MEBCs in EZSI I (n) are shown in Table I.

C. Voltage and Current Stresses of Components in MEBC

The voltage and current stresses of the components in MEBC are calculated in two steps. First, we use MEBC voltage and current to represent the voltage and current of components in MEBC, that is, $V = f(B_k, V_{Bk\cdot ON/OFF})$, and $I = f(B_k, I_{Bk\cdot ON/OFF})$. Second, by eliminating the intermediate variable $V_{Bk\cdot ON/OFF}$ or $I_{Bk\cdot ON/OFF}$ in (28) or (32), the voltage and current stress of components in MEBC can be obtained.

In a word, the voltage and current stresses across components inside the MEBC can be obtained from

$$V_g \rightarrow V_{B1\_ON/OFF} \rightarrow V_{C/D}, I_{in} \rightarrow I_{B1\_ON/OFF} \rightarrow I_{C/D} \tag{36}$$

where $V_{C/D}$ and $I_{C/D}$ are the voltage and current stresses on capacitors and diodes in MEBC, respectively.

Thus, the voltage and current stresses of all components of the proposed ZSI can be obtained by the modularization method and can be expressed as functions of B, B_k, and shoot-through duty cycle D. This method simplifies the complexity of inverter analysis and provides convenience for the proposal and analysis of new ZSI.

V. TYPICAL EZSI

This article takes two-stage EZSI as an example for analysis and experimental verification.

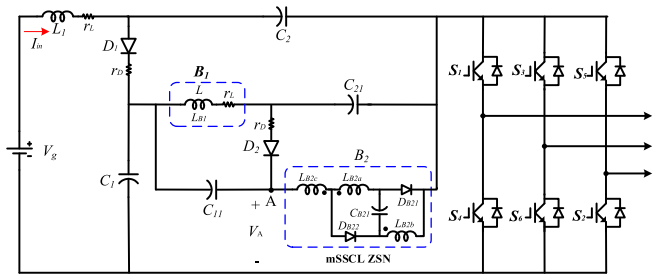


Fig. 15. Schematic diagram of EZSI I ($n = 2$) L-mSSCL.

A. Typical EZSI I (n = 2) L-mSSCL

Fig. 15 is the diagram of the EZSI I ($n = 2$) L-mSSCL, which consists of inductor L_{B1} (MEBC1) and mSSCL network (MEBC2). Due to its quasi-Z-source network framework, the proposed inverter has a continuous input current and a low voltage overshoot on the switches. It provides high voltage boosting capability results from two MEBCs structure. In the shoot-through state, the L cell and mSSCL cell are charged in parallel, which reduces the current stress of the components, while in the nonshoot-through state, the L and mSSCL are discharged in series, which correspondingly reduces the voltage stress of the components.

We analyze the proposed EZSI I ($n = 2$) L-mSSCL with the modular analysis method presented in Sections III and IV. The boost factor of the inverter can be derived as $B = f(B^*)$ (8) and $B^* = f(B_1, B_2)$ (17). Embedding the inductor L into a basic modular boost circuit, as shown in Fig. 6, the boost factor B_1 can be expressed as

$$B_1=\frac{(1-D)R}{(1-D)^2R+r_L} \tag{37}$$

where r_L is the ESR of the inductor L_{B11}, D is the shoot-through duty ratio, R is the equivalent dc-link load, $R=\frac{8R_x(1-D)}{3M^2}$, R_x is the xth phase load, and x = a, b, or c.

Considering the effect of parasitic resistance and leakage inductance of the coupled-inductor, the calculation of boost factor B_2 is relatively complicated. We define the coupling coefficient $k=\frac{L_m}{L_m+L_k}$, $\frac{V_{Lk}}{V_{Lm}}=\frac{L_k}{L_m}=\frac{1-k}{k}=\alpha$.

The basic modular boost circuit with an embedded mSSCL cell is shown in Fig. 16. The parasitic resistance of the winding and the diode that have great influence on the circuit are considered. The basic modular boost circuit with an mSSCL cell has two operating modes: shoot-through state and nonshoot-through state.

The voltage across winding N_1 during shoot-through state and nonshoot-through state is, respectively, expressed as

$$\begin{aligned}
V_{N1ON} &= \frac{V_g-V_F}{1+\alpha-\gamma}=\frac{V_{CB21}+V_F}{1+\alpha}\\
V_{N1OFF} &= \frac{V_g+V_{CB21}-V_{PN}}{2+2\alpha-\gamma}
\end{aligned} \tag{38}$$

where $\gamma = N_3/N_1$, $N_2/N_1 = 1$.

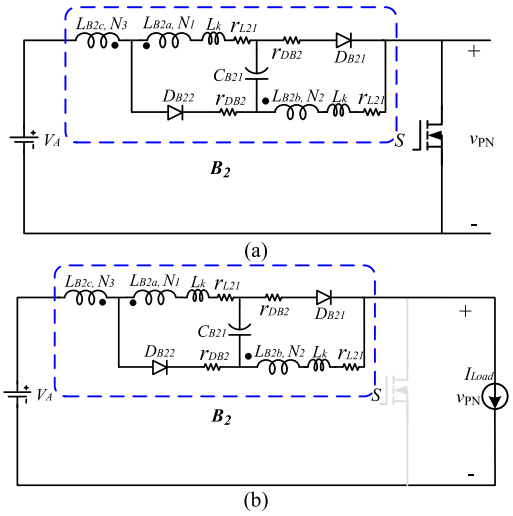


Fig. 16. Basic modular boost circuit with embedded mSSCL cell. (a) Shoot-through state. (b) Nonshoot-through state.

Using the volt–second balance principle to the winding N_1, one has

$$D\left(\frac{V_{\rm A}-V_F}{1+\alpha-\gamma}\right)+(1-D)\left(\frac{V_{\rm A}+V_{\rm CB21}-V_{\rm PN}}{2+2\alpha-\gamma}\right)=0$$
$$D\left(\frac{V_{\rm CB21}+V_F}{1+\alpha}\right)+(1-D)\left(\frac{V_{\rm A}+V_{\rm CB21}-V_{\rm PN}}{2+2\alpha-\gamma}\right)=0 \quad (39)$$

where $V_{\rm A}$ is the input voltage of the MEBC 2.

On solving for $V_{\rm PN}$, $V_{\rm PN}$ can be written as

$$V_{\rm PN}=\frac{(2+2\alpha-\gamma)(V_{\rm g}-V_F)}{(1+\alpha-\gamma)(1-D)}-2r_{\rm L}I_{\rm LB2aOFF}-\frac{(2D(1+\alpha-\gamma)+n)r_{\rm L}I_{\rm LB2aON}}{(1+\alpha-\gamma)(1-D)}. \quad (40)$$

The boost factor B_2 is

$$B_2=\frac{(2+2\alpha-\gamma)(1-\frac{V_{\rm F}}{V_A})}{(1+\alpha-\gamma)(1-D)}-2\frac{r_{\rm L}I_{\rm LB2aOFF}}{V_A}-\frac{(2(1+\alpha-\gamma)D+\gamma)\frac{r_{\rm L}I_{\rm LB2aON}}{V_A}}{(1+\alpha-\gamma)(1-D)} \quad (41)$$

where $I_{\rm LB2aOFF}$ and $I_{\rm LB2aON}$ are the average current of the winding $N_1(N_2)$ at the nonshoot-through stage and the shoot-through stage, respectively

$$I_{\rm LB2aOFF}=i_{\rm PN}=\frac{V_{\rm PN}}{(1-D)R}=\frac{B_{\rm x}V_A}{(1-D)R}$$
$$I_{\rm LB2aON}=\frac{(B_{\rm x}-1)(1-D)}{D}I_{\rm LB2aOFF}. \quad (42)$$

On substituting (41) into (40), the boost factor of the MEBC 2 embedded basic modular boost circuit is

$$B_2=\frac{(2+2a-\gamma)(B_{\rm ideal}V_{\rm g}-B_{2,\rm ideal}V_{\rm F})DR}{k_1V_{\rm g}+((B_{2,\rm ideal}-1)\gamma^2+k_2V_{\rm g}} \quad (43)$$

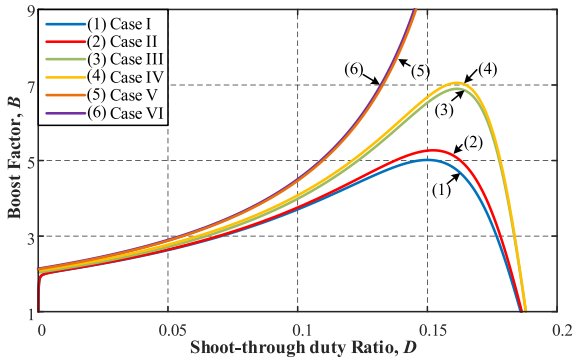


Fig. 17. Boost factor B versus D of EZSI ($n=2$) L-mSSCL.

where $B_{\rm ideal}=\frac{B^*_{2,\rm ideal}}{1-B^*_{2,\rm ideal}D}$, $B^*_{2,\rm ideal}=\frac{B_{1,\rm ideal}B_{2,\rm ideal}}{B_{1,\rm ideal}+B_{2,\rm ideal}-B_{1,\rm ideal}B_{2,\rm ideal}}$, $B_{2,\rm ideal}=\frac{(2-\gamma)}{(1-\gamma)(1-D)}$, $k_1=(1+\alpha-\gamma)(1-D)DB_{\rm ideal}R$, $B_{1,\rm ideal}=\frac{1}{(1-D)}$, $k_2=2(1+\alpha-\gamma)(1+\gamma(B_{2,\rm ideal}D-1)B_{\rm ideal}r_{\rm L}$.

Using (8), (16), and (43), the boost factor B of the proposed EZSI ($n=2$) L-mSSCL with the parasitic resistance and leakage inductance of the coupled inductor can be derived and be calculated by computer.

With the measured ESR of the components as shown in Table VI, we depicted the boost factor B as a function of shoot-through duty cycle D with the following six different cases.

Case I: $r_{L1}=0.25\,\Omega$, $r_{L21}=0.5\,\Omega$, $r_{\rm SW}=0.05\,\Omega$, $V_F=0.75\,{\rm V}$, $\alpha=0.04$, $\gamma=0.116$;
Case II: $r_{L1}=0.25\,\Omega$, $r_{L21}=0.5\,\Omega$, $r_{\rm SW}=0\,\Omega$, $V_F=0.75\,{\rm V}$, $\alpha=0.04$, $\gamma=0.116$;
Case III: $r_{L1}=0.25\,\Omega$, $r_{L21}=0\,\Omega$, $r_{\rm SW}=0\,\Omega$, $V_F=0.75\,{\rm V}$, $\alpha=0.04$, $\gamma=0.116$;
Case IV: $r_{L1}=0.25\,\Omega$, $r_{L21}=0\,\Omega$, $r_{\rm SW}=0\,\Omega$, $V_F=0\,{\rm V}$, $\alpha=0.04$, $\gamma=0.116$;
Case V: $r_{L1}=0\,\Omega$, $r_{L21}=0\,\Omega$, $r_{\rm SW}=0\,\Omega$, $V_F=0\,{\rm V}$, $\alpha=0.04$, $\gamma=0.116$;
Case VI: $r_{L1}=0\,\Omega$, $r_{L21}=0\,\Omega$, $r_{\rm SW}=0\,\Omega$, $V_F=0\,{\rm V}$, $\alpha=0$, $\gamma=0.116$.

Fig. 17 shows the boost factor of the proposed EZSI ($n=2$) L-mSSCL under the consideration of parasitic parameters. It can be seen from Fig. 17 that the boost capacity of the inverter is affected by the coupling coefficient k and ESR of the inductors. The ESR of the primary winding of coupled inductor and input inductor L_1 and L_2 of MEBC1 have a great effect on the boost capacity of the inverter. However, the coupling coefficient k of the coupled inductor has little effect on the boost capacity. Thus, we try our best to reduce the ESR of inductors and coupled inductor when designing the prototype.

To simplify the analysis of the inverter, the coupling coefficient k of the coupled inductor is chosen to be equal to 1, which means that the windings of the coupled inductor are fully coupled. In the absence of parasitic parameters, the peak dc-link

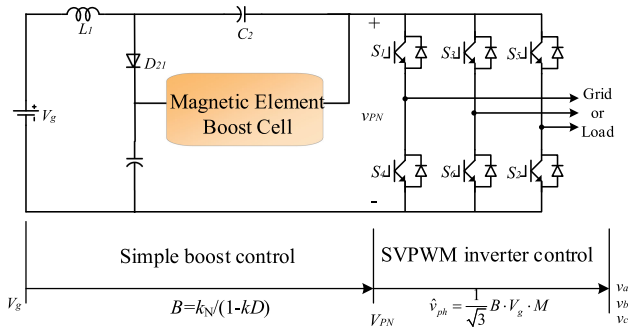


Fig. 18. Control strategy of the proposed EZSI.

voltage of the EZSI ($n = 2$) L-mSSCL can be simplified to

$$V_{\mathrm{PN}} = \frac{2-\gamma}{1-\gamma-(5-3\gamma)D} V_g. \tag{44}$$

In the simple boost control method [2], the shoot-through duty cycle D of the ZSIs can be expressed as

$$D = \frac{T_{\mathrm{sh}}}{T} = 1 - M \tag{45}$$

where T_{sh} is the shoot-through interval, T is the shoot-through periodic time, and M is the modulation index of the VSI.

The control of the proposed inverter is divided into two parts: controlling the shoot-through duty cycle D to achieve the boosting dc-link peak voltage, and controlling the modulation index M to realize the inversion. In fact, the two kinds of control are realized together. The main reason why a ZSI can use a set of switches of inverter bridge to achieve both dc-link boost and inversion functions is that there is no energy exchange between the dc-link and ac output of the VSI in the traditional zero state, and the switches of inverter bridge can be used to achieve the shoot-through state. The control strategy of the proposed inverter is shown in Fig. 18.

Fig. 19(a) shows the space vector diagram of the qZSI. The switching state pattern of the EZSI ($n = 2$) L-mSSCL is shown in Fig. 19(b), where a shoot-through state is injected at the center of the zero state.

By substituting (44) into (43), the boost factor B of the EZSI ($n = 2$) L-mSSCL can be rewritten in terms of M as

$$B = \frac{2-\gamma}{1-\gamma-(5-3\gamma)(1-M)} = \frac{1}{\frac{5-3\gamma}{2-\gamma}M - 2}. \tag{46}$$

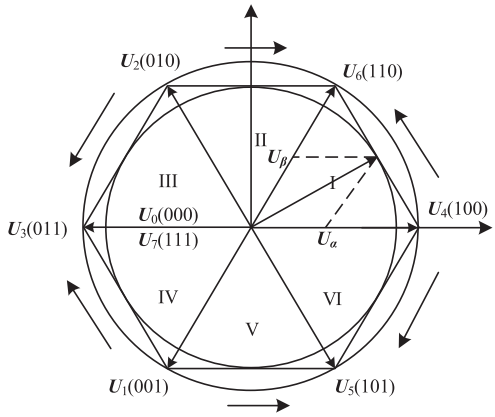
The output peak phase voltage of the three-phase voltage-source inverter is given by

$$\hat{v}_{ph} = \frac{V_g}{\sqrt{3}} BM = \frac{V_g}{\sqrt{3}} \frac{M}{\frac{5-3\gamma}{2-\gamma}M - 2}. \tag{47}$$

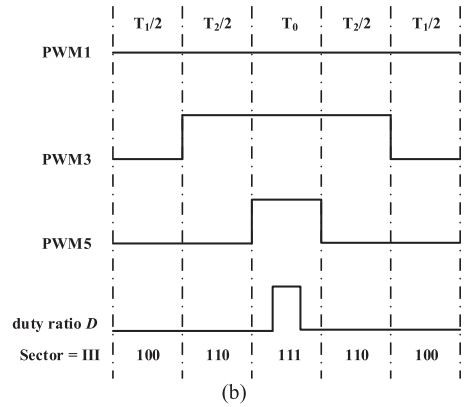
From (46), the voltage inversion gain G of the EZSI ($n = 2$) L-mSSCL can be defined as

$$G = \frac{\hat{v}_{ph}}{V_g} = \frac{BM}{\sqrt{3}} = \frac{M}{\sqrt{3}(\frac{5-3\gamma}{2-\gamma}M - 2)}. \tag{48}$$

In this section, we use the modular analysis method presented in Sections III and IV to derive the boost factor B of the inverter



(a)



(b)

Fig. 19 SVPWM control of the EZSI ($n = 2$) L-mSSCL. (a). Voltage space vectors and sectors. (b) Switching sequences in Sector III and the proposed scheme of injecting shoot-through state.

TABLE II
STATE VARIABLES OF THE TWO ANALYSIS METHODS

Traditional analysis	Modular analysis
10 dimensional equation of state	Equation (8)
	1-dimensional equation of state
	4-dimensional equation of state

and study the stress of the components. Compared with the traditional analysis method, the modular analysis method decouples the high-dimensional equation of state into several low-dimensional equations of state, which simplifies the calculation and analysis process. In the proposed EZSI ($n = 2$) L-mSSCL, there are up to ten state variables, which are decoupled into one 1-dimensional system, one 4-dimensional system, and equation (8) when analyzed with modularity. The state variables of the two analysis methods are shown in Table II.

B. Comparison Study

In order to further study the advantages of EZSI and the effectiveness and convenience of modular analysis method, we quantitatively compare the mSSCL qZSI in [20] with proposed EZSI ($n = 2$) L-mSSCL, including the stress of components and the efficiency of the inverter. The circuit diagram of the mSSCL

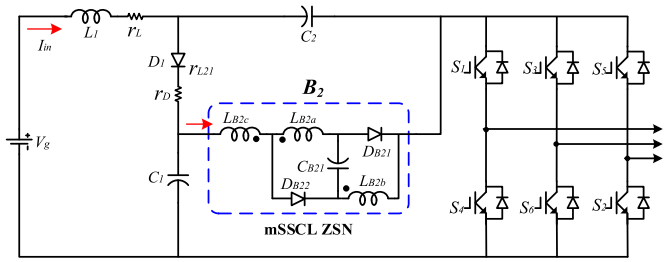


Fig. 20. mSSCL qZSI in [20].

TABLE III
VOLTAGE/CURRENT STRESS OF COMPETITORS

	mSSCL qZSI in [20]	Proposed EZSI(n=2) L- mSSCL
V	$V_{CB21}=\frac{M-\sqrt{3}G(2M-1)}{-2M}V_g$	$V_{CB21}=\frac{M-\sqrt{3}G(3M-2)}{-2M}V_g$
	$V_{DB21}=\frac{M-\sqrt{3}G(2M-1)}{-M^2}V_g$	$V_{DB21}=\frac{M-\sqrt{3}G(3M-2)}{-2M^2}V_g$
	$V_{DB22}=\frac{M-\sqrt{3}G(2M-1)}{-M^2}V_g$	$V_{DB22}=\frac{M-\sqrt{3}G(3M-2)}{-2M^2}V_g$
I	$I_{DB21}=\frac{1}{2(1-M)}I_{in}$	$I_{DB21}=\frac{1}{2(1-M)}I_{in}$
	$I_{LB2a}=\frac{6GM-3G-2\sqrt{3}M}{6G(1-M)}I_{in}$	$I_{LB2a}=\frac{12GM-9G-2\sqrt{3}M}{6G(1-M)}I_{in}$
	$I_{LB2b}=\frac{3GM-\sqrt{3}M}{3G(1-M)}I_{in}$	$I_{LB2b}=-\frac{6GM-3G-\sqrt{3}M}{3G(1-M)}I_{in}$
	$I_{CB21}=-\frac{3GM-3G-\sqrt{3}M}{3G(1-M)}I_{in}$	$I_{CB21}=-\frac{6GM-6G-\sqrt{3}M}{3G(1-M)}I_{in}$

qZSI is shown in Fig. 20. Both inverters have an identical MEBC (mSSCL), so the inverter performance is more comparable.

In the stress comparison study, the parasitic resistance is ignored. In this case, the stress of mSSCL qZSI and EZSI ($n = 2$) L-mSSCL can be obtained by (27), (28), (33), (34), and Table I, as shown in Table III.

Fig. 21 shows the comparison of voltage/current stresses on the corresponding components of mSSCL qZSI and proposed EZSI ($n = 2$) L-mSSCL. From Fig. 21(a) and (b), the current stresses on windings of the coupled inductor of EZSI ($n = 2$) L-mSSCL are much smaller than that of mSSCL qZSI under the condition of the same voltage inversion gain G. The voltage stress across the diode and capacitor is smaller than that of the mSSCL qZSI, which reduces the component cost.

Due to the low current and voltage stresses of the components in the MEBC, the proposed EZSI ($n = 2$) L-mSSCL can use components with low rated voltage/current to achieve high voltage and large current required by the three-phase inverter, which facilitates the modularization and standardization of the system and reduces costs.

An equivalent circuit of the proposed EZSI ($n = 2$) L-mSSCL with the parasitic resistances is shown in Fig. 22, where r_{CE} is the IGBT ON-resistance, R_F is the diode forward resistance, V_F is the diode threshold voltage, r_L is the ESR of the inductor L_1 and L_{B1}, r_C is the ESR of the capacitors, P_o is the output power

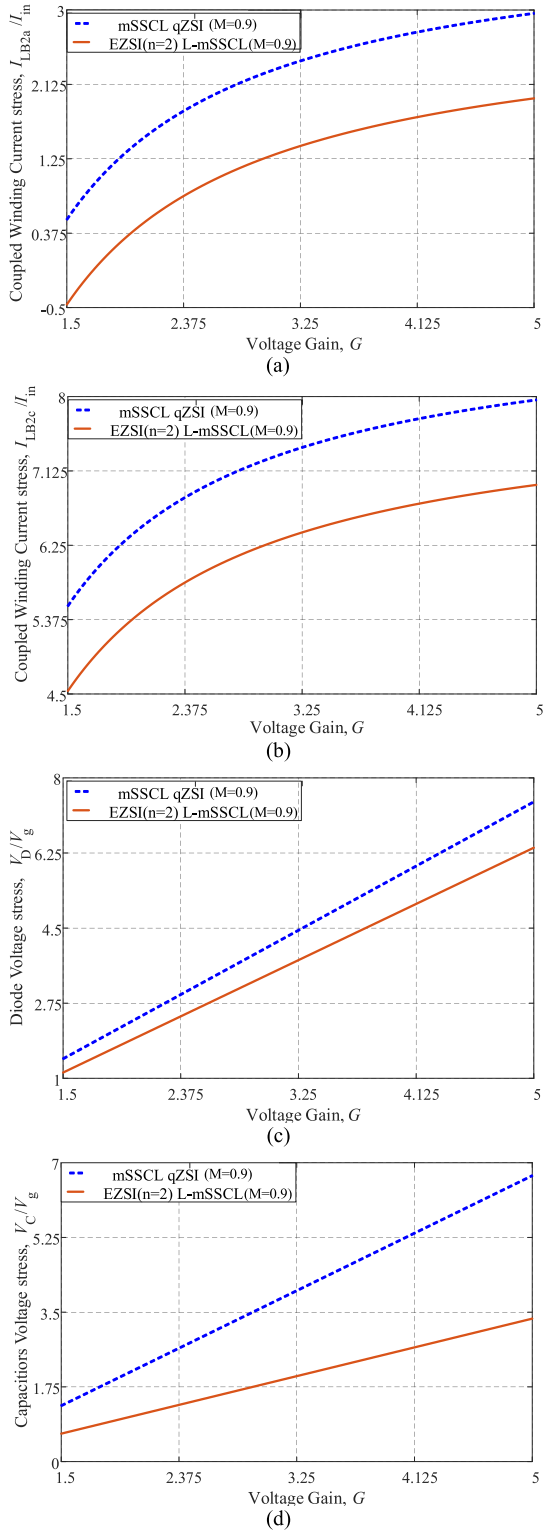


Fig. 21. Voltage/current stress comparison. (a) I_{LB2a}, (b) I_{LB2c}, (c) V_D, (d) V_C.

of the inverter, and C_{CE} is the junction capacitance between collector and emitter.

The conduction loss will be evaluated assuming that the inductor current i_{L1} is ripple free and equals the dc input current

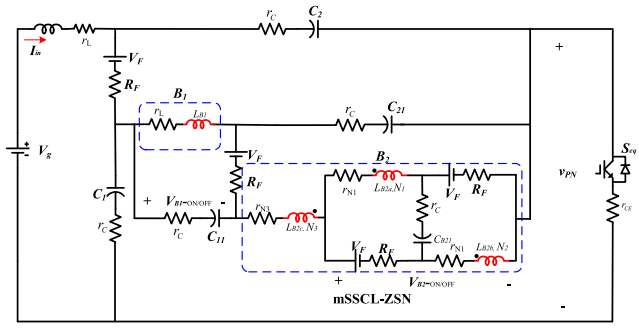


Fig. 22. Equivalent circuit of the EZSI ($n = 2$) L-mSSCL with parasitic resistances and the diode offset voltage.

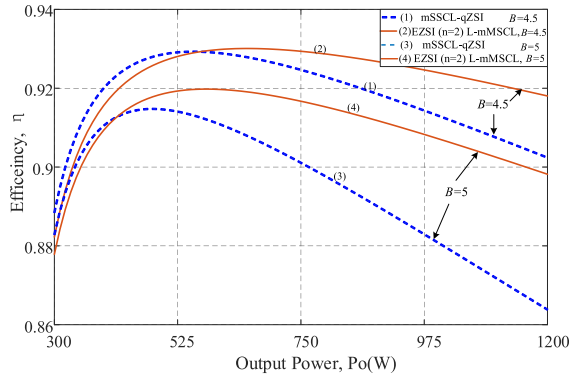


Fig. 23. Efficiency of the EZSI ($n = 2$) L-mSSCL and mSSCL qZSI versus output power $P_{\rm o}$.

$I_{\rm in}$. The switch current can be approximated by

$$i_{\rm sh} = \begin{cases} \frac{B-1}{BD} I_{in} = \frac{B-1}{D} I_o & 0 < t \le DT \\ 0 & DT < t \le T \end{cases} \tag{49}$$

resulting in its rms value

$$I_{\rm shrms} = \sqrt{\frac{1}{T}\int_0^T i_{\rm sh}^2 dt} = \frac{B-1}{\sqrt{D}} I_o = \frac{(B-1)P_o}{\sqrt{D}V_{\rm PN}}. \tag{50}$$

Thus, one obtains the total power dissipation in the IGBT as

$$\begin{aligned} P_{\rm IGBT} &= P_{r\rm CE} + \frac{1}{2} P_{\rm SWeq} \\ &= r_{\rm CE} \frac{2(B-1)^2 P_o^2}{3{V_{\rm PN}}^2} + \frac{3 f_s C_{\rm CE} {V_{\rm PN}}^2}{4}. \end{aligned} \tag{51}$$

Likewise, the overall diodes conduction loss is

$$P_D = P_{\rm VF} + P_{\rm RF} = \frac{B^2(3D+1)R_F P_o^2}{2(1-D)DV_{\rm PN}^2} + \frac{3BV_F P_o}{V_{\rm PN}}. \tag{52}$$

The inductor currents are

$$i_{L1} = i_{LB} = I_{in} = BI_o \tag{53}$$

$$\begin{aligned} i_{LB2a} &= i_{LB2b} \\ &= \begin{cases} \frac{B(1-4D)-2}{2BD} I_{\rm in} = \frac{B(1-4D)-2}{2D} I_o & 0 < t \le DT \\ \frac{1+2BD}{B(1-D)} I_{\rm in} = \frac{1+2BD}{(1-D)} I_o & DT < t \le T \end{cases} \end{aligned} \tag{54}$$

and the inductors loss is

$$\begin{aligned} P_{rL} &= r_L I_{L1\rm rms}^2 + r_L I_{LB1\rm rms}^2 + r_{N1}(I_{LB21\rm arms}^2 + I_{LB21\rm brms}^2) \\ &\quad + r_{N3} I_{LB21\rm crms}^2 \\ &= \frac{2B^2 r_L P_o^2}{V_{\rm PN}^2} + \frac{(B^2(24D^2-9D+1)+4B(5D-1)+4)r_{N1}P_o^2}{2(1-D)DV_{\rm PN}^2} \\ &\quad + \frac{(B^2(8D^2-5D+1)+B(6D-2)+1)r_{N2}P_o^2}{(1-D)DV_{\rm PN}^2} \end{aligned} \tag{55}$$

then, the power loss in capacitors is

$$\begin{aligned} P_{rC} &= r_C I_{C\rm rms}^2 \\ &= r_C(I_{C1\rm rms}^2 + I_{C2\rm rms}^2 + I_{C11\rm rms}^2 + I_{C21\rm rms}^2 + I_{CB21\rm rms}^2) \\ &= \frac{(B^2(11D^2-6D+2)+2B(5D-2)+3)r_C P_o^2}{(1-D)DV_{\rm PN}^2}. \end{aligned} \tag{56}$$

TABLE IV
MEASURED PARASITIC PARAMETERS OF THE INDUCTORS

Topologies	Parameter	Value	Parameter	Value
mSSCL	$r_{\rm N1}$	1.0 (Ω)	$r_{\rm N3}$	0.5 (Ω)
L-mSSCL	$r_{\rm N1}$	1.0 (Ω)	$r_{\rm N3}$	0.2 (Ω)

Therefore, the total power dissipation of the EZSI ($n = 2$) L-mSSCL is

$$\begin{aligned} P_{\rm LS} &= P_{\rm IGBT} + P_D + P_{rL} + P_{rC} \\ &= r_{\rm CE}\frac{2(B-1)^2 P_o^2}{3{V_{\rm PN}}^2} + \frac{3 f_s C_{\rm CE} V_{\rm PN}^2}{4} + \frac{B^2(3D+1)R_F P_o^2}{2(1-D)DV_{\rm PN}^2} \\ &\quad + \frac{3BV_F P_o}{V_{\rm PN}} \\ &\quad + \frac{((B^2(24D^2-9D+1)+4B(5D-1)+4)r_{N1}+2(B^2(8D^2-5D+1)}{2(1-D)DV_{\rm PN}^2} \\ &\quad + \frac{B(6D-2)+1)r_{N2}+4B^2(1-D)Dr_L)P_o^2}{2(1-D)DV_{\rm PN}^2} \\ &\quad + \frac{(B^2(11D^2-6D+2)+2B(5D-2)+3)r_C P_o^2}{(1-D)DV_{\rm PN}^2}. \end{aligned} \tag{57}$$

The power loss derivation of the mSSCL qZSI is similar to that of the proposed EZSI ($n = 2$) L-mSSCL.

Fig. 23 shows the efficiency η of the mSSCL qZSI and EZSI ($n = 2$) L-mSSCL as a function of the output power for $r_{\rm CE} = 0.05\ \Omega$, $R_{\rm F} = 0.008\ \Omega$, $V_{\rm F} = 0.75$ V, $r_{\rm L} = 0.25\Omega$, $r_{\rm C} = 0.003\ \Omega$, and $C_{\rm CE} = 2$ nF. The ESR of the coupled inductor is shown in Table IV.

It is apparent from Fig. 23 that the efficiency η of the EZSI ($n = 2$) L-mSSCL is much higher than that of mSSCL qZSI, and benefits from its high boosting capacity and low voltage/current stress of the components. With the increase of the boost factor B, the efficiency gap between EZSI ($n = 2$) L-mSSCL and mSSCL qZSI increases. It can be seen from Fig. 24 that the power loss of the inductors accounts for the highest proportion of total loss in qZSIs. In EZSI ($n = 2$) L-mSSCL, the loss of switches, diodes, inductors, and capacitors are 17 W, 32 W, 30 W, and 5 W at $P_{\rm o} = 1000$ W, respectively. The efficiency $\eta = 1000/(1000+84) = 92.3\%$.

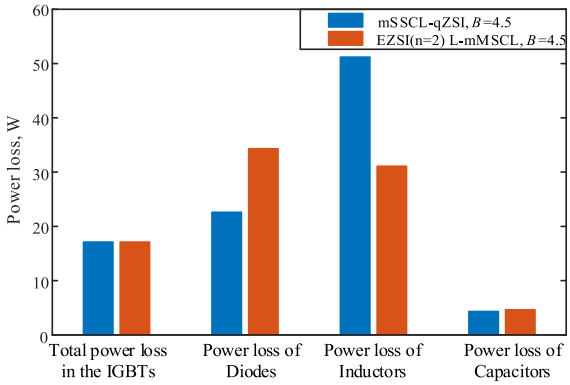


Fig. 24. Power loss distributions of the two qZSIs mentioned in this paper at $P_o = 1000$ W.

C. Inductor and Capacitor Design of the EZSI (n = 2) L-mSSCL

In the shoot-through state, the inductors will be charged by capacitors and input source. Hence, we will have

$$V_{\mathrm{L1(ON)}} = V_{\mathrm{g}} + V_{\mathrm{C2}} = (B - \frac{B}{B_{\mathrm{n}}^*} + 1)V_{\mathrm{g}} = L_1 \frac{di_{L1}}{dt} \quad (58)$$

$$V_{\mathrm{BL1(ON)}} = \frac{B}{B_n} V_{\mathrm{g}} = L_{\mathrm{BL1}} \frac{di_{\mathrm{BL1}}}{dt}. \quad (59)$$

The inductors can be designed as

$$L_{\mathrm{BL1}} = \frac{DT_{\mathrm{s}} V_{\mathrm{BL1(ON)}}}{r_{\mathrm{L}} i_{\mathrm{BL1}}} = \frac{D^2 B T_s V_{\mathrm{g}}}{r_{\mathrm{L}}(B_1 - 1) I_{\mathrm{in}}} = \frac{D^2 T_s R}{r_{\mathrm{L}}(B_1 - 1)B} \quad (60)$$

$$L_1 = \frac{DTV_{\mathrm{L1(ON)}}}{r_{\mathrm{L}} i_{\mathrm{L1}}} = \frac{B(1-D)DT_{\mathrm{s}} V_{\mathrm{g}}}{r_{\mathrm{L}} B \frac{V_{PN}}{R}} = \frac{(1-D)DT_s R}{r_{\mathrm{L}} B} \quad (61)$$

where R is the equivalent dc-link load, $R = \frac{8R_x(1-D)}{3M^2}$, R_x is the xth phase load, $x = a$, b, or c, T_{s} is the switching period, and r is the current ripple ratio, here $r = 0.2$.

In the shoot-through state, the capacitors' current is equal to inductors' current; hence, we have

$$i_{\mathrm{C1(ON)}} = \frac{B(1-D)-1}{BD} I_{\mathrm{in}} = C_1 \frac{dV_{C1}}{dt} \quad (62)$$

$$i_{\mathrm{C2(ON)}} = I_{\mathrm{in}} = C_2 \frac{dV_{C2}}{dt} \quad (63)$$

$$i_{\mathrm{C11(ON)}} = \frac{B_2 - 1}{B_2 D} I_{in} = C_{11} \frac{dV_{C11}}{dt} \quad (64)$$

$$i_{\mathrm{C21(ON)}} = \frac{B_1 - 1}{B_1 D} I_{in} = C_{21} \frac{dV_{C21}}{dt} \quad (65)$$

$$i_{\mathrm{CB21(ON)}} = \frac{1}{B_2 D} I_{in} = C_{B21} \frac{dV_{\mathrm{CB21}}}{dt}. \quad (66)$$

Thus, the capacitors can be calculated as

$$C_1 = \frac{DT_s i_{\mathrm{C1(ON)}}}{r_{\mathrm{v}} V_{\mathrm{C1}}} = \frac{\frac{B(1-D)-1}{BD} DT_s I_{\mathrm{in}}}{r_{\mathrm{v}}(1 + BD)V_g}$$

$$= \frac{(B(1-D)-1)T_{\mathrm{s}} B}{r_{\mathrm{v}}(1+BD)R} \quad (67)$$

$$C_2 = \frac{DT_s i_{\mathrm{C2(ON)}}}{r_v V_{\mathrm{C2}}} = \frac{DT_s I_{\mathrm{in}}}{r_v(B(1-D)-1)V_g}$$

$$= \frac{DT_s B^2}{r_v(B(1-D)-1)R} \quad (68)$$

$$C_{11} = \frac{DT_s i_{\mathrm{C11(ON)}}}{r_v V_{\mathrm{C11}}} = \frac{DT_s \frac{B_2-1}{B_2 D} I_{in}}{r_v(B - \frac{B}{B_1})V_{\mathrm{g}}} = \frac{T_s(B_2-1)B_1 B}{r_v(B_1-1)R} \quad (69)$$

$$C_{21} = \frac{DT_s i_{\mathrm{C21(ON)}}}{r_{\mathrm{v}} V_{\mathrm{C21}}} = \frac{DT_s \frac{B_1-1}{B_1 D} I_{in}}{r_{\mathrm{v}}(B - \frac{B}{B_2})V_{\mathrm{g}}} = \frac{T_s(B_1-1)B_2 B}{r_{\mathrm{v}}(B_2-1)R} \quad (70)$$

$$C_{\mathrm{B21}} = \frac{DT_s i_{\mathrm{CB21(ON)}}}{r_v V_{\mathrm{CB21}}} = \frac{DT_s \frac{1}{B_2 D} I_{in}}{r_v \frac{B}{(1-\gamma)B_2} V_g} = \frac{(1-\gamma)T_{\mathrm{s}} B}{r_v R} \quad (71)$$

where r_v is the voltage ripple ratio, and here $r_v = 0.02$.

An A_P method has been selected to design the coupled-inductor of MEBC 2 [47]. The effective cross-sectional area of core is

$$A_{\mathrm{P}} = A_{\mathrm{c}} W_{\mathrm{a}} = \left(\frac{P_{\mathrm{t}} \times 10^4}{J K_{\mathrm{u}} K_{\mathrm{f}} B_{\mathrm{m}} f_s} \right) \mathrm{cm}^4 \quad (72)$$

where P_{t} is the total apparent power, $P_{\mathrm{t}} = (1+\eta)P_{\mathrm{o}}/\eta$, J is current density, $J = K_{\mathrm{j}} {A_{\mathrm{P}}}^{0.125}$, K_{j} is the constant related to current density, $K_{\mathrm{j}} = 590$ A/cm^2, K_{u} is the window utilization factor, $K_{\mathrm{u}} = 0.4$, K_{f} is the waveform coefficient, $K_{\mathrm{f}} = 4$, B_{m} is the flux density, $B_{\mathrm{m}} = 0.2$T, and f_{s} is the frequency, $f_{\mathrm{s}} = 20$ kHz. Hence, A_{p} can be rewritten as

$$A_{\mathrm{P}} = A_{\mathrm{c}} W_{\mathrm{a}} = \left(\frac{P_{\mathrm{t}} \times 10^4}{K_{\mathrm{u}} K_{\mathrm{f}} K_{\mathrm{j}} B_{\mathrm{m}} f} \right)^{\frac{1}{1-0.125}} \mathrm{cm}^4. \quad (73)$$

Then, the core of coupled inductor and A_{c} can be selected by calculating the value of A_P.

In the shoot-through state, the voltage across excitation inductor L_{m} of the coupled inductor is

$$V_{\mathrm{LB2a(ON)}} = \frac{(1-D)}{1-\gamma-D(5-3\gamma)} V_{\mathrm{g}}. \quad (74)$$

The turns of windings can be expressed as

$$N_1 = N_2 = \frac{V_{\mathrm{LB21\_on}} \times 10^6}{K_{\mathrm{f}} f B_{\mathrm{m}} A_{\mathrm{c}}}, N_3 = \gamma N_1. \quad (75)$$

The excitation inductance L_{m} can be expressed as

$$L_{\mathrm{m}} = \frac{DT_s V_{\mathrm{LB21(ON)}}}{r I_{\mathrm{m}}} = \frac{DT_{\mathrm{s}} \frac{(1-D)}{1-\gamma-D(5-3\gamma)} V_{\mathrm{g}}}{r(1-\gamma) I_{\mathrm{in}}}. \quad (76)$$

D. Novel EZSI I (n = 1) SCΓZSN

Fig. 25 is a novel EZSI based on the switched-capacitor integrated Γ-Z-source network, named as EZSI I ($n = 1$) SCΓZSN.

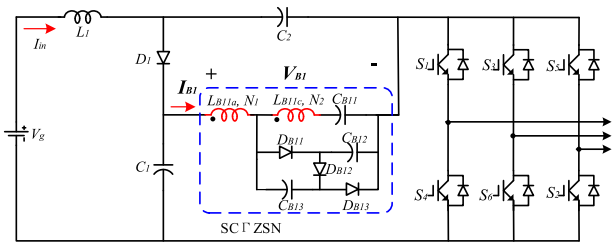
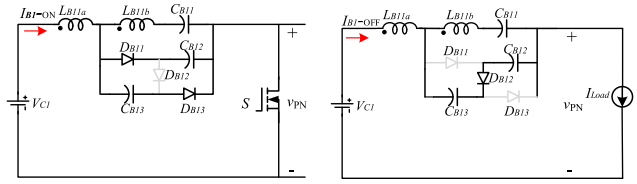


Fig. 25. EZSI I ($n = 1$) SCΓZSN.



(a) (b)

Fig. 26. EZSI I ($n = 1$) SCΓZSN. (a) Shoot-through state. (b) Nonshoot-through state.

It consists of a qZSI framework and a novel MEBC. The steady-state characteristic of the inverter is studied by using the modular analysis method presented in Sections III and IV.

*1) Steady-State Analysis of EZSI I (*n *= 1) SCΓZSN:* SCΓZSN-based basic modular boost circuit is shown in Fig. 26. The voltage equation at shoot-through state and nonshoot-through state can be written as

$$\begin{cases} V_{\mathrm{LB11}a\_\mathrm{ON}} = V_{\mathrm{CB12}} + V_{C1} \\ V_{\mathrm{LB11}b\_\mathrm{ON}} = -(V_{\mathrm{CB13}} + V_{\mathrm{CB12}}) \\ V_{\mathrm{LB11}a\_\mathrm{ON}} = nV_{\mathrm{LB11}b\_\mathrm{ON}} \end{cases} \\ \begin{cases} V_{\mathrm{LB11}a\_\mathrm{OFF}} = V_{\mathrm{CB12}} + V_{\mathrm{CB13}} - V_{\mathrm{PN}} + V_{C1} \\ V_{\mathrm{LB11}b\_\mathrm{OFF}} = -(V_{\mathrm{CB13}} + V_{\mathrm{CB12}}) \\ V_{\mathrm{LB11}a\_\mathrm{OFF}} = \gamma V_{\mathrm{LB11}b\_\mathrm{OFF}} \end{cases}. \tag{77}$$

Applying the volt–second balance principle to windings of the coupled-inductor, one has

$$\begin{cases} D \cdot V_{\mathrm{LB11}a\_\mathrm{ON}} + (1-D) \cdot V_{\mathrm{LB11}a\_\mathrm{OFF}} = 0 \\ D \cdot V_{\mathrm{LB11}b\_\mathrm{ON}} + (1-D) \cdot V_{\mathrm{LB11}b\_\mathrm{OFF}} = 0 \end{cases}. \tag{78}$$

The peak dc-link voltage V_{PN} is

$$V_{\mathrm{PN}} = \frac{1+\gamma}{1-\gamma-D} V_{C1} = B_1 V_{C1}. \tag{79}$$

By using (77) and (78), the capacitor and diode voltages can be expressed as

$$V_{\mathrm{CB11}} = \frac{\gamma(2-D)}{1-\gamma-D} V_g,\ V_{\mathrm{CB12}} = \frac{\gamma}{1-\gamma-D} V_g$$
$$V_{\mathrm{CB13}} = \frac{\gamma}{1-\gamma-D} V_g \tag{80}$$
$$V_{\mathrm{DB11}} = V_{\mathrm{DB12}} = V_{\mathrm{DB13}} = V_{\mathrm{CB12}} = V_{\mathrm{CB13}} = \frac{\gamma}{1-\gamma-D} V_g. \tag{81}$$

TABLE V
VOLTAGE/CURRENT STRESS OF EZSI I ($N = 1$) SCΓZSN

	EZSI(n=1) SCΓZSN
V	$V_{C1} = \frac{1-\gamma-D}{1-\gamma-(2+\gamma)D} V_g$, $V_{C2} = \frac{2\gamma+D}{1-\gamma-(2+\gamma)D} V_g$
	$V_{D1} = \frac{1+\gamma}{1-\gamma-(2+\gamma)D} V_g$, $V_{CB11} = \frac{\gamma(2-D)}{1-\gamma-(2+\gamma)D} V_g$
	$V_{CB12} = \frac{\gamma}{1-\gamma-(2+\gamma)D} V_g$, $V_{CB13} = \frac{\gamma}{1-\gamma-(2+\gamma)D} V_g$
I	$I_{D1} = \frac{1}{1-D} I_{in}$, $I_{C1\_ON} = \frac{B_1-1}{B_1 D} I_{in} = \frac{2\gamma+D}{(1+\gamma)D}$
	$I_{C2\_ON} = I_{in}$, $i_{DB12} = \frac{1}{1-D} I_{in}$, $i_{DB11} = i_{DB13} = \frac{1}{D} I_{in}$
	$i_{CB21\_ON} = \frac{2-D}{(1+\gamma)D} I_{in}$, $i_{CB21\_OFF} = \frac{2-D}{(1+\gamma)(1-D)} I_{in}$
	$i_{CB12\_ON} = i_{CB13\_ON} = \frac{1}{D} I_{in}$, $i_{CB12\_OFF} = i_{CB13\_OFF} = \frac{1}{1-D} I_{in}$

Substituting (79) into (9), the boost factor of the EZSI I ($n = 1$) SCΓZSN can be written

$$B = \frac{B_n^*}{1 - B_n^* D} = \frac{B_1}{1 - B_1 D} = \frac{1+\gamma}{1-\gamma-(2+\gamma)D}. \tag{82}$$

The current/voltage stress can be obtained by the modular analysis method easily, which is listed in Table V.

Using the modular analysis method, the steady-state analysis of a new EZSI is very convenient.

2) Comparison of Voltage and Current Stresses: The comparison of the boost factor and stresses on components of the proposed EZSI I ($n = 1$) SCFZSI with two existing promising inverters have been analyzed. The quantitative comparison of performance is shown in Table VI, and the visual stress comparison is shown in Fig. 27.

3) Comparison of Magnetic Elements: For the same input source V_{g}, voltage gain G, and load R_x, all the three inverters have the same average input current I_{in}, but different current ripple and flux density swings for the same L_1, the same number of turns, and the core size of inductor. The input inductor current ripple Δi_{L1} and the flux density swing ΔB are given as

$$\Delta i_{L1} = \frac{V_{L1}}{L_1} DT \tag{83}$$
$$\Delta B = \mu \frac{N}{l} \Delta i = \mu \frac{N}{l} \cdot \frac{V_{L1}}{L_1} DT$$
$$= \mu \frac{N}{l} \cdot \frac{V_{L1}}{\frac{\mu A_e N^2}{l}} DT = \frac{V_{L1}}{N A_e} DT \tag{84}$$

where V_{L1} is the voltage across input inductor L_1 during the shoot-through interval, DT is the shoot-through interval, N is the number of the turns of input inductor L_1, and A_{e} is the core cross-sectional area of the L_1.

From (84), the input inductor current ripple and flux density swing of the three candidates are directly proportional to

TABLE VI
COMPARISON OF THE PROPOSED EZSI ($N = 1$) SCΓZSI AND SCL QZSI, MSSCL QZSI

	SCL qZSI	mSSCL qZSI	EZSI I (n=1) SCΓZSN
No. of diodes	3	3	4
No. of passive elements	3-windings CL 3 capacitors	3-windings CL 3 capacitors	2-windings CL 5 capacitors
Boost Factor	$\frac{n+2}{1-(3+n)D}$	$\frac{2-n}{1-n-(3-2n)D}$	$\frac{1+n}{1-n-(2+n)D}$
Capacitors Voltage stress	$V_{C21}=\frac{\sqrt{3}G(2M-1)-M}{M}V_g$	$V_{C21}=\frac{\sqrt{3}G(2M-1)-M}{M}V_g$	$V_{CB12}=V_{CB13}=\frac{\sqrt{3}G(2M-1)-M}{M(M+1)}V_g$ $V_{CB11}=\frac{\sqrt{3}G(2M-1)-M}{M}V_g$
Diodes Voltage stress	$V_{DB21}=V_{DB22}=\frac{\sqrt{3}G(2M-1)-M}{M^2}V_g$	$V_{DB21}=V_{DB22}=\frac{\sqrt{3}G(2M-1)-M}{M^2}V_g$	$V_{DB11}=V_{DB12}=V_{DB13}=\frac{\sqrt{3}G(2M-1)-M}{M(M+1)}V_g$
Coupled Windings Current stress	$I_{L21a}=\frac{6GM-3G-2\sqrt{3}M}{6G(1-M)}I_{in}$ $I_{L21c}=-\frac{3GM-6G-\sqrt{3}M}{3G(1-M)}I_{in}$	$I_{L21a}=\frac{6GM-3G-2\sqrt{3}M}{6G(1-M)}I_{in}$ $I_{L21c}=\frac{3GM-\sqrt{3}M}{3G(1-M)}I_{in}$	$I_{LB11a}=\frac{3GM-\sqrt{3}M}{3G(1-M)}I_{in}$ $I_{LB11b}=\frac{M-\sqrt{3}G(M-2)}{\sqrt{3}G(1-M)}I_{in}$

shoot-through duty ratio D. D is represented by voltage gain G

$$\begin{cases} D_{\mathrm{SC\Gamma}} = \frac{3G(\gamma-1)+\sqrt{3}(\gamma+1)}{\sqrt{3}(\gamma+1)-3G(\gamma+2)} \\ D_{\mathrm{SCL}} = \frac{\sqrt{3}(\gamma+2)-3G}{\sqrt{3}(\gamma+2)-3(\gamma+3)G} \\ D_{\mathrm{mSSCL}} = \frac{\sqrt{3}(\gamma-2)-3(\gamma-1)G}{(9-6\gamma)G+\sqrt{3}(\gamma-2)} \end{cases}. \tag{85}$$

By substituting the values of D from (84) into (85), and giving $\gamma = 0.443$, the normalized input current ripple and flux density swing for the three inverters are plotted in Fig. 28. It is apparent that for the same voltage gain G, the EZSI I ($n = 1$) SCΓZSI has a smaller input current ripple and flux density swing compared to other two qZSIs.

Suppose that the inverters have the same total number of turns N_{tot} of the coupled inductor (three windings in SCL qZSI and mSSCL qZSI, while two windings in the EZSI I ($n = 1$) SCΓZSI), the core sizes are compared. The flux density swing of the coupled inductor can be expressed as

$$\Delta B = \frac{V_{Nx}T}{N_x A_e}D, \tag{86}$$

where N_x is the number of the windings.

During the shoot-through interval, we have

$$\begin{cases} V_{\mathrm{Na\_SC\Gamma}} = \frac{\sqrt{3}G}{(\gamma+1)}V_g \\ V_{\mathrm{Na\_SCL}} = \frac{\sqrt{3}G}{2+\gamma}V_g \\ V_{\mathrm{Na\_mSSCL}} = \frac{\sqrt{3}G}{2-\gamma}V_g \end{cases} \tag{87}$$
$$\begin{cases} N_a^{\mathrm{SC\Gamma}} = \frac{1}{1+\gamma}N_{\mathrm{tot}} \\ N_a^{\mathrm{SCL}} = \frac{1}{2+\gamma}N_{\mathrm{tot}} \\ N_a^{\mathrm{mSSCL}} = \frac{1}{2-\gamma}N_{\mathrm{tot}} \end{cases}$$

where V_{Na_x} is the voltage stress across the primary winding of the coupled inductor.

On substituting the voltage stress of the windings and number of turns from (87) into (86), the normalized flux density swing ΔB for the candidates are

$$\begin{aligned} \tfrac{N_{\mathrm{tot}}A_e}{V_g T}\Delta B_{\mathrm{SC\Gamma}} &= \sqrt{3}GD_{\mathrm{SC\Gamma}} = \tfrac{(3G(\gamma-1)+\sqrt{3}(\gamma+1))G}{(\gamma+1)-\sqrt{3}G(\gamma+2)} \\ \tfrac{N_{\mathrm{tot}}A_e}{V_g T}\Delta B_{\mathrm{SCL}} &= \sqrt{3}GD_{\mathrm{SCL}} = \tfrac{(\sqrt{3}(\gamma+2)-3G)G}{(\gamma+2)-\sqrt{3}(\gamma+3)G} \\ \tfrac{N_{\mathrm{tot}}A_e}{V_g T}\Delta B_{\mathrm{mSSCL}} &= \sqrt{3}GD_{\mathrm{mSSCL}} = \tfrac{(\sqrt{3}(\gamma-2)-3(\gamma-1)G)G}{\sqrt{3}(3-2\gamma)G+(\gamma-2)}. \end{aligned} \tag{88}$$

Fig. 29 shows the normalized flux density swing of the couple inductor as a function of the voltage gain G with $\gamma = 0.443$. It can be observed that for the same core cross-sectional area A_{e} and total number of turns for the two windings (L_{B11a}, L_{B11b}) as that for three windings (L_{B21a}, L_{B21b}, and L_{B21c}) for SCL and mSSCL, the coupled inductor of EZSI I ($n = 1$) SCΓZSI has a lower ΔB and, hence, a lower core loss.

VI. EXPERIMENTAL RESULTS

The proposed EZSI ($n = 2$) L-mSSCL and EZSI ($n = 1$) SCΓZSN were built in laboratory to validate the analysis. The system parameters of EZSI ($n = 2$) L-mSSCL and EZSI ($n = 1$) SCΓZSN are shown in Tables VII and VIII, respectively. The experiment used three-phase ac outputs loaded with three 50 Ω resistive loads in a Y-connection. The control board is composed of a DSP controller (TMS320F28335), driving, and protection circuit.

Fig. 30 shows the experimental results for the proposed EZSI ($n = 2$) L-mSSCL with a shoot-through duty cycle of $D = 0.1$ and a modulation index of $M = 0.90$. From Fig. 30(a) and (b), one can observe that the capacitor voltages' V_{C1} and V_{C2} are boosted to 100 and 186 V in the steady state, which is slightly smaller than the calculated result by (20), resulting from power loss of ESR of the components. The peak dc-link voltage V_{PN} is boosted to 310 V. Hence, the boost factor of the dc-link voltage can be calculated to be 310/80 = 3.87.

The proposed EZSI ($n = 2$) L-mSSCL has a continuous input current, and obtains low voltage overshoot across the

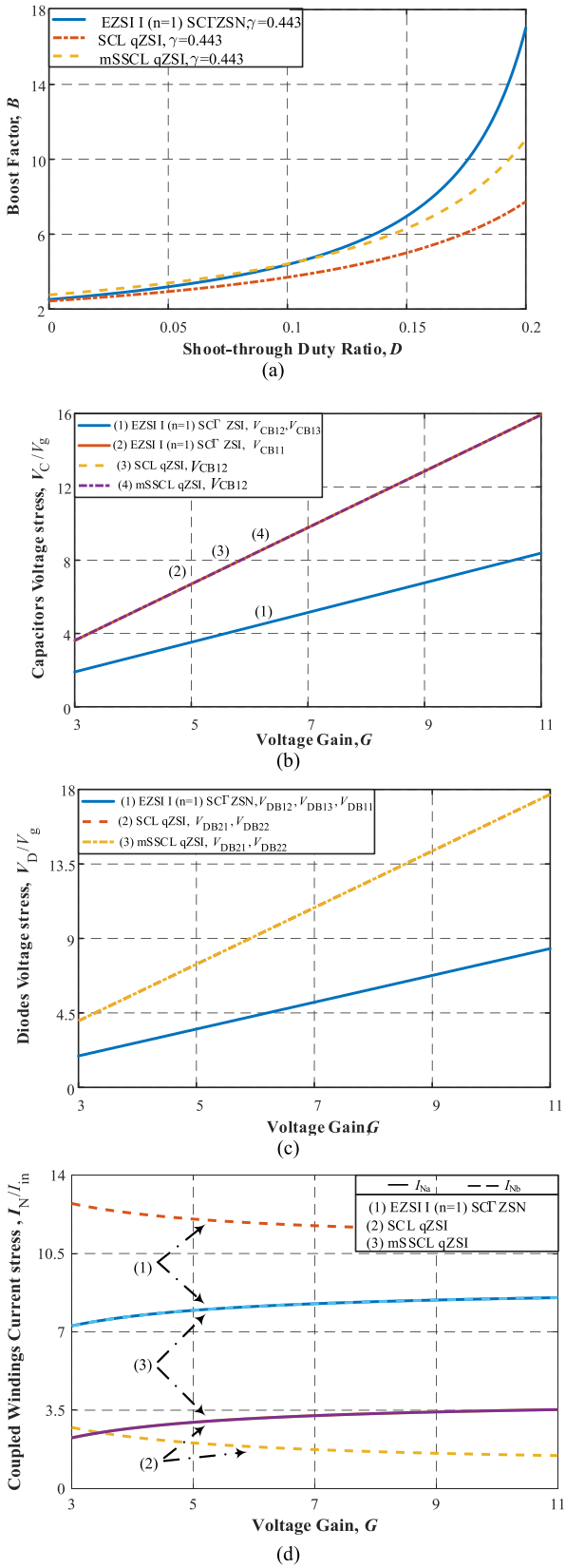


Fig. 27. Comparison of EZSI I ($n = 1$) SCΓZSN and existing promising inverters. (a) Boost factor versus shoot-through duty ratio. (b) Capacitor voltage stress. (c) Diode voltage stress. (d) Current stress on coupled-inductor.

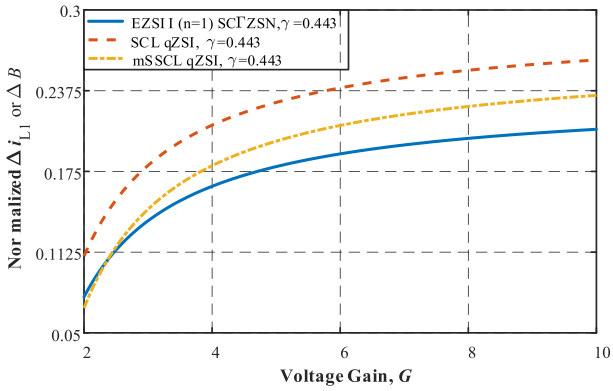


Fig. 28. Comparison of normalized input inductor current and flux density swing.

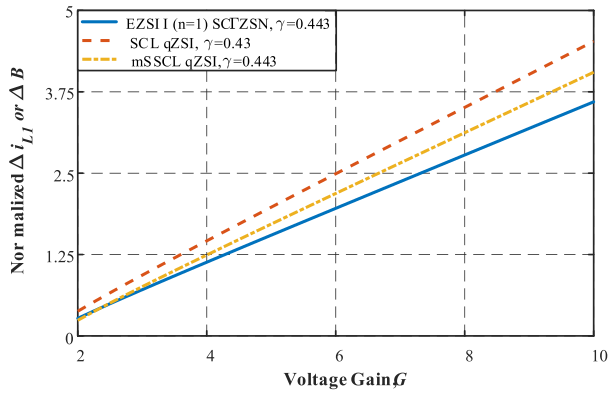


Fig. 29. Comparison of normalized flux density swing and inductor current ripple for coupled-inductor of the candidates.

TABLE VII
SYSTEM PARAMETERS OF Fig. 15

	Parameter	Value
Output stage	Output phase voltage	120 V_{RMS}
	Frequency	60 Hz
Input stage	Input voltage V_g	80 V
Inverter	Rated power P	1 kVA
	Switching frequency f_s	20 kHz
	Outer filter inductor L_f	1 mH
	Outer filter capacitor C_f	50 μF
	Inductor L_1	500 μH
	Capacitor C_1,C_2	470 μF
L	Inductors L_{B1}	500 μH
mSSCL	Inductor L_{B21a}	500 μH
	Transformer turn ratio γ	0.116
	Capacitor C_{B21}	100 μF

H-bridge due to its high-frequency capacitive current loop. From Fig. 30(b), we can observe that the output peak phase voltage is $v_a = 168\ V_{\rm ac}$, which is basically consistent with the theoretical analysis, as shown in (47) and (48). Fig. 30(c) shows the voltage

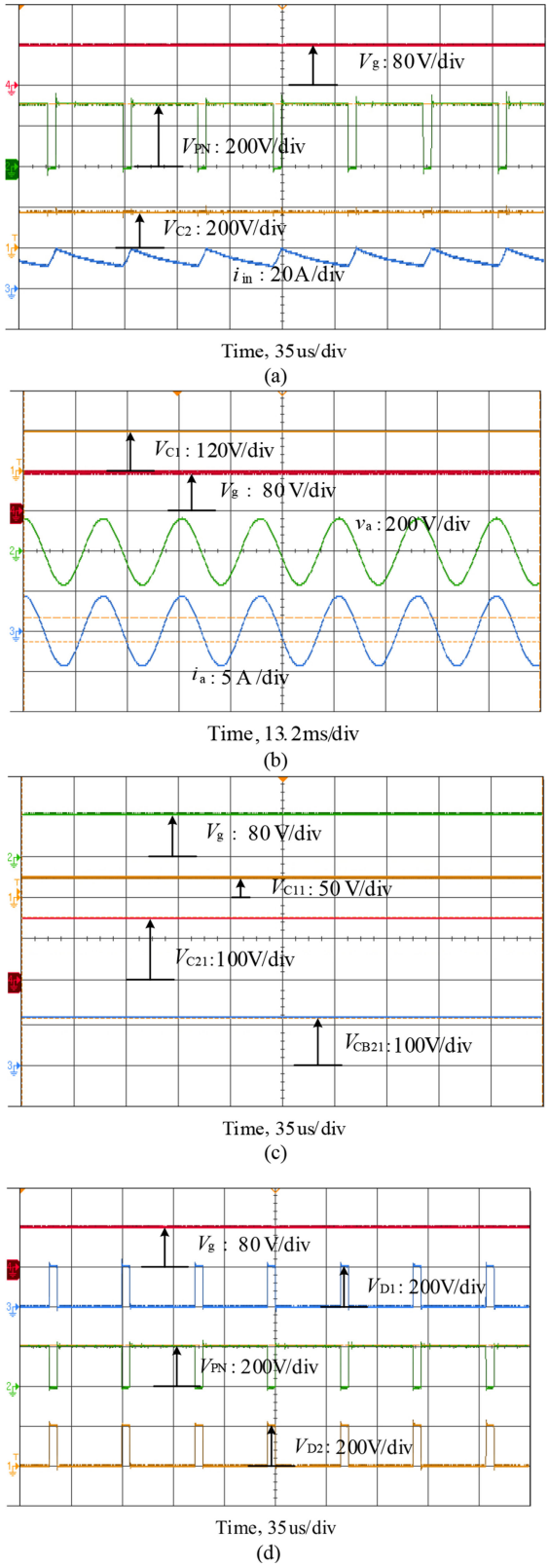


Fig. 30. Experimental results of the proposed EZSI ($n = 2$) L-mSSCL. (a) Source voltage V_g, V_{C2}, V_{PN}, i_{in}. (b) V_g, V_{C1}, output phase voltage v_a, output phase current i_a; (c) V_g, V_{C21}, V_{C11}, V_{CB21}. (d) V_g, V_{D1}, V_{D2}, V_{PN}.

TABLE VIII
SYSTEM PARAMETERS OF Fig. 25

	Parameter	Value
Output stage	Output phase voltage	120 V_{RMS}
	Frequency	60 Hz
Input stage	Input voltage V_g	80 V
Inverter	Rated power P_o	1 kVA
	Switching frequency f_s	10 kHz
	Outer filter inductor L_f	1 mH
	Outer filter capacitor C_f	50 μF
	Inductor L_1	500 μH
	Capacitor C_1,C_2	470 μF
SCΓZSN	Inductor L_{B21a}	504 μH
	Transformer turn ratio γ	0.443
	Capacitors C_{B11}, C_{B12}, C_{B13}	100 μF

stress of capacitors V_{C11}, V_{C21}, and V_{CB21}. The results are consistent with the theoretical analysis.

The voltage stress waveforms of the diodes are shown in Fig. 30(d), and the voltage results are almost consistent with those of the theoretical analysis, as shown in Table III.

Fig. 31 shows the corresponding experimental results of novel EZSI ($n = 1$) SCΓZSN in a simple boost control strategy. The coupling coefficient of the coupled inductor of the improved coupled inductor is $k = 1/(1+(7.2/504)) = 0.986$. The peak dc-link voltage is boosted to 316 V from the input source voltage 100 V. The experimental dc boost factor is, thus, about 3.2 times, which is reflected by V_{PN} and V_g in the traces of Fig. 28(a). The capacitor voltage can be boosted to $V_{C1} = 120$ V and $V_{C2} = 200$ V. Similar to EZSI II ($n = 2$) L-mSSCL, the novel EZSI ($n = 1$) SCΓZSN also has a continuous input current and low dc-link voltage overshoot. The output peak phase voltage can boost to $v_a = 168$ V_{ac}; hence the inversion gain $G = 168/100 = 1.68$, as shown in Fig. 31(b). Fig. 31(c) and (d) shows the capacitors voltage V_{CB11}, V_{CB12}, V_{CB13}, diodes voltage v_{DB11}, v_{DB12}, v_{DB13}, and peak dc-link voltage, respectively. The results are basically the same as theoretical analysis.

Fig. 31(e) shows the current waveforms of the windings N_1 and N_2. During the shoot-through state, the capacitor C_1 and series capacitor C_{B12} (C_{B13}) transfer their energy to winding N_1, and the currents i_{N1} increases linearly. The capacitor C_{B12} (C_{B13}) transfer its energy to winding N_2 and C_{B11}, and the currents i_{N2} increase linearly. Since capacitor C_{B11} changes from the discharge state to the charging state, thus, at the beginning of charging, the current increases rapidly. After the shoot-through state, the inverter enters the traditional zero state, where there is no energy exchange between the dc-link and the ac output. In this interval, the windings N_1 and N_2, dc source V_g, and the input inductor L_1 together charge the capacitor C_2, and the current i_{N1}, i_{N2} drops rapidly. During the nonshoot-through state, the windings N_1 and N_2 release their energy to the output, and the current in windings change gently.

The measured efficiency curves of the proposed EZSI ($n = 2$) L-mSSCL and mSSCL qZSI as a function of output power

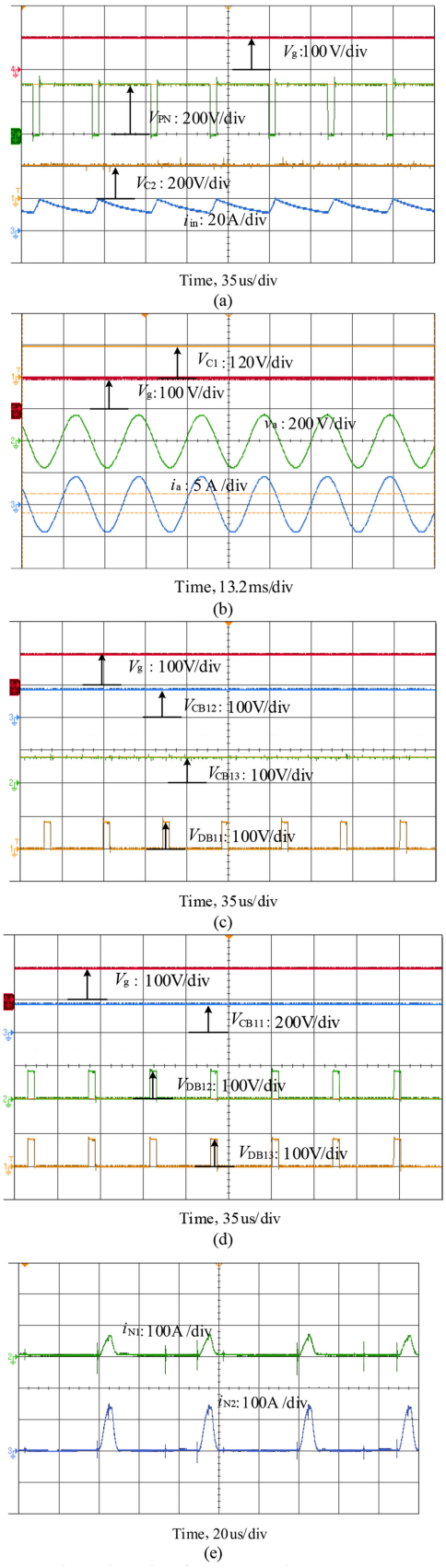


Fig. 31. Experimental results of the proposed EZSI ($n = 1$) SCΓZSN. (a) Source voltage V_g, V_{C2}, V_{PN}, i_{in}. (b) V_g, V_{C1}, output phase voltage v_a, output phase current i_a. (c) V_g, V_{CB12}, V_{CB13}, V_{DB11}. (d) V_g, V_{CB11}, V_{DB12}, V_{DB13}. (e) i_{N1}, i_{N2}.

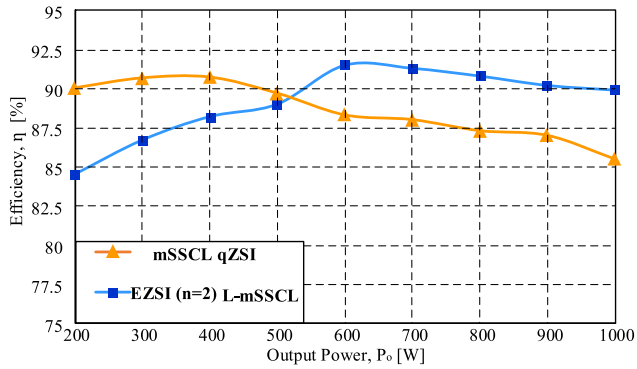


Fig. 32. Measurement efficiency versus P_o for proposed EZSI ($n = 2$) *L*-mSSCL and mSSCL qZSI.

P_o at $V_g = 80$ V are shown in Fig. 32. From Fig. 32, we can obtain that the maximum efficiency of proposed EZSI ($n = 2$) *L*-mSSCL occurs at half the rated power, reaching 91.5%. At the rated power of the inverter, the efficiency of EZSI ($n = 2$) *L*-mSSCL is higher than that of mSSCL qZSI, with an efficiency value of 90%.

VII. Conclusion

This article proposes an EZSI architecture. By selecting different MEBCs, arbitrary buck–boost voltage conversion is achieved at the ac output of the inverter. By combining different MEBCs, several new types of ZSIs can be presented. The proposed architecture calculates voltage gain of an inverter, and voltage and current stresses of a component in a modular manner. Thus, it simplifies inverter analysis and improves accuracy of theoretical analysis. In traditional ZSIs, the shoot-through current of the MEBCs is relatively high, while the voltage of the MEBCs is relatively high in the nonshoot-through state. For the proposed EZSIs, the MEBCs are charged in parallel in the case of the shoot-through state, which reduces the current stress of components inside the MEBCs. In the nonshoot-through state, the MEBCs are discharged in series, which decreases the voltage stress of components inside the MEBCs. This modular circuit facilitates the design of high-power ZSIs by using low-voltage small-current components to reduce the system cost. In addition, the modular architecture facilitates further system expansion.

Appendix

Additional comparison of the one-stage EZSI ($n = 1$) and two-stage EZSI ($n = 2$) competitors have been performed in this Appendix.

We have added a comparison of three other sets of inverters, namely, CMVR I qZSI in [49], CMVR II qZSI in [49], SCL qZSI in [41], and their corresponding two-stage EZSI ($n = 2$) L-CMVR I, EZSI ($n = 2$) L-CMVR II, and EZSI ($n = 2$) L-SCL. The diagrams of the abovementioned inverters are shown in Fig. 33.

The calculated voltage/current stress is shown in Tables IX –XI, respectively. A visual comparison of the stresses is shown in Fig. 34.

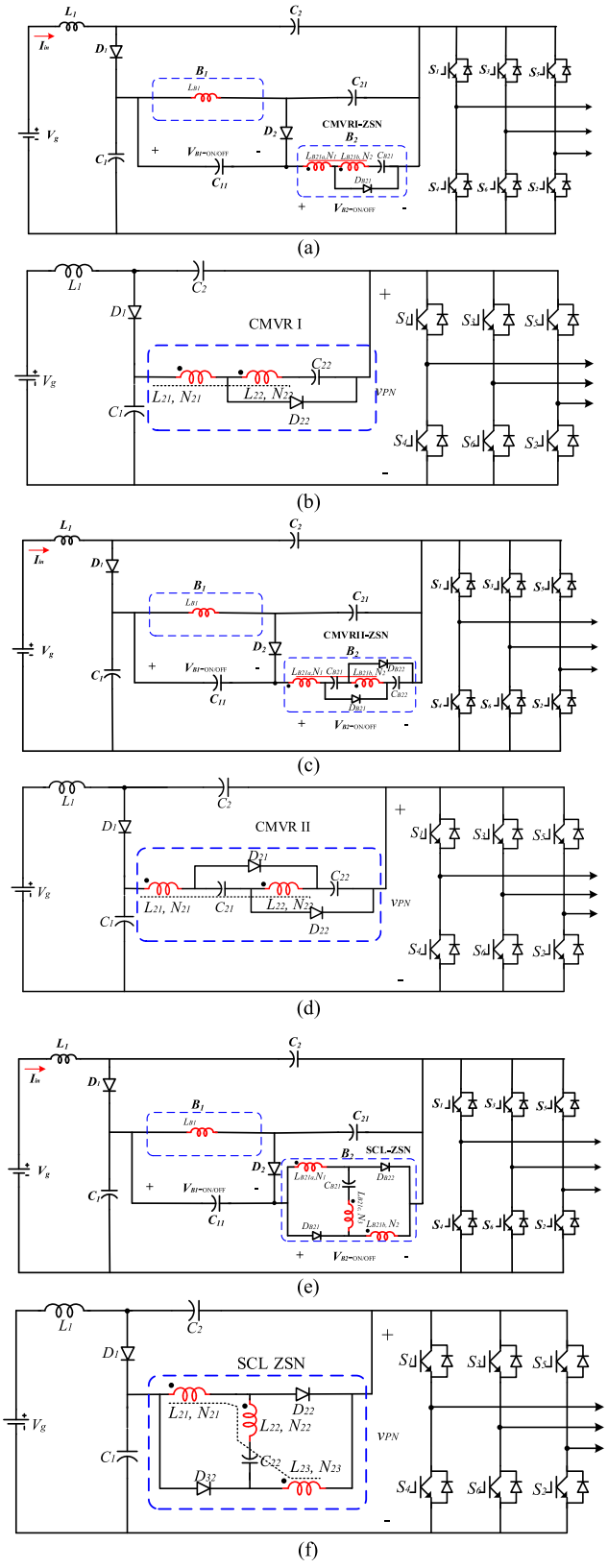


Fig. 33. Diagram of the competitors. (a) EZSI ($n = 2$) L-CMVR I, (b) CMVR I qZSI in [49], (c) EZSI ($n = 2$) L-CMVR II, (d) CMVR II qZSI in [49], (e) EZSI ($n = 2$) L-SCL, (f) SCL qZSI in [41].

TABLE IX
VOLTAGE/CURRENT STRESS OF EZSI ($N = 1$) CMVR I AND EZSI ($N = 2$) L-CMVR I

Stress	EZSI (n=1) CMVR I	EZSI (n=2) L- CMVR I
V_C	$V_{C21}=\frac{M-\sqrt{3}G(2M-1)}{-2M}V_g$	$V_{CB21}=\frac{M-\sqrt{3}G(3M-2)}{-2M}V_g$
V_D	$V_{D21}=\frac{M-\sqrt{3}G(2M-1)}{-M^2}V_g$	$V_{DB21}=\frac{M-\sqrt{3}G(3M-2)}{-M^2}V_g$
I_D	$I_{D21}=\frac{1}{1-M}I_{in}$	$I_{DB21}=\frac{1}{1-M}I_{in}$
I_N	$I_{L21a}=\frac{3GM-\sqrt{3}M}{3G(1-M)}I_{in}$	$I_{LB21a}=\frac{6GM-3G-\sqrt{3}M}{3G(1-M)}I_{in}$
	$I_{L21b}=-\frac{3GM-3G-\sqrt{3}M}{3G(1-M)}I_{in}$	$I_{LB21b}=-\frac{6GM-6G-\sqrt{3}M}{3G(1-M)}I_{in}$
I_C	$I_{C21}=-\frac{3GM-3G-\sqrt{3}M}{3G(1-M)}I_{in}$	$I_{CB21}=-\frac{6GM-6G-\sqrt{3}M}{3G(1-M)}I_{in}$

TABLE X
VOLTAGE/CURRENT STRESS OF EZSI ($N = 1$) CMVR II AND EZSI ($N = 2$) L-CMVR II

Stress	EZSI (n=1) CMVR II	EZSI (n=2) L-CMVR II
V_C	$V_{C21}=\frac{M-\sqrt{3}G(2M-1)}{-2M}V_g$	$V_{CB21}=\frac{M-\sqrt{3}G(3M-2)}{-2M}V_g$
	$V_{C22}=\frac{M-\sqrt{3}G(2M-1)}{-2M}V_g$	$V_{CB22}=\frac{M-\sqrt{3}G(3M-2)}{-2M}V_g$
V_D	$V_{D21}=\frac{M-\sqrt{3}G(2M-1)}{-M^2}V_g$	$V_{DB21}=\frac{M-\sqrt{3}G(3M-2)}{-2M^2}V_g$
	$V_{D22}=\frac{M-\sqrt{3}G(2M-1)}{-M^2}V_g$	$V_{DB22}=\frac{M-\sqrt{3}G(3M-2)}{-2M^2}V_g$
I_D	$I_{D21}=\frac{1}{1-M}I_{in}$	$I_{DB21}=\frac{1}{1-M}I_{in}$
I_N	$I_{L21a}=\frac{3GM-\sqrt{3}M}{3G(1-M)}I_{in}$	$I_{LB21a}=\frac{6GM-3G-\sqrt{3}M}{3G(1-M)}I_{in}$
	$I_{L21b}=-\frac{3GM-6G-\sqrt{3}M}{3G(1-M)}I_{in}$	$I_{LB21b}=-\frac{6GM-9G-\sqrt{3}M}{3G(1-M)}I_{in}$
I_C	$I_{C21}=-\frac{3GM-3G-\sqrt{3}M}{3G(1-M)}I_{in}$	$I_{CB21}=-\frac{6GM-6G-\sqrt{3}M}{3G(1-M)}I_{in}$

TABLE XI
VOLTAGE/CURRENT STRESS OF EZSI ($N = 1$) SCL AND EZSI ($N = 2$) L-SCL

Stress	EZSI (n=1) SCL	EZSI (n=2) L- SCL
V_C	$V_{C21}=\frac{M-\sqrt{3}G(2M-1)}{-2M}V_g$	$V_{CB21}=\frac{M-\sqrt{3}G(3M-2)}{-2M}V_g$
V_D	$V_{D21}=\frac{M-\sqrt{3}G(2M-1)}{-M^2}V_g$	$V_{DB21}=\frac{M-\sqrt{3}G(3M-2)}{-2M^2}V_g$
	$V_{D22}=\frac{M-\sqrt{3}G(2M-1)}{-M^2}V_g$	$V_{DB22}=\frac{M-\sqrt{3}G(3M-2)}{-2M^2}V_g$
I_D	$I_{D21}=\frac{1}{2(1-M)}I_{in}$	$I_{DB21}=\frac{1}{2(1-M)}I_{in}$
I_N	$I_{L21a}=\frac{6GM-3G-2\sqrt{3}M}{6G(1-M)}I_{in}$	$I_{LB21a}=\frac{12GM-9G-2\sqrt{3}M}{6G(1-M)}I_{in}$
	$I_{L21b}=-\frac{3GM-6G-\sqrt{3}M}{3G(1-M)}I_{in}$	$I_{LB21b}=-\frac{6GM-6G-\sqrt{3}M}{3G(1-M)}I_{in}$
I_C	$I_{C21}=-\frac{3GM-3G-\sqrt{3}M}{3G(1-M)}I_{in}$	$I_{CB21}=-\frac{6GM-6G-\sqrt{3}M}{3G(1-M)}I_{in}$

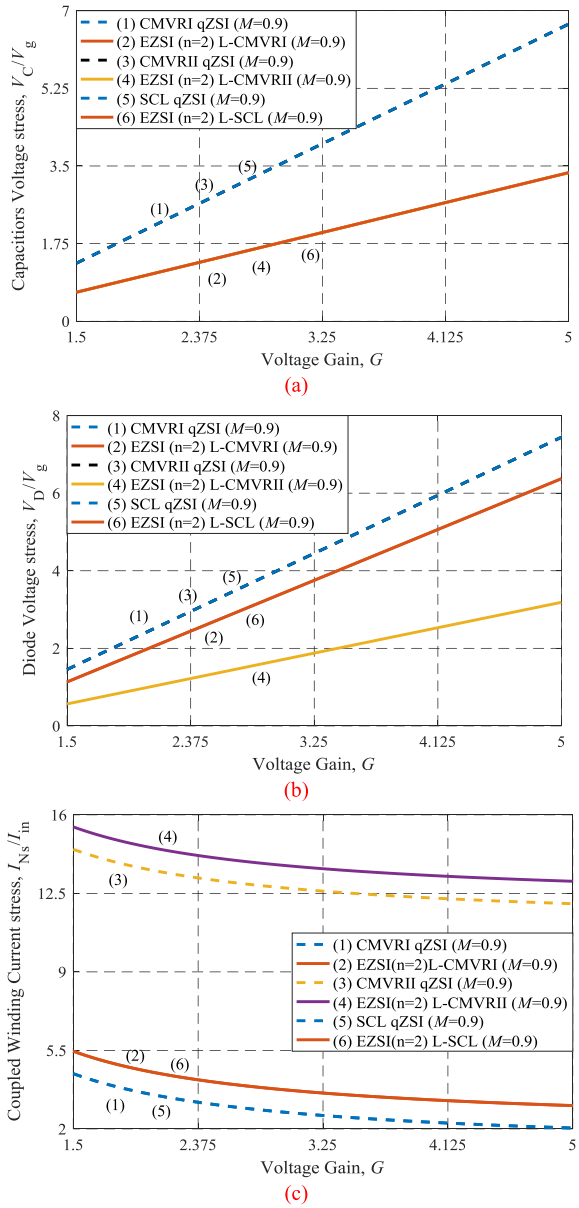


Fig. 34. Voltage/current stress of the components in abovementioned inverters. (a) Voltage stresses across the capacitors. (b) Voltage stresses across the diodes. (c) Current stresses on the windings.

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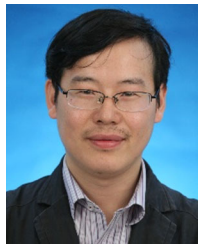

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