Design and Control of Power Fluctuation Delivery for Cell Capacitance Optimization in Multiport Modular Solid-State Transformers

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***Abstract*—Modular multilevel converter (MMC)-based solid-state transformers (SSTs) have gained increasing interest lately. Topologies consisting of cells made of directly coupled MMC submodules (SMs) and dual-active-bridge (DAB) modules have been introduced to form multiport SSTs to interface different grid entities. Designated as modular SSTs (M-SSTs), such devices can interconnect hybrid ac–dc distribution systems and enable flexible power flow control among participating grids with different voltage forms and levels. However, the large capacitors needed to suppress power fluctuations in the power cells are a major contributor to the SST's poor power density. This article first proposes a power fluctuation delivery (PFD) control strategy for M-SST cell capacitance optimization. Through a modified phase-shift control, the low-frequency fluctuating power in the MMC SMs is transferred to the DAB's secondary side and is automatically canceled there. As a result, the cell capacitance requirement is significantly reduced. Considering the modified ripple power path, both power semiconductors and the high-frequency transformers in DABs are affected. Therefore, the design considerations of a single M-SST cell (1 MMC SM + 1 DAB) with/without PFD control are elaborated for a 2-MVA M-SST example. It is shown that the cell capacitance can be reduced to 10% of its original value, and the power density of the whole cell is increased by 50% with only 0.22% drop in the overall efficiency. The feasibility and effectiveness of the proposed method are verified by simulation results in this 2-MVA case and experimental results obtained from a 4.8-kVA scaled-down M-SST prototype.**

***Index Terms*—Capacitance optimization, modular multilevel converter (MMC), power fluctuation, solid-state transformer (SST).**

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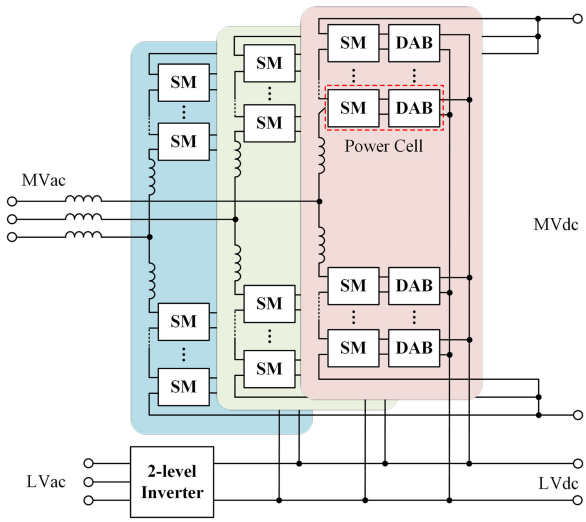

Fig. 1. Simplified topological diagram of the M-SST.

I. Introduction

As A key enabling device for future distribution grid system implementation, various solid-state transformers (SSTs) have been introduced [1], [2]. Of all the proposed configurations, the modular SST (M-SST) structure consisting of power cells formed by directly coupling modular multilevel converter (MMC) [3] submodules (SM) and dual-active-bridge (DAB) modules is developed to offer both ac and dc ports at both medium-voltage (MV) and low-voltage (LV) levels [4]. As shown in Fig. 1, the M-SST can be used to interface different grid entities via its ports and facilitate flexible power control among them. However, the M-SST cells require large capacitors on the MMC side to suppress power fluctuations, and these capacitors contribute greatly to the volume and material cost of the entire converter. From the power density analysis of a 1-MVA M-SST design [5], it was revealed that the power cell capacitors occupy about 62% of the total volume of the SST. To improve the power density, cell capacitance optimization is important.

The selection of the cell capacitance value is directly related to the low-frequency voltage ripples in steady-state operation, which is generated by MMC arm instantaneous power and circulating current. The dominant voltage ripples include the first-, second, and third-order components. In a conventional MMC,

a circulating current suppression scheme is proposed in [6] to eliminate the third-order voltage ripples; circulating injection and arm energy control are proposed in [7] and [8], respectively, with which the second-order voltage ripples can be reduced effectively, while the first-order ripples are not suppressed and the existing arm circulating current would increase the operation loss and current stress of the MMC, and third harmonic voltage injection method is adopted in [9] and [10] to alleviate both capacitor voltage ripples and arm current stress; however, this method cannot be used in the M-SST for there is no power transformer at the MVac side and the harmonic voltage will affect the MVac grid operation. These methods, in general, are based on control strategies embedded in the MMC controller and can effectively suppress voltage ripples in the MMC SMs. In [11], a hardware scheme is introduced, where power ripple links are designed for the three-phase SMs in a conventional MMC-based motor drive through extra dual-half-bridge modules, and the low-frequency voltage ripples could be eliminated to reduce capacitors volume. It is an effective approach to optimize cell capacitance in a drive system especially considering the low-speed operation region requirements.

Compared with the conventional MMCs composed only of standalone SMs, in an M-SST, an alternative power ripples flow path has been provided by the DABs whose outputs are paralleled to provide the LV-side dc bus. Taking advantage of this unique structure, this article proposes a power fluctuation delivery (PFD) control strategy for M-SST power cell voltage ripple suppression. By implementing a modified phase-shift control in the DABs, not only the dc power but also the fluctuating ac power from the MMC side are delivered to the LVdc bus, and the low-frequency voltage ripple on the power cell capacitors can be eliminated [12].

The proposed PFD control has the following advantages.

1) The low-frequency capacitor voltage ripple can be fully eliminated in theory, resulting in a significant reduction in the cell capacitance requirement.
2) The fluctuation power delivered through the DABs gets canceled on the LVdc side and will not affect the LV-side load.
3) The second-order circulating current in the MMC arms is naturally mitigated.
4) The control strategy for PFD is easy to implement and will not affect the performance of the existing voltage and power control in the M-SST.

However, the PFD control causes the power fluctuations to flow into the DABs and requires the redesign of the power semiconductors and high-frequency transformers (HFTs) in the DAB modules to handle the extra current stress. While the cell capacitance is reduced, the volume of the DABs will increase. In addition, voltage ripples near the MMC switching frequency still exist on cell capacitors with PFD control, and the corresponding selection method for cell capacitance value has not been investigated before.

To fully evaluate the benefits of the proposed method, design considerations for a single power cell of M-SST with/without PFD control, including the selection of cell capacitors, power semiconductors, HFTs, and heatsinks, are elaborated with a 2-MVA M-SST design case. Results reveal that with PFD control, the cell capacitance can be reduced to 10%, and the power density of one power cell can be increased by 50% with a merely 0.22% drop in the overall efficiency relative to the M-SST operated with standard control.

In brief, this article intends to contribute in the following aspects:

1) developing the PFD method for M-SST as a natural fit, which enables capacitance optimization in its power cells without introducing additional hardware;
2) design of cell capacitance of the M-SST with PFD control based on the high-frequency voltage ripples;
3) redesign procedure of the M-SST power cell with PFD control, where the effects of power ripples on DABs are fully considered, such that the cell's power density and efficiency of the M-SST are evaluated in a reasonable range;
4) the proposed PFD method is verified through a scaled-down but fully fledged experimental platform.

The rest of this article is organized as follows. Section II describes the circuit topology and the operation principle of the M-SST. Section III presents the basic idea of the proposed PFD method and develops the detailed control strategy. Design considerations for the M-SST cell with and without PFD control are elaborated in Section IV. Section V shows simulation results with a 2-MVA M-SST at different load conditions. Section VI demonstrates experimental results obtained from a 4.8-kVA prototype for verification of the method. Finally, Section VII concludes this article.

II. Topology and Operation Principle of the M-SST

The single-phase equivalent circuit diagram and its power cell structure of the M-SST are shown in Fig. 2. The MMC part is incorporated to provide a stable MVdc port for dc grid connection, as well as flexible active/reactive power flow control for the MVac grid by adjusting the ac-side voltage magnitude and phase. Each MMC SM is directly tied to a DAB module whose secondary side is paralleled with the other DAB outputs to integrate LVdc entities. In Fig. 2, u_a and i_a are the grid voltage and current of the a phase, respectively; Z_s denotes the grid impedance; e_{a1} and e_{a2} are the equivalent ac output voltages of the MMC; u_{ap} and u_{an} are the upper and lower arm voltages, respectively; i_{ap} and i_{an} are the arm currents; $U_{\rm MV}$ and $I_{\rm MV}$ are the MVdc voltage and current, respectively; C is the SM capacitance; u_{oapk} is the kth SM output voltage of the phase A upper arm; u_{capk} and i_{capk} are the voltage and current of the SM capacitor, respectively; i_{iapk} is the input current of the SM; i_{dapk} is the input current of the DAB; $U_{\rm LV}$ and $I_{\rm LV}$ are the LVdc voltage and current, respectively; and N is the number of SMs per MMC arm.

Assume the MVac side grid voltage and current are

$$u_a = U_m \sin \omega t, \quad i_a = I_m \sin(\omega t - \varphi) \tag{1}$$

where U_m and I_m are the magnitudes of the grid voltage and current, ω is the grid frequency, and φ is the power factor angle.

The equivalent ac output voltages of the MMC is

$$e_{a1} = e_{a2} = E_m \sin(\omega t - \delta), m = 2E_m/U_{\rm MV} \tag{2}$$

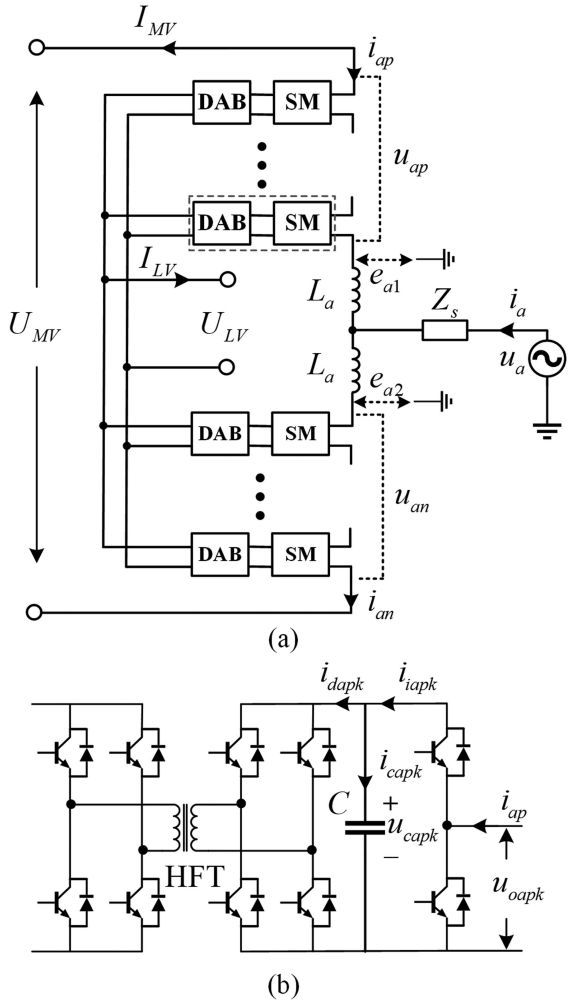

Fig. 2. Single-phase equivalent circuit of the M-SST. (a) Simplified circuit diagram. (b) Structure of a power cell.

where m is the modulation index of the MMC, δ is the power angle, and E_m is the magnitude of the voltage.

In steady-state operation, the three-port active power balance is expressed as

$$(3/2)E_m I_m \cos(\delta-\varphi) = U_{\rm MV} I_{\rm MV} + U_{\rm LV} I_{\rm LV}. \tag{3}$$

According to [13], cell capacitor voltage ripple will lead to second-order circulating current; thus, the arm current of phase A is

$$i_{ap} = -\frac{1}{3} I_{\rm MV} - \frac{1}{2} i_a + i_c, i_{an} = -\frac{1}{3} I_{\rm MV} + \frac{1}{2} i_a + i_c$$
$$i_c = I_c \sin(2\omega t - \varphi_c) \tag{4}$$

where I_c and φ_c are the magnitude and phase angle of the circulating current, respectively.

According to [13], the arm voltage of phase A is

$$u_{ap} = \sum_{k=1}^{N} u_{oapk} = \frac{1}{2} U_{\rm MV} - e_a,$$
$$u_{an} = \sum_{k=1}^{N} u_{oank} = \frac{1}{2} U_{\rm MV} + e_a. \tag{5}$$

Combining (3)–(5), the instantaneous input power of phase A upper arm is expressed as

$$p_{ap} = u_{ap} \cdot i_{ap} = p_{\rm dc} + p_{\rm ac1} + p_{\rm ac2} + p_{\rm ac3}$$
$$p_{\rm dc} = \frac{U_{\rm LV} I_{\rm LV}}{6}$$
$$p_{\rm ac1} = -\frac{U_{\rm MV} I_m}{4} \sin(\omega t - \varphi) + \frac{E_m I_{\rm MV}}{3} \sin(\omega t - \delta)$$
$$p_{\rm ac2} = \frac{U_{\rm MV} I_c}{2} \sin(2\omega t - \varphi_c) - \frac{E_m I_m}{4} \cos(2\omega t - \delta - \varphi)$$
$$p_{\rm ac3} = \frac{E_m I_c}{2} \cos(3\omega t - \varphi_c - \delta) \tag{6}$$

where $p_{\rm dc}$, p_{ac1}, p_{ac2}, and p_{ac3} are the dc power, first-order, second-, and third-order power ripple components, respectively.

From (6), compared with MMC, extra active power $p_{\rm dc}$ exists in M-SST's arm input power, which is transferred to the LVdc-side load through the DAB. The switching frequency of the DAB is usually set in the range of 5–20 kHz for keeping the volume of the HFT small. Adopting closed-loop LVdc voltage control, the control bandwidth of the DAB controller is selected as 1/10 of the switching frequency. As the high input impedance characteristics of the DAB within the control bandwidth [14], the low-frequency power ripples p_{ac1}, p_{ac2}, and p_{ac3} will mainly go into the cell capacitor. These power ripples will lead to capacitor energy variation, given as

$$p_{\rm ac1} + p_{\rm ac2} + p_{\rm ac3} = \sum_{k=1}^{N} u_{capk} \cdot C \frac{du_{capk}}{dt}. \tag{7}$$

Considering the uniformity of capacitor voltage dynamic behavior in the same arm, the capacitor voltage of phase A upper arm could be calculated based on (7), which is shown as

$$u_{\rm cap} = U_c - \frac{1}{C} \left[\frac{m I_{\rm MV}}{6\omega} \cos(\omega t - \delta) + \frac{I_m}{4\omega} \cos(\omega t - \varphi) \right.$$
$$- \frac{m I_m}{16\omega} \sin(2\omega t - \delta - \varphi) - \frac{I_c}{4\omega} \cos(2\omega t - \varphi_c)$$
$$\left. + \frac{m I_c}{12\omega} \sin(3\omega t - \delta - \varphi_c) \right]. \tag{8}$$

In (8), U_C is the dc component of the capacitor voltage. The low-frequency voltage ripples are related to cell capacitance, M-SST port active and reactive power, and circulating current. In fact, the cell capacitor is an energy buffer for the instantaneous arm power flowing through the MMC. Therefore, the low-frequency voltage ripples inevitably exist and cannot be fully eliminated by the MMC itself.

III. PFD Control of M-SST for Cell Capacitance Optimization

A. PFD Theoretical Analysis

The selection of the cell capacitance in an M-SST is directly related to the low-frequency voltage ripples, as given in (8). If the low-frequency fluctuations of the instantaneous arm input power can be diverted by control and do not enter the capacitors, the cell capacitance value can be naturally optimized. The

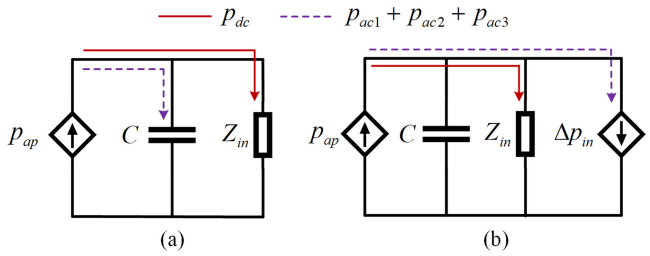

Fig. 3. Equivalent circuit and power flow path in the M-SST cell. (a) Without PFD control. (b) With PFD control.

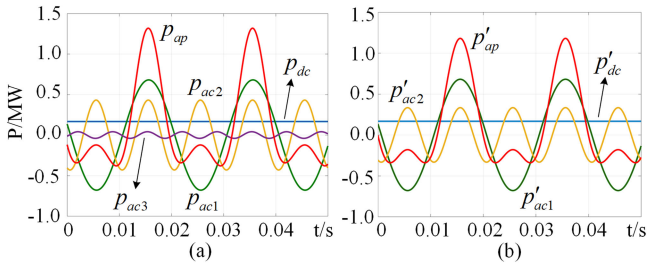

Fig. 4. Phase A upper arm instantaneous input power (2-MVA M-SST case listed in Table I; MVdc load = 1 MW and LVdc load = 1 MW). (a) Without PFD control. (b) With PFD control.

basic idea of the proposed PFD control is to take advantage of the unique power cell structure of the M-SST to transfer the fluctuating power to the LVdc side through the DAB. As shown in Fig. 3(a), without PFD, based on (6) and considering that the input impedance of the DAB, $Z_{\rm in}$, is much larger than the capacitor reactance in the low-frequency range, the dc component in (6) will flow into the DAB and be delivered to the LVdc bus, while the low-frequency ac components in (6) will flow into the SM capacitor and cause voltage ripples. However, if an extra ac input power control $\Delta p_{\rm in}$ is incorporated in the DAB in addition to its LVdc voltage loop and force the low-frequency ac power to change path toward the DAB, as shown in Fig. 3(b), the capacitor voltage ripples could be eliminated. In theory, the low-frequency voltage ripples can be fully eliminated with PFD control. Moreover, the delivered fluctuating powers of all cells in the six MMC arms will be automatically summed up and canceled at the LVdc bus. The feasibility and effect of the PFD method are analyzed theoretically in this section.

Assuming that there are no low-frequency power ripples flowing into the cell capacitors with the PFD control performing ideally, the capacitor voltage becomes a constant value ignoring the switching frequency component

$$u_{capk}(t) \approx U_c. \tag{9}$$

Therefore, no second-order circulating current exists, and the arm current of phase A is

$$i'_{ap} = -\frac{1}{3}I_{\rm MV} - \frac{1}{2}i_a, \quad i'_{an} = -\frac{1}{3}I_{\rm MV} + \frac{1}{2}i_a. \tag{10}$$

The arm voltage is the same as (5). Combining (5) and (10), the instantaneous input power of phase A upper arm with PFD control could be expressed as

$$\begin{aligned} p'_{ap} &= u_{ap}\cdot i'_{ap} = p'_{\rm dc} + p'_{\rm ac1} + p'_{\rm ac2} \\ p'_{\rm dc} &= \frac{U_{\rm LV}I_{\rm LV}}{6} \\ p'_{\rm ac1} &= -\frac{U_{\rm MV}I_m}{4}\sin(\omega t-\varphi) + \frac{E_m I_{\rm MV}}{3}\sin(\omega t-\delta) \\ p'_{\rm ac2} &= -\frac{E_m I_m}{4}\cos(2\omega t-\delta-\varphi). \end{aligned} \tag{11}$$

As shown in Fig. 4, compared with (6), the second- and third-order power ripples resulting from the circulating current are eliminated with PFD control in (11). Therefore, PFD control could achieve cell capacitor optimization, circulating current suppression, and arm power ripples reduction at the same time.

Based on Fig. 3(b), the sum of input power of DAB modules in the phase A upper arm is equal to the arm input power (11) with PFD control, which can be expressed as

$$\sum_{k=1}^{N} p_{dapk} = p'_{ap} \tag{12}$$

where p_{dapk} is the input power of the kth DAB module in the phase A upper arm.

Neglecting the internal power loss of the DABs, all DABs of the M-SST supply power for the LVdc-side load collectively

$$p_{\rm LVdc} = \sum_{k=1}^{N}(p_{dapk} + p_{dank} + \cdots + p_{dcnk}) = U_{\rm LV}I_{\rm LV} \tag{13}$$

where $p_{\rm LVdc}$ is the LVdc-side power absorbed from the DABs.

From (13), $p_{\rm LVdc}$ only consists of the dc power component, for the low-frequency power ripples among arms are automatically canceled when delivered to the LVdc side. Therefore, PFD control will not affect LV-side voltage control and load power.

B. Control Strategy of the M-SST With PFD

The control strategy of the M-SST with PFD is shown in Fig. 5. Due to the cell capacitors, MMC and DABs are decoupled, and their control strategies could be designed independently.

The MMC control consists of the outer and inner loops for regulating its voltages and currents, a phase-locked loop (PLL) for ac-side grid synchronization, and a capacitor voltage balance control for equalizing cell capacitor voltages. MVdc voltage control is applied in the outer loop, which also provides the active current reference. Active and reactive current control in the *dq* rotation frame is used in the inner loop to regulate the currents and generate the arm voltage references. The capacitor voltage balance control provides an additional duty ratio for the SM output based on the arm current direction and capacitor voltage. With the PFD control, the low-frequency fluctuating power in the capacitors is eliminated; thus, the circulating current control loop normally required in an MMC is not necessary.

The DAB control scheme consists of the LVdc voltage control, the PFD control, and the input power detection. The LVdc voltage control provides a common phase-shift reference Φ^* for all DABs, meaning that the common duty ratio is used, such

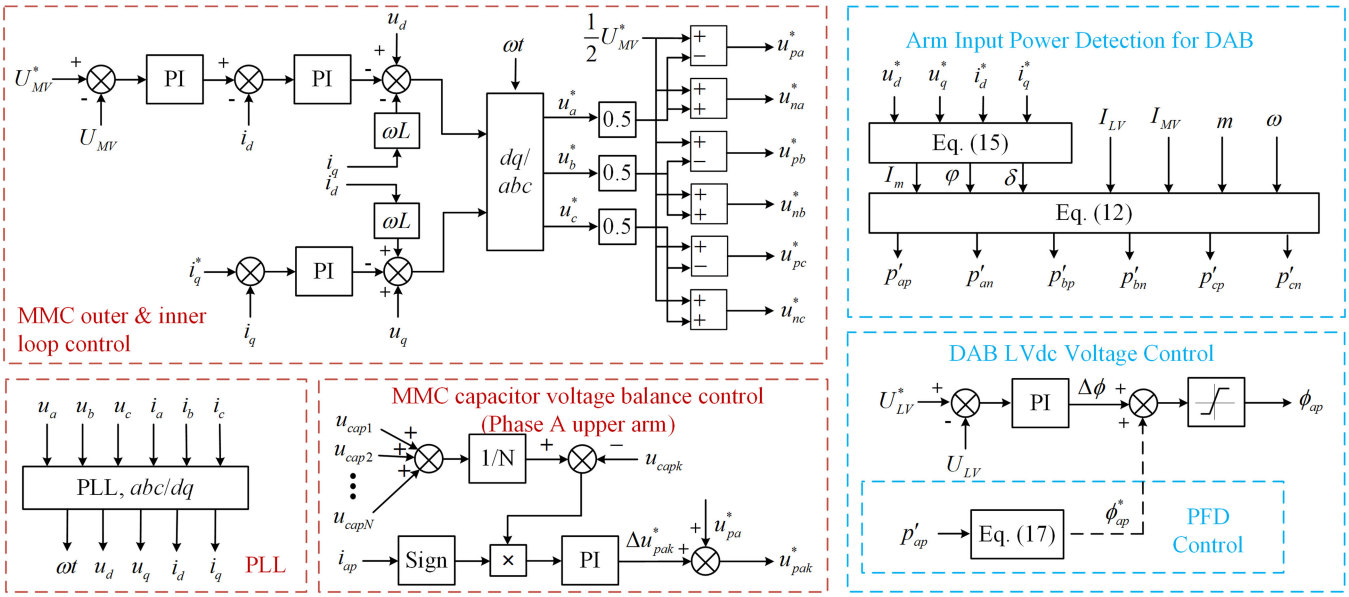

Fig. 5. Overall control block diagram of the M-SST with PFD control.

that stable sharing of the LVdc load power among all DABs is achieved [15]. The input power detection calculates the arm input power online according to the M-SST's real-time operation points. This calculated input power ripples serves as the PFD controller's input, whereas its output produces an additional phase shift $\Delta\Phi$. Therefore, the DABs in the same arm will have the same variable phase-shift angle and transfer both the dc and the fluctuating ac powers to the LVdc bus. The core elements of the PFD control, i.e., input power detection and phase-shift angle calculation, will be elaborated in the following.

The arm input power with PFD control is given in (11), which is related to the M-SST operation point. To avoid using too many current sensors, an input power online detection scheme is developed. In (11), the MVdc current $I_{\rm MV}$ can be detected by the MVdc-side current sensor, the LVdc current $I_{\rm LV}$ can be detected by the LVdc-side current sensor, the modulation index m can be derived using the detected MVdc and MVac voltages, and the grid angular frequency ω can be acquired by the PLL. However, the MVac current amplitude I_m, the power angle δ, and the power factor angle φ cannot be acquired directly and need to be calculated online.

As shown in Fig. 4, with the grid voltage and current references in the dq rotating reference frame easily acquired by the MMC controller, these unknown variables are calculated as

$$I_m = \sqrt{i_d^{*2} + i_q^{*2}}, \quad \cos\varphi = \frac{i_d^*}{I_m}, \sin\varphi = -\frac{i_q^*}{I_m}$$
$$E_m = \sqrt{u_d^{*2} + u_q^{*2}}, \quad \cos\delta = \frac{u_d^*}{E_m}, \sin\varphi = -\frac{u_q^*}{E_m}. \tag{14}$$

With (11) and (14), the arm input power can be calculated online under different operation points. In practice, the filter for switching frequency component suppression will cause some delay in the online calculation, which may lead to slight amplitude and phase errors in the power ripples detection.

Based on (11), the DAB input power should be controlled to track the detected arm input power. The power equation of any DAB in the upper arm of phase A is [16]

$$p_{dapk} = \frac{\phi_{ap}[\pi - \phi_{ap}]nU_cU_{\rm LV}}{2\pi^2 f_d L_d}. \tag{15}$$

In (15), n is the HFT ratio, f_d is the DAB square wave frequency, and L_d is the leakage inductance of the HFT. The phase-shift angle with fluctuating input power is calculated as

$$\phi_{ap}^* = \frac{\pi - \sqrt{\pi^2 - 8\frac{p_{dapk}\pi^2 f_d L_d}{nU_{\rm LV}U_c}}}{2}, \quad \phi_{ap}^*(t) > 0$$
$$\phi_{ap}^* = \frac{-\pi + \sqrt{\pi^2 + 8\frac{p_{dapk}\pi^2 f_d L_d}{nU_{\rm LV}U_c}}}{2}, \quad \phi_{ap}^*(t) < 0. \tag{16}$$

IV. Design Considerations of M-SST Power Cells With/Without PFD Control

With the PFD control applied, the fluctuating powers in the cells will not affect the LVdc load as they are all canceled. However, these power ripples will flow into DAB and affect its power devices and HFT ratings. In this section, based on a 2-MVA M-SST case listed in Table I, design considerations of the M-SST power cells with/without PFD control are elaborated, including cell capacitors, HFTs, power semiconductors, and heatsinks. According to the designed devices, the power density variation of one cell is evaluated to reveal the benefit of the PFD control in optimizing the cell volume. Considering the power loss increase with PFD control, the overall efficiency of the M-SST should also be estimated.

TABLE I
PARAMETERS OF A 2-MVA M-SST

Parameter	Value	Parameter	Value
Power ratings	MVac: 2 MVA MVdc: 1 MW LVdc: 1 MW	Number of SMs Arm inductance SM capacitor	24 8 mH 940 μF
MVac voltage	10 kV	MMC switching frequency	1 kHz
MVdc voltage	20 kV	DAB switching frequency	10 kHz
LVdc voltage	800 V	HFT turns ratio	1.04:1

A. Cell Capacitor Design

The cell capacitance should be selected to effectively reduce voltage ripples. Unattenuated voltage ripples will increase the voltage stress of power semiconductors and, in contrast, leads to higher circulating current, power loss, and arm current stress and deteriorated operation performance of the M-SST. Considering the practical cost and volume limitations of cell capacitors, the allowable maximum voltage fluctuation rate is set in the range of 5–10%. In this article, this rate ε is set as

$$\varepsilon = \frac{\max|u_{\text{cap}} - U_c|}{U_c} = 10\%. \tag{17}$$

Based on the control of Fig. 5 and the parameters of Table I, the simulation result of cell capacitor voltage in the 2-MVA M-SST is shown in Fig. 6(a). Without PFD control, the capacitor voltage varies in the range of $\pm 10\%\ U_c$. When PFD control is enabled, voltage ripples are greatly reduced to $\pm 1\%\ U_c$.

Because of the higher capacitor impedance at lower frequencies, the voltage ripples in (8) are the dominant factors for voltage variations without PFD control, as shown in Fig. 6(b). Equation (8) is the same as the capacitor voltage equation in a conventional MMC. Therefore, the cell capacitance selection method in the MMC based on capacitor energy [17] can be directly adopted for the M-SST

$$\Delta W_c = \frac{2}{3} \times \frac{S}{mN\omega}\left(1 - \left(\frac{m\cos(\varphi - \delta)}{2}\right)^2\right)^{3/2} \tag{18}$$

where ΔW_c is the maximum capacitor energy variation value and S is the rated capacity of the M-SST.

Meanwhile, ΔW_c can also be expressed through the capacitor voltage fluctuation rate as

$$\Delta W_c = \frac{1}{2} C U_c^2 (4\varepsilon). \tag{19}$$

The M-SST is mainly used for active power interaction among multiple distribution grids; thus, reactive power requirement is not considered in this article, which means $\varphi = \delta$. Based on (18) and (19), the cell capacitance for the test case without PFD control is selected as

$$C \geq 900\,\mu\text{F}. \tag{20}$$

In addition, the rms current of the cell capacitors should be considered. The rated rms current of the selected capacitor in practice should be higher than the calculated value in theory. Based on double Fourier transformation and Taylor expansion, the capacitor current i_{cap} can be expressed as

$$\begin{aligned} i_{capk} = &\left(\frac{mI_{\text{MV}}}{6} - \frac{I_m}{4}\right)\sin(\omega t - \delta) \\ &- \frac{1}{8} m I_m \cos(2\omega t - 2\delta) + \sum_{p=1}^{\infty} \frac{2I_{\text{MV}}}{3\pi p} \sin\left(p\frac{\pi}{2}\right) \\ &\cdot J_0\left(p\frac{\pi}{2}m\right)\sin(p\omega_c t) + \sum_{p=1}^{\infty}\sum_{q=-\infty}^{\infty} \frac{2I_{\text{MV}}}{3\pi p} \sin\left[(p-q)\frac{\pi}{2}\right] \\ &\cdot J_q\left(p\frac{\pi}{2}m\right) \times \sin(p\omega_c t + q\omega t - q\delta) \\ &- \sum_{p=1}^{\infty}\sum_{q=-\infty}^{\infty} \frac{I_m}{2\pi p} \cos\left[(p-q)\frac{\pi}{2}\right] \cdot K_q\left(p\frac{\pi}{2}m\right) \\ &\times \cos(p\omega_c t + q\omega t - q\delta) \end{aligned}$$

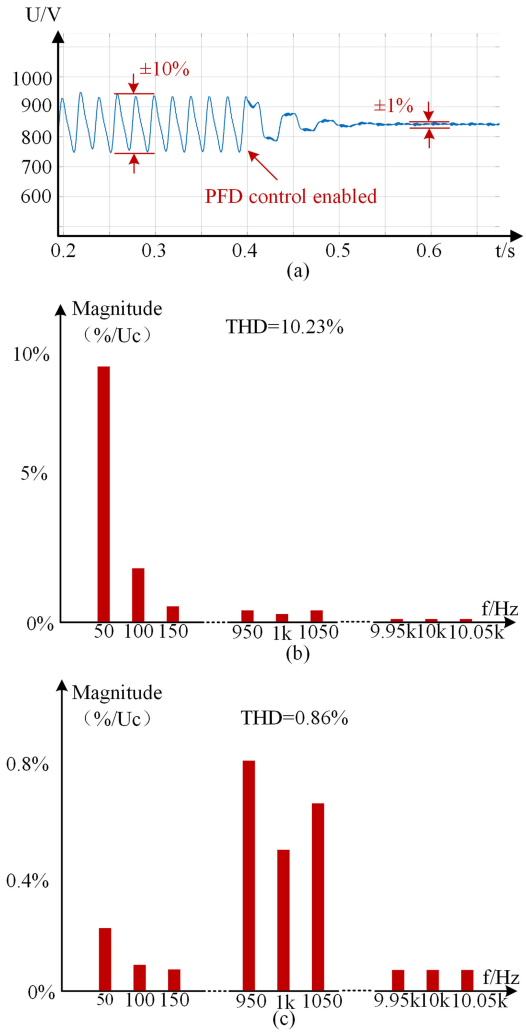

Fig. 6. Simulation results of 2-MVA M-SST's cell capacitor voltage (MVdc load = 1 MW and LVdc load = 1 MW). (a) Capacitor voltage waveform with/without PFD control. (b) Capacitor voltage harmonic analysis without PFD control. (c) Capacitor voltage harmonic analysis with PFD control.

$$-\sum_{r=1}^{\infty}\left[\frac{8U_c[\cos(r\phi_{ap})-1]}{(2\pi r)^2 L_d f_d}\right]\cos(r\omega_d t)$$
$$+\sum_{r=1}^{\infty}\left[\frac{4U_c[r\phi_{ap}\cos(r\pi)+r\phi_{ap}-2\sin(r\phi_{ap})]}{(2\pi r)^2 L_d f_d}\right]\sin(r\omega_d t)$$
$$J_q\left(p\frac{\pi}{2}m\right)=\sum_{l=1}^{\infty}(-1)^l\frac{(p\frac{\pi}{2}m)^{q+2l}}{2^{q+2l}l!(q+l)!}$$
$$K_q\left(p\frac{\pi}{2}m\right)=\sum_{l=1}^{\infty}(-1)^l\frac{(p\frac{\pi}{2}m)^{q-1+2l}(2l+1)}{2^{q-1+2l}l!(q-1+l)!(2l+2)} \quad (21)$$

where ω_c is the switching frequency of MMC and $\omega_d = 2\pi f_d$ is the switching frequency of the DAB. The detailed calculation process is shown in the Appendix.

In (21), the capacitor input current consists of three components: low-frequency components caused by arm input power ripples, high-frequency components caused by MMC pulsewidth modulation (PWM), and high-frequency components caused by DAB square modulation.

The current ripples resulting from the DAB in (21) are inversely proportional to the DAB switching frequency. In general, the DAB switching frequency is much higher than that of the MMC to optimize the size of the HFT. Therefore, its effects on cell capacitor current are much smaller than the MMC PWM. In the 2-MVA M-SST case, the rms value of the capacitor current ripples caused by DAB is less than 5% of the total harmonics and considered negligible.

Based on (21), the maximum rms value of each harmonic order component of the capacitor current can be calculated under the rated power condition of the M-SST, where the MVdc LVdc loads are both set as 1 MW in this case. The maximum total rms capacitor current I_c is estimated as

$$I_c=\sqrt{I[\omega]^2+I[2\omega]^2+I[\omega_c]^2+I[\omega_c\pm\omega]^2+I[\omega_c\pm2\omega]^2}$$
$$=39\,\mathrm{A} \quad (22)$$

where $I[\omega]$, $I[2\omega]$, $I[\omega_c]$, $I[\omega_c\pm\omega]$, $I[\omega_c\pm2\omega]$ are the rms values of the first-order, second-order, PWM carrier frequency, and sideband harmonic components, respectively.

Considering (20) and (22), the TDK power electronic film capacitor "B25620B1947K103" is selected for the M-SST without PFD control, featuring 940-μF value, 1100-V rated dc voltage, 100-A maximum current, and 1827-cm^3 volume.

With PFD control, the cell capacitance can be optimized, for the low-frequency voltage ripples are totally eliminated as shown in Fig. 6(c). The capacitance selection also depends on the voltage fluctuations, which is caused by the high-frequency capacitor current in (21). Therefore, the capacitor voltage with PFD control is estimated as

$$u_{capk}=U_c-\frac{2I_{\mathrm{MV}}}{3\pi\omega_c C}\cdot J_0(\frac{\pi}{2}m)\cos(\omega_c t)$$
$$+\frac{2I_{\mathrm{MV}}}{3\pi(\omega_c+2\omega)C}\cdot J_1(\frac{\pi}{2}m)\cos(\omega_c t+2\omega t-2\delta)$$
$$-\frac{2I_{\mathrm{MV}}}{3\pi(\omega_c-2\omega)}\cdot J_{-1}(\frac{\pi}{2}m)\cos(\omega_c t-2\omega t+2\delta)$$
$$-\frac{I_m}{2\pi(\omega_c+\omega)C}\cdot K_1(\frac{\pi}{2}m)\sin(\omega_c t+\omega t-\delta)$$
$$+\frac{I_m}{2\pi(\omega_c-\omega)C}\cdot K_{-1}(\frac{\pi}{2}m)\sin(\omega_c t-\omega t+\delta). \quad (23)$$

In (23), higher order harmonics are not considered, and the maximum allowable capacitor voltage fluctuation can be set as εU_c:

$$\varepsilon U_c \geq |\Delta U[\omega_c]|+|\Delta U[\omega_c\pm\omega]|+|\Delta U[\omega_c\pm2\omega]| \quad (24)$$

where $\Delta U[\omega_c]$, $\Delta U[\omega_c\pm\omega]$, and $\Delta U[\omega_c\pm2\omega]$ are the voltage magnitudes of the carrier harmonic and sideband harmonics, respectively.

Based on (24), the cell capacitance for the 2-MVA M-SST with PFD control can be selected as

$$C' \geq 105\,\mu\mathrm{F}. \quad (25)$$

The maximum capacitor rms current I_c' is also estimated under the rated power condition, based on the high-frequency current given in (21)

$$I_c=\sqrt{I[\omega_c]^2+I[\omega_c\pm\omega]^2+I[\omega_c\pm2\omega]^2}=24\,\mathrm{A}. \quad (26)$$

Considering (25) and (26), the TDK power electronic film capacitor "B25631B1127K100", with 120-μF value, 1100-V rated dc voltage, 50-A maximum current, and 368-cm^3 volume, is selected for the M-SST power cell with PFD control.

A huge volume reduction is observed comparing the two selected cell capacitors in the 2-MVA M-SST case. However, the low-frequency power ripples will flow into the DAB with PFD control and affect the design of the HFT, power semiconductors, and heatsink. These devices should be redesigned, and the power density of the whole power cell should be evaluated to reveal the real benefits of PFD control.

B. HFT Design

With PFD control, the phase-shift angle of the DAB is no longer a constant value in the steady state, but is directly related to the fluctuating DAB input power, and (16) is simplified as

$$\phi_{ap}(t)=f[p_{dapk}(t)]. \quad (27)$$

Equation (27) is a monotonically increasing function. Assuming that the side voltages of the DAB are matched, the peak transformer current $i_{L\max}$ is calculated as [16]

$$i_{L\max}=\frac{U_c\phi_{ap\max}}{2\pi f_d L_d}=\frac{U_c f\{\max[p_{dapk}(t)]\}}{2\pi f_d L_d}. \quad (28)$$

When the DAB input current is at its peak, the phase-shift angle and the transformer current reach their maximum values as well.

The transformer current is of trapezoidal shapes with different phase-shift angles. Based on (11), the first- and second-order grid frequency components of input power are introduced to the

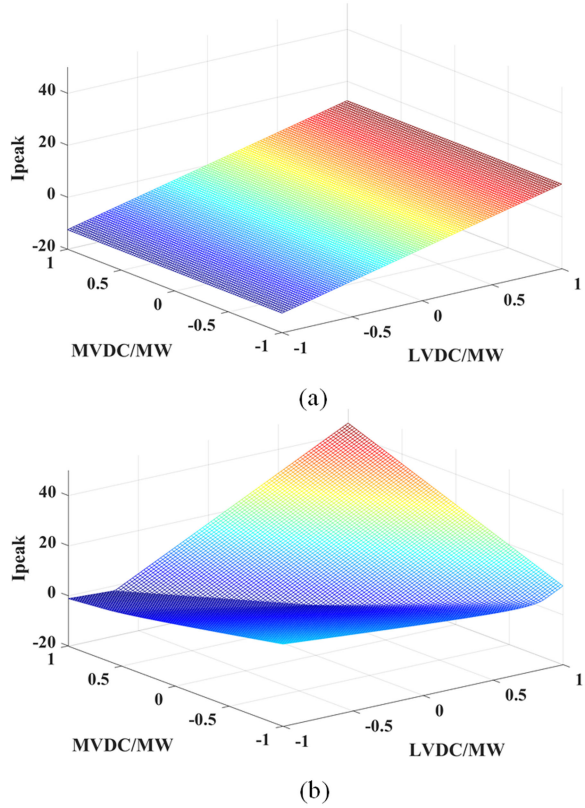

Fig. 7. DAB peak current in the whole operation range. (a) DAB peak current without PFD control. (b) DAB peak current with PFD control.

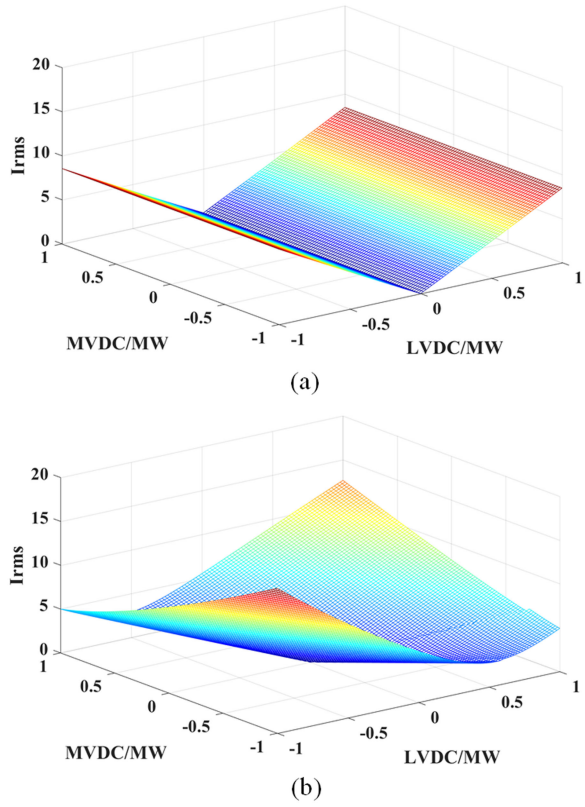

Fig. 8. DAB rms current in the whole operation range. (a) DAB rms current without PFD control. (b) DAB rms current with PFD control.

angle. Therefore, rms transformer current $i_{L\mathrm{rms}}$ is determined by the integral of one fundamental period

$$i_{L\mathrm{rms}} = \sqrt{\frac{\omega}{2\pi}\int_0^{\frac{2\pi}{\omega}} \frac{U_c\phi_{ap}^2(t)\left\{U_c[\pi-\phi_{ap}(t)]+\phi_{ap}(t)\right\}}{8\pi^3 f_d^2 L_d^2}dt}. \tag{29}$$

Based on (28), (29), and the parameters given in Table I, the three-dimensional DAB peak and rms current curves with and without PFD control are plotted for the whole operation region for the 2-MVA M-SST, as shown in Figs. 7 and 8, respectively. Several conclusions can be drawn regarding the currents.

1) The DAB current is only related to the LVdc-side power without PFD; however, with PFD control in effect, due to the fluctuating power in (11), the HFT current is related to both the MVdc- and LVdc-side powers.
2) The maximum DAB peak current occurs when the MVdc and LVdc powers are at their rated values of 1 MW each. With PFD control, a significant increase from 12.2 to 33.5 A in the DAB peak current is observed. Higher peak current requires larger safe operating area (SOA) of the power devices.
3) The maximum rms current increases from 9.5 to 13.6 A with PFD control. Higher rms current will affect the power capacity of the HFT and thermal design of the power devices and heatsink.

The HFT should be redesigned to adapt to the fluctuating power flow caused by the PFD control. The varied phase-shift angle does not change the magnitude of the square-wave voltage, and the core loss of the HFT will not be affected according to the Steinmetz equation [18]. However, the increase of rms current, as shown in Fig. 8, will require larger capacity and results in extra winding loss for the HFT. The "Ap method" is used for redesigning the HFT, where the main objective of the method is to search for the optimum total loss (core loss + winding loss) for the HFT at rated power, and to design the corresponding flux density, current density, number of turns, core volume, and winding volume [18]. Based on the parameters given in Table I and the calculated rms currents, the original and redesigned HFT parameters are listed in Table II for the 2-MVA M-SST design. The results show that the volume of the HFT will increase by

TABLE II
PARAMETERS OF THE DAB HFT

Parameter	Original HFT	Redesigned HFT
Optimum flux density	0.1799T	0.1659T
Operation frequency	10kHz	10kHz
Optimum Ap	1666cm^4	2395cm^4
Winding volume	463cm^3	608cm^2
Core volume	259cm^3	340cm^3
Current density	1.33×10^{6}A/m^2	1.27×10^{6}A/m^2
Winding loss	30W	36W
Core loss	15W	23W

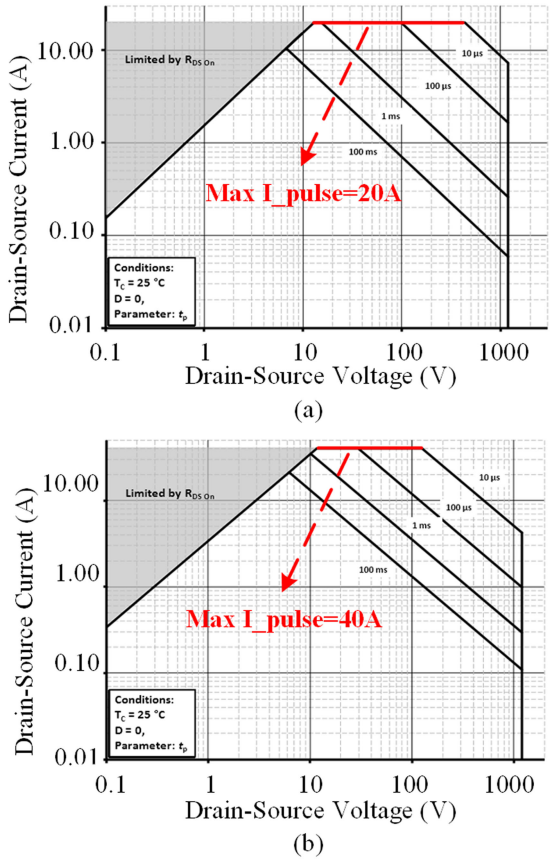

Fig. 9. SOA of the selected SiC-MOSFET. (a) SOA of SiC-MOSFET for original design. (b) SOA of SiC-MOSFET for PFD design.

31% (from 722 to 948 cm^3) with PFD control, and the power loss of the HFT under rated condition will increase from 45 to 59 W.

C. Power Semiconductor Design

The increased peak and rms currents of the DAB with PFD control also affect the SOA and thermal design of the power semiconductors. In general cases, the SOA design margin for power devices is usually large enough, and the thermal constraint is the main factor determining the reselection of power devices. However, in this specific case, because the PFD control caused much less variation in the rms current than in the peak current, the capacity and heat dissipation of the reselected power devices will not increase significantly, but the new device should be able to handle the worst-case peak current.

SiC-MOSFETs are selected for the DAB switching at 10 kHz due to their lower switching loss. Since the peak current increases from 12.2 to 33.5 A with PFD, the reselection of power devices is required to ensure that the new peak current is within the power device's SOA [19]. The increase in the rms current from 9.3 to 13.2 A only has a slight effect on the power device choice. For the 2-MVA M-SST design, the 1200-V-10-A SiC-MOSFET (Cree C2M0280120D) is a suitable choice for the original design, as shown in Fig. 9(a), allowing a maximum of 20-A pulsed drain current within its SOA; with PFD applied and causing increased peak current stress, a 1200-V-30-A SiC-MOSFET (Cree C2M0160120D) is selected for the new design, with which a maximum of 40-A pulsed drain current is permitted within its SOA, as shown in Fig. 9(b).

These two SiC-MOSFETs have the same packaging, so the reselection of the power device has no impact on the power density of the new M-SST cells. Moreover, the volume increase of the redesigned HFT is about only 30%. In fact, with the added PFD control, the internal power ripples of the MMC are taken over by the higher power density components, i.e., the power semiconductors and the HFT of DAB, from the lower power density cell capacitors.

In contrast, with PFD control, the power loss of SiC-MOSFET is changed due to the power ripples. Considering that zero-voltage switching (ZVS) operation of the DAB for the voltages of both sides is matched, only the conduction loss is evaluated in this article. Based on [20], the conduction loss of SiC-MOSFET $P_{c,\mathrm{mos}}$ and the conduction loss of reverse diode $P_{c,d}$ could be estimated as

$$P_{c,\mathrm{mos}} = \frac{\omega}{2\pi}\int_0^{\frac{2\pi}{\omega}} d_{\mathrm{mos}}(t) i_{dapk}^2(t)\cdot R_{\mathrm{on}} dt$$

$$P_{c,d} = \frac{\omega}{2\pi}\int_0^{\frac{2\pi}{\omega}} d_d(t)[i_{dapk}^2(t)\cdot R_d + i_{dapk}(t)\cdot V_d]dt \quad (30)$$

where d_{mos} is the duty cycle of the SiC-MOSFET, R_{on} is the ON-state resistance, d_d is the duty cycle of the diode, R_d is the diode resistance, and V_d is the diode forward voltage.

The conduction loss calculation could refer to [21]. The result shows that, for the 2-MVA case, without PFD control, the conduction loss of one pair of SiC-MOSFET + diode is 41 W; with PFD control and the reselected switches, the conduction loss will increase to 47 W.

D. Heatsink Design

Heatsink is another essential component affected by the PFD control, which should be redesigned to adapt to the power loss variation of power semiconductors.

In this article, the air cooling technique is used for its higher thermal performance than natural cooling. For one half-bridge of the DAB, the heatsink could be selected based on the total power loss and thermal resistance

$$R_{sa} < [(T_j - T_a)/(4P_{c,mos} + 4P_{c,d})] - R_{jc} - R_{cs} \quad (31)$$

where R_{sa} is the thermal resistance of heatsink, T_j is the target temperature, T_a is the external temperature, R_{jc} is the equivalent thermal resistance of power semiconductors, and R_{cs} is the thermal resistance of semiconductors to heatsinks.

For the 2-MVA M-SST case, T_j is set as 100 °C, T_a is set as 25 °C, R_{cs} is set as 0, and R_{jc} could be calculated based on the provided datasheet.

Based on (31), without PFD control, the thermal resistance of heatsink for one half-bridge should be less than 0.46 °C /W. The heatsink "FHS-A7015S61" from Delta Electronics, which features 0.43 °C /W thermal resistance and 277-cm^3 volume, is selected.

TABLE III
DESIGN OF MAIN COMPONENTS FOR 2-MVA M-SST'S POWER CELL

	Component	Manufacturer	Type	Features	Volume(cm^3)	Loss (W)
Standard Control	Cell capacitor	TDK	B25620B1947K103	940μF, 1100V DC, 100A	1827	/
	HFT	/	/	0.1799T, Ap=1666cm^4	722	45
	SiC-MOSFET+Diode	CREE	C2M0280120D	1200V-10A, 20A pulse current	/	41
	Heatsinks for DAB	Delta	FHS-A7015S61	0.43°C/W thermal resistance	277	/
PFD Control	Cell capacitor	TDK	B25631B1127K100	120μF, 1100V DC, 50A	368	/
	HFT	/	/	0.1659T, Ap=2395cm^4	948	59
	SiC-MOSFET+Diode	CREE	C2M0160120D	1200V-30A, 40A pulse current	/	47
	Heatsinks for DAB	Delta	FHS-A7015B62	0.31°C/W thermal resistance	324	/
MMC-side	IGBT+Diode	Mitsubishi	CM75DY-34T	1700V-75A	/	137
	Heatsinks for MMC	Delta	FHS-A7015B62	0.31°C/W thermal resistance	324	/

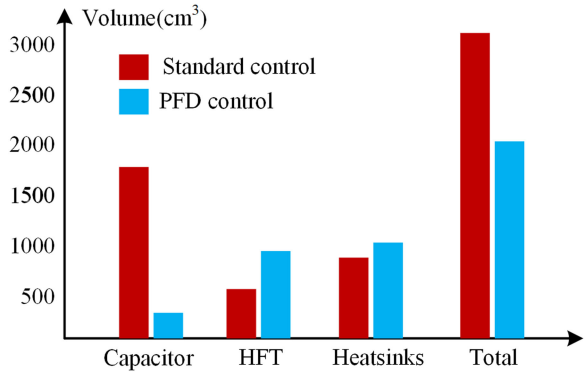

Fig. 10. Volume comparison of M-SST power cell with/without PFD control.

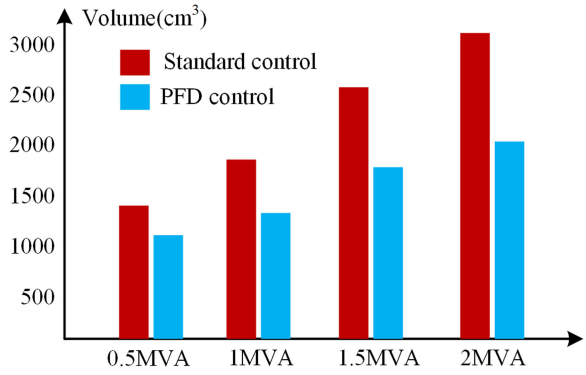

Fig. 11. Cell volume reduction of M-SST in different capacities.

With PFD control, the thermal resistance of the heatsink for one half-bridge should be less than 0.34 °C /W. The heatsink "FHS-A7015B62" from Delta is selected, which features 0.31 °C /W thermal resistance and 324-cm^3 volume.

E. Power Density Evaluation of One M-SST Cell

To reveal the benefits of PFD control, the power density of one power cell is evaluated in this section. Based on the analysis above, the design and selection results of each component are listed in Table III, where the DAB's secondary-side component selection is the same as the primary-side component because the turns ratio is close to 1. In addition, the power semiconductor and heatsink selection for the MMC is also listed in Table III, which is kept unchanged with/without PFD control. An insulated-gate bipolar transistor (IGBT) is used for the half-bridge of the MMC, because of its lower switching frequency and lower cost compared with SiC-MOSFET. The power loss of IGBT could be estimated according to [21].

For one power cell, it consists of one cell capacitor, one HFT, eight SiC-MOSFET + diode, two heatsinks for the DAB, two IGBT + diode, and one heatsink for the MMC. The volume of power semiconductors is much smaller than other components and could be neglected. For the 2-MVA M-SST case, the volume comparison for one power cell with/without PFD control is shown in Fig. 10.

From Fig. 10, the cell capacitor, which is the dominant element in the volume of the cell, is greatly optimized with PFD control. The total cell volume is reduced from 3427 to 2288 cm^3 with PFD control, even though some volume increase is observed in HFT and heatsinks. It is shown that the power density of the cell can be increased by 50% with PFD and redesigned cell components.

Using the same evaluation scheme, the cell volumes of M-SST designs with power ratings of 0.5, 1, and 1.5 MVA, are also calculated with and without PFD control. The results given in Fig. 11 show that the cell volume reductions are 22%, 24%, 28%, and 33%, respectively. It can be seen that the method introduces more volume reduction benefit for higher power applications.

F. Efficiency Evaluation of the M-SST

According to Table III, the power loss distribution of one power cell is shown in Fig. 12. The power ripples will mainly increase the power loss of the DAB's SiC-MOSFET. For the redesigned HFT, the extra loss is very small and has a negligible effect on the efficiency of the M-SST.

In summary, based on the power loss shown in Fig. 12, the efficiency of the M-SST in rated operation point is 97.67% without PFD control and 97.45% with PFD control. This means that a 50% power density increase is obtained with PFD at the expense of a 0.22% drop in overall efficiency.

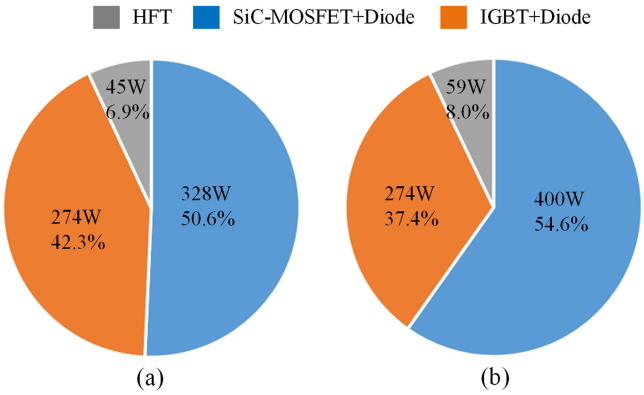

Fig. 12. Loss distribution of M-SST power cell. (a) Without PFD control. (b) With PFD control.

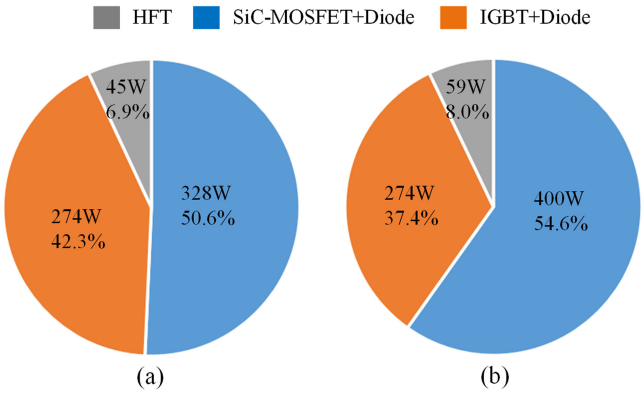

Fig. 13. Diagram of M-SST simulation configuration.

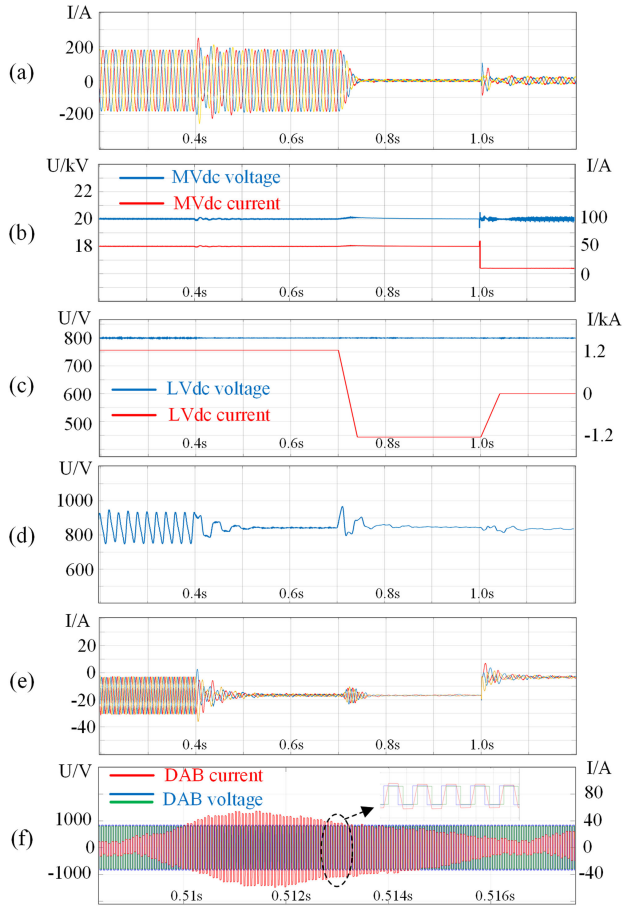

Fig. 14. Simulation results of M-SST with PFD control under different load conditions. (a) MVac grid current. (b) MVdc voltage and current. (c) LVdc voltage and current. (d) Capacitor voltage of phase A upper arm. (e) Three-phase circulating current. (f) DAB ac voltage and current with PFD control.

V. Simulation and Experimental Verifications

A. Simulation Results

To verify the effectiveness of PFD control on M-SST capacitor optimization, as shown in Fig. 13, a MATLAB-Simulink model is built for the 2-MVA test case with parameters listed in Table I. The MVac port of the M-SST is connected to a 10-kV ac grid; on the MVdc and LVdc sides, purely resistive loads are used. The MVdc voltage is regulated by the MMC at 20 kV dc; in addition, the reactive power of the MVac side is controlled to be 0. The LVdc voltage is controlled by the DAB at 800 V dc, where the same phase shift is used for all DABs.

Three load conditions (LC) are simulated as follows.

LC A: rated power condition. The MVdc load is 400 Ω and the LVdc load is 0.64 Ω, which means that the MVdc and LVdc sides each absorbs 1-MW power from the MVac side.

LC B: reverse power condition. The MVdc load is 400 Ω and the LVdc load is bypassed; the LVdc power source 1 MW is connected, which means that the MVdc side absorbs 1-MW active power from the LVdc side.

LC C: light-load condition. The MVdc load is 2 kΩ and the LVdc load is bypassed, which means that the MVdc side absorbs 200-kW active power from MVac.

The simulation process is given as follows.

At $t = 0$ s, the M-SST operates at LC A without PFD control; at $t = 0.4$ s, PFD control is adopted, and M-SST still operates at LC A; at $t = 0.7$ s, LC A is switched to LC B; and at $t = 1.0$ s, LC B is switched to LC C.

The simulation results are shown in Fig. 14. Fig. 14(a) shows the MVac grid current waveform. It can be seen that MVac-side power supply is not affected by PFD control. Fig. 14(b) shows the MVdc-side voltage and current waveform. The MVdc voltage keeps stable at 20 kV, and the MVdc-side power consumption is not affected by PFD control. Fig. 14(c) shows the LVdc-side voltage and current waveforms. The LVdc voltage keeps stable at 800 V, and there is no ripple in the LVdc current under PFD control, which implies that the three-phase power ripples are eliminated naturally at the LVdc side, verifying (13). Fig. 14(a)–(c) shows the external port voltage and current curves of the M-SST. It can be concluded that PFD control only transfers the internal power ripples without influencing the basic voltage and current controls in different load conditions. Fig. 14(d) shows the cell capacitor voltage waveform. When standard control is adopted, ±10% capacitor voltage ripples could be observed. With PFD control, the voltage ripples are greatly reduced to ±1%. In different load conditions, the voltage ripple reduction

TABLE IV
PARAMETERS OF SCALED-DOWN M-SST PROTOTYPE

Parameter	Value	Parameter	Value
Power rating	4.8 kVA	Cell dc voltage	40 V
MVac voltage	80 V	MMC switching frequency	1 kHz
MVdc voltage	160 V	DAB switching frequency	6 kHz
LVdc voltage	40 V	HFT ratio	1:1
Number of SMs	24	MVdc load	5.3 Ω
Arm inductance	0.5 mH	LVdc load	0.22 Ω
Cell capacitance	10 mF	LVdc capacitance	10 mF

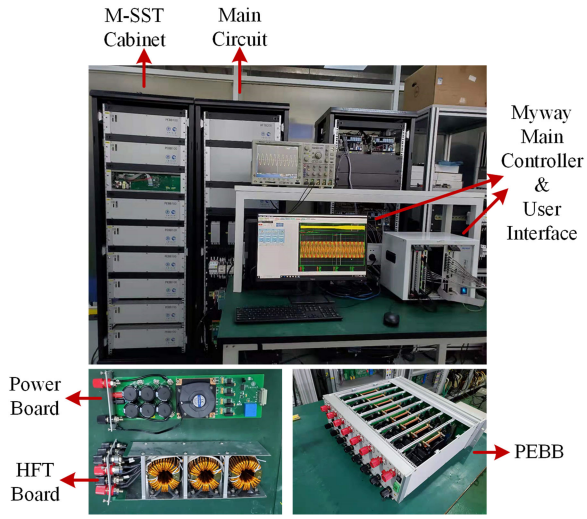

Fig. 15. 4.8-kVA M-SST experimental platform.

performance is almost identical. In fact, at LC C, there is no active power requirement from the LVdc side; thus, only the power ripples are transferred by the DAB to achieve capacitor optimization. Fig. 14(e) shows the circulating current waveform. When PFD control is adopted, the second-order component circulating current could be eliminated naturally. Fig. 14(f) shows the DAB ac-side voltage and current waveform with PFD control. The introduced power ripples will result in a low-frequency envelope in the DAB current. However, the DAB voltages on both sides are perfectly matched as the capacitor voltage fluctuations are completely eliminated. Hence, the ZVS condition of the DAB could be achieved in any operation point. This means that with PFD control, the DAB steady-state operation performance can be optimized.

B. Experimental Verifications

A 4.8-kVA scaled-down M-SST platform is constructed for experimental verifications of the proposed PFD control. The parameters of the platform are listed in Table IV. Fig. 15 shows a picture of prototype in which five-level MMC and 24 DABs are installed. The experiment results are shown in Fig. 16(a)–(e).

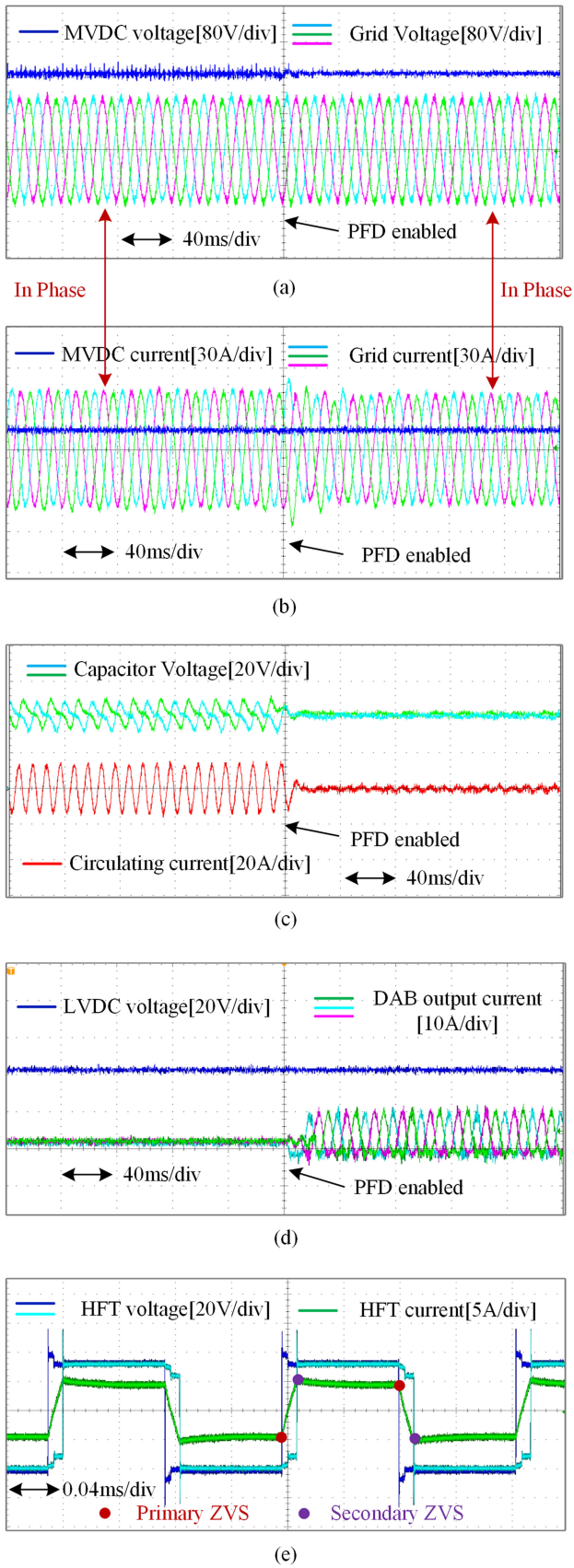

Fig. 16. Experiment results of M-SST with PFD control. (a) MVac and MVdc voltage. (b) MVac and MVdc current. (c) Cell capacitor voltage and circulating current. (d) LVdc voltage and DAB output current. (e) HFT voltage and current.

The MVac and MVdc voltages are shown in Fig. 16(a). The MVdc voltage maintains when PFD control is engaged, and its ripple is reduced due to the PFD-caused reduction of capacitor voltage fluctuations. Fig. 16(b) shows the MVac and MVdc current waveforms. The amplitude and phase of the MVac current remain unchanged with PFD, which means that the active power and power factor of the MVac port are not affected by the PFD control. The cell capacitor voltage and circulating current of phase A are shown in Fig. 16(c), where a significant reduction of voltage fluctuation is observed (from ± 5 to ± 0.5 V). Meanwhile, the circulating current is eliminated naturally. The LVdc voltage and the output currents of DABs from three of the upper arm cells, each located in one of the three phases, are shown in Fig. 16(d). With PFD control, low-frequency envelopes start to appear in the DABs' output current, indicating that the fluctuating powers are being transferred to the LVdc bus. However, since the three-phase power ripples are canceled with each other, the LVdc voltage remains unaffected. In Fig. 16(e), the primary- and secondary-side voltages and currents of an HFT with PFD control are demonstrated. With the reduction of the capacitor voltage ripples, the square wave voltages of the two sides are matched, and therefore, ZVS is achieved.

VI. Conclusion

A PFD control scheme is proposed in this article for cell capacitance optimization in multiport M-SSTs. The following conclusions can be drawn.

1) The cell capacitor voltage ripples result mainly from the low-frequency power fluctuations. With PFD control, the fluctuating powers are delivered to the LVdc side through the DABs, and thus, the capacitor voltage ripples and circulating currents in the MMC are eliminated. At the LVdc side, the fluctuating powers from all the three phases are canceled with each other and will not affect the operation of the LVdc loads.
2) The PFD control increases the peak and rms currents of the DAB; thus, redesign of the HFT and reselection of power devices and heatsinks are necessary. The design considerations are elaborated for M-SST power cell with PFD control. A 2-MVA M-SST case analysis shows that the benefits of capacitance reduction from applying the PFD control are much larger than the cost of the HFT, power device, and heatsink reselection in terms of power density of the M-SST cell. The cell capacitance can be reduced to 10%, and the power density of the whole cell can be increased by 50% in this case with the 0.22% drop of the overall efficiency.

In essence, the PFD control is a method to shift the internal power fluctuations of the MMC from the cell capacitors to the higher power density components, namely the power devices and HFTs in the DABs. Therefore, it inevitably requires increased ratings of the power devices, heatsinks, and HFTs, which are quantitatively estimated in Section IV.

It is worth nothing that according to Fig. 8, there is much higher rms current and loss associated with PFD control in light-load conditions as compared with no PFD control. In fact, it is not necessary for the PFD to transfer 100% of the fluctuating power to the LVdc side in light-load condition due to reduced ripples amplitudes. An adaptive PFD control can be developed so that both operation efficiency and power density of the M-SST are optimized.

Appendix

With PFD control, the cell capacitor voltage ripples of the M-SST are mainly caused by the high-frequency currents coming from the MMC PWM and DAB square modulation. These current ripples are solved in the following.

A. Current Ripples Caused by MMC PWM

Fig. 17 shows the carrier voltage, modulation voltage, and SM input current waveform of phase A upper arm SM. In Fig. 17, $u_c(t)$ is the carrier voltage, and $u_r(t)$ is the modulation voltage.

When $u_r(t) > u_c(t)$, an SM is inserted to the MMC circuit, and the SM input current equals the arm current, i.e., $i_{iap}(t) = i_{ap}(t)$. When $u_r(t) < u_c(t)$, the SM is bypassed from the MMC circuit, and the SM input current equals zero, i.e., $i_{iap}(t) = 0$. In one carrier period, the arm current $i_{ap}(t)$ can be viewed as a constant value. Hence, the SM input current consists of multiple square waves, as shown in Fig. 17, and can be solved by double Fourier transform.

Based on Fig. 17, the carrier and modulation waveforms are expressed as

$$u_r(t) = \frac{1}{2} - \frac{1}{2} m \sin(\omega t - \delta) = \frac{1}{2} - \frac{1}{2} m \sin y \tag{A1}$$

$$u_c(t) = \begin{cases} \frac{1}{\pi}(x - \pi) + 1, & x \in [0, \pi] \\ -\frac{1}{\pi}(x + \pi) + 1, & x \in [-\pi, 0] \end{cases}$$

$$x = \omega_c t. \tag{A2}$$

To simplify the analysis, the reactive power requirement of the MVac side is not considered, and the arm current $i_{ap}(t)$ is

$$\varphi = \delta, i_a = I_m \sin(\omega t - \delta) = I_m \sin y$$

$$i_{ap} = -\frac{1}{3} I_{\mathrm{MV}} - \frac{1}{2} I_m \sin y. \tag{A3}$$

$i_{ap}(t)$ can be decomposed to ac and dc components as

$$i_{ap\_\mathrm{dc}} = -\frac{1}{3} I_{\mathrm{MV}}, i_{ap\_\mathrm{ac}} = -\frac{1}{2} I_m \sin y. \tag{A4}$$

Based on Fig. 3, in this carrier period, the switching time of the SM is

$$x = \pi(1 - m \sin y)/2, \quad t \in [0, \pi]$$

$$x = -\pi(1 - m \sin y)/2, \quad t \in [-\pi, 0]. \tag{A5}$$

According to the superposition principle, the harmonics of $i_{iap}(t)$ could be calculated by i_{ap_dc} and i_{ap_ac}, respectively.

1) Harmonics of $i_{iap}(t)$ Caused by i_{ap_dc}: Assuming that p is the harmonic order of carrier wave and q is the harmonic order of modulation wave, $A_{pq} + jB_{pq}$ is the Fourier coefficient of $i_{iap}(t)$ caused by i_{ap_dc}.

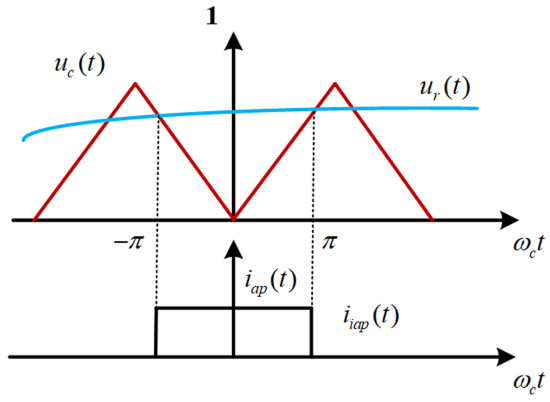

Fig. 17. Carrier voltage, modulation voltage, and SM input current waveform.

1) When $p = 0$ and $q = 0$, we have

$$A_{00} + jB_{00} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\frac{\pi}{2}(1-m\sin y)}^{\frac{\pi}{2}(1-m\sin y)}\left(-\frac{1}{3}I_{\mathrm{MV}}\right)dxdy = -\frac{1}{3}I_{\mathrm{MV}}. \tag{A6}$$

2) When $p = 0$ and $q > 0$, we have

$$A_{0q} + jB_{0q} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\frac{\pi}{2}(1-m\sin y)}^{\frac{\pi}{2}(1-m\sin y)}\left(-\frac{1}{3}I_{\mathrm{MV}}\right) \times e^{jqy}dxdy = \begin{cases} j\frac{mI_{\mathrm{MV}}}{6}, & q = 1 \\ 0, & q > 1. \end{cases} \tag{A7}$$

3) When $p > 0$ and $q = 0$, we have

$$A_{p0} + jB_{p0} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\frac{\pi}{2}(1-m\sin y)}^{\frac{\pi}{2}(1-m\sin y)}\left(-\frac{1}{3}I_{\mathrm{MV}}\right) \times e^{jpx}dxdy. \tag{A8}$$

Based on the Bessel function, (A8) could be solved as

$$A_{p0} + jB_{p0} = j\frac{2I_{\mathrm{MV}}}{3\pi p}\sin\left(p\frac{\pi}{2}\right)\cdot J_0\left(p\frac{\pi}{2}m\right). \tag{A9}$$

1) When $p > 0$ and $q \neq 0$, we have

$$A_{pq} + jB_{pq} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\frac{\pi}{2}(1-m\sin y)}^{\frac{\pi}{2}(1-m\sin y)}\left(-\frac{1}{3}I_{\mathrm{MV}}\right) \times e^{jpx}\cdot e^{jqy}dxdy. \tag{A10}$$

Based on the Taylor expansion and the Bessel function, (A10) could be solved as

$$A_{pq} + jB_{pq} = j\frac{2I_{\mathrm{MV}}}{3\pi p}\sin\left[(p-q)\frac{\pi}{2}\right]\cdot J_q\left(p\frac{\pi}{2}m\right)$$
$$J_q\left(p\frac{\pi}{2}m\right) = \sum_{l=1}^{\infty}(-1)^l\frac{\left(p\frac{\pi}{2}m\right)^{q+2l}}{2^{q+2l}l!(q+l)!}. \tag{A11}$$

2) *Harmonics of $i_{iap}(t)$ Caused by i_{ap_ac}:* Assuming that $A'_{pq} + jB'_{pq}$ is the Fourier coefficient of $i_{iap}(t)$ caused by i_{ap_ac}, using the same calculation method shown in (A6)–(A11), the coefficient can be solved.

1) When $p = 0$ and $q = 0$, we have

$$A'_{00} + jB'_{00} = \frac{1}{4}mI_m. \tag{A12}$$

2) When $p = 0$ and $q > 0$, we have

$$A'_{0q} + jB'_{0q} = \begin{cases} -jI_m/4, & q = 1 \\ -mI_m/8, & q = 2 \\ 0, & q = 0. \end{cases} \tag{A13}$$

3) When $p > 0$ and $q = 0$, we have

$$A'_{p0} + jB'_{p0} = 0 \tag{A14}$$

4) When $p > 0$ and $q \neq 0$, we have

$$A_{pq} + jB_{pq} = -\frac{I_m}{2\pi p}\cos\left[(p-q)\frac{\pi}{2}\right]\cdot K_q\left(p\frac{\pi}{2}m\right)$$
$$K_q\left(p\frac{\pi}{2}m\right) = \sum_{l=1}^{\infty}(-1)^l\frac{\left(p\frac{\pi}{2}m\right)^{q-1+2l}(2l+1)}{2^{q-1+2l}l!(q-1+l)!(2l+2)}. \tag{A15}$$

Combining (A6)–(A15), the SM input current $i_{iap}(t)$ is

$$\begin{aligned} i_{iap} = & -\frac{1}{6}I_{\mathrm{MV}} + \frac{1}{8}mI_m + \left(\frac{mI_{\mathrm{MV}}}{6} - \frac{I_m}{4}\right)\sin(\omega t - \delta) \\ & - \frac{1}{8}mI_m\cos(2\omega t - 2\delta) \\ & + \sum_{p=1}^{\infty}\frac{2I_{\mathrm{MV}}}{3\pi p}\sin\left(p\frac{\pi}{2}\right)\cdot J_0\left(p\frac{\pi}{2}m\right)\sin(p\omega_c t) \\ & + \sum_{p=1}^{\infty}\sum_{q=-\infty}^{\infty}\frac{2I_{\mathrm{MV}}}{3\pi p}\sin\left[(p-q)\frac{\pi}{2}\right]\cdot J_q\left(p\frac{\pi}{2}m\right) \\ & \times\sin(p\omega_c t + q\omega t - q\delta) \\ & - \sum_{p=1}^{\infty}\sum_{q=-\infty}^{\infty}\frac{I_m}{2\pi p}\cos\left[(p-q)\frac{\pi}{2}\right]\cdot K_q\left(p\frac{\pi}{2}m\right) \\ & \times\cos(p\omega_c t + q\omega t - q\delta). \end{aligned} \tag{A16}$$

In (A16), the dc component will transfer to the DAB side, because no dc current flows into the cell capacitor in the steady state. With PFD control, the first- and second-order components in (A16) are also transferred to the DAB side. Meanwhile, the carrier-order components and sideband components of current harmonic will flow into the cell capacitor.

B. Current Ripples Caused by DAB Square Modulation

Fig. 18 shows the DAB input current wave without PFD control. According to [16], in half DAB square wave period,

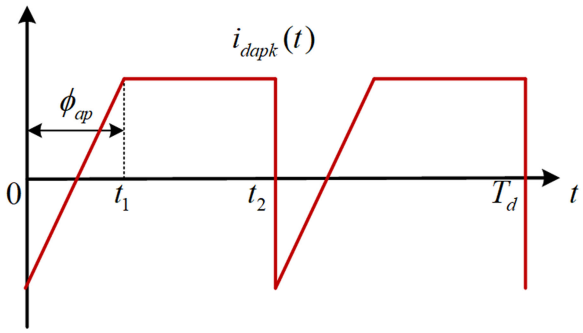

Fig. 18. DAB input current wave without PFD control.

the DAB input current $i_{dapk}(t)$ can be expressed as

$$i_{dapk}(t) = \begin{cases} -\frac{U_c\phi_{ap}}{2\pi f_d L_d} + \frac{2U_c}{L_d}t, & 0 \le t \le t_1 \\ \frac{U_c\phi_{ap}}{2\pi f_d L_d}, & t_1 \le t \le t_2 \end{cases}$$
$$t_1 = \phi_{ap}/(2\pi f_d). \tag{A17}$$

As a periodic function, $i_{dapk}(t)$ is composed of dc component and ac harmonics based on Fourier analysis

$$i_{dapk}(t) = C_0 + \sum_{r=1}^{\infty}[C_r\cos(r\omega_d t) + D_r\sin(r\omega_d t)]. \tag{A18}$$

In (A18), the Fourier coefficient is solved as

$$C_0 = \frac{2}{T_d}\int_0^{\frac{T_d}{2}} i_{dapk}(t)dt = p_{dapk}/U_c$$
$$C_r = \frac{4}{T_d}\int_0^{\frac{T_d}{2}} i_{dapk}(t)\cos(n\omega_d t)dt = \frac{8U_c[\cos(r\phi_{ap})-1]}{(2\pi r)^2 L_d f_d}$$
$$D_r = \frac{4}{T_d}\int_0^{\frac{T_d}{2}} i_{dapk}(t)\sin(n\omega_d t)dt$$
$$= -\frac{4U_c[r\phi_{ap}\cos(r\pi) + r\phi_{ap} - 2\sin(r\phi_{ap})]}{(2\pi r)^2 L_d f_d} \tag{A19}$$

where T_d is the period of the DAB square wave.

In (A19), the dc component of $i_{dapk}(t)$ is provided by the MMC SM input current, and the ac components of $i_{dapk}(t)$ are provided by the cell capacitor. Combining (A16), (A18), and (A19), the capacitor input current is derived as (21).

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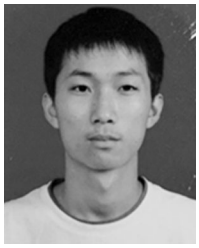

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