Control Design of a Single-Phase Inverter Operating With Multiple Modulation Strategies and Variable Switching Frequency

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***Abstract*—This article presents a control linearization technique for a single-phase single-stage inverter with multiple modulation strategies. The power topology is based on an flying capacitor multi-level (FCML) inverter, and the control is based on the plant inversion. The proposed technique allows decoupling the control of the input current and the output voltage, which simplifies the control in two ways: first, the control of both variables is independent and second, the controllers are independent of the modulation applied, thanks to the plant inversion. This control is implemented in an field-programmable gate array. Since the converter operates at variable frequency, two different data acquisition alternatives are explored: sampling at variable frequency (once per switching cycle) or sampling at constant frequency (higher than the switching frequency).The proposed control is validated by simulation and experimental results with a 1-kVA prototype.**

***Index Terms*—Control design, dc–ac power conversion, digital control, inverters, solar energy, switching converters.**

I. Introduction

In THE last decade, photovoltaic (PV) systems are increasingly being recognized as a sustainable energy solution to mitigate the depletion of the fossil fuel and the greenhouse effect. In PV applications, the current drawn from the panel must be dc. AC currents reduce the efficiency and degrade the PV system [1], [2]. Due to that, a power conversion interface is needed between the grid and the PV panel.

To promote the search for new solutions, Google and IEEE launched in 2014 the Little Box Challenge, an open competition to design and build the smallest nonisolated 2-kVA single-phase inverter [3] with a roughly ten times reduction in size compared with commercially available inverters at that time. The main specifications of that competition are listed in Table I. To emulate the behavior of a PV panel, a 450 V_{DC} voltage source with a 10-Ω series resistor is used.

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TABLE I
Main Specifications

Parameter	Value
Input Voltage	$450\ V\ R_{serie} = 10\ \Omega$
Output Voltage	$240\ V_{rms}$@60 Hz
Nominal Power	2 kVA
Power Factor	$PF \in [0.7, 1]$ leading or lagging
THD	$\leq 5\%$
Input current ripple	$\leq 20\%$
Efficiency	$\geq 95\%$
Volume	$\leq 40\ \mathrm{in}^3$
Leakage current	≤ 50 mA

To minimize the input current ripple, single-phase inverters must store energy to buffer the pulsating double-line frequency power flow at the output port. The simplest way to handle the instantaneous power mismatch is to place a bulky electrolytic capacitor at the input port. But, unfortunately, electrolytic capacitors have short lifetime and low reliability [4]. To reduce the capacitance requirements keeping the input current constant, different techniques can be applied, such as [5] –[9]. The same problem appears in power factor correction (PFC) converters; in this case, the pulsating power port is the input port [10]–[12]. A review of the main solutions presented to the Little Box Google Challenge is done in [13]. More details of some of those works can be found in [14]–[19]. In this article, the solution presented is fundamentally different from the two-stage or active filter solution referenced earlier. The proposed single-stage inverter (explained more in detail in Section II) interfaces the input, output, and storage port processing the minimum possible indirect power, achieving a size reduction [20]. This optimum power flow between the three ports is only possible applying different modulations along the line cycle, considering at any instant each port as a "quasi-static" dc port. In [21], the different operation modes are described, whereas this article is dedicated to the control methodology used, describing in detail the design and limitations of the different control loops and the feedforward active power estimation.

Each switching sequence or "mode" has a set of transfer functions, this means that the plant of the system changes along the line cycle. Furthermore, those transfer functions are coupled. To homogenize the system and to decouple the input and output port control, a plant inversion is included in the control scheme.

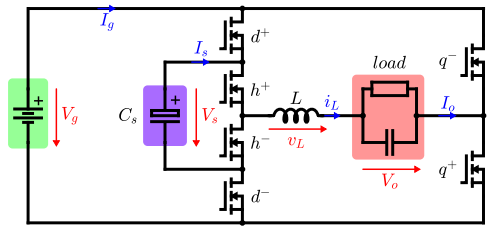


Fig. 1. Simplified schematic of the flying capacitor inverter.

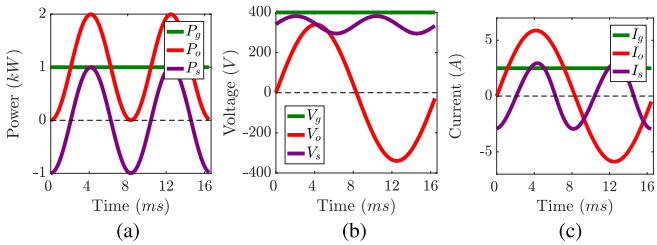


Fig. 2. (a) Power, (b) voltage, and (c) current in the three ports for 1 kVA, PF $= 1$ and $C_s = 90\,\mu$F with $\langle V_s \rangle = 340$ V.

This plant inversion is analyzed in Section III. Once the system is homogeneous, in Section IV, the control design of the different control loops is analyzed. Section V explains some considerations that have to be taken into account to discretize a system operating at variable frequency. Finally, the experimental results of the converter are presented in Section VI.

II. Topology

The converter under consideration, schematically presented in Fig. 1, is a flying capacitor [22] with the distinctive feature that the flying capacitor voltage, in this case, instead of being tightly regulated at switching frequency at $V_g/2$, is used to balance the instantaneous power mismatch between the dc input and the pulsating output, to get the desired power flow between the three ports. Therefore, in this article, the control only regulates the average voltage of the storage capacitor allowing a 25% discharge ratio at double line frequency. To have an optimal power processing, the average voltage is regulated at 340 V. Theoretical waveforms for the three ports at 1 kW and $C_s = 90\,\mu$F are shown in Fig. 2. This topology, however, suffers from large common mode voltage between input and output at switching frequency, and hence, a filter is required to limit the leakage current through the parasitic capacitance between input and ground. The common mode filter is designed to limit this current to be below 50 mA_{rms} as specified in the little box challenge (LBC) competition. As it does not affect the control design, Fig. 1 does not include it and the design is not described in this article.

To get a high power density converter, a multimode modulation is applied along the line cycle [23]. Applying different "switching sequences" (or "operation modes"), the converter operates in the fundamental limit of this type of converters, as explained in [20] and [24], processing the minimum possible indirect power for a three-port energy buffered converter.

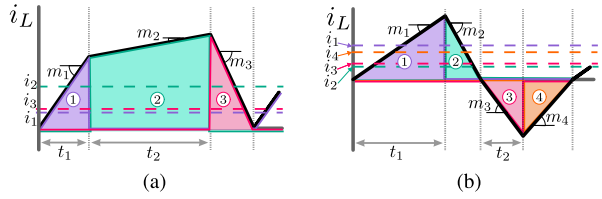


Fig. 3. Operation modes. (a) Trapezoidal mode. (b) Triangular mode.

At any instant along the line cycle, several modulations may be used, obtaining the same voltages and currents at the three ports, but yielding very different losses due to different inductor and semiconductor usage. Namely, there are up to 19 different modes, which can be classified based on the inductor current waveform, in two types: trapezoidal modes [see Fig. 3(a)], and triangular modes [see Fig. 3(b)].

A. Trapezoidal Modes

The inductor current i_L is always positive (or negative). This type of mode is composed by three switching states, as represented in Fig. 3(a), each state is represented in different colors. The average current of the first switching state is named i_1, in the same way the average value of the second i_2 and third interval i_3 can be obtained. These currents (i_1, i_2, and i_3) are always considered positive, which means that in positive trapezoidal modes, $i_L = i_1 + i_2 + i_3$, whereas in negative trapezoidal modes [symmetrical to the one represented in Fig. 3(a)], $i_L = -(i_1 + i_2 + i_3)$. The inductor current slops are named as m_1, m_2, and m_3, and they are considered positive as they are represented in Fig. 3(a), in other words, m_1 and m_3 are always positive, whereas m_2 can be positive or negative. Two independent times define these modes, these times are the duration of the first (t_1) and the second (t_2) switching states.

B. Triangular Modes

In this case, the inductor current is positive during two switching states and negative in the other two switching states [as in the trapezoidal modes, the triangular modes can be symmetrical to the one represented in Fig. 3(b), the two first states negative and the third and fourth state positive]. Once again, i_1, i_2, i_3, and i_4 are the average current of each state and are always considered positive. For triangular modes, the duration of the second and fourth intervals depends on the duration of the first and third one, respectively. For this reason, the two independent times that define these modes are the duration of the first (t_1) and the third (t_2) switching state. Once again, m_1, m_2, m_3, and m_4 are the inductor current slope in each switching state considered them positive, as represented in Fig. 3(b).

In order to select the most appropriate mode at any instant, a decision criterion is needed [23]. In this article, the indirect power ($P_{\text{ind}L}$) is used as a metric to choose the best mode [25]. The indirect power is the actual power processed by the reactive

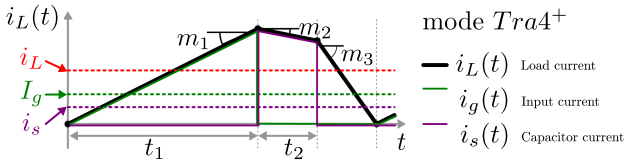


Fig. 4. Trapezoidal tribuck mode (Tra4$^+$).

components, in this particular case by the inductor, and as described in [24] is defined as

$$P_{\text{ind}L} = \frac{1}{2 \cdot T} \int_0^T |v_L(t) \cdot i_L(t)| dt. \tag{1}$$

The application of different switching sequences (operation modes) along the line cycle increases the complexity of the control, since the converter has a different plant for each mode. Applying averaging over a switching cycle removes the fast-scale time varying nature of the converter [26], but since different switching sequences are applied depending on the voltages and currents at the different ports, the system can be considered a hybrid system. To decouple the input and output control loops and to remove the dependence on the mode applied, a plant inversion is included in the control scheme.

III. Plant Inversion

Each "mode" is a combination of switching states in a predefined order. As shown in Fig. 3, two independent times (t_1, t_2) define unambiguously each switching mode. To reduce the switching losses, the converter operates in boundary conduction modes (BCMs). Due to that, the averaged inductor and input current for every specific mode k no longer depend on the previous switching cycle. Those currents depend on the two independent times, t_1 and t_2, algebraically according to

$$< i_L > \; = f_k\left(t_1, t_2, x, V_g\right) \tag{2}$$

$$< i_g > \; = g_k\left(t_1, t_2, x, V_g\right) \tag{3}$$

where f_k and g_k are nonlinear algebraic functions of the times t_1 and t_2, respectively, the state $x = (v_s, v_o)$ defined as the storage capacitor voltage and the output voltage, V_g the input voltage, and $k = \ldots, -2, -1, 0, 1, 2, \ldots$ the sequence (or mode) selected for each specific angle along the line cycle. Fig. 4 shows one of these sequences, named Tra4$^+$, in this particular case, the average value of the inductor current and the input current can be defined, following the notation describe in the description of the trapezoidal modes (see Section II) as

$$< i_L > \; = \frac{\frac{1}{2} m_1 \left(1 + \frac{m_1}{m_3}\right) t_1^2 + \frac{1}{2} m_2 \left(1 + \frac{m_2}{m_3}\right) t_2^2}{t_1 \left(1 + \frac{m_1}{m_3}\right) + t_2 \left(1 + \frac{m_2}{m_3}\right)} + \frac{m_1 \left(1 + \frac{m_2}{m_3}\right) t_1 t_2}{t_1 \left(1 + \frac{m_1}{m_3}\right) + t_2 \left(1 + \frac{m_2}{m_3}\right)} \tag{4}$$

$$< i_g > \; = \frac{\frac{1}{2} m_1 \left(1 + \frac{m_1}{m_3}\right) t_1^2}{t_1 \left(1 + \frac{m_1}{m_3}\right) + t_2 \left(1 + \frac{m_2}{m_3}\right)} \tag{5}$$

where the current slopes m_1, m_2, and m_3 are calculated as the voltage applied across the inductor divided by the inductor value, considering them positives according to Fig. 3(a) and (b). This means that for trapezoidal modes, m_1 and m_2 are positive if the inductor current increases and m_3 is positive if the inductor current decreases. However, for triangular modes, m_1 and m_4 are positive if the inductor current increases and m_2 and m_3 are positive if the inductor current decreases.

Taking into account that for a given reference input current and reference output current, it is possible to determine if for a specific mode k, there exists a solution, and, in that case, to calculate the times t_1 and t_2 that will provide the desired values for the input and inductor current. t_1 and t_2 are calculated solving the following nonlinear equations for each sequence:

$$i_L^{\text{ref}} = f_k\left(t_1, t_2, x, V_g\right) \tag{6}$$

$$i_g^{\text{ref}} = g_k\left(t_1, t_2, x, V_g\right). \tag{7}$$

For all the trapezoidal modes, these equations are

$$t_1 = 2\sqrt{\frac{i_1 i_3}{m_1 m_3}} \left[\left(1 - \frac{m_1}{m_2}\right)\sqrt{\frac{i_1 m_3}{i_3 m_1}} + 1 + \frac{m_3}{m_2}\right] \tag{8}$$

$$t_2 = t_1 \frac{m_3\sqrt{\frac{i_3 m_1}{i_1 m_3}} - m_1}{m_2}. \tag{9}$$

In the particular case of mode Tra4$^+$, as shown in Fig. 4, during the first switching state, the inductor current flow from the input port to the load, during the second switching state, the storage capacitor supplies the current to the load and finally the third switching state is a freewheeling state. According to that the average current of each state can be calculated as

$$i_1 = i_g^{\text{ref}} \tag{10}$$

$$i_3 = i_L^{\text{ref}} - i_g^{\text{ref}} - i_s. \tag{11}$$

In this article, since the converter operates in BCM, the switching frequency varies along the line cycle and also depends on the load.

Soft-switching techniques are recommended to get high power density even using wide bandgap semiconductor, as GaN high electron mobility transistors (HEMTs). To reduce switching losses, zero voltage switching (ZVS) has been implemented. To achieve ZVS in all transitions, a minimum energy has to be stored in the inductor at the beginning of each transition to charge or discharge the parasitic capacitance of the switches involved in the transition. This means that the inductor has to operate with positive and negative threshold current in all modes [21], [27].

Therefore, the operation modes have to include more switching states to achieve ZVS in all the transitions, as shown in Fig. 5. The plant inversion explained earlier based on the ideal modes is not accurate enough if we want to obtain a tight regulation, as it is shown in the next section. These new states make the equations

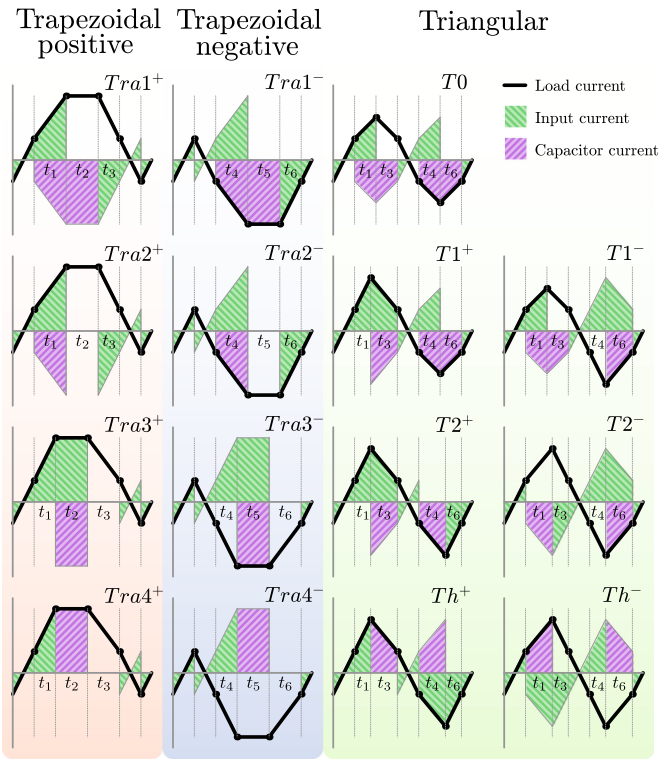


Fig. 5. Operation modes for $V_s > V_g/2$. The switching state and the applied times are depicted for each mode.

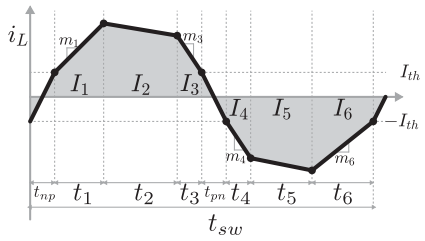


Fig. 6. Generalized inductor current waveform for all operation modes.

much more complex and, therefore, cannot be synthesized in the field-programmable gate array (FPGA).

It may be solved simplifying the algorithm to calculate the plant inversion, including the effect of the additional states. All operation modes shown in Fig. 5 are modeled through a generic waveform shown in Fig. 6. Giving the state sequence of the operation mode, slopes m_{1-6}, currents I_{1-6} and I_{th}, and the control times t_{1-6} can be calculated. With I_{1-6} and m_{1-6}, the control times t_{1-6} are obtained through the following system of equations:

$$\begin{cases} I_1 = \frac{t_1}{t_{sw}} \cdot (I_{th} + t_1 \cdot \frac{m_1}{2}) \\ I_2 = \frac{t_2}{t_{sw}} \cdot (I_{th} + t_1 \cdot \frac{m_1}{2} - t_3 \cdot \frac{m_3}{2}) \\ I_3 = \frac{t_3}{t_{sw}} \cdot (I_{th} + t_3 \cdot \frac{m_3}{2}) \\ I_4 = \frac{t_4}{t_{sw}} \cdot (-I_{th} + t_4 \cdot \frac{m_4}{2}) \\ I_5 = \frac{t_5}{t_{sw}} \cdot (-I_{th} + t_4 \cdot \frac{m_4}{2} - t_6 \cdot \frac{m_6}{2}) \\ I_6 = \frac{t_6}{t_{sw}} \cdot (-I_{th} + t_6 \cdot \frac{m_6}{2}) \end{cases} \tag{12}$$

where $t_{sw} = t_{np} + t_1 + t_2 + t_3 + t_{pn} + t_4 + t_5 + t_6$. t_{np} is the time it takes from $-I_{th}$ to I_{th}, $t_{np} = 2 \cdot L \cdot I_{th}/(V_g - V_o)$, and t_{pn} is the time it takes to go from I_{th} to $-I_{th}$, $t_{pn} = 2 \cdot L \cdot I_{th}/(V_g + V_o)$.

As in the previous case, (12) is nonlinear, and unfortunately the analytical solution to t_{1-6} as a function of m_{1-6} and I_{1-6} requires some area and time to be computed. To reduce the computational cost maintaining a good accuracy, an iterative method is proposed. The method is the following fixed point-iteration [28]:

$$\begin{cases} t_1[n] = I_1 \cdot \frac{t_{sw}[n-1]}{I_{th} + t_1[n-1] \cdot \frac{m_1}{2}} \\ t_2[n] = I_2 \cdot \frac{t_{sw}[n-1]}{I_{th} + t_1[n-1] \cdot \frac{m_1}{2} + t_3[n-1] \cdot \frac{m_3}{2}} \\ t_3[n] = I_3 \cdot \frac{t_{sw}[n-1]}{I_{th} + t_3[n-1] \cdot \frac{m_3}{2}} \\ t_4[n] = I_4 \cdot \frac{t_{sw}[n-1]}{-I_{th} + t_4[n-1] \cdot \frac{m_4}{2}} \\ t_5[n] = I_5 \cdot \frac{t_{sw}[n-1]}{-I_{th} + t_4[n-1] \cdot \frac{m_4}{2} - t_6[n-1] \cdot \frac{m_6}{2}} \\ t_6[n] = I_6 \cdot \frac{t_{sw}[n-1]}{-I_{th} + t_6[n-1] \cdot \frac{m_6}{2}} \end{cases} \tag{13}$$

where I_{1-6} and m_{1-6} are the values previously calculated and I_{th} is a stored value in the FPGA. This inversion method is explained more in detail in [21].

One additional advantage of the ZVS modulation is that the switching frequency varies from $30-160$ kHz and the times t_{1-6} change smoothly, as explained in [21]. While with the ideal modulation at certain instants along the line cycle (typically closed to a transition between two modes), the switching frequency tends to be very low, and the assumption of "quasi-static" dc ports is no longer valid. To limit the minimum switching frequency, modes with higher $P_{\text{ind}L}$ should be included, unfortunately some transitions from one operation mode to another involve a sharp change in the times t_1 and t_2 and, therefore, in the switching frequency. These sharp changes can negatively affect to the common mode noise.

IV. Control

Fig. 7 represents the completed control scheme proposed in this article. The block called "Mode selector & Plant inversion" described in [21] chooses the best switching mode in terms of the indirect power processed by the inductor taking into account the desired currents (input and inductor current) and the voltages in the three ports (input, output, and storage capacitor) and calculates the times to synthesize those desired currents, as shown in (13).

Assuming that the plant inversion is accurate enough, we can obtain two differential equations that define our control problem

$$i_{C_o}(t) = i_L(t) - i_o(t) \rightarrow C_o \frac{dv_o}{dt} = i_L^{\text{ref}} - i_o \tag{14}$$

$$p_{C_s}(t) = P_{in} - p_o(t) \rightarrow v_s C_s \frac{dv_s}{dt} = v_g i_g^{\text{ref}} - v_o i_L^{\text{ref}}. \tag{15}$$

From those equations, it can be noticed that the output voltage v_o can be controlled using i_L^{ref} (15) and the storage capacitor voltage v_s can be controlled using i_g^{ref} (14). Both equations are first-order equations and independent of each other assuming

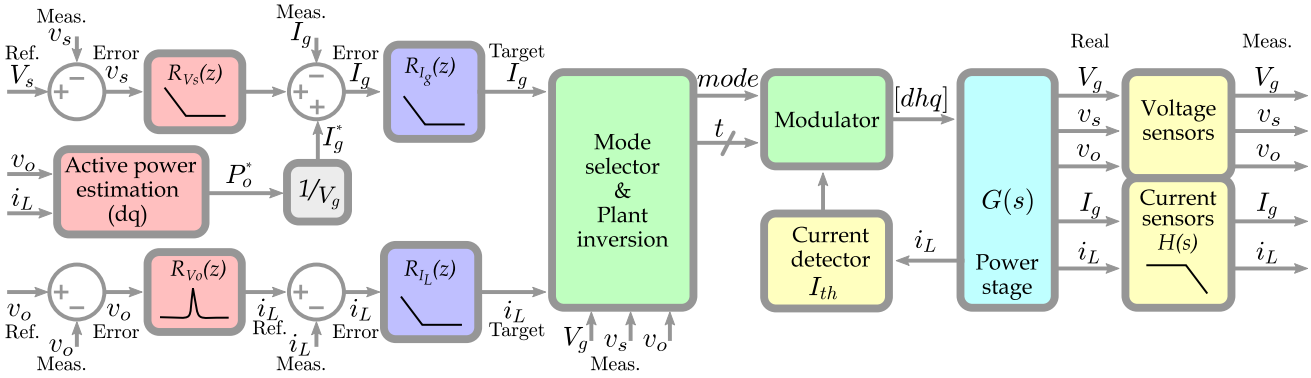


Fig. 7. Complete control scheme.

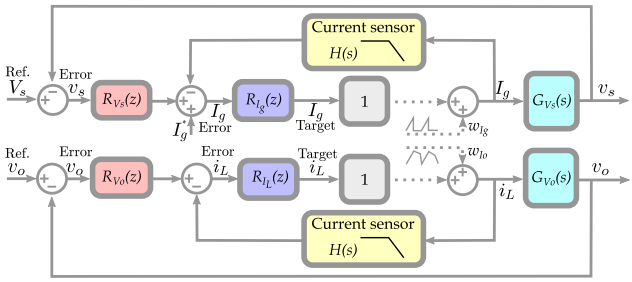


Fig. 8. Simplified control scheme, modeling the plant inversion as a unit gain block.

that the output power is a perturbation for the storage capacitor voltage loop as it is explained in the following.

Then, the control problem is simplified to two independent first-order single-input single-output (SISO) systems. As shown in Fig. 8, each SISO system is composed of an inner current loop and an outer voltage loop for each system. The design methodology of each control loop is described in the following sections, and in more detail in [29].

A. Current Loops

As can be seen in Fig. 8, the two current loops are equivalent due to the plant inversion. The aim of these control loops is to regulate the average value of each current as fast as possible. The main problem to have a fast dynamic is that as the converter operates in BCM, the inductor current and, therefore, the input current have a large ripple. In other words, the current ripple should be neglected by the control, regulating only the mean value. It is not straightforward to determine the instant of time in which the value of the instantaneous current is similar to its average value in a switching cycle, as can be done in a conventional buck converter sampling the inductor current in the middle of the duty cycle. Therefore, the best option is to include a filter in the feedback path to attenuate the current ripple.

Taking into account these considerations, the system can be modeled as in Fig. 8. The current ripple is considered a perturbation (w), the behavior of the current sensors is represented as a first-order low-pass filter (H) and the plant (G) is equal to the unit gain.

The loop gain (L) can be calculated as

$$L = R \cdot G \cdot H \tag{16}$$

and the output of these systems (the actual currents) can be modeled as

$$i_{\text{actual}} = \frac{R \cdot G}{1+L} i_{\text{ref}} + \frac{1}{1+L} w. \tag{17}$$

As the converter operates with variable frequency (30–200 kHz), the cutoff frequency of the current sensor filter is set around 100 Hz to get enough attenuation of the current ripple when the converter works at its minimum switching frequency. Taking into account the behavior of the current sensors to assure the stability of the current loops, the controller have been designed trying to follow the input reference in the whole frequency range. The zero of the PI controller is set slightly below the cutoff frequency of the filter obtaining an approximately unitary closed-loop gain for any frequency. Consequently, the bandwidth of the current loops is 100 Hz and the phase margin is 65°. Since the bandwidth is far from the minimum switching frequency (equal to the sampling frequency, as explained in the following), the effect of the delay of the digital control can be neglected.

The error introduced by the nonideal plant inversion can also be modeled as a perturbation. In this case, the control loop must correct these errors. As explained earlier, the control loop is designed to regulate the system taking into account only low frequency perturbation, which is the main reason why an accurate plant inversion is very important for this control scheme.

The bode plot of both current control loops is shown in Fig. 9.

B. Output Voltage Loop

As discussed in the previous section, the behavior of the current loops from its reference to its output can be considered as a unity gain block. With that assumption and from (14), the design of the output voltage loop is discussed. The transfer function for the output voltage is

$$G_{Vo}(s) = \frac{V_o(s)}{i_L(s)} = \frac{Z_{\text{load}}(s)}{1 + Z_{\text{load}}(s) C_o s} \tag{18}$$

where Z_{load} is the impedance of the load and C_o is the output capacitor.

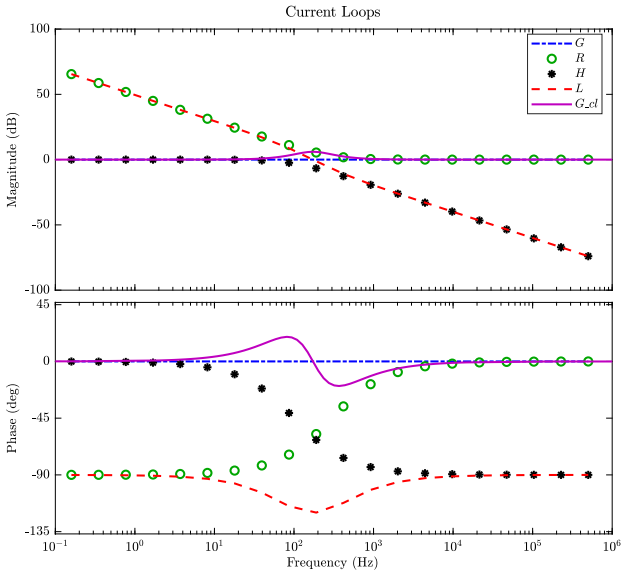


Fig. 9. Bode plots of the different transfer functions presented in the control current loops: plant G (blue), filter sensor H (black), regulator R (green), loop gain L (red), and closed-loop gain G_{cl} (magenta).

For this type of system, a conventional stationary frame regulator, such as PI, is an interesting option because of its simplicity. But the PI controller can only provide finite gain at nonzero frequencies, which means that it is not possible to obtain a zero steady-state error regulating a sinusoidal signal. However, proportional resonant (PR) (19) regulators have an infinite gain at a certain frequency, therefore they are frequently used in applications in which it is desired to control sinusoidal waveforms [30]. In consequence, a PR controller is chosen as the output voltage regulator

$$R_{Vo}(s) = k_p + \frac{k_i s}{s^2 + \omega^2}. \tag{19}$$

The control of this inverter is implemented in an FPGA due to the necessity of a high speed in complex calculation and to parallelize different tasks without prioritizing some tasks over others. To reduce the area and the processing time, fixed-point arithmetic is used. As a result of the narrow band and infinite gain of PR controllers, special attention must be taken in the discretization [31] not to degrade these characteristics. More details about the discretization method are presented in Section V.

C. Storage Capacitor Voltage Loop

The storage capacitor voltage loop regulates the average value at $0.85 \cdot V$. As in the previous section, this loop design is based on the assumption that the input current loop behaves as unity gain block. In this case, the plant can be obtained from (15)

$$G_{Vs}(s) = \frac{V_s(s)}{i_g(s)} = \frac{V_g}{V_s^{\text{ref}} C_s s}. \tag{20}$$

As mentioned in Section II, the flying capacitor is used to balance the instantaneous power mismatch between the input and output port. But during a load step, ideally the input port should adapt the power delivered to the load keeping the energy of the storage

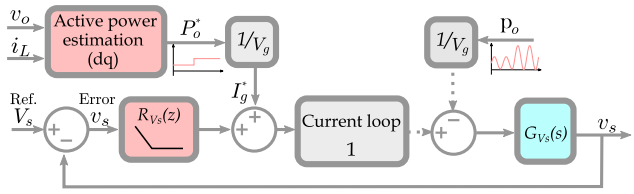


Fig. 10. Storage capacitor voltage loop with active power estimation feedforward loop.

capacitor constant. This means that on one hand, the control of the storage capacitor voltage should regulate the average value, allowing the 120-Hz ripple. Having a constant storage capacitor voltage reference, the bandwidth of this control loop has to be low enough to neglect the ripple, as in the case of the current control loops. But on the other hand, this capacitor is designed to handle only the unbalance between the input and the output power in steady state. Which means that with a low-bandwidth control loop, it has not enough stored energy to maintain its voltage in an appropriate range if a load step occurs or in other words, a fast dynamic control loop is needed to adjust the input current reference after a load step. A good compromise between the input current ripple and the response under a load step would not be possible without increasing the capacitance if the input current ripple is limited to the steady-state ripple (20%), or in other words, if we want to have a 25% discharge ratio over the storage capacitor.

To solve this problem, the control presented in Fig. 10 is proposed, this control scheme consists on a slow dynamic feedback control loop, to maintain low input current ripple in steady state, and a feedforward loop with the estimation of the active power delivered to adapt as fast as possible the input current reference under a load step.

The transfer functions of Fig. 10 are described in (20) and (21). As the plant already has an integral behavior, a proportional regulator will be sufficient to control the system

$$R_{Vs}(s) = k_R = i_{g,pp}/V_{s,pp}. \tag{21}$$

Therefore, the loop gain of this control loop can be expressed as

$$L_{Vs}(s) = R_{Vs} \cdot G_{Vs} = \frac{i_{g,pp}}{V_{s,pp}} \frac{V_g}{V_{c,\text{mean}}} \frac{1}{C_s s}. \tag{22}$$

From (21) and (22), and assuming that the inner current loops behave as a unity gain block, the maximum bandwidth loop can be calculated

$$f_{\text{BW,max}} = \frac{i_{g,pp}}{I_g} f_{\text{line}}. \tag{23}$$

The converter under consideration is a 2-kW inverter with a 400 V_{DC} input voltage and 240 V_{rms} at 60–Hz output voltage, the storage capacitor voltage has to be controlled around 340 V with a 100-V ripple. To comply with a 20% maximum input ripple, the maximum bandwidth is 12 Hz. Similar results are obtained for a 1-kW prototype as the storage capacitor scales with the power, and the input current ripple allowed is a percentage of the input current.

To have zero dc error under a perturbation of the output power, instead of using just a proportional controller, a PI controller has been implemented with its pole at very low frequency (around 1 Hz). The previous analysis is still valid considering that at higher frequencies, the system behaves as the one with the proportional controller.

To estimate the active power of linear load, three different solutions have been studied.

1) dq Output Power Estimation: The dq synchronous reference frame transformation can be used to rotate the reference frames of ac waveforms such that they become dc signals, but the original dq transformation can only be applied to three-phase systems [32]. One approach to extending the dq theory to single-phase converters is to use a quarter period time delayed version of the signal as the orthogonal vector [33].

The active power can be calculated using the dq transformation as

$$P_o = Re\{V_{dq} I_{dq}\} = \frac{1}{2}\left(V_d I_d + V_q I_q\right). \tag{24}$$

This approach allows adapting the input current reference in a quarter period time.

2) $\alpha\beta$ Output Power Estimation: To reduce significantly the computational cost, the stationary reference frame $\alpha\beta$ is used obtaining similar results. As for the dq transformation, the orthogonal variable is obtained shifting 90° the original signal. With this transformation, the active power delivered to the load can be obtained as

$$P_o = Re\{V_{\alpha\beta} I_{\alpha\beta}\} = \frac{1}{2}\left(v_\alpha i_\alpha + v_\beta i_\beta\right) \tag{25}$$

where

$$\begin{aligned} v_\alpha &= v_o(t) = V_o \sin(\omega t) \\ v_\beta &= v_o(t)_{\angle -\underline{90^\circ}} = V_o \sin(\omega t - \pi/2). \end{aligned} \tag{26}$$

Both alternatives need to store a quarter period of the output current and voltage to get the orthogonal component but the calculations are much simpler in the $\alpha\beta$ transformation

$$\begin{pmatrix} V_d \\ V_q \end{pmatrix} = \begin{pmatrix} \sin\theta & -\cos\theta \\ \cos\theta & \sin\theta \end{pmatrix} \begin{pmatrix} v_\alpha \\ v_\beta \end{pmatrix}. \tag{27}$$

Since we are using the $\alpha\beta$ transformation, instead of storing the output voltage and the output (or inductor) current in two dedicated memories, we only store the output power reducing the memory requirements. In this way, the active power calculation is simplified to

$$P_o = \frac{1}{2}\left(v_o(t) i_o(t) + v_o(t)_{\angle -\underline{90^\circ}} i_o(t)_{\angle -\underline{90^\circ}}\right). \tag{28}$$

3) Generalized Output Power Estimation: The methods presented earlier are no longer valid with nonlinear loads as the active output power does not fulfill (28).

In [33], an analysis including systems with harmonics is also carried on, but with nonlinear loads, there are odd and even harmonics. Therefore, the first harmonic that has to be filtered in the dq transformation is mapped at the line frequency. This means that the two methods explained earlier are no longer a fast estimation and only increase the complexity of the system without any improvement of the dynamics during a load step, as shown in Section VI.

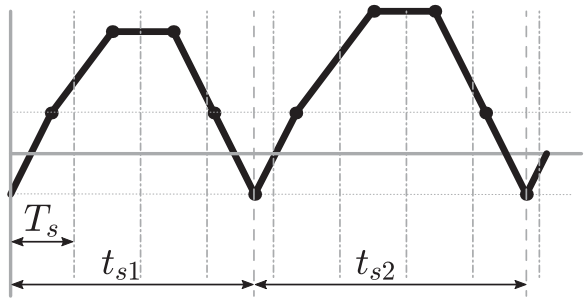


Fig. 11. Fixed frequency versus variable frequency sampling.

In this article, we propose a different approach to calculate the active power. We integrate the output power over half a line cycle. The memory needed is twice the one needed in the case of linear loads, but it still can be implemented on the selected FPGA, and can be used with any type of load

$$P_o = \frac{1}{T}\int_{t-T}^{t} i(t)v(t)dt = \frac{2}{T}\int_{t-T/2}^{t} i(t)v(t)dt. \tag{29}$$

V. Sampling Frequency and Discretization

As the converter operates in BCM, the switching frequency is variable. To control a converter with variable switching frequency, basically, there are two alternatives: Either calculate the control variables at a fixed frequency or compute the control algorithms once per switching cycle (Fig. 11).

Due to the plant inversion, the complex modulation scheme, and the mode selector, the converter is controlled digitally while the switching frequency is variable. With this type of systems, special attention has to be taken into account to assure the stability. Regarding the quantization resolution and limit cycling, the small-signal gain of the digital pulsewidth modulation (DPWM) or digital pulse-frequency modulation varies proportionally to the switching frequency [34]. At high frequency, the resolution of the DPWM is limited by the maximum clock frequency; if its resolution is lower than the resolution of the analog to digital converter (ADC), limit cycles may appear. To prevent this issue, some authors adjust the resolution of the ADC depending on the switching frequency. In this article, the ADC resolution is constant (12 b) and the clock frequency is 50 MHz and this effect is included in VHDL simulations to assure the stability of the system over the whole range of operation.

The most common approach to control a system operating at variable switching frequency is to sample at a fixed frequency higher than the switching frequency, sampling several times per switching cycle. Thereby, phase lag can be reduced but oversampling can inject high frequency disturbances [35]–[37] due to the high frequency ripple of the currents and voltages measured. To reduce the ripple, the most straightforward solution is to include a low-pass filter, but this also affects the maximum bandwidth achievable, as seen in the analysis of the current control loops.

The best benefit of oversampling controllers is the phase lag reduction. Unfortunately, for this particular case, we cannot take

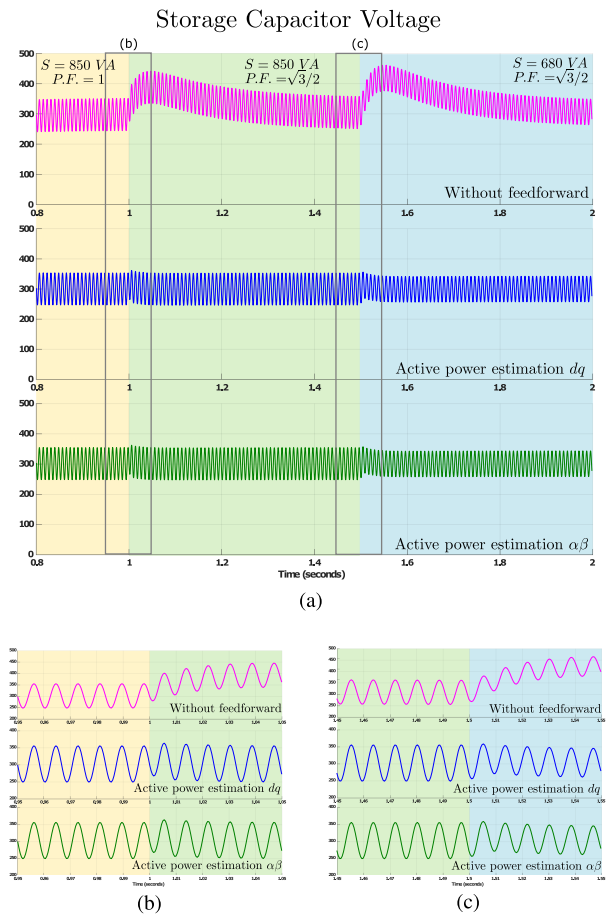


Fig. 12. a) Complete simulation of different storage capacitor voltage loops. b) and c) detail waveforms at 1s and 1.5s. From top to bottom: conventional low bandwidth control loop (magenta), control loop with active power estimation using dq (blue) and control loop with active power estimation using $\alpha\beta$ (green).

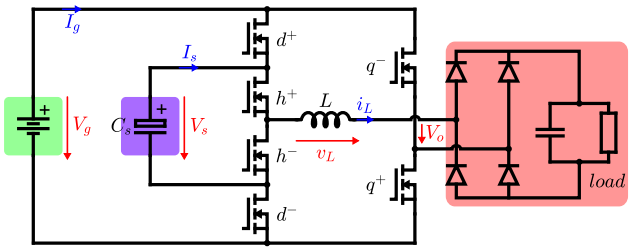


Fig. 13. Diode bridge rectifier load.

advantage of the lag reduction. The variables t_1 and t_2 cannot be updated if there is a transition between operation modes. This means that for the case under study, the maximum phase lag is set by the minimum switching frequency instead of the sampling frequency. Another alternative would be to sample at the variable frequency once per switching cycle.

As mentioned in Section IV, the control can be designed in continuous domain, regardless if the digital controllers are operating at constant frequency or at variable frequency. Continuous systems can be defined using the state-space model as a set of

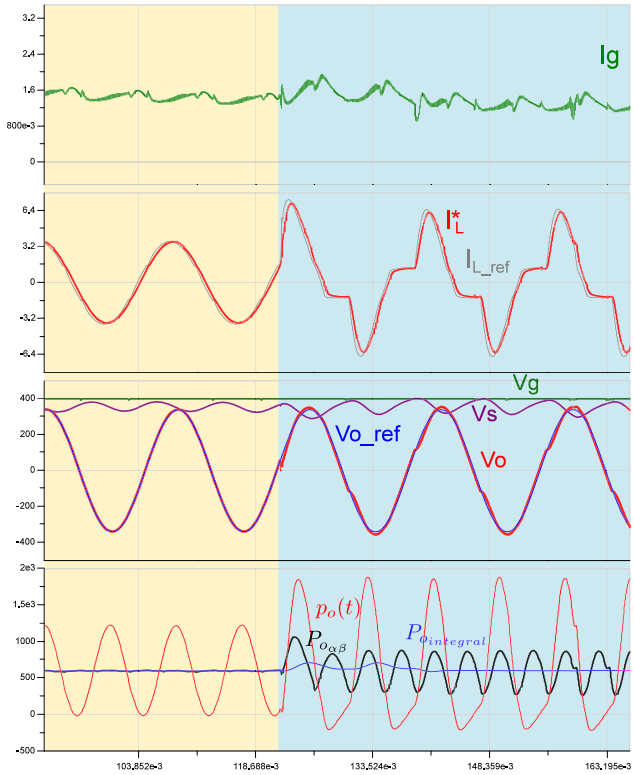


Fig. 14. Simulated waveform of the inverter with a nonlinear load. From top to bottom: Input current (green), inductor current filtered (red) and inductor current reference (gray), input voltage (green), storage capacitor voltage (purple), output voltage reference (blue) and output voltage (red), and output power (red), output power estimation ($\alpha\beta$) (black) and output power estimation (integral) (blue).

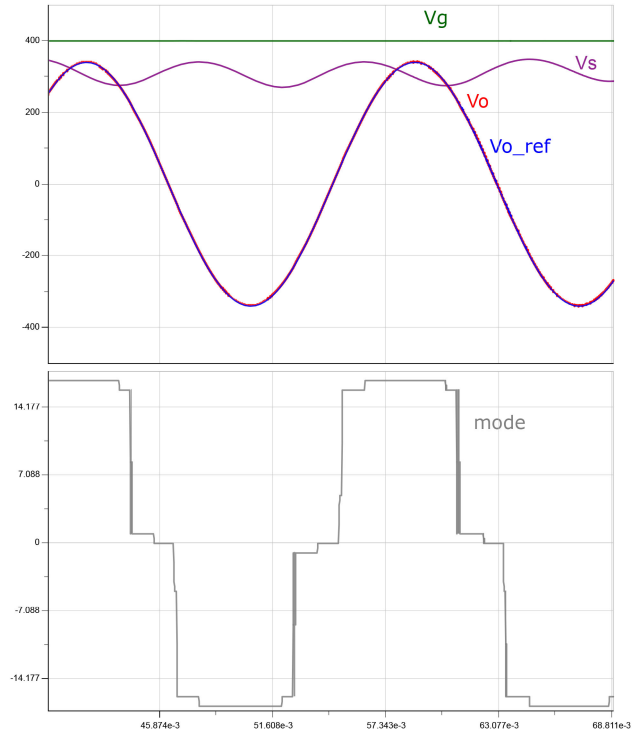


Fig. 15. Detail of Fig. 19. From top to bottom: Input voltage (green), storage capacitor voltage (purple), output voltage reference (blue), and output voltage (red) and operational mode applied.

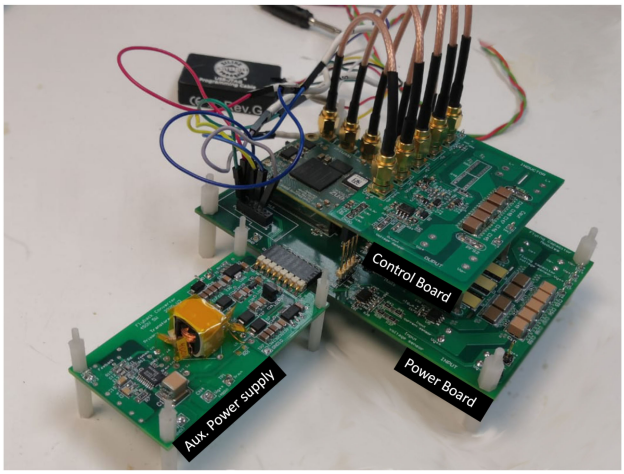


Fig. 16. Prototype used for experimental validation.

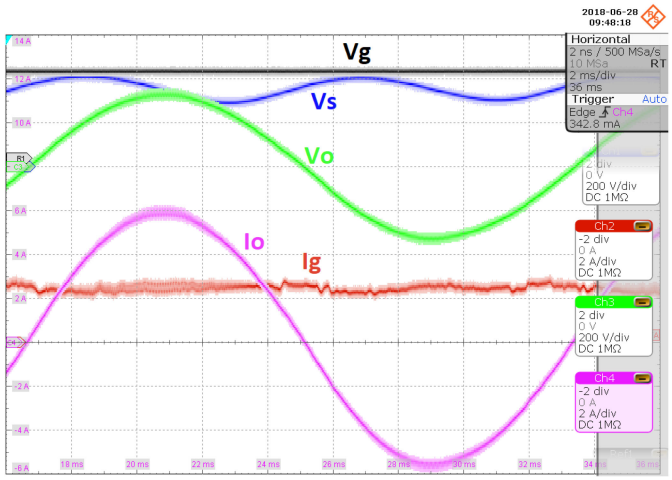
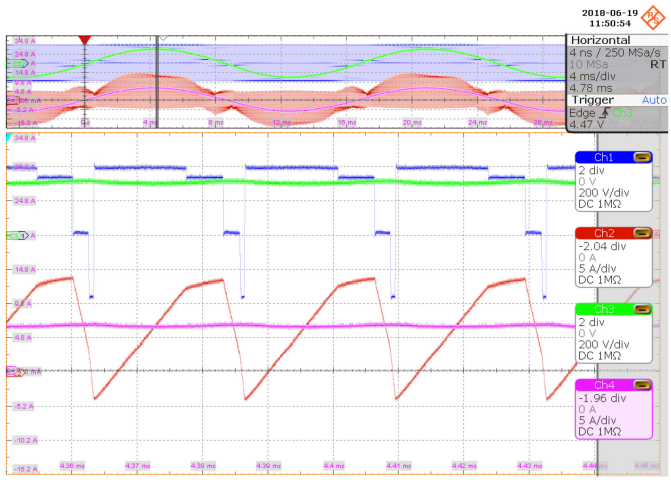
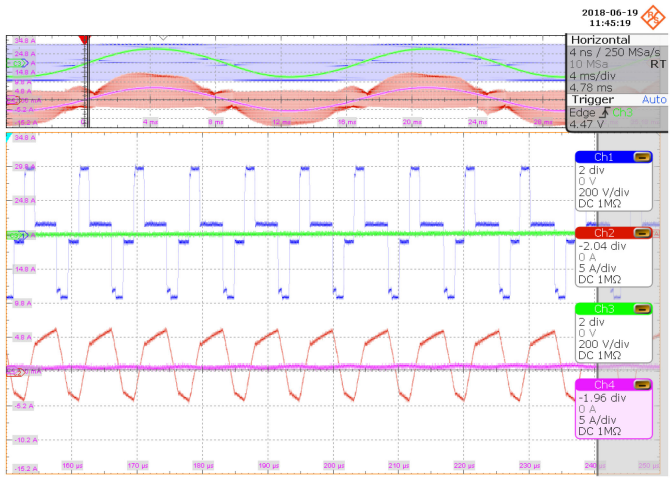


Fig. 17. Experimental waveform of the inverter at line frequency. Input voltage (black), storage capacitor voltage (blue), output voltage (green), input current (red), and output current (magenta).



(a)



(b)

Fig. 18. Experimental waveform of the inverter at switching frequency. Output voltage (green), inductor voltage (blue), inductor current (red) and output current (magenta). a) trapezoidal mode b) triangular mode.

first-order differential equations as

$$\begin{cases} \dot{x} = Ax + Bu \\ y = Cx + Du. \end{cases} \tag{30}$$

Once the system is defined in the continuous domain, it can be discretized

$$\begin{cases} x_{k+1} = Gx_k + Hu_k \\ y_k = Cx_k + Du_k \end{cases} \tag{31}$$

$$G(T) = e^{AT} \tag{32}$$

$$H(T) = \left(\int_0^T e^{A\lambda} d\lambda \right) B. \tag{33}$$

If the sampling frequency is not constant, the system matrix G and the control matrix H depend on the switching period as can be seen in (32) and (33). Therefore, the discrete system is a time-variant system, which means that it cannot be reduced to a transfer function. Choosing the forward Euler method

$$z = 1 + sT \tag{34}$$

to illustrate this problem, the discrete system can be written as

$$\begin{cases} x_{k+1} = (AT + I)\, x_k + BTu_k \\ y_k = Cx_k + Du_k. \end{cases} \tag{35}$$

Therefore, it is necessary to operate with state variables instead of with a transfer function. Only in the case of first-order systems, operating with transfer function is equivalent to working with state variables. Generally, when controlling at variable frequency, the control is based on the plant inversion of first-order system as in [38] or otherwise PI controllers are implemented [39]. But in our case, we design a PR controller (19) to regulate the output voltage.

Moreover, as mentioned earlier, due to the narrow band and infinite gain of PR controllers, special attention must be taken in the discretization [31]. To reduce the finite word length effect [40]–[42], the δ-operator is used. The δ-operator can be defined in terms of the shift operator z and the sampling time Δ as

$$\delta^{-1} = \frac{\Delta z^{-1}}{1 - z^{-1}}. \tag{36}$$

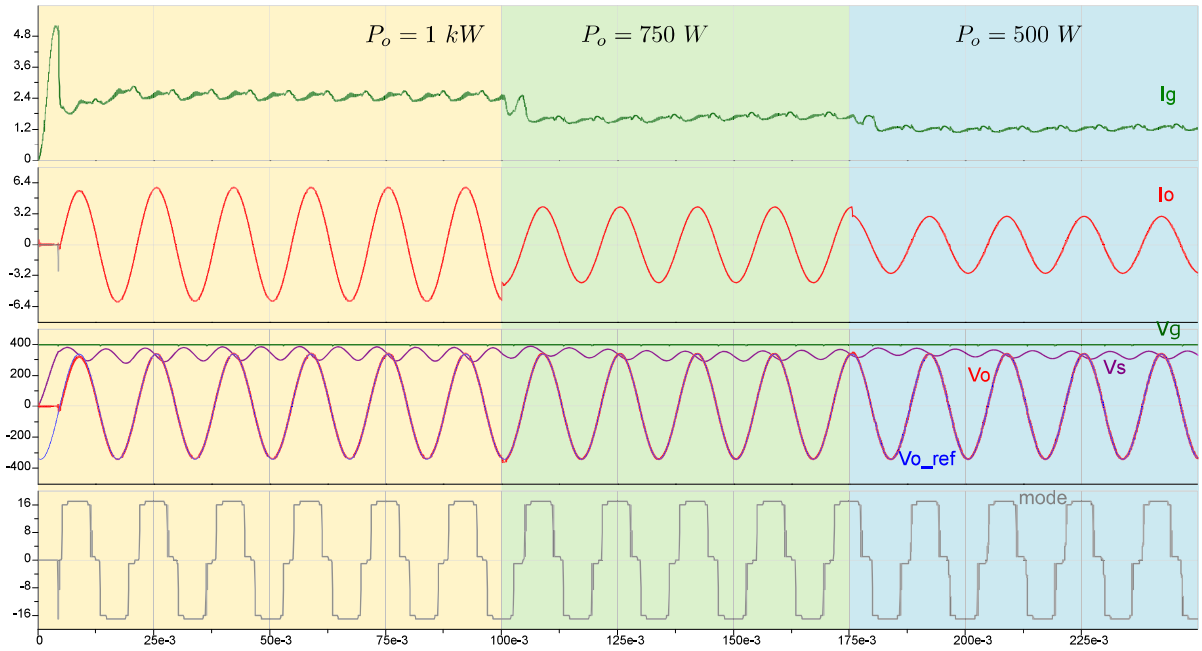


Fig. 19. Simulated waveform of the inverter with a load step from 1 kW to 750 W at 100 ms and from 750 kW to 500 W at 175 ms. From top to bottom: Input current (green), output current (red), input voltage (green), storage capacitor voltage (purple), output voltage reference (blue), and output voltage (red) and operational mode applied.

Two different implementations, the δ-operator and shift-operator, have been simulated with MATLAB Simulink and the minimum size needed for all the coefficients have been calculated using the fixed-point tool. The δ-operator allows using 16-b word length resolution, instead of the 35-b word length resolution needed for the shift transformation, which means less computation effort

$$\begin{cases} \dot{\boldsymbol{x}} = \begin{pmatrix} 0 & 1 \\ -\omega_r & 0 \end{pmatrix} \boldsymbol{x} + \begin{pmatrix} 0 \\ 1 \end{pmatrix} V_o^{\text{error}} \\ I_{\text{out}}^{\text{ref}_R} = \begin{pmatrix} 0 & k_i \end{pmatrix} \boldsymbol{x} \\ I_{\text{out}}^{\text{ref}_P} = k_p V_o^{\text{error}} \\ I_{\text{out}}^{\text{ref}} = I_{\text{out}}^{\text{ref}_R} + I_{\text{out}}^{\text{ref}_P}. \end{cases} \tag{37}$$

Thereby, using the forward Euler method $s = \delta$, the discrete PR controller can be calculated as

$$\begin{cases} \delta x_1\{k\} = x_2\{k-1\} \\ \delta x_2\{k\} = -\omega^2 x_1\{k-1\} + V_o^{\text{error}}\{k-1\} \\ I_{\text{out}}^{\text{ref}}\{k\} = 2k_i x_2\{k\} + k_p V_o^{\text{error}}\{k-1\} \\ x_1\{k\} = T_{sw}\{k-1\}\delta x_1\{k\} + x_1\{k\} \\ x_2\{k\} = T_{sw}\{k-1\}\delta x_2\{k\} + x_2\{k\}. \end{cases} \tag{38}$$

This discretization method can be extended to any type of regulator.

VI. Validation, Simulation, and Experimental Results

In this section, a comparison between the different alternatives to estimate the output power is presented.

As mentioned in Section IV-C, the bandwidth of the feedback control loop is limited. A PI controller has been designed to have a bandwidth of 10 Hz. For linear loads, the dq transformation and the $\alpha\beta$ transformation are the best alternatives as they only store a quarter period. To compare both solutions with a conventional control without the feedforward active power estimation, a simplified Simulink model has been implemented. At 1 s [see Fig. 12(b)], a load step occurs, changing the power factor from 1 to $\sqrt{3}/2$ maintaining the apparent power. At 1.5 s [see Fig. 12(c)], the load maintains the power factor changing the apparent power from 850 to 680 VA. As shown in Fig. 12(a), similar results can be obtained using $\alpha\beta$ stationary reference frame (blue) or using dq rotating reference frame (green). In less than three line cycles, the system reaches the steady state, whereas a large deviation from the reference occurs with a conventional feedback loop (magenta), as expected.

To analyze the behavior of this system with a nonlinear load, a diode bridge rectifier is connected to the output of the inverter, as shown in Fig. 13.

As mention in Section IV-C.3, the qd and $\alpha\beta$ estimation is not valid for nonlinear load and an alternative based on a half cycle moving average (half cycle output power integral) is proposed. As can be seen in Fig. 14, the system operates correctly with any type of load. In the bottom part of the figure, the actual output power (red), the estimated power using the $\alpha\beta$ transformation (black), and the generalized output power estimation (blue) for a linear load (yellow background area) both alternatives ($\alpha\beta$ and integral) are equivalent. But with a nonlinear load (blue background area), the active power calculated using $\alpha\beta$ transformation presents a high ripple, whereas the generalized method calculates correctly the active power.

In order to validate the control proposed earlier, many simulations have been carried out. Not only with electrical simulations, such as those presented in Fig. 15, Figs. 19 and 20 were obtained using Gecko circuit [43], but also the system behavior within the FPGA was simulated with the HDL ModelSim [44], to prove

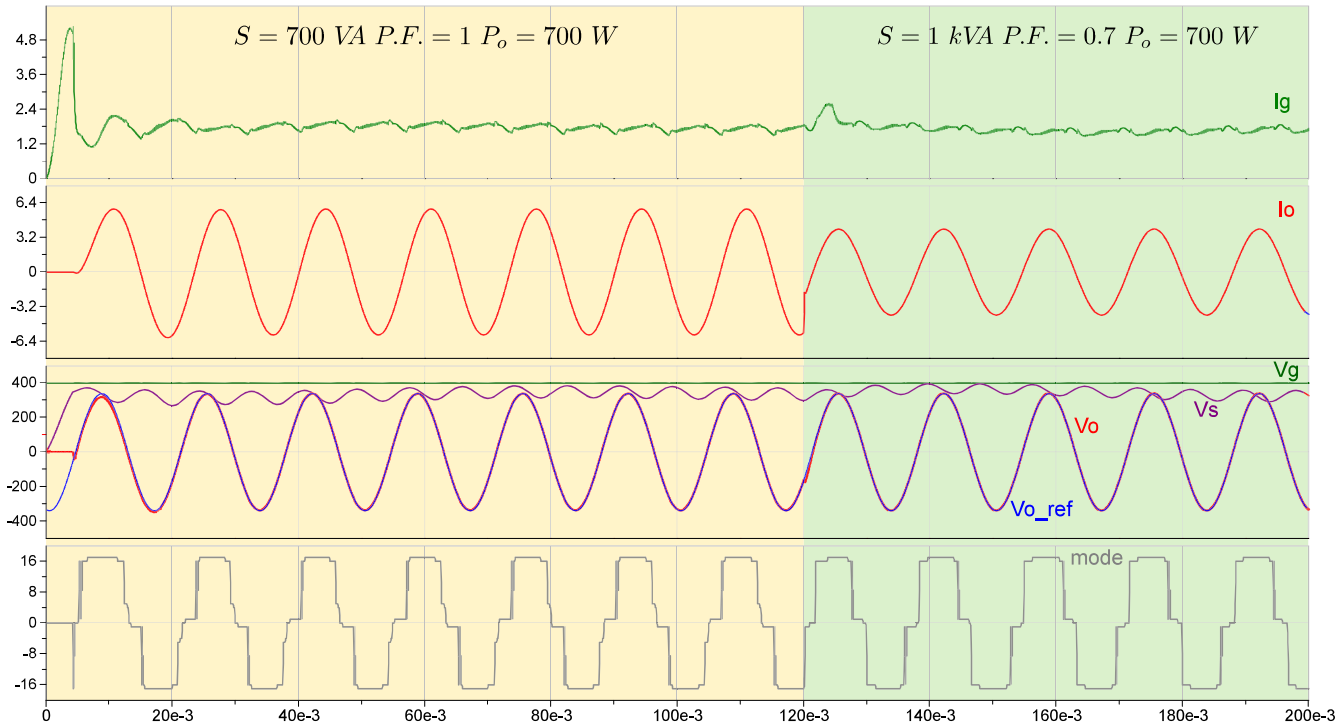


Fig. 20. Simulated waveform of the inverter with a load step from 700 W to 1 kVA(P.F. = 0.7) at 120 ms. From top to bottom: Input current (green), output current (red), input voltage (green), storage capacitor voltage (purple), output voltage reference (blue), and output voltage (red) and operational mode applied.

TABLE II
PROTOTYPE

Component	Part Number
Power Switches	GS66516T
Inductor	80 µH custom design
Storage Capacitor	90 µF ($216xX6S$ 2.2 µF 450V)
Control Board	TE0711-01-100-2C
	ARTIX-7 A100T 100 MHz 32 MB
Input Voltage	400 V
Output Voltage	240 V_{rms}@60 Hz
Nominal Power	1 kVA
Switching frequency range	30 kHz – 160 kHz
Efficiency	98%

that all the algorithms work correctly in a fixed point system. Fig. 15 shows the steady-state waveforms of the inverter supplied from 400 $V_{\rm DC}$ input voltage and generating an output voltage of 240 $V_{\rm rms}$ at 60 Hz, similar results were obtained with the prototype shown in Fig. 16 which main characteristics and components are listed in Table II, as can be seen in Fig. 17 and Fig. 18.

In Fig. 19, at 100 ms, a load step from 1 kW to 750 W is applied and at 175 ms, a second load step from 750 kW to 500 W is applied. The system recovers to the steady state in less than three line cycles. Fig. 19 shows a load step down from 700 W to 1 kVA (power factor P.F.=1−0.7) at 120 ms. In both simulations, the first 5 ms, the converter is charging the storage capacitor, after that during the rest of the simulation, the output voltage total harmonic distortion (THD) is lower than 0.5% and input current ripple is remained lower than 17%.

As mentioned earlier, the control was implemented in an Artix7 FPGA in order to reduce the computational time required for the plant inversion and to implement the complex control modulation reducing the delays. The control has been successfully validated with an experimental prototype, obtaining an efficiency of 98.2% at 1 kW with an output voltage THD lower than 3%.

VII. CONCLUSION

This article describes the control algorithm proposed for a single-phase inverter. The topology selected is an flying capacitor multi-level (FCML) inverter. To optimize the volume, the flying capacitor is designed to handle the instantaneous power mismatch between the input and the output port. The converter operates with multiple modulation strategies along the line cycle to get the optimum power flow between the three ports at any instant.

To assure an ac output voltage demanding a dc input current, one possibility is to design one set of controllers valid for all the operation modes. Due to the high plant variation of the different modes and the cross-coupling between the input and output port, this method limits the design space for the control. The selected alternative is to include the plant inversion of each mode. With an accurate identification, this method homogenizes and simplifies the control into two SISO systems. One SISO system regulates the output voltage with an inner current loop and the other one regulates the input current with an outer storage capacitor voltage loop to set the input current reference. Thanks to the plant inversion, the design of the two current loops are equivalent.

A PR controller is designed to regulate the sinusoidal output voltage, this type of controller has ideally an infinite gain at the

resonance frequency. Compared with conventional PI controller, PR designs provide zero error at the resonance frequency (line frequency), which makes them very useful for ac applications, but due to the narrow band and infinite gain, especial attention must be taken in the discretization process to avoid finite word length effects.

Regarding the input current, the control has to assure that under a load step, the energy is extracted from the input port, whereas in steady state, the storage capacitor balances the power mismatch between the dc input and the ac output. To assure both conditions, a low bandwidth feedback loop is designed to reduce the input current ripple and a feedforward active power estimation is included to adapt the input current reference during a load step. Three different alternatives have been analyzed: dq, $\alpha\beta$, and a half period moving average (or "generalized method"). The dq and $\alpha\beta$ methods only need to store a quarter period information and the $\alpha\beta$ estimation requires less computational effort but they are only valid for linear loads. Half cycle information is needed in the "generalized method" reducing the dynamic of the feedforward path, through this method has the advantage that is valid for all types of loads.

This control has been implemented in a digital system (an Artix7 FPGA). Instead of sampling at constant frequency, as the converter operates at variable frequency, we measure once per switching cycle. Due to the mode transitions, oversampling at a fixed frequency does not present the advantage of reducing the delay, and controlling at variable frequency reduces the computational cost as the FPGA only has to calculate the times that have to be applied once per switching cycle. To control the system at variable frequency, transfer functions cannot be defined as the system is time variant, consequently it has been controlled operating with the state variables.

Simulation and experimental results have been presented to validate this control proposal.

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