An Active Bypass Pulse Injection-Based Low Switching Frequency PWM Approach for Harmonic Compensation of Current-Source Converters

Jinwei He, Changhao Zhang, Ming Lei, Junfei Han, Peijian Guo, and Yunwei Li, *Fellow, IEEE*

***Abstract*—In this article, a bypass pulse injection-based pulsewidth modulation approach is proposed for mitigating line current harmonics of grid-tied current-source converters (CSCs) operating at a low switching frequency. First, the relationship between the CSC output harmonic current and the format of the bypass pulse is analyzed. Then, through online adjustment of both bypass pulse location and width, the seventh harmonic component of the output current is actively regulated to mitigate the corresponding seventh line harmonic current. Meanwhile, this action may be associated with additional amplification of the fifth output current. To deal with this issue, the unsymmetrical selective harmonic elimination (SHE) modulation with online adjustable switching angles is applied to further mitigate the fifth harmonic line current. It has been experimentally validated that with the application of both the bypass pulse injection and the unsymmetrical SHE-based modulation approaches, both the fifth and the seventh harmonic line currents can be simultaneously suppressed with ultralow switching frequency below 1 kHz.**

***Index Terms*—Current-source converter (CSC), power quality, selective harmonic elimination (SHE).**

I. Introduction

As a counterpart of a voltage-source converter, a high-power current-source converter (CSC) has been widely used in medium-voltage high-power electric drives due to its simple structure, superior short-circuit blocking, and bidirectional power flow capability [1]–[2]. Promoted by the fast development of power semiconductor technologies such as SiC-based devices and reverse-blocking IGCTs, a CSC is drawing increased attention in other promising high-power applications, such as hybrid HVdc using both pulsewidth modulation (PWM) CSCs and line-commutated CSCs, wind energy conversion system, and energy storage system using superconducting coils [3]–[8].

It is important to note that the aforementioned applications usually involve with high-power CSCs. In order to reduce the switching loss of high-power CSCs, their switching frequencies are typically less than 1 kHz [9]. Under the case of such low switching frequency, a selective harmonic elimination (SHE) modulation method is preferred for its excellent harmonic mitigation performance [10], [11]. For the traditional SHE approach, it satisfies a few constraints, which are as follows:

1) the waveform must be half-cycle and quarter-cycle symmetrical;
2) on either side of the $\pi/6$ and $5\pi/6$ positions, the pulse pattern must be an antimirror image;
3) no PWM action is allowed in the center $\pi/3$ width of each half cycle [12].

Commonly, the switching angles of SHE are predetermined in an offline manner in order to eliminate the selected low-order harmonic components. However, it is necessary to note that for grid-tied CSCs, the line current can still be highly distorted by excitations from grid voltage harmonic distortions, even when the low-order harmonic components of the output current have already been sufficiently mitigated by using SHE.

To deal with the aforementioned limitations, many efforts have been made as reported in recent literature. First, the selective harmonic control (SHC) [13], which is essentially a type of unsymmetrical SHE modulation, has been developed to actively regulate the fifth harmonic output current magnitude and phase angle. Then, by setting up an optimal fifth harmonic output current reference, the line current fifth harmonic distortion can be effectively rejected. In this case, a 2-D lookup table of SHC switching angles shall be predetermined through offline iterative calculation according to the adjustment range of the fifth harmonic output current magnitude and angle. However,

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it is worth mentioning that compensating the most dominated fifth harmonic line current component cannot always ensure a satisfactory line current performance. For a practical medium-voltage CSC, in order to obtain the proper tradeoff between filter size and switching ripple filtering performance [14], the filter capacitance is selected between 0.3 and 0.6 p.u. and the line inductance is in the range of 0.1–0.15 p.u. [10], [14], [15]. Accordingly, the resonant frequency of the CL filter is in between fifth and seventh harmonic frequencies and the seventh line current harmonic distortion can also be obvious. Unfortunately, single harmonic frequency tuned SHC method can hardly be extended to simultaneously compensate the fifth and the seventh harmonic line currents, as a complex four-dimensional lookup table is needed for this control target and the corresponding data storage space will dramatically increase. Alternatively, through injecting sixth harmonic frequency jittering signal in the reference current phase angle, it is interesting to find that either the fifth or the seventh harmonic line current can be actively compensated [16]. Then, by adopting both the SHC modulation and the delay angle control at the same time [17], it is feasible to compensate two most dominated fifth and seventh harmonic line currents at the same time. However, it is necessary to note that injecting harmonic signal in the reference output current angle needs an accurate detection of the real-time grid frequency. Therefore, the performance of this method can be affected in weak grid applications where the PCC voltage frequency is less stiff.

In order to overcome the aforementioned issues, an alternative simultaneous fifth and seventh line current harmonics compensation approach is proposed via the combination of SHC and flexible bypass pulse injection in the modulation process. First, the impacts of injecting narrow bypass pulse in the output current are investigated and it is seen that both the location and the width of the bypass pulse can be tuned to actively compensate the seventh harmonic line current. In addition, the additional fifth harmonic current distortion associated with the bypass pulse injection and the original fifth harmonic line current excited by grid voltage harmonics are further compensated utilizing the SHC approach. Experimental results have been conducted to demonstrate that the proposed method can effectively mitigate both fifth and seventh line harmonic currents, in various situations with varying grid voltage harmonic magnitudes and phase angles.

II. Proposed PWM Approach

Fig. 1 shows the diagram of a grid-tied CSC system. The converter bridge is connected to the main grid v_g by using an output *CL* filter. The capacitance and inductance of the output *CL* filter are C_f and L_f, respectively. The CSC bridge is composed of six switches $S_1 \sim S_6$, as shown in the right-hand side of the figure.

The principle of the line current harmonic compensation is also sketched in Fig. 1. First, the performance of the conventional SHE modulation is shown in the top half. In this case, the output current i_{out} has little low-order harmonics. Note that the high-frequency switching ripples of i_{out} is not illustrated here for

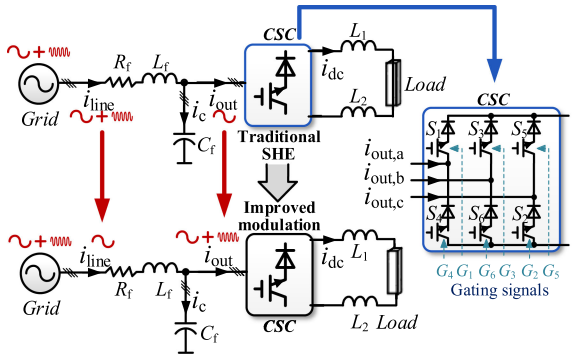

Fig. 1. Diagram of a grid-tied high-power CSC system.

the low-frequency harmonic performance analysis. However, the line current i_{line} in this case is distorted by the excitation of the grid voltage v_g harmonic components.

On the other hand, it is seen from the bottom of the figure that the line current i_{line} becomes sinusoidal when the output current i_{out} actively injects proper harmonic currents through improved modulation.

A. Introduction to SHE and SHC

The normalized output current pattern $i^*_{\text{out,SHE}}$ using the traditional SHE modulation is shown in Fig. 2, where $\theta_1 \sim \theta_{12}$ and $\tau_1 \sim \tau_{12}$ are switching angles. The constraints of the traditional SHE can be described by the following equation:

$$\theta_i = \frac{\pi}{3} - \theta_{13-i}, \text{i} = 7, 8, \ldots, 12 \tau_i = \pi - \theta_i, i = 1, 2, \ldots, 12. \tag{1}$$

As θ_1–θ_6 are free angles, the normalized output PWM current waveform is expressed as

$$i^*_{\text{out,SHE}}(\omega_0 t) = f_{\text{SHE}}(\omega_0 t, \theta_1, \theta_2, \ldots, \theta_6) \tag{2}$$

where $\omega_0 t$ is the input of the output current response function f_{SHE}, θ_1–θ_6 are the function parameters, and ω_0 is the fundamental frequency. Then, according to the Fourier theory, the output current waveform using the traditional SHE modulation can be expressed by a family of sinusoidal waveforms as

$$\begin{aligned} i^*_{\text{out,SHE}}(\omega_0 t) &= \sum_{h=1}^{\infty} \hat{I}^*_{\text{out,SHE},h} \\ &= \sum_{h=1}^{\infty} [A^*_{\text{SHE},h} \sin(h\omega_0 t + \varphi^*_{\text{SHE},h})] \end{aligned} \tag{3}$$

where h is the harmonic order, $\hat{I}^*_{\text{out,SHE},h}$ is the hth harmonic content of $i^*_{\text{out,SHE}}$, and $A^*_{\text{SHE},h}$ and $\varphi^*_{\text{SHE},h}$ are the magnitude and phase angle of $\hat{I}^*_{\text{out,SHE},h}$, respectively.

By choosing the free angles of θ_1–θ_6 in (2), it is able to completely eliminate the harmonic content at a few selected frequencies, such as the fifth and seventh harmonic components.

Nevertheless, due to the constrain of quarter-wave symmetrical, it can be easily derived through Fourier analysis that the phase angle of line current harmonic $\varphi^*_{\text{SHE},h}$ is fixed to 0, which

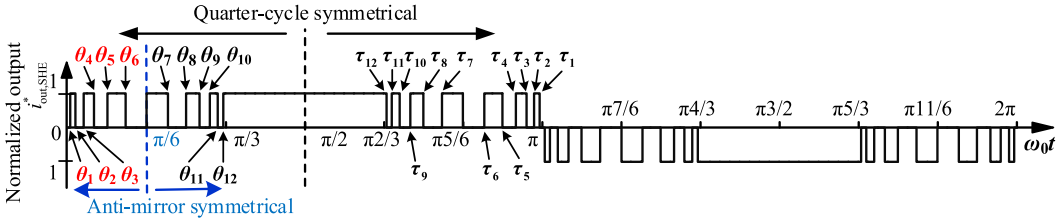

Fig. 2. Normalized output current waveform using the traditional SHE modulation (13-pulse).

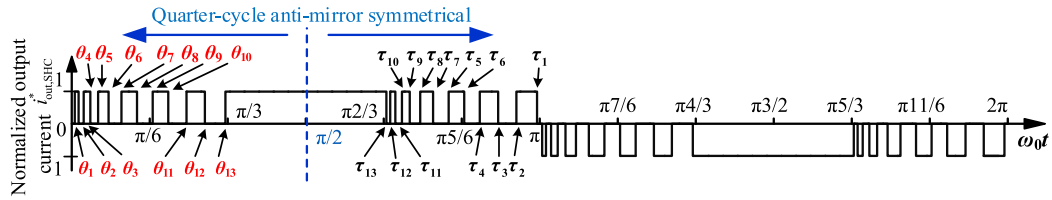

Fig. 3. Normalized output current waveform using SHC modulation (13-pulse).

means the phase angles of harmonic components cannot be controlled by using the conventional SHE. To extend the flexibility of the CSC, the constraints of the SHE were reconsidered in [13] and a new unsymmetrical SHE approach, also be named as SHC, was developed. In this modulation category, the PWM pattern is quarter-cycle antimirror symmetrical as shown in Fig. 3. In this case, $\theta_1 \sim \theta_{13}$ are all free angles and the dependent angles $\tau_1 \sim \tau_{13}$ are simply determined as

$$\tau_i = \frac{2\pi}{3} + \theta_i, i = 1, 2, \ldots, 13. \tag{4}$$

When the SHC PWM pattern is implemented, the normalized output phase current $i^*_{\text{out,SHC}}$ can be descripted in a similar manner as

$$i^*_{\text{out,SHC}}(\omega_0 t) = f_{\text{SHC}}(\omega_0 t, \theta_1, \theta_2, \ldots, \theta_{13}). \tag{5}$$

As $\theta_1 \sim \theta_{13}$ are all free angles, it can be used to tune magnitude and phase angle of the output current harmonic components at a few selected harmonic frequencies. In the theory, for a 13-pulse PWM output current, it can be applied to freely tune harmonic components up to at six selected frequencies. However, this needs a 12-D lookup table to store the switching angles, which is obviously not applicable for real-time digital applications. Alternatively, considering the attenuation of the fifth line current is the most needed as the output *CL* filter natural resonance frequency is often close to the fifth harmonic frequency, a 2-D lookup table is adopted to control the output current fifth harmonic component magnitude and phase angle.

B. Bypass Pulse Injection Approach

It is worth mentioning that the regulation of a single frequency fifth harmonic component of the output current using SHC is not sufficient to guarantee a good mitigation of line current ripples. In fact, a grid-tied CSC often has the nontrivial seventh harmonic line current that also needs to be properly suppressed. To deal with this challenge, a bypass pulse injection in the output PWM current is proposed. The principle of the bypass pulse injection

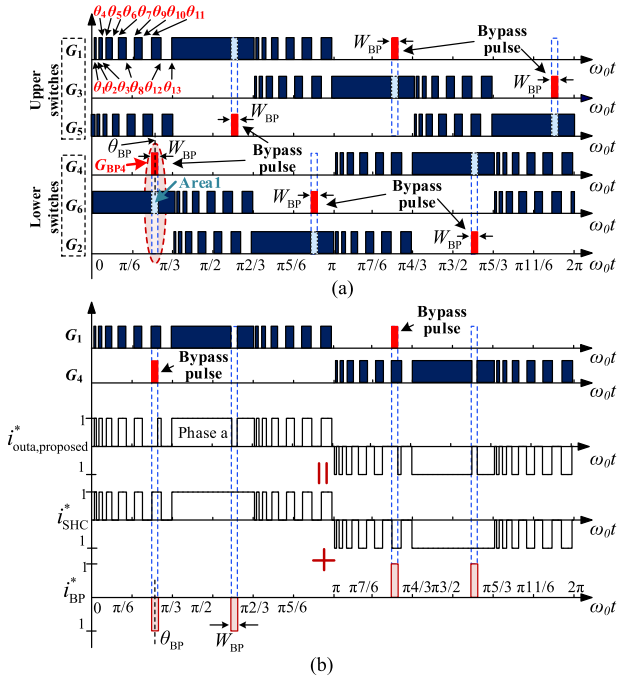

Fig. 4. Gating signals and output current waveform with the combination of bypass pulse injection and SHC. (a) Gating signals of CSC. (b) Normalized output current waveform (Phase-*a*).

is shown in Fig. 4, where it is seen that the gating signal of each switch has an additional narrow bypass signal (red bar). According to the switching constraint of the CSC, implementing additional bypass gating signal for a switch means the switches of other phases in the same category (either upper switches or lower switches) shall be turned OFF during the period of this bypass signal injection. For instance, a bypass signal G_{BP4} is implemented in the gating signal G_4 and the width and center location angle of the bypass signal are expressed as W_{BP} and θ_{BP}, respectively. In this case, the gating signal of G_6 must be turned

OFF during this short period as demonstrated by the blue region (Area1). Note that there is $\pi/3$ phase displacement between adjacent bypass gating signals. Accordingly, once the bypass width $W_{\rm BP}$ and location $\theta_{\rm BP}$ of $G_{\rm BP4}$ in G_4 are determined, the bypass pulses of other gating signals are also obtained.

According to the modified gating signals with bypass pulses, the output current waveform of a CSC can be easily determined. For instance, assuming that the dc rail current is fixed for analysis, normalized phase-a output current $i^*_{{\rm out}a,{\rm proposed}}$ using the proposed modulation is solely determined by the gating signals of G_1 and G_4, as shown in Fig. 4(b). It can be clearly seen that $i^*_{{\rm out}a,{\rm proposed}}$ is composed of an SHC-based output current $i^*_{\rm SHC}$ and a bypass pulse current $i^*_{\rm BP}$ as

$$\begin{aligned} i^*_{{\rm out}a,{\rm proposed}}(\omega_0 t) &= i^*_{\rm SHC}(\omega_0 t) + i^*_{\rm BP}(\omega_0 t) \\ &= f_{\rm SHC}(\omega_0 t, \theta_1, \ldots, \theta_{13}) \\ &\quad + f_{\rm BP}(\omega_0 t, W_{\rm BP}, \theta_{\rm BP}) \end{aligned} \tag{6}$$

where $f_{\rm BP}$ is the bypass current response function, which is determined by the pulsewidth $W_{\rm BP}$ and location $\theta_{\rm BP}$, as shown in the following.

The harmonic spectrum of $i^*_{\rm BP}$ can be obtained by the Fourier analysis as

$$\begin{aligned} i^*_{\rm BP}(\omega_0 t) &= \sum_{h=1}^{\infty} \hat{I}^*_{{\rm BP},h} \\ &= \sum_{h=1}^{\infty} [A^*_{{\rm BP},h} \sin(h\omega_0 t + \varphi^*_{{\rm BP},h})] \end{aligned} \tag{7}$$

where $\hat{I}^*_{{\rm BP},h}$ is the hth harmonic component of $i^*_{\rm BP}$. The magnitude $A^*_{{\rm BP},h}$ and phase angle $\varphi^*_{{\rm BP},h}$ of $\hat{I}^*_{{\rm BP},h}$ are given as

$$A^*_{{\rm BP},h} = \sqrt{{a_h}^2 + {b_h}^2} \tag{8}$$

$$\varphi^*_{{\rm BP},h} = \tan^{-1}(b_h/a_h) \tag{9}$$

$$\begin{cases} a_h = \frac{1}{\pi}\int_0^{2\pi} [i^*_{\rm BP}(\omega_0 t, W_{\rm BP}, \theta_{\rm BP}) \sin(h\omega_0 t)] d(\omega_0 t) \\ b_h = \frac{1}{\pi}\int_0^{2\pi} [i^*_{\rm BP}(\omega_0 t, W_{\rm BP}, \theta_{\rm BP}) \cos(h\omega_0 t)] d(\omega_0 t). \end{cases} \tag{10}$$

For the bypass pulse current $i^*_{\rm BP}$ as shown in the bottom of Fig. 4(b), the detailed expression of the coefficients $A^*_{{\rm BP},h}$ and $\varphi^*_{{\rm BP},h}$ are given as

$$A^*_{{\rm BP},h} = \frac{4\sqrt{6}}{h\pi} \sin(hW_{\rm BP}) \tag{11}$$

$$\varphi^*_{{\rm BP},h} = \begin{cases} -h(\theta_{\rm BP} - \frac{\pi}{3}), & (h-1)/2 \text{ is odd} \\ -h(\theta_{\rm BP} - \frac{\pi}{3}) + \pi, & (h-1)/2 \text{ is even.} \end{cases} \tag{12}$$

As seen in (11) and (12), both the fifth harmonic component $\hat{I}^*_{{\rm BP},5}$ and the seventh harmonic component $\hat{I}^*_{{\rm BP},7}$ are produced when bypass pulses are injected. Fig. 5 further shows the magnitudes $A^*_{{\rm BP},5}$and $A^*_{{\rm BP},7}$ and phase angles $\varphi^*_{{\rm BP},5}$ and $\varphi^*_{{\rm BP},7}$ response of $\hat{I}^*_{{\rm BP},5}$ and $\hat{I}^*_{{\rm BP},7}$ with varying bypass pulse location $\theta_{\rm BP}$ and width $W_{\rm BP}$. It can be seen that both $A^*_{{\rm BP},5}$ and $A^*_{{\rm BP},7}$ increase with higher bypass pulsewidth $W_{\rm BP}$. In addition, $\varphi^*_{{\rm BP},5}$ and $\varphi^*_{{\rm BP},7}$ change at fifth and seventh times of the bypass pulse location $\theta_{\rm BP}$, respectively. Note that the bypass pulse location $\theta_{\rm BP}$ is in between 0 and $\pi/3$, which is demonstrated as the restricted area in Fig. 5(b). For bypass pulses out of this area, it may have overlapping with other mandatory output current pulses.

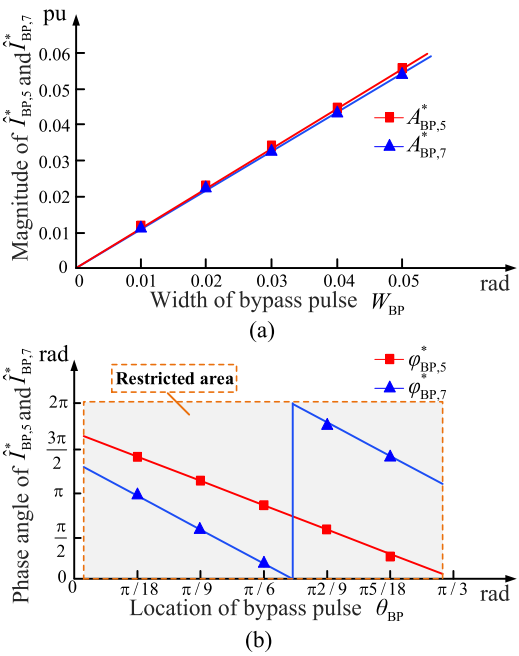

Fig. 5. Normalized magnitude and phase angle response of $\hat{I}^*_{{\rm BP},5}$ and $\hat{I}^*_{{\rm BP},7}$ with varying bypass pulse location $\theta_{\rm BP}$ and width $W_{\rm BP}$. (a) Magnitude response. (b) Phase angle response.

It can be further seen that when the bypass pulse location angle $\theta_{\rm BP}$ is with the restricted area in Fig. 5, it is sufficient to produce a seventh harmonic current component $\hat{I}^*_{{\rm BP},7}$ with an arbitrary phase angle. Accordingly, in this article, the bypass pulse injection approach is adopted to carry out the seventh-order harmonic control task.

The reason of defining the restricted area of the bypass pulse location is further demonstrated in Fig. 6. As the width of the bypass pulse is narrow, a seven-pulse SHC PWM pattern is selected to clearly demonstrate the performance of the system.

Fig. 6(a) shows the gating signals and output current waveform (phase a), while the bypass pulse location $\theta_{\rm BP}$ is 35°, where $G_{\rm BP4}$ is the bypass pulse signal of G_4. It is seen that due to the involvement of $G_{\rm BP4}$, the gating signal of G_6 must be changed, and the blue region of G_6 (Area 1) means the device must be turned OFF during the dwell time of the bypass pulse $G_{\rm BP4}$. According to a fact that the sequence gating signals of devices has $\pi/3$ displacement, the bypass pulse current can be obtained as shown in the bottom of Fig. 6(a).

On the other hand, when the bypass pulse location $\theta_{\rm BP}$ is 75°, the corresponding system performance is shown in Fig. 6(b). As illustrated, the adding of $G_{\rm BP4}$ in device gating signal G_4 causes the deduction of gating dwell time in both G_6 and G_2 (Area 1 and Area 2). According to the sequence displacement relationship between devices, the bypass pulse current of the phase-a is shown in the bottom of Fig. 6(b). Comparing to the

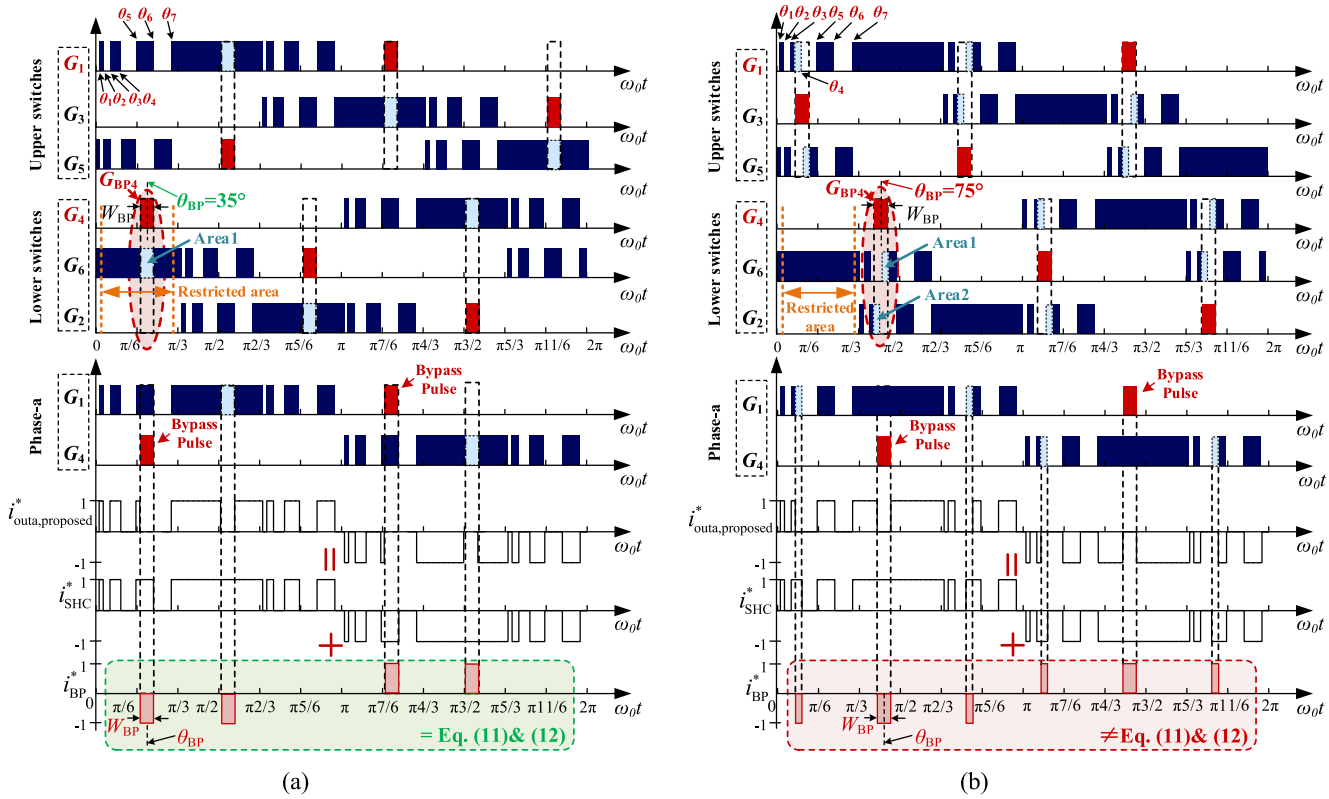

Fig. 6. Gating signals and output current waveform under the proposed approach with different bypass pulse location. (a) Within the restricted area. (b) Out of the restricted area.

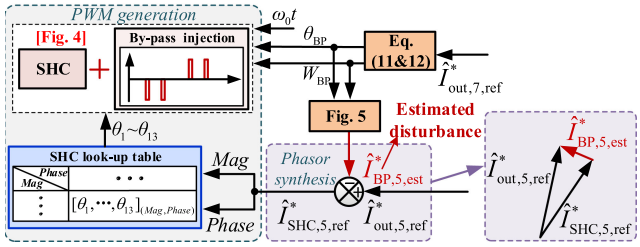

Fig. 7. Diagram of fifth and seventh harmonic output current control.

counterpart in Fig. 6(a), it is seen that the bypass pulse current has six pulses in a fundamental cycle in this case and it is obvious that the magnitude and phase angle adjustment feature in (11) and (12) cannot be maintained.

Nevertheless, when the seventh harmonic output current is controlled using bypass pulse injection, fifth output current $\hat{I}^*_{\mathrm{BP},5}$ is inevitably induced, as given in (7). Thanks to the flexibility of SHC modulation, the additional fifth harmonic component $\hat{I}^*_{\mathrm{BP},5}$ from bypass pulse injection can be easily compensated by properly selecting switching angles θ_1–θ_{13} of SHC. The proposed decoupled modulation is further demonstrated in Fig. 7. As seen, the bypass pulse location θ_{BP} and width W_{BP} are solely determined by the seventh harmonic output current reference according to (11) and (12) when $h = 7$. Meanwhile, the fifth reference current of the SHC is obtained by the fifth reference output current $\hat{I}^*_{\mathrm{out},5,\mathrm{ref}}$ and the estimated disturbance $\hat{I}^*_{\mathrm{BP},5,\mathrm{est}}$ as

$$\hat{I}^*_{\mathrm{SHC},5,\mathrm{ref}} = \hat{I}^*_{\mathrm{out},5,\mathrm{ref}} - \hat{I}^*_{\mathrm{BP},5,\mathrm{est}} \tag{13}$$

where $\hat{I}^*_{\mathrm{out},5,\mathrm{ref}}$ is the fifth output current reference and $\hat{I}^*_{\mathrm{BP},5,\mathrm{est}}$ is the estimated fifth harmonic output current caused by bypass pulse injection, according to Fig. 5.

Finally, the bypass pulse location θ_{BP} and width W_{BP}, SHC output current reference $\hat{I}^*_{\mathrm{SHC},5,\mathrm{ref}}$, and the instantaneous output current angle $\omega_0 t$ are sent to a digital modulation to produce gating signals of the CSC.

III. Proposed Control Approach

When both the fifth and the seventh harmonic output currents are fully controlled by using the cooperative operation of the bypass pulse injection and the low switching frequency SHC modulation, it is feasible to actively mitigate the line current harmonics by the adjustment of corresponding output current harmonic components. The principle of the line current harmonic control is demonstrated by hth harmonic equivalent circuit of the system, as shown in Fig. 8, where the grid is modeled by an hth harmonic voltage source $\hat{V}_{g,h}$ and the CSC bridge output is modeled by a controlled current source as

$$\hat{I}_{\mathrm{out},h} = \hat{k}_h \cdot \hat{I}_{\mathrm{line},h} = K_h \angle \delta_h \cdot (G_{SDFT,h}(jh\omega_0) \cdot \mathrm{i}_{\mathrm{line}}) \tag{14}$$

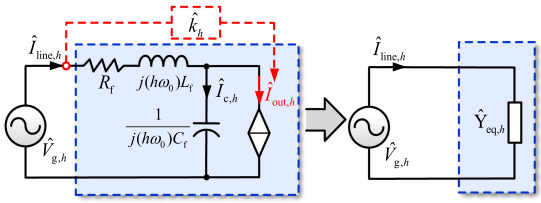

Fig. 8. Equivalent circuit of a grid-tied CSC with the proposed active line current harmonic control.

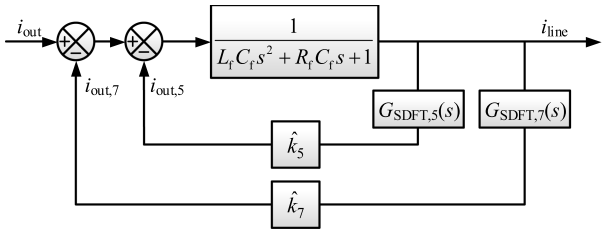

Fig. 9. Block diagram of a grid-tied CSC with the proposed active line current harmonic control.

where $\hat{k}_h$ is a complex number gain of the controlled current source, K_h and δ_h are the magnitude and the angle of the complex number, respectively, the *h*th line current harmonic component $\hat{I}_{\text{line},h}$ is extracted by a sliding discrete Fourier transform (SDFT), and $G_{\text{SDFT},h}(jh\omega_0)$ is the transfer function of the SDFT [18]. With this regulator in (14), the response of the line current to the grid harmonic voltage is easily determined as

$$\hat{I}_{\text{out},h} = \hat{\text{Y}}_{eq,h} \cdot \hat{\text{V}}_{g,h} \tag{15}$$

$$\hat{\text{Y}}_{\text{eq},h} = \frac{jh\omega_0 \text{C}_f}{(1-(h\omega_0)^2 \text{L}_f \text{C}_f) + jh\omega_0 \text{R}_f \text{C}_f - \text{K}_h \angle \delta_h \cdot \text{G}_{SDFT,h}(jh\omega_0)} \tag{16}$$

where $\hat{Y}_{\text{eq},h}$ is the equivalent admittance of the system and $G_{\text{SDFT},h}(jh\omega_0)$ in the denominator equals to $1\angle 0^0$ at the selected fifth and seventh harmonic frequencies.

A. Design of Active Line Current Harmonic Regulation

It is easy to know that the gain $\hat{k}_h$ in (14) should not be too high to avoid system instability. To maintain a good control of line current harmonics with proper stability margin, it is necessary to properly select the angles and magnitudes of gains at fifth and seventh harmonic frequencies. By setting a fixed term as $\rho = ((1-(h\omega_0)^2 L_f C_f)^2 + (h\omega_0 R_f C_f)^2)^{1/2}$, the magnitude of the admittance can be re-expressed as

$$|\hat{\text{Y}}_{\text{eq},h}| = \frac{h\omega_0 \text{C}_f}{\sqrt{\text{K}_h{}^2 + \rho^2 - 2\text{K}_h \rho \sin\left(\delta_h + \tan^{-1}\left(\frac{1-(\text{h}\omega_0)^2 \text{L}_f \text{C}_f}{\text{h}\omega_0 \text{R}_f \text{C}_f}\right)\right)}}. \tag{17}$$

For a gain $\hat{k}_h$ with fixed magnitude K_h, it is easy to obtain that the admittance achieves the minimal value at the *h*th harmonic frequency as

$$|\hat{\text{Y}}_{\text{eq},h}|_{\min} = \frac{\text{h}\omega_0 \text{C}_f}{\sqrt{\text{K}_h{}^2 + \rho^2 + 2\text{K}_h \rho}} \tag{18}$$

when the angle of the gain $\hat{k}_h$ is

$$\delta_{h,\text{optimal}} = \frac{3\pi}{2} - \tan^{-1}\left(\frac{1-(h\omega_0)^2 \text{L}_f \text{C}_f}{h\omega_0 \text{R}_f \text{C}_f}\right). \tag{19}$$

With the fixed angle $\delta_{h,\text{optimal}}$, the design of magnitude K_h is further demonstrated by root locus analysis as shown in the following.

For harmonic performance analysis, a simplified block diagram [12] can be adopted, as shown in Fig. 9, where SDFT is roughly modeled to a resonant controller series with delay as

$$G_{\text{SDFT},h}(s) = \frac{1}{\tau_0 s + 1} \cdot \frac{2\omega_c'' s}{s^2 + 2\omega_c'' s + (h\omega_0)^2} \tag{20}$$

where *h* is the harmonic order, ω_c is the cutoff frequency of the equivalent resonant controller, and τ_0 is the time constant of the delay. According to Fig. 9, the closed-loop transfer function of the system at harmonics can be given as

$$G_{\text{har}}(s) = \frac{\frac{1}{L_f C_f s^2 + R_{L_f} C_f s + 1}}{1 - \sum_{h=5,7} G_{\text{SDFT},h}(s) \cdot \frac{1}{L_f C_f s^2 + R_{\text{Lf}} C_f s + 1} \cdot \hat{k}_h}. \tag{21}$$

With the system parameters as shown in Table II, the fifth and seventh harmonic control performances of the CSC system are shown in Fig. 10. First, Fig. 10(a) shows the fifth harmonic performance of the system when the coefficient angle δ_5 is fixed at $\delta_{5,\text{optimal}}$, while the magnitude K_5 increase from 0 to 3. It can be seen that when K_5 increases, the poles P_3 and P_4 move away from the imaginary axis, while the poles P_1 and P_2 are pushed to close the imaginary axis. To get proper tradeoff between stability margin and damping performance, K_5 is selected as 1.0. Similarly, K_7 is also selected at 1.0.

In addition to the stability analysis of the system, the harmonic mitigation performance is examined. In this part, the magnitude response of the line current harmonic to grid voltage harmonic component ($|\hat{Y}_{\text{eq},h}|$) is shown in Fig. 11, where the angles δ_5 and δ_7 are determined by (19) as $\delta_{5,\text{optimal}}$ and $\delta_{7,\text{optimal}}$, respectively. It can be seen that when the magnitude of the gains K_5 and K_7 are both zero, $|\hat{Y}_{\text{eq},h}|$ has 5.48 and 3.25 dB response at the fifth and the seventh harmonic frequencies, respectively. Furthermore, when the gains K_5 and K_7 are both set to 1.0, it can be seen that the magnitude response $|\hat{Y}_{\text{eq},h}|$ is reduced to only –7.84 and –6.21 dB. As mentioned earlier, high gain K_h is often associated with wide bypass injection that may affect the dc rail current regulation. Accordingly, in this article, the magnitudes of the control gain K_h are set to 1.0 for both fifth and seventh harmonic line current control.

In addition, in the case of $K_5 = K_7 = 1.0$, the magnitude response of admittance $|\hat{Y}_{\text{eq},h}|$ considering the variations of the gain angle δ_h are shown in Fig. 11(b), where the variable $\Delta\delta_h$ means the deviation of the angle δ_h with respect to the

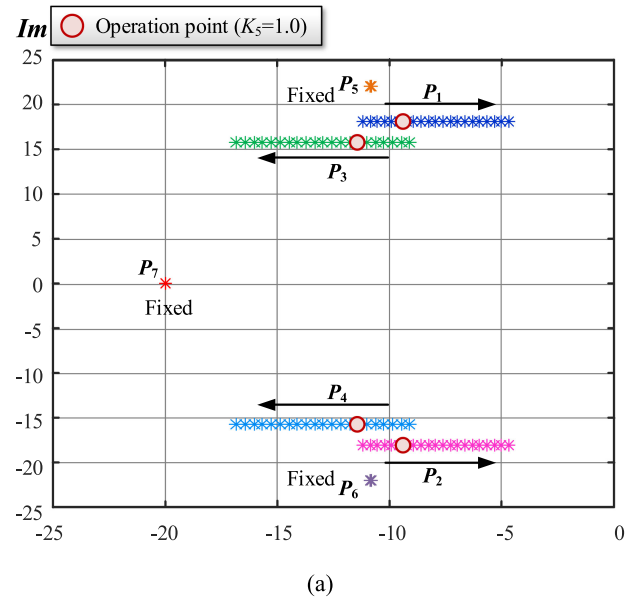

Fig. 10. Root locus of the system with different harmonic control gain. (a) Root locus diagram of the system when $K5$ changes from 0 to 3, while δ_5 is fixed at $\delta_{5,\ \mathrm{optimal}}$. (b) Root locus diagram of the system when K_7 changes from 0 to 3, while δ_7 is fixed at $\delta_{7,\mathrm{optimal}}$.

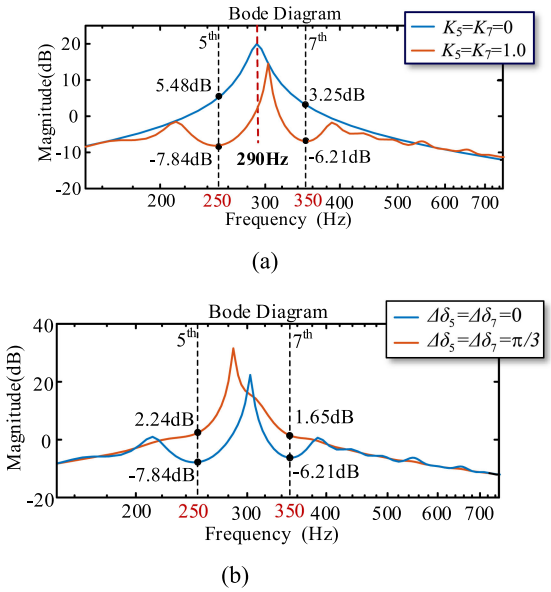

Fig. 11. Magnitude responses of admittance $|\hat{Y}_{\mathrm{eq},h}|$. (a) Magnitude responses of admittance $|\hat{Y}_{\mathrm{eq},h}|$ with different gain magnitudes $K5$ and $K7$ when $\delta\ 5 = \delta 5$, optimal, $\delta\ 7 = \delta\ 7$, optimal. (b) Magnitude responses of admittance $|\hat{Y}_{\mathrm{eq},h}|$ with different gain angles $\delta\ 5$ and $\delta\ 7$ when $K5 = K7 = 1.0$.

optimal harmonic angle $\delta_{h,\mathrm{optimal}}$ in (19). Similarly, it is seen that when $\Delta\delta_5 = \Delta\delta_7 = 0$, the magnitude response is low at –7.84 dB at fifth harmonic frequency and –6.21 dB at the seventh harmonic frequency. However, when the angles drifts away from the optimal values in (19) with $\Delta\delta_5 = \Delta\delta_7 = \pi/3$, it is seen that the admittance magnitude increases to 2.24 and 1.65 dB at the fifth and the seventh harmonic frequencies, respectively.

B. Complete Control Algorithm: Based on the previous analysis, the complete control diagram of a grid-tied CSC system is obtained as given in Fig. 12. The system is mainly composed of three parts. First, the dc rail current is regulated by using a delay angle control approach [19]. In this controller, a phase-locked loop (PLL) is adopted to obtain the instantaneous phase angle of the grid voltage as θ_g. Meanwhile, the dc-link current I_{dc} is regulated by a simple PI regulator to get the delay angle θ_{delay} of the fundamental current reference with respect to the main grid voltage angle θ_g. Then, the reference current angle is obtained as $\theta_{\mathrm{ref}} = \theta_g + \theta_{\mathrm{delay}}$.

In addition, the line current quality enhancement is achieved in the following two steps.

First, the instantaneous fifth and seventh line harmonic current components are extracted by SDFT extractors as $\hat{I}_{\mathrm{line},5}$ and $\hat{I}_{\mathrm{line},7}$, respectively. The fifth and seventh line current harmonic components are multiplied by complex number gains $\hat{k}_5$ and $\hat{k}_7$, respectively, and then, they are normalized with respect to the dc rail current reference $I_{\mathrm{dc,ref}}$ to determine the normalized harmonic output current reference as $\hat{I}^*_{\mathrm{out},5,\mathrm{ref}}$ and $\hat{I}^*_{\mathrm{out},7,\mathrm{ref}}$.

Second, the bypass pulse dwell time W_{BP} and the center location θ_{BP} are obtained according to (11) and (12) to produce the desired seventh harmonic output current. The injection of the bypass pulse also causes additional disturbance to the fifth harmonic output current as $\hat{I}^*_{\mathrm{BP},5,\mathrm{est}}$, as shown in Fig. 5. In this case, the reference of the normalized fifth SHC output current $\hat{I}^*_{\mathrm{SHC},5,\mathrm{ref}}$ shall be determined by the fifth output reference current for line current harmonic compensation as $\hat{I}^*_{\mathrm{out},5,\mathrm{ref}}$ minus the estimated disturbance from bypass pulse injection as $\hat{I}^*_{\mathrm{BP},5,\mathrm{est}}$.

Finally, when the reference current angle θ_{ref}, the bypass pulsewidth W_{BP} and location θ_{BP}, and the switching angles θ_1– θ_{13} from the lookup table for the fifth harmonic line current mitigation are all collected, a digital modulator is adopted to produce the gating signals of the CSC.

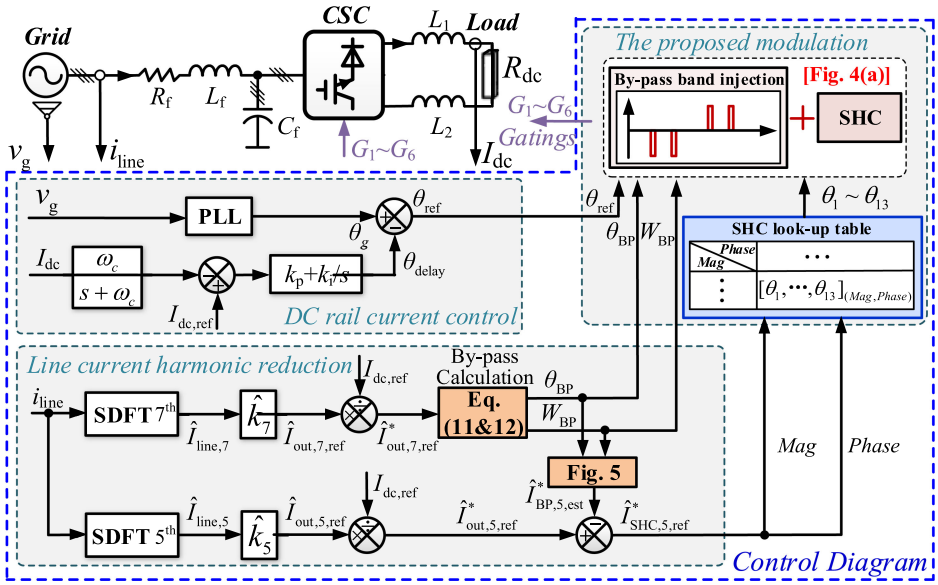

Fig. 12. Diagram of the proposed harmonic compensation method.

TABLE I
PARAMETERS OF THE SIMULATED SYSTEM

System Parameters	Values
Rated power	1 MW
Voltage(rms, line-to-line)	4160V/50Hz
Line inductance (L_f)	0.1p.u.
Capacitance (C_f)	0.43p.u.
DC link inductance (L_1 L_2)	0.36p.u.
DC load (R_{dc})	0.87p.u.
Control Parameters	**Values**
Switching Frequency	750Hz
$\hat{k}_5$	$1.0\angle 189.2°$
$\hat{k}_7$	$1.0\angle 4.2°$
k_p	0.01 rad/A
k_i	0.4 rad/(A·s)

IV. VALIDATIONS

A. Simulation Validation

In order to validate the proposed modulation and control strategy, a 1-MW medium-voltage grid-tied CSC system is simulated in the MATLAB/Simulink. The key parameters are given in Table I, which are selected according to the medium-voltage active front end of Power Flex 7000 from Rockwell Automation [23]. Note that the CSC at 1 MW under the conventional 13-pulse SHE modulation has the switching frequency at 650 Hz. However, due to the adoption of the proposed modulation approach with bypass pulse injection, the switching frequency of the system increases from 650 to 750 Hz. In this simulation, the grid voltage has 2% fifth and 2% seventh harmonic distortions and it also has 20% dips in the middle of the simulation process.

The validation under grid voltage sag is composed of three stages, as shown in Fig. 13. At stage 1, it is seen that the line current is sinusoidal with only 4.38% total harmonic distortion (THD) by the application of the proposed modulation approach, even when the grid voltage is distorted with fifth and seventh harmonics. At the beginning of stage 2 at 0.5 s, it is seen that the three-phase grid has a sudden voltage dip at 0.2 p.u. It is seen that the line current is obviously distorted at the beginning of the second stage. Nevertheless, the distortions rapidly decay and the line current quality is improved with 4.29% THD during the steady-state operation of the second stage. In addition, the grid voltage goes back to the nominal value at 0.7 s. As expected, the system line current also has distortions at the beginning of transition but it becomes sinusoidal again with only 4.42% THD when the system becomes stable.

The simulated gating signals as well as the output PWM current of phase-*a* under the proposed modulation strategy is further shown in Fig. 14. From the simulated results, the influence of the bypass pulse injection can be clearly seen, where G_{BP1} and G_{BP4} are the bypass pulse signal injected in gating signals G_1 and G_4, respectively. It can be seen that due to the involvement of very narrow bypass pulses, the line current THD can be maintained within 5% under the case of grid voltage distortion.

B. Experimental Validation

To further validate the correctness of the proposed approach, experiments have been carried out in a laboratory test rig, as shown in Fig. 15, where the grid is emulated by a three-phase programmable ac source and a CSC is regulated by a DSP+FPGA-based controller. The key circuit and control parameters can be seen from Table II. In this test, the 13-pulse SHC is selected.

1) Steady-State Performance: First, the steady-state performance of the system under the situation of the distorted grid voltage is investigated. Fig. 16(a) shows the line current and

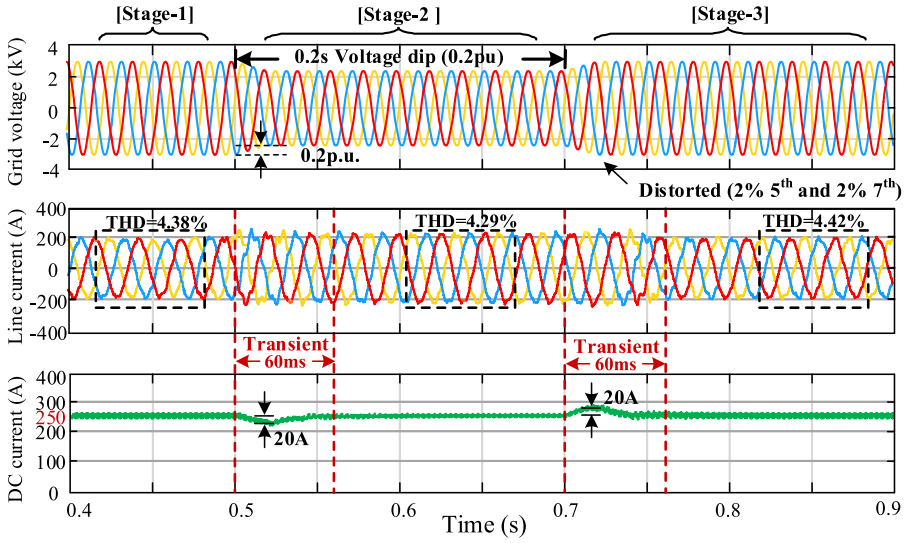

Fig. 13. Medium-voltage CSC transient performance during grid voltage dips and the exist of harmonics.

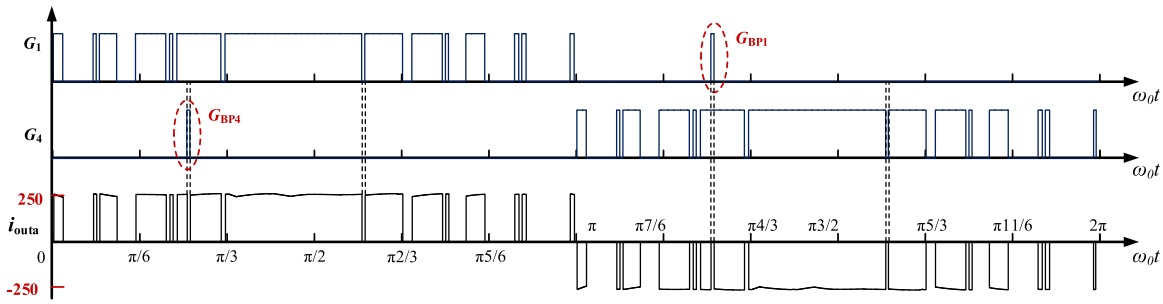

Fig. 14. Gating signals and output PWM current (phase-a) of stage 1.

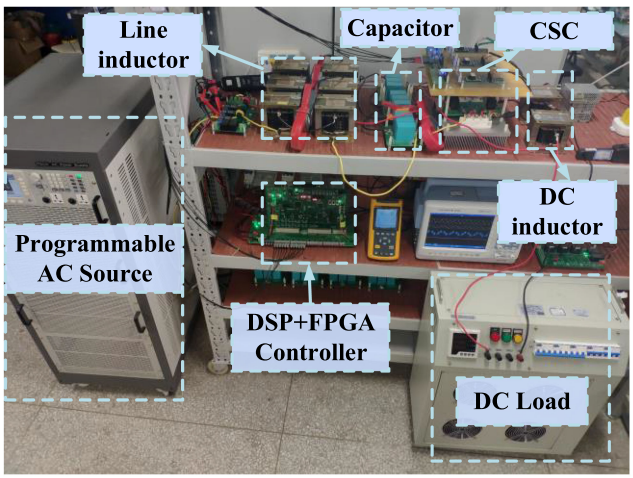

Fig. 15. Experimental CSC prototype.

TABLE II
PARAMETERS OF THE EXPERIMENTAL SYSTEM

System Parameters	Values
Voltage(rms, line-to-line)	100V/50Hz
Rated power	1kW
Line inductance (L_f)	0.1p.u.
Capacitance (C_f)	0.3p.u.
DC link inductance (L_1 L_2)	0.3p.u.
DC Load (R_{dc})	1.0p.u.
Control Parameters	**Values**
Switching Frequency	750Hz
$\hat{k}_5$	1.0∠191.3°
$\hat{k}_7$	1.0∠3.5°
k_p	0.9 rad/A
k_i	1.5 rad/(A·s)

output current performance of the CSC, when the grid voltage is slightly distorted with 2.5% fifth and 2.5% seventh harmonic components. The phase angles of fifth and seventh harmonic voltages are set to $\varphi_{Vg5} = \pi/2$ and $\varphi_{Vg7} = 3\pi/4$, respectively. It can be clearly seen that when the conventional SHE approach is used, the line current is highly distorted with 16.9% THD. On the other hand, it can be seen that by using the proposed approach, the output current waveform involves additional bypass pulses to reject the line current distortion. Accordingly, line current harmonic components are mitigated and the THD is reduced to only 3.8%.

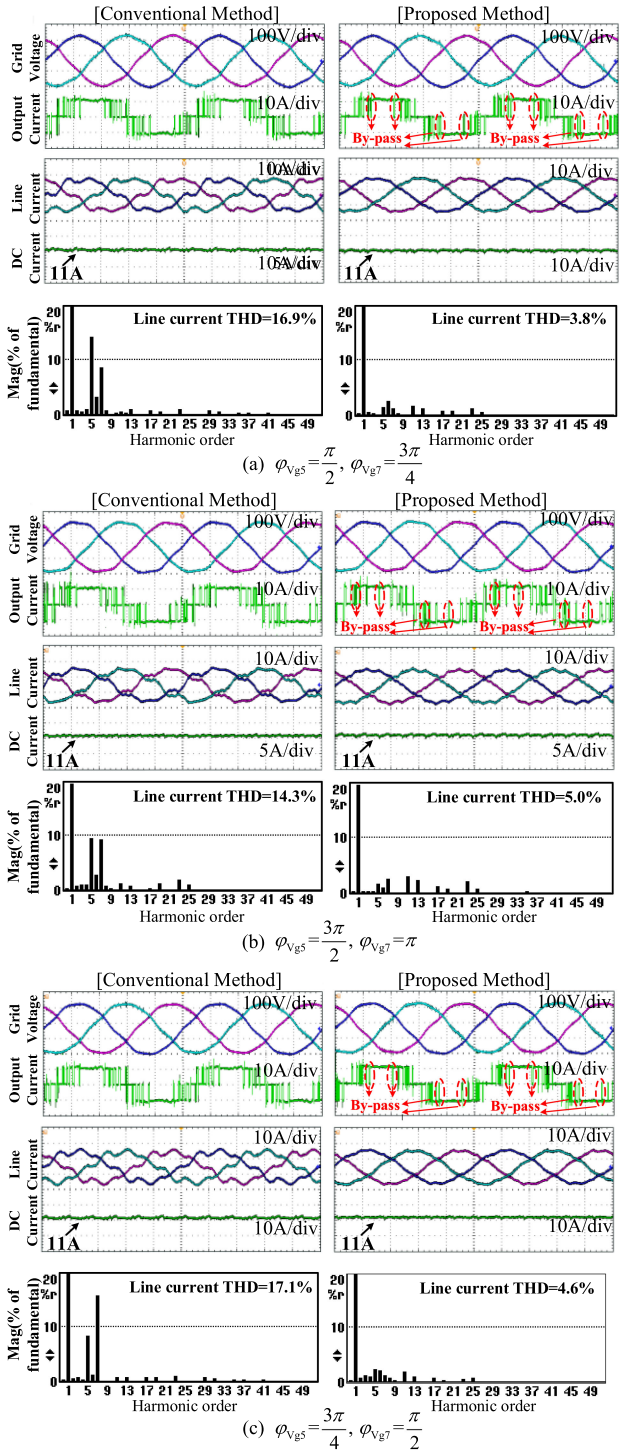

Fig. 16. CSC steady-state performance using the traditional SHE and the proposed method under the case of distorted grid voltage.

In addition, the performances of the system with different grid voltage harmonic component phase angles are shown in Fig. 16 (b) and (c). It can be noticed that by using the conventional SHE, the line current distortion is obviously amplified and the corresponding THD is in between 14.3% and 17.1% depending on the phase angles φ_{Vg5} and φ_{Vg7} of grid voltage harmonic components. On the other hand, it is seen that by using the proposed active harmonic rejection method, narrow bypass pulses are injected into the output current. Accordingly, the line current quality is always significantly improved comparing to the counterparts using the conventional SHE modulation. The THD of the line current is no more than 5% with the improved modulation approach.

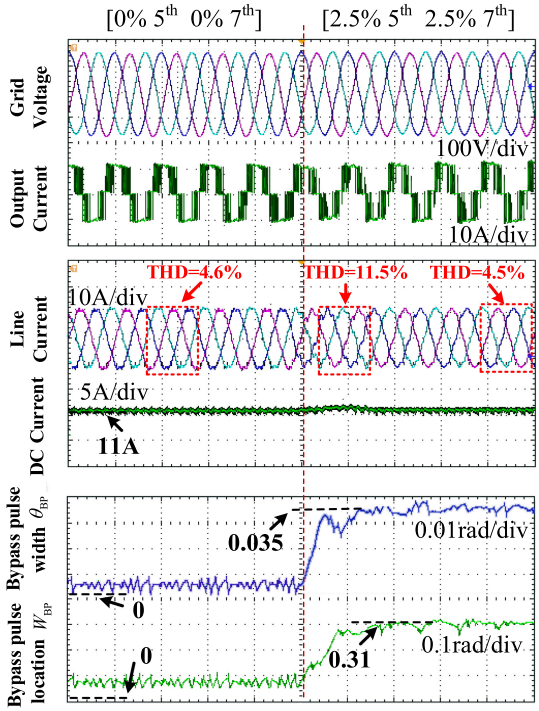

Fig. 17. CSC dynamic performance during the sudden increase of the grid harmonic voltage.

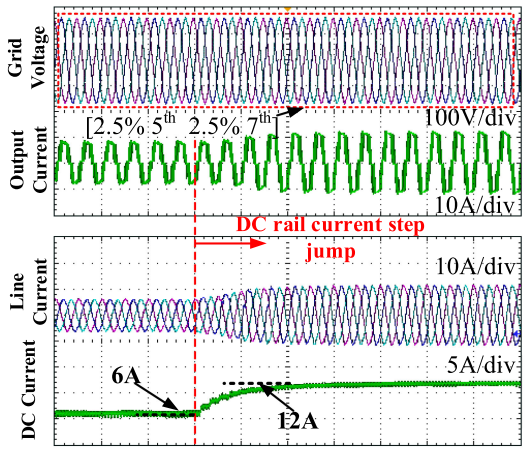

Fig. 18. CSC dynamic performance during dc rail current change.

2) Dynamic Performance: The dynamic performance of the system by using the proposed approach is also tested, as shown in Figs. 17 and 18.

Fig. 17 shows the performance of the system when the grid voltage changes from purely sinusoidal to with 2.5% fifth and 2.5% seventh harmonic contents. It is seen that when the grid voltage is ripple free, the line current of the CSC has a good quality with 4.6% THD. On the other hand, when the grid voltage

TABLE III
PERFORMANCE COMPARISONS OF THREE DIFFERENT MODULATION METHODS

Performance	Conventional 13-pulse SHE	13-pulse SHC	Proposed method
Output current harmonic control	×	√	√
Memory storage for simultaneously 5th and 7th harmonics control	×	4-dimensional look-up table (GB level)	2-dimensional look-up table (KB level)
Additional switching actions per cycle	None	None	4
Switching frequency	650Hz	650Hz	750Hz

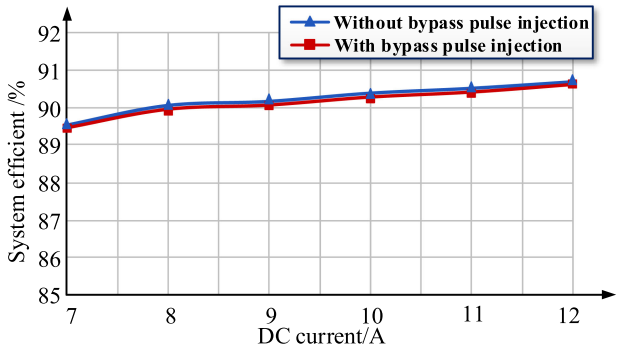

Fig. 19. Experimental system efficiency under different dc currents.

becomes distorted, the line current is slightly affected in the beginning of the transition. Nevertheless, due to the adjustment of the bypass pulse and the adoption of SHC, the line current ripples rapidly reduce and the steady-state line current returns to sinusoidal again with only 4.5% THD.

In addition, the bypass pulse location θ_{BP} and width W_{BP} in the entire process are shown in the bottom of Fig. 17, where it can be seen that W_{BP} and θ_{BP} is almost zero when the grid voltage is ripple free. On the other hand, when the grid voltage becomes distorted, the bypass pulsewidth W_{BP} changes to around 0.035 rad and the location angle θ_{BP} gradually stabilizes at around 0.31 rad, in order to compensate the line current harmonics that are excited by grid voltage distortions.

Finally, the performance of the system during the dynamic adjustment of the dc rail current from 6 to 12 A is shown in Fig. 18. In this case, the grid voltage is always distorted with 2.5% fifth and 2.5% seventh harmonic components. It is seen that the line current can always have good quality and there are no obvious oscillations in the entire dc rail current adjustment process.

3) System Efficiency: The loss performance of the grid-tied CSC is also experimentally tested. It should be noted that due to laboratory facility limitations, it is difficult for us to measure the detailed loss of each component of the system. Alternatively, we have used a power meter to obtain the total power loss of the system under different dc currents, as shown in Fig. 19. It is seen that the system efficiency is only slightly reduced when using the proposed approach.

This is mainly because the switching frequency of the proposed strategy increases from 650 to 750 Hz due to the bypass pulse injection, which brings roughly 15% additional switching loss according to the estimation approach in [20]–[22]. However, as the switching loss is relatively lower than the conduction loss in the CSC system, the efficiency reduction of the system is fairly minor.

V. CONCLUSION

In this article, a low switching frequency grid-tied CSC is actively controlled to maintain a good line current quality performance, even when the grid voltage has nontrivial distortions. In order to simultaneously regulate the most two dominated fifth and seventh line current harmonic components, the proposed method is composed of two types of compensators. First, a simple bypass pulse injection approach is developed to address the seventh harmonic line current via the dynamic tuning of the bypass pulsewidth and location. Meanwhile, an SHC-based modulation is adopted to further mitigate the fifth line current caused by both the grid voltage fifth harmonic component and the disturbance from the bypass pulse injection. With the aforementioned approaches, both the fifth and the seventh line current harmonics are mitigated with minimal couplings. Comprehensive experimental results have been provided to validate the effectiveness of the proposed approach.

Finally, the comparisons of three modulation approaches, namely SHE, SHC, and the proposed approach, are shown in Table III. It is seen that both the SHC and the proposed method have the capability to simultaneously control fifth and seventh output current harmonics. However, a 4-D lookup table is needed when using SHC, which will be a great challenge for the digital processor. When using the proposed approach, only a 2-D lookup table is needed due to the invention of the bypass pulse injection method.

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