A Review of SiC IGBT: Models, Fabrications, Characteristics, and Applications

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***Abstract*—Along with the increasing maturity for the material and process of the wide bandgap semiconductor silicon carbide (SiC), the insulated gate bipolar transistor (IGBT) representing the top level of power devices could be fabricated by SiC successfully. This article presents a thorough review of development of SiC IGBT in the past 30 years. The progresses of models, structure design, and performance in SiC IGBT are summarized. The challenges resulting from fabrication process and switching characteristics are discussed and analyzed in detail. The experimental results and existing problems in SiC IGBT-based applications are summarized in the end.**

***Index Terms*—Applications, characteristics, device models, insulated gate bipolar transistor (IGBT), review, silicon carbide, structure designs.**

I. Introduction

THE insulated gate bipolar transistor (IGBT) combining high input impedance of metal oxide semiconductor field-effect transistor (MOSFET) and high current density of bipolar devices shows great advantages in the medium-frequency high-power fields [1]. Si IGBT with high voltage and current is mainly targeted for use in traction systems, industrial applications, high voltage direct current transmission (HVDC), and emerging pulsed power application. In these fields, ultrahigh voltage is designed to reduce the number of devices in series and simplify the converter topologies [2]. The maximum voltage of Si IGBT has been reported to reach 8.4 kV [3], which is close to the limit of Si devices. Frequency and operating temperature greatly limit the further development of Si IGBT in these fields as well. As the wide bandgap material, SiC has higher breakdown field strength, higher intrinsic temperature, higher thermal conductivity, and higher carrier saturation drift velocity [4]. Therefore, SiC IGBT device shows stronger competitiveness in high voltage, high temperature, and high power fields, as shown in Table I. The excellent static and dynamic performances of SiC IGBTs make up for the shortcomings of SiC MOSFETs and SiC gate turn-OFF thyristors (GTOs). Among SiC polytypes and channel types, the SiC IGBT with 4H-polytype and n-channel is preferred due to the low forward voltage (V_f), fast switching, and wide safe operating area. The high bulk mobility and low current gain of wide-base pnp-transistor in 4H-SiC n-IGBT are helpful for a good tradeoff between V_f and switching loss ($E_{\rm sw}$). Although the bulk mobility of SiC IGBT is lower than that of Si IGBT, the V_f of SiC IGBT is lower than that of Si IGBT under the same blocking capability. It is worth noting that the problems in terms of SiC/SiO_2 interface properties, electromagnetic interference (EMI), and short-circuit withstand capability impede the utilization of SiC IGBTs.

Although the SiC IGBTs have not been commercialized so far, great progress has been made in the past 30 years, as shown in Fig. 1. From 1996 when the first SiC IGBT was fabricated [5], to 2010, the SiC p-channel IGBT has been studied extensively, because of the available n+ substrate with low resistivity and defect density. The performance of p-IGBT has been improved continually, especially after the introduction of carrier storage layer (CSL) [6]. The fabricated n-channel IGBT during this period exhibits very poor performance due to immature technology and p-type substrate with high resistivity and defect density [7]. Until the free-standing technology proposed by Cooper in 2010 [8], the research focus of SiC IGBT turned to SiC n-channel IGBT because the free-standing technology provides a method to grow p+ collector on n+ substrate. After that, SiC n-IGBT shows more and more excellent static and dynamic characteristics. The blocking voltage of SiC IGBT has also exceeded 27 kV [9], becoming the promising device in high voltage fields. The SiC IGBT could reduce the differential specific ON-resistances ($R_{\rm on,sp,diff}$) by more than one order of magnitude, compared with the SiC MOSFET of the same rated voltage. Therefore, it is encouraging for power conversion systems with transmission power greater than 100 kW, although the $E_{\rm sw}$ of SiC IGBT is higher than that of SiC MOSFET. Recently, the 12–15 kV SiC IGBT modules have been developed [10]–[12], based on which the prototypes of the first solid-state transformer and the first Marx generator have been built as well [13], [14].

The rest of this article is organized as follows. Section II summarizes the SiC IGBT models developed in different circuit simulators. In Section III, the critical factors limiting the commercialization of SiC IGBT are analyzed. In addition, new design concepts or technologies implemented in SiC IGBT structure are also summarized to enhance the performance of

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TABLE I
COMPARISONS OF PERFORMANCE BETWEEN HIGH VOLTAGE DEVICES

Device type	(1) Bulk mobility ($cm^2/V\cdot s$)	(2) V_f @35A/cm^2 (V)	(3) dv/dt (kV/μs)	Stored Charge	Gate oxide reliability	Channel mobility ($cm^2/V\cdot s$)	(4) SCWT	RBSOA /FBSOA
Si N-IGBT	1350 (P)	2*4.5 (2*8.4kV)	5	High	High	350-400	Long	Narrow
4H-SiC N-IGBT	940 (N)	5 (15kV)	300	Medium	Low	0.5-100	Short	Wide
4H-SiC P-IGBT	120 (Al)	5.5 (15kV)	/	Low	Medium			Medium
6H-SiC N-IGBT	410 (N)	/	/	Medium	Medium			Wide
6H-SiC P-IGBT	100 (Al)	7.5 (550V)	/	Low	High			Medium
4H-SiC NMOSFET	940 (N)	7.2 (15kV)	70	Near Zero	Low			/
4H-SiC N-GTO	940 (N)	<4 (15kV)	15	High	/	/		Widest

[1]P = Phosphorus, N = Nitrogen, Al = Aluminum.
[2]The voltage in "()" is rated blocking voltage of devices.
[3]The values of dv/dt is the maximum value in the reported research works.
[4]The SCWT is short-circuit withstand time.

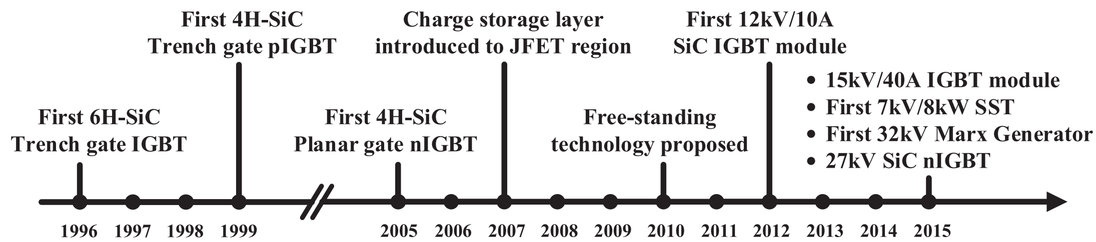


Fig. 1. Important milestones of SiC IGBT.

TABLE II
CHARACTERISTICS OF SiC IGBT MODELS

Papers	[1]	[17], [18], [19]	[20]	[21]	[22]	[23]
Year	2012	2013-2019	2013	2014	2015	2018
Device Type	15kV NPT p-channel	13kV FS p and n-channel	1.2kV n-channel	12kV & 20kV FS n-channel	15kV FS n-channel	>12kV FS n and p-channel
Simulator	Saber & Pspice	SPICE3F5	Simulink	Saber	Simulink	Saber, HSpice, Spectre
Achievement	First unified physical model	400 times faster than 2D numerical simulation	Integrated electro-thermal coupling model	Fully prediction of different temperature, voltage and current	Fully prediction of static, turn-on and turn-off behaviors	Unified physical model of FS type Si, SiC, n, P IGBT
Limitation	Limited to NPT structure	Lack of experimental results under punch-through	Neglect of transient behaviors	Low accuracy at low current	Partial expression fitted by functions	Approximation taken to simplify the model
Static accuracy	+++	++	+++	+	++	+++
Turn-on accuracy	/	++	/	/	++	/
Turn-off accuracy	+++	+++	/	++	+	+++

them. In Section IV, the $R_{\mathrm{on,sp,diff}}$ of high voltage power devices are compared. The unique switching characteristics are analyzed in detail according to the waveforms variations. In addition, the gate drivers customized according to characteristics of SiC IGBT are surveyed as well. Finally, several typical applications of SiC IGBT are illustrated in Section V. It is followed by the conclusion of the whole article.

II. SiC IGBT MODEL RESEARCH

SiC IGBT devices are at the stage of development, and cannot be commercialized on a large scale. The application of this high-voltage and high-temperature devices is faced with challenges of immature packaging (cooling, insulation, etc.), driver (EMI) and protection [overvoltage, overcurrent (OC), overheating (OT)]. Therefore, for the device manufacturers and circuit designers, the appropriate SiC IGBT model is helpful to understand its working principle, optimize the structure, and predict the performances.

In this article, all the SiC IGBT models developed in the circuit simulators are mathematical model [15]. Hefner IGBT model is the most classical mathematical model based on semiconductor physics. The model mainly includes equivalent circuits of MOSFET and ambipolar diffusion theory to explain bipolar transistor. It also includes the nonquasi-static effect and nonlinear capacitance effect to analyze the transient process accurately [16]. The SiC IGBT models in Table II follow Hefner Si IGBT model, but the SiC IGBT models still need further improvement to simulate its unique characteristics. The change of material

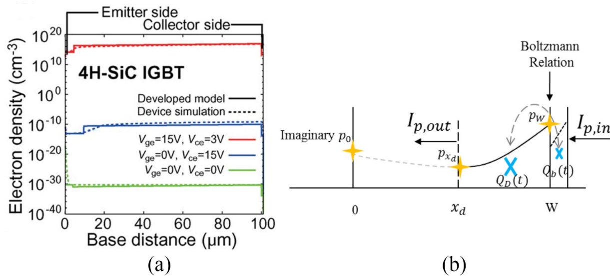


Fig. 2. Base region carrier distributions are modeled by (a) piecewise function [17] and (b) exponential function [22].

from Si to SiC makes the models more difficult to converge. Therefore, it needs to be simplified properly. In addition, the two-slope voltage transition during switching process needs to be taken into account in the models.

Table II summarizes all SiC IGBT models since 2012. As n-channel SiC IGBT gradually replaces p-channel, the simulation models also transfer from the original p-channel to n-channel. The physical model of non-punch-through (NPT) SiC IGBT is proposed for the first time in [1]. The static and dynamic behaviors of p-channel SiC IGBT and static behaviors of n-channel SiC IGBT are verified in Saber and Pspice. Because the developed model has no buffer layer and is essentially a Hefner model, the model cannot simulate SiC IGBT devices with buffer layer, which are widely used nowadays. However, the relatively simple NPT structure enables the model to simulate the static and turn-OFF behaviors accurately. The p-channel SiC IGBT model is also developed in [17] and is verified by numerical simulation results. The model does not use Hefner's base carrier distribution model based on the ambipolar diffusion equation, but uses a piecewise function to simulate the base carrier distribution, as shown in Fig. 2(a). This abrupt carrier distribution results in the simulation of the model in SPICE3F5 400 times faster than the numerical simulation [18]. However, it also causes three-slope voltage transition with moderate accuracy in the 2013 version. The model is further improved and verified under various temperature in 2019 version, when the interface traps model and temperature dependence model of intrinsic carrier density and carrier lifetime are incorporated [19].

The work in [20] simplifies the Hefner IGBT model greatly, which uses the drain current of the MOSFET (I_D) and the current gain of BJT (β) in (1) to obtain the collector current of IGBT (I_C). The main contribution of [20] is the electrothermal model of SiC IGBT, which was developed by the simplified electrical model and three-dimensional finite-element based thermal model. However, the electrothermal model ignores the heavy injection effect and voltage drop. Therefore, it can only simulate the static characteristics.

$$I_C(\beta + 1)I_D. \tag{1}$$

The work in [21] extends Hefner Si IGBT model with buffer layer to field-stop (FS) SiC IGBT. With the help of parameters extraction software tool, 20 physical and structural parameters are extracted from the static and dynamic waveforms. Furthermore, the model simulates the static curves of 12 and 20 kV SiC IGBT at different temperatures and the turn-OFF process at different temperatures, voltages, and currents. It is noteworthy that obvious deviations could be seen between the static curves of simulation and measurement, which may be due to deviations of static parameters fitting. In addition, when the SiC IGBT enters the punch-through state, the accuracy of the model decreases, especially in the case of low current. Therefore, the unique punch-through effect should be included in SiC IGBT models when extending the Si models to the SiC models.

Similar to [17], the work in [22] also simplifies the carrier distribution, as shown in Fig. 2(b). The model in [22] uses the exponential expression to describe carrier density distribution and linearization to describe temperature-dependent parameters. Therefore, some parameters (current, diffusion capacitance, threshold voltage, and the variation of transconductance with temperature) related to carrier density are approximate value, which results in the model accuracy depending on the fitting results. However, this model verifies static, turn-ON and turn-OFF behaviors under different temperature and gate resistance for the first time.

A unified IGBT model for Si/SiC, p/n-channel is developed in [23], which is based on [1] and Hefner model. The validity of the model is verified by Si n-channel IGBT and SiC n-channel and p-channel IGBT. Compared with [21], the static and turn-OFF process are more accurate, even if some simplifications are made. In dc–dc–ac circuit simulation, the run of several hundred milliseconds in Saber takes 0.0156 s, which indicates that the unified model is more suitable for system-level simulation.

These physics-based mathematical models, verifying the characteristics of SiC IGBT to some degree, become the useful tool for circuit designers. However, the verified models with high-accuracy static, turn-ON and turn-OFF characteristics are still not available. The complex parameters extraction process becomes one of the limitations of the implementation of the model in the circuit simulators, especially under different temperatures. In addition, the compatibility with commercial simulators is necessary to be further improved. Therefore, modeling SiC IGBT needs to compromise the simulation accuracy and simulation speed. Efficient SiC IGBT models, such as simplified physics-based models or high-accuracy behavioral models, are the main trends in predicting the electrothermal behaviors of circuits.

III. Challenges of SiC IGBT Fabrication

Although SiC IGBT has great theoretical advantages over other high voltage devices, the poor quality of wafer and immature fabrication technologies prevent SiC IGBT from commercialization. The main challenges for SiC IGBT are the fabrication of SiC n-IGBT, insufficient lifetime, poor SiC/SiO_2 interface properties and lack of high voltage, high temperature packaging. Therefore, these problems are analyzed in detail and some efforts for improving SiC IGBT performance, including optimized growth process and new designs of bulk structure, are also explained.

A. Fabrication of n-Channel SiC IGBT

As mentioned above, n-channel SiC IGBT has greater advantages as a high voltage switch and becomes the main research

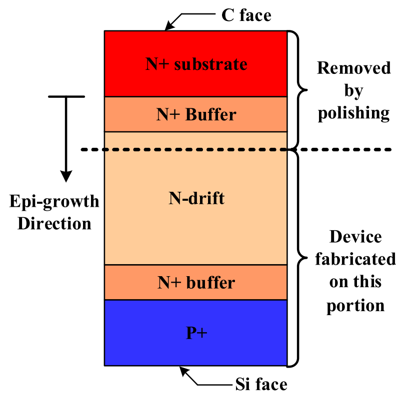


Fig. 3. Inverted-growth process of free-standing technology.

focus. Unfortunately, n-channel SiC IGBT needs high doping p-type collector as hole-injection layer. However, in commercial p-type substrate, quality is poor, and resistivity is high (~2.5 Ω·cm) [24]. The advantages of n-channel SiC IGBT are reduced. Therefore, free-standing technology was proposed by Wang and Cooper for the first time, as shown in Fig. 3 [8]. The n- and p+ epilayers growing on n-type substrate serves as the drift region and supporting substrate/collector of n-channel SiC IGBT. After that, there are several research works of n-channel SiC IGBT based on free-standing, and the test results of these devices vary. Similar to Cooper's results, n-channel SiC IGBT fabricated by Chowdhury shows poor conductance modulation [25]. It may be attributed to the low injection efficient due to the very thin and low doping concentration of p-type collector. Compared with the p-type collector formed by epitaxy, that formed by ion implantation has a native disadvantage in injection efficiency. Although Yonezawa *et al*. obtained n-channel SiC IGBT with low $R_{\mathrm{on,sp,diff}}$, their results showed that with the increase of device size, the $R_{\mathrm{on,sp,diff}}$ showed a degradation trend [26]. This phenomenon may be caused by the variation of carrier lifetime distribution.

The p-type epilayer, used as supporting substrate, needs to be thick enough and high enough in doping concentration to ensure mechanical strength and low series parasitic resistance. However, in thick p-type epilayer, the doping concentration is limited by the formation of thin ohmic contacts, growth rate, surface roughness, and in-grown defects [24], [27]. In addition, it is very difficult to remove the n-type substrate due to the hardness and chemical inertness of SiC. Complete separation of substrate, the carrier lifetime reduction and wafer bow, caused by removing substrate process, should be improved further as well [28], [29].

B. *Defects and Lifetime Enhancement*

The quality of SiC wafer directly determines the performance, reliability, stability, and yield of SiC IGBT device, and indirectly affects the cost of fabrication. Defects in SiC wafers mainly include intrinsic material defects, such as electronic traps $Z_{1/2}$ and $EH_{6/7}$, and structural defects caused by epitaxial growth, such as micropipe, dislocations (threading dislocations or basal plane dislocations), 3C inclusions, stacking fault (SF), etc. The micropipe density is usually used to grade SiC wafers. At present, the micropipe density of SiC wafer has been reduced to less than 3 cm^{-2}, and the lowest is 0.1 cm^{-2}, realizing "zero micropipe" [30], [31]. In addition, other defects are also reduced to a reasonable range by the optimized growth process and postgrowth treatment, which leads to the commercialization of low voltage 4H-SiC MOSFET devices [32]. However, for SiC IGBT, the above defects as the recombination center greatly reduce the carrier lifetime in thick drift region. It is known that high voltage SiC bipolar devices require a long lifetime to reduce the V_f drop. In addition, the carrier lifetime dominates the tradeoff between V_f and switching speed. Therefore, much longer lifetime is necessary to achieve the lifetime control of bipolar devices.

It is well known that the main lifetime-killers of carriers are $Z_{1/2}$ and $EH_{6/7}$ related to carbon vacancy. By C+ ion implantation/annealing, thermal oxidation/annealing, or optimization of growth conditions, the concentrations of these two kinds of defects could be reduced to a very low level, as low as 10^{11} cm^{-3} [33]. The corresponding lifetime can reach more than 10 μs, which is enough for high voltage devices (several kV). However, for the SiC IGBT with the voltage of more than 10 kV, it is not enough because of the extremely thick drift region. In the epilayers with low $Z_{1/2}$ concentration ($<10^{13}$ cm^{-3}), other defects and surface recombination begin to dominate carrier lifetime. These defects include in-grown SF (IGSF), dislocations, grain boundaries, carrot defect, half-loop array, morphological defect, etc. [34]–[37]. The IGSF with low formation energy is a quantum well structure and efficient recombination center, which dominates the carrier lifetime. Different types of IGSF could reduce lifetime from 40% to 95% [37].

Despite many efforts to reduce these defects, they still exist and greatly affect the carrier lifetime. In addition, the inhomogeneity of lifetime distribution, the tradeoffs between different defect density, the tradeoffs between target defects and new defects caused by post-growth, and the contradiction between epitaxial growth on C-face and Si-face, further hinder the commercialization of SiC IGBT [33], [36]. Supply of large size and high quality material and low defect density epitaxial growth processes are the key points to realize the commercialization of SiC IGBT.

C. *SiC/SiO$_2$ Interface Properties*

SiC IGBT shows superior performance, compared with Si IGBT. However, conventional material SiO_2 is still used as gate dielectric, which leads to new issues in the SiC/SiO_2 interface. Although the native silicon dioxide of SiC is readily formed in oxidizing ambient at high temperature like the Si IGBT, additional carbon (C) clusters will be generated in the oxidation process, besides the near-interface traps. The trap density of SiC/SiO_2 interface is one or two orders of magnitude of that of Si/SiO_2 interface due to the extra carbon clusters [38]. Such a high interface trap density (10^{13} cm^{-2}) leads to a large reduction in the channel mobility of SiC MOS structure, while channel mobility of Si MOS structure is only reduced by a factor 2 from its bulk mobility [39]. In addition, the high density of interface traps (D_{it}) causes the threshold voltage shift, the static

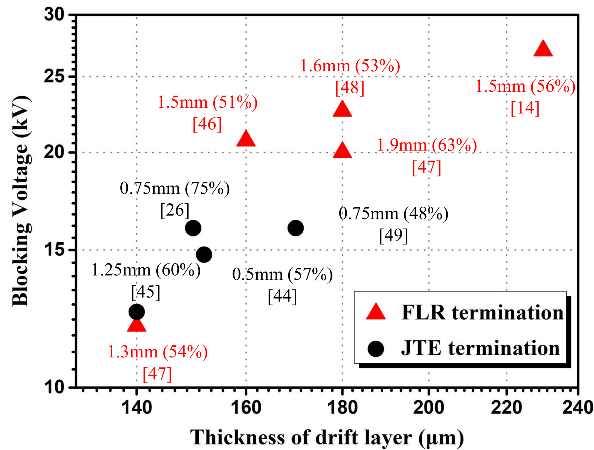


Fig. 4. Terminations used in various drift thickness SiC IGBT devices. The length of termination and termination area as a percentage of chip area are labeled.

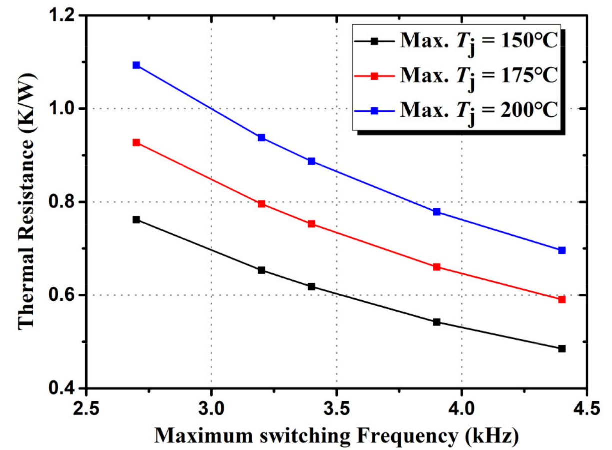


Fig. 5. Relationship between the maximum switching frequency and thermal resistance of 15 kV SiC IGBT module under different maximum rated T_j.

and dynamic current amplitude degradation, increase of the turn-off current tail and the increase of leakage current in the blocking state [40]. Introducing nitrogen is the most effective method to reduce the D_{it} in postoxidation annealing (POA). After POA, the channel mobility is around 50 cm^2/v·s. However, POA introduces defects in the oxides and causes reliability problems. To achieve a high quality interface like Si/SiO_2, it is necessary to remove the remaining C atoms and near-interface traps completely.

Another important problem is the high electric field of oxide layer. According to Gauss law, in 4H SiC IGBT, the electric field in SiO_2 is 2.5 times that in SiC. Compared with Si IGBT, higher critical electric field in SiC IGBT makes electric field in SiO_2 higher. In many research works, the dielectric with high dielectric constant (high-k) is used to replace the SiO_2 to reduce the electric field ratio between gate dielectric and SiC [41], [42]. However, the new dielectrics still have poor interface with high density of interface defect and larger leakage current due to the lower band offset in the new dielectric/SiC interface. Although the stack structure with SiO_2 and high-k could reduce the leakage current and improve the channel mobility to some degree, the compatibility with the existing mass manufacturing and the long-term robustness under high voltage operation are difficult to handle.

D. Termination Technologies

Reliable and robust edge terminations should be carefully designed to sustain the high voltage of SiC IGBT devices. Terminations allow device to support more than 90% of the bulk breakdown voltage [43]. To date, junction termination extension (JTE) and field limiting rings (FLRs) are two main termination technologies applied to SiC IGBT. Furthermore, terminations used in available SiC IGBT devices are summarized in Fig. 4 [26], [44]–[49]. In order to alleviate the crowded edge electric field effect, the termination length of SiC IGBT is much longer than that of the Si counterparts. Termination area accounts for more than 50% of the chip area, resulting in enlarged chip area and, therefore, a nonoptimal cost/area ratio.

Accurate control of the implantation doses and significant area consumption are necessary for JTE technology to achieve a uniform electric field. Therefore, JTE technology is mainly used in lower voltage devices, while FLR technology targets for high voltage devices. However, FLR technology used in high voltage devices consumes a large area as well. To solve this problem, FLRs technologies with linearly or regionally optimizing the distances and JTE rings technology combining JTE and FLR are proposed [43], [50], [51]. The former technology reduces the termination length by 30% and increases the breakdown voltage by 23%. The latter reduces the termination area by 20%–30% to achieve the same breakdown voltage.

E. Packaging Technologies

At present, the SiC IGBT is still packaged in the wire-bonding module [2], [10], [13], [52], in which the failure of bonding wires and solder failure are the common lifetime limiting factors. In addition, voltage breakdown and partial discharge caused by ultrahigh voltage bring a greater challenge to the insulating material. The intersection point of conductor, dielectric and encapsulation is the weak point exposed to high electric field, which may exceed the breakdown electric field strength of the materials. Therefore, the selection of high breakdown electric field materials, smooth electrodes and enough electrodes clearance need to be focused on. Even so, there are still a series of problems, such as the extra displacement current caused by the high dielectric constant of the insulating layer, the complexity of processing, and the increased module size.

To realize the insulation capability between the chip and the heatsink in SiC IGBT module, several millimeters of insulating layer is required when the Al_2O_3 or AlN ceramic is used. It is no doubt that a large thermal resistance and thermal capacity are introduced, which leads to a larger junction temperature (T_j) of SiC IGBT module, thus threatening the solder and bonding wires lifetime. In the SiC IGBT module, the thermal resistance of ceramics accounts for nearly one-third of the total thermal resistance [53]. Fig. 5 shows the relationship between the maximum switching frequency and thermal resistance of 15 kV SiC IGBT module under different maximum rated T_j. 175 °C is the

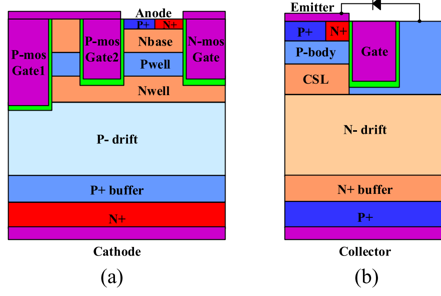


Fig. 6. Upper technologies. (a) Trench cluster IGBT (TC-IGBT). (b) Diode clamped shield IGBT (DCS-IGBT).

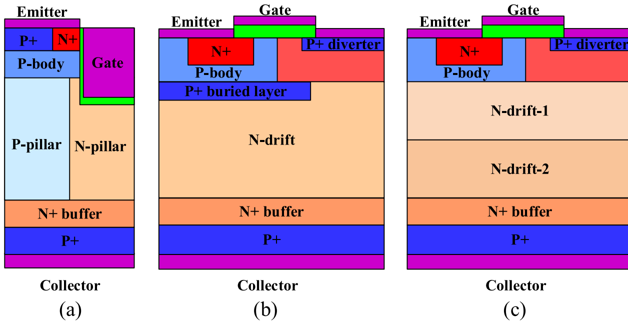


Fig. 7. Middle technologies. (a) Superjunction. (b) P+ buried layer. (c) Depletion-controlled (DC) structure.

highest T_j that the wire-bonding module could withstand. Due to the large thermal resistance of SiC IGBT module, only several kilohertz could guarantee the T_j below the maximum value. Therefore, it is important to improve the temperature withstand capability and reduce the thermal resistance of the module. New packaging technologies such as free bonding-wire connection, nano-silver sintering, and double-sided cooling may be the key technologies to solve the above problems related to SiC IGBT module.

F. New Structural Designs

Although SiC IGBT has several superior properties over Si IGBT in terms of blocking voltage, thermal conductivity, and switching speed, the conventional IGBT structure limits the properties of SiC material. Therefore, some new solutions of structure and parameter optimization are proposed to improve the electrical performances and reliability of SiC IGBT. New structures and parameters optimizations are summarized and divided into upper technologies, middle technologies, and lower technologies, as shown in Figs. 6–8. The advantages of new structures are also summarized in Tables III–V [8], [25], [26], [44], [54]–[63]. Most of these proposed technologies aim to achieve lower V_f and fast switching. How to reduce V_f of SiC IGBT is an important issue in the design of SiC IGBT devices, especially in low frequency and high power applications. Therefore, some structures and parameters are optimized to enhance the conductivity modulation, thus to achieve a lower V_f. As a result, carriers stored in drift increase and are difficult to be swept out during the turn-OFF process, which increases the tail

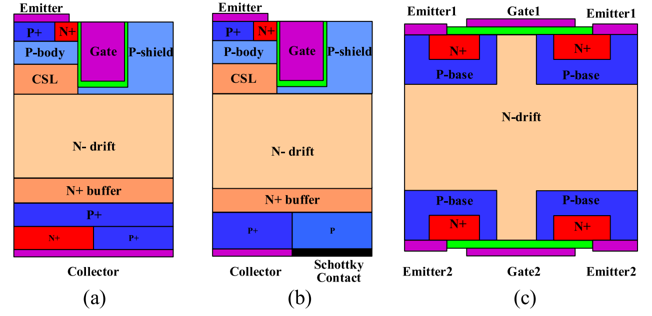


Fig. 8. Lower technologies. (a) Backside npn-collector (npn-IGBT). (b) Collector side schottky contact (SC-IGBT). (c) Bidirectional IGBT (BD-IGBT).

TABLE III
ADVANTAGES OF UPPER TECHNOLOGIES

Upper technologies	Advantages
Trench cluster IGBT (TC-IGBT) [54]	• Lower V_f • Lower E_{sw} • Lower saturation current
Diode clamped shield IGBT (DCS-IGBT) [55]	• Lower interface electric field • Faster switching • Lower current overshoot • Lower saturation current
JFET width optimization [8], [25], [26], [44]	• Lower V_f

TABLE IV
ADVANTAGES OF MIDDLE TECHNOLOGIES

Middle technologies	Advantages
Buffer layer thickness [58]	• Faster switching • Lower current bump • Lower current overshoot
P+ buried layer [59]	• Better tradeoff between V_f and saturation current • Better tradeoff between E_{on} and d*i*/dt
Carrier storage layer (CSL) [25]	• Lower V_f
Superjunction [60], [61]	• Better tradeoff between V_f and BV
Depletion-controlled (DC) structure [62]	• Suppression of d*v*/dt and EMI

TABLE V
ADVANTAGES OF LOWER TECHNOLOGIES

Lower technologies	Advantages
Backside npn-collector (npn-IGBT) [56]	• Better tradeoff between V_f and E_{off}
Collector side schottky contact (SC-IGBT) [57]	• Better tradeoff between V_f and E_{off}
Bi-directional IGBT (BD-IGBT) [63]	• Bi-directional conduction • Adjustable V_f and E_{sw} by gate signals

current and turn-OFF loss. Therefore, the tradeoffs between E_{off} and V_f ($TB_{Eoff,\,Vf}$) are used to evaluate the static and dynamic performances of new structures and parameters optimizations.

$TB_{Eoff,\,Vf}$ of high voltage Si IGBT, conventional SiC IGBT, and new structure SiC IGBT under several tunable parameters are compared and presented in Fig. 9. The n-channel, p-channel SiC IGBT, and Si IGBT are represented by blue, red, and green, respectively. The filled and open symbols are conventional and new structure in SiC IGBT. Collector side Schottky contact

Fig. 9. $TB_{E\mathrm{off},\,Vf}$ under tunable parameters for SiC IGBT devices. The tradeoff curve of DCS-IGBT is zoomed in in inset.

Fig. 10. $R_{\mathrm{on,sp,diff}}$ of Si and SiC devices reported in references.

(SC-IGBT), trench cluster IGBT (TC-IGBT), and diode clamped shield IGBT (DCS-IGBT) based on trench gate IGBT are compared with conventional SiC IGBT. First, $TB_{E\mathrm{off},\,Vf}$ of SiC IGBT are better than the 8 kV Si IGBT of the highest voltage level in the available Si IGBT, which shows the superiority of SiC IGBT in the high voltage fields [3]. Although the $TB_{E\mathrm{off},Vf}$ curves of three conventional trench gate SiC IGBT are different because of different structural parameters, all the new structures show better $TB_{E\mathrm{off},Vf}$ than conventional SiC IGBT. The $TB_{E\mathrm{off},\,Vf}$ curves marked in red representing p-channel SiC IGBT are much worse than those of n-channel SiC IGBT, but closer to Si IGBT. It further demonstrates the advantages of n-channel SiC IGBT in $TB_{E\mathrm{off},Vf}$.

Fundamentally, the enhanced conductivity modulation and fast carrier removal are necessary to optimize the $TB_{E\mathrm{off},\,Vf}$. In TC-IGBT structure, as shown in Fig. 6(a), the multilayers MOS and NPNP thyristor composite structure above drift region enhances the conductivity modulation during ON-state and help remove the excess carriers during turn-OFF [54]. As for DCS-IGBT and SC-IGBT (or npn-IGBT), fast switching is achieved due to the fast carriers removal by screening the capacitive coupling C_{GC} and formation of reverse electric field at the backside, respectively [55]–[57]. In addition, moderate tradeoff is achieved by adjusting the buffer thickness [10], as shown in Fig. 9. Therefore, the development of new structure is a promising way to further improve the static and dynamic performances of SiC IGBT devices.

IV. SiC IGBT Characteristics and Gate Drivers

The behaviors of SiC IGBT are quite different from those of Si IGBT because of its wide bandgap material and extremely high operating voltage. The SiC IGBT behaviors mainly include static and dynamic characteristics, which varies with the device structure, circuit parameters, and temperature.

A. Static Characteristics

The forward characteristics are important parts of the static characteristics, which could be described by $R_{\mathrm{on,sp,diff}}$. Therefore, $R_{\mathrm{on,sp,diff}}$ of SiC IGBT devices with different blocking voltage is summarized in Fig. 10. The $R_{\mathrm{on,sp,diff}}$ of SiC IGBT is lower than Si IGBT and SiC MOSFET in general, due to the fact of shorter drift region thickness or conductivity modulation. Although different device parameters cause the dispersion of $R_{\mathrm{on,sp,diff}}$, the lowest available $R_{\mathrm{on,sp,diff}}$ of SiC IGBT is much lower than SiC MOSFET limit [64]. In addition, p-channel devices show poorer forward characteristics than n-channel devices. Therefore, n-channel SiC IGBT is a promising device in high power fields [65].

The blocking capability characteristics related to termination technologies are described in Section III-D.

B. Dynamic Characteristics

SiC IGBT is mainly used to drive inductive loads. Double pulse test (DPT) is typically used to evaluate the switching characteristics of power devices. DPT circuit and switching waveforms of SiC IGBT are shown in Fig. 11. C_1 and C_2 are parasitic capacitance. According to the current waveform, the turn-OFF process is divided into five phases, and the turn-ON process is divided into three phases.

1) Turn-OFF Process: Phase I: Current drop at the beginning of turn-OFF. Ideally, the load current consists of collector current and diode current. Before the IGBT voltage rises to the dc bus voltage, the diode is cut off, and the load current is equal to the collector current. However, there are parasitic capacitors in diodes, load inductors, and SiC IGBT. The displacement current (i_{C1} and i_{C2}) generated at very high d*v*/d*t* flows through parasitic capacitors, which reduces the collector current [48], [66]. The displacement current is usually neglected in Si IGBT due to low d*v*/d*t*.

Phase II: Current bump process. The displacement current generated by high d*v*/d*t* on the diffusion capacitance provides the base drive current to internal pnp transistor. Therefore, the magnitude of current bump is determined by d*v*/d*t* and common-emitter current gain. With the increase of voltage, although capacitance and d*v*/d*t* decrease, the current gain of PNP transistor increases due to the reduced undepleted region, as shown in (2). These three factors determine the magnitude of

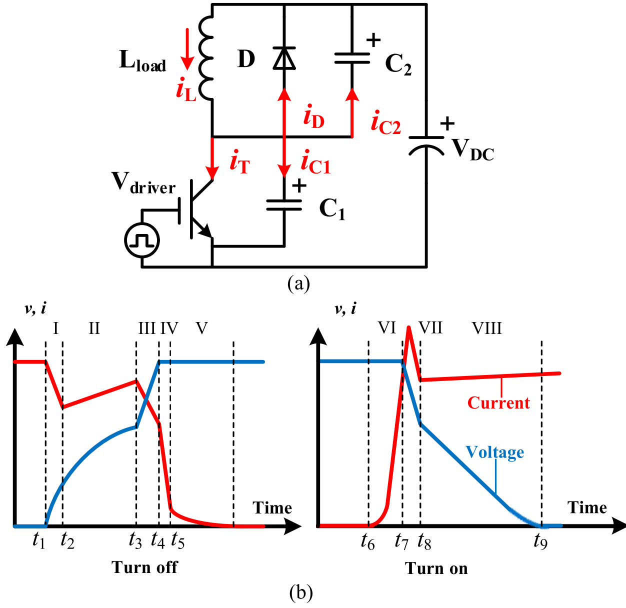


Fig. 11. (a) DPT equivalent circuit. (b) Typical switching waveforms of SiC IGBT during hard switching.

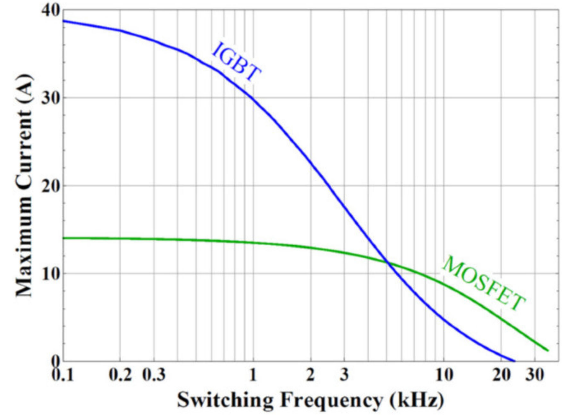


Fig. 12. Comparison of maximum controllable current for the 15 kV 4H-SiC MOSFETs and the 15 kV 4H-SiC n-IGBTs in a hard switching application [68].

current bump.

$$\beta = \frac{1}{\cosh(W_{\text{undepleted}}/L_a) - 1}. \quad (2)$$

Phases I and II are also known as sweep-out phases. In this process, the electric field generated by reverse biased PN junction of the depletion region clears the excess carriers, which exponentially distribute in the drift region. The charge to be swept out is determined by (3), where C is the diffusion capacitance [67].

$$C = \frac{\Delta Q}{\Delta V}. \quad (3)$$

Phase III: After punch-through. The charges are mainly cleared by the recombination of buffer layers [57]. Here, C in (3) becomes depletion capacitance with a small value [10], [46]. Therefore, the charges that need to be removed are few, which causes a rapid rise in voltage. And the current bump decreases due to the drastic decrease of C and the dramatic increase of dv/dt. In addition, the displacement current increases, so the collector current begins to decrease.

Phase IV: Diode turn-ON. Once the V_{CE} reaches to the bus voltage, the diode turns ON and the current transfers from SiC IGBT to the diode. Voltage overshoot is typically negligible due to lower current.

Phase V: Tail current. The recombination of minority carriers removes charge, while the stored charge is still very small.

2) Turn-ON Process: Phase VI: Current increase after gate voltage (V_{GE}) reaching threshold voltage (V_{TH}). The current increase is controlled by V_{GE}, once the channel is formed.

Phase VII: Reverse recovery of diode. After collector current reaches to load current, the extreme high dv/dt results in the high current overshoot.

Phase VIII: After punch-through. The low depletion capacitance becomes the high diffusion capacitance, which leads to slower dv/dt [10]. It is easy to produce oscillation after current overshoot because of parasitic inductance and parasitic capacitance of diode and load. In particular, a larger common-emitter parasitic inductance may aggravate the oscillation process [52].

In resistive–inductive load, the turn-ON process is basically the same as that of inductive load. However, in resistive load, zero current switching and great damping lead to the reduction of the current overshoot [53].

C. Competitions Between SiC IGBT and SiC MOSFET

The lower V_f and fast switching are always compromised by each other. Lower V_f and fast switching are preferred in low and high switching frequency fields, respectively. Since both on-state loss and E_{sw} increase with increasing current, the current capability is closely related to switching frequency, as shown in Fig. 12 [68]. The maximum current decreases with increasing switching frequency due to E_{sw} dominating the power dissipation under high switching frequency. SiC IGBT exhibits higher current capability over SiC MOSFET, when switching frequency is lower than 5 kHz. Even in high switching frequency, current capability of SiC MOSFET is slightly greater than SiC IGBT, which shows SiC IGBT is a promising device used in high voltage, high current, and high frequency applications.

D. Gate Drivers for SiC IGBT

Gate drivers for SiC IGBT is still not commercialized, considering high insulation capability, low coupling capacitance, low cost, reasonable size, high efficiency, high reliability, etc. At present, the topology and control strategies of Si IGBT or MOSFET are still used for the gate driver prototype of SiC IGBT/MOSFET [69]–[73], which includes isolated power supply, signal isolation, power amplification circuits. It is popular that transformer and optical fiber are used for power transmission and signal transmission, respectively, in design for SiC IGBT gate drivers. In the power transmission stage, the design of isolation transformer is an important part. Bulk size, winding

TABLE VI
GATE DRIVERS FOR SiC IGBT

References	DC Insulation Capability (kV)	Coupling Capacitance @50MHz (pF)	Functions	Target Devices
[69]	100kV	3.4	• Passive driving; • Shoot-through protection	15kV SiC IGBT
[70]	30kV	1.45	• Passive driving	10kV SiC IGBT/MOSFET
[71]	/	3.5	• Passive driving	15kV SiC IGBT/MOSFET
[72]	20kV	<1.5	• Active driving; • Protections: OT, OC, ST; • State-monitor; • Communication	15kV SiC IGBT 10kV SiC MOSFET
[73]	55kV	2	• Passive driving; • Short circuit protection;	10kV SiC MOSFET

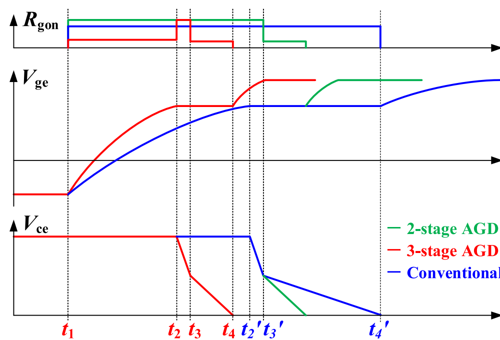
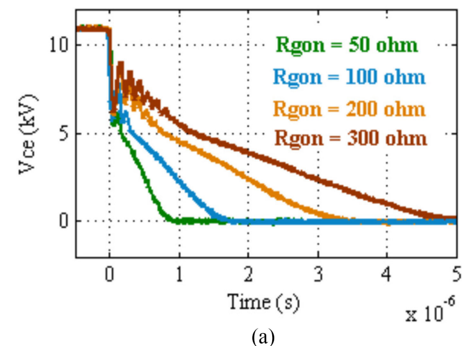


Fig. 13. Representation of conventional driver and AGD during turn-ON.



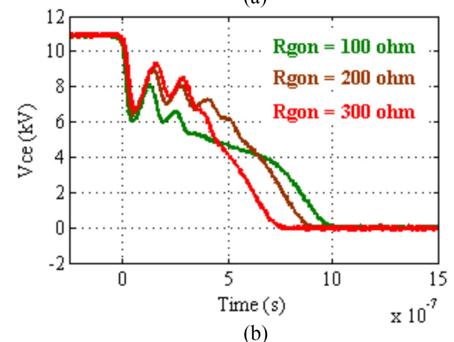


Fig. 14. Voltage waveforms of 15 kV SiC IGBT with conventional gate driver (a) and two-stage AGD(b). [67]

mode, core material, insulation capability, coupling capacitance, magnetizing inductance, and cost of the transformer counter each other. When the gate driver is exposed to the high voltage side, the high dv/dt will produce displacement current across the coupling capacitance, which will disturb the control signal. The coupling capacitance depends on the winding area on the core [70]. Therefore, the coupling capacitance is several pico-farads when winding enameled wires on the core, while the coupling capacitance could be reduced to less than 1 pF by one turn or PCB integrated transformer [70]. However, it also increases the leakage inductance of the transformer. Another underestimated design consideration is the efficiency and thermal distribution caused by conduction loss, switching loss, and core loss. Reasonable designs of input voltage, turns ratio, and switching frequency of H-bridge are effective ways to improve efficiency. Gate drivers developed in recent years are summarized in Table VI.

As shown in Fig. 11, the distinct two-slope variation of SiC IGBT during switching generates high dv/dt above punch-through voltage (V_{PT}) and high E_{sw} below V_{PT}, simultaneously. Therefore, the active gate drivers (AGD) with fast changing gate resistance are necessary to drive the SiC IGBT reliably and efficiently. A typical operating principle of AGD during turn-ON is shown in Fig. 13. During t_1–t_2, the R_{gon} is small to reduce the turn-ON delay. During t_2–t_3, the R_{gon} turns to be very large to limit dv/dt. During t_3– t_4, the R_{gon} becomes a small value to shorten the voltage falling time. The changing of R_{gon} could be realized by RC delay circuit or fast BJT [67], [72]. Different from the conventional driving control, as shown in Fig. 14, using two-stage AGD, suppressing dv/dt suppression and minimum turn-ON loss are achieved, simultaneously.

V. SiC IGBT APPLICATIONS

SiC IGBT provides new solutions and improved performance for power conversion system. However, the comprehensive integrating control of voltage sharing, current sharing, soft switching, driving and modulation needs to be reconsidered, because the high voltage, high dv/dt, and high temperature of SiC IGBT bring great challenges to the whole converter and peripheral auxiliary circuits.

A. Soft Switching

Ultrahigh voltage and fast switching generates high dv/dt and E_{sw} on SiC IGBT. The simple zero voltage switching (ZVS) with external snubber capacitors can realize

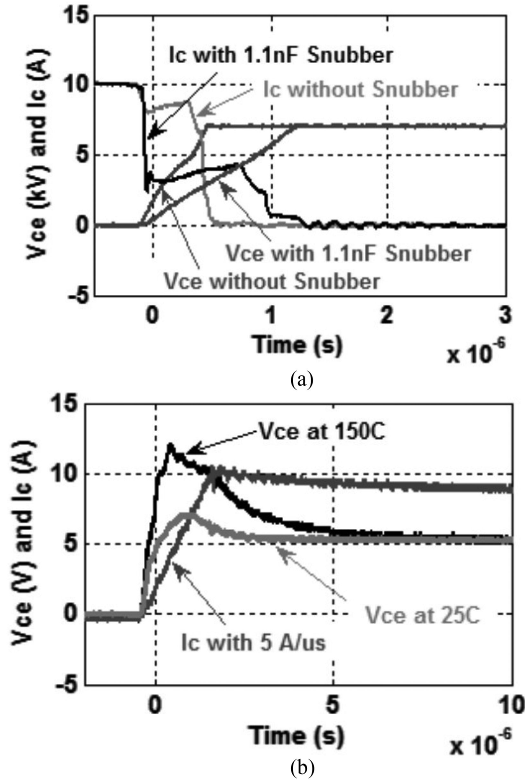


Fig. 15. Switching waveforms of ZVS. (a) Turn-OFF. (b) Turn-ON [66].

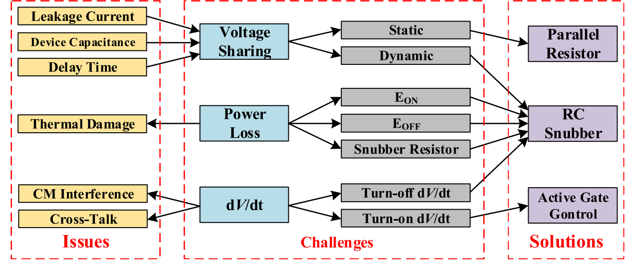


Fig. 16. Control strategy of SiC IGBT devices in series from [77].

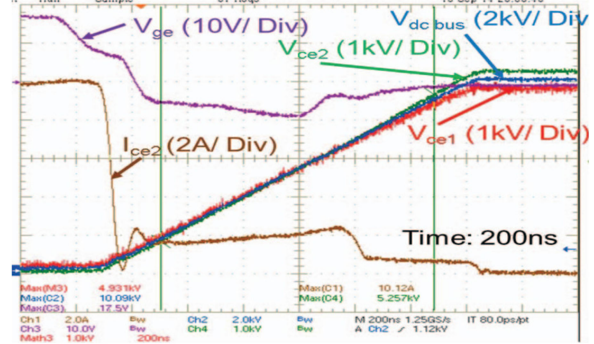


Fig. 17. Voltage sharing of 15 kV SiC IGBT with RC snubber (15 Ω, 2.2 nF) [78].

TABLE VII
COMPARISON OF DC–AC OPERATION OF 15 kV SiC IGBT WITH SOFT SWITCHING AND HARD SWITCHING

	Soft switching	Hard switching
Total power loss (W)	68.89 – 80	355
Junction temperature (°C)	46.87 – 49.16	130.5 – 135.65
AC pole dv/dt (kV/µs)	6.02	30.77
Common mode current (A)	1.8	9.23

full ZVS turn-ON and near ZVS turn-OFF [66], [74], [75]. In fact, the SiC IGBT without external snubber capacitor achieves partially ZVS turn-OFF, as shown in Fig. 15(a). The displacement current flowing through parasitic capacitance (C_1 and C_2) reduces the collector current at the beginning of turn-OFF. However, the current bump in phase II prevents the ZVS process. Therefore, the parallel snubber capacitor makes the turn-OFF closer to ZVS, as shown in Fig. 15(a). During the turn-ON of ZVS, due to conductance modulation lag in the drift region, the turn-ON voltage overshoot related to di/dt stress and temperature may trigger spurious short-circuit protection, as shown in Fig. 15(b).

It is noteworthy that the energy of parasitic capacitor and external snubber capacitor will be fed back to source during turn-OFF. Therefore, the real device loss can be calculated by thermal resistance of heatsink. The calculation and experimental results of soft switching and hard switching are compared in Table VII [76]. Compared with hard switching, soft switching not only reduces device loss significantly, but also greatly reduces dv/dt stress, thus reducing common mode current.

B. Series Connected SiC IGBT

Modular multilevel converter is used to enable a single device to handle a higher grid voltage. However, devices with higher blocking voltage are needed in the applications of high voltage two-level converter, or three-level converter with higher voltage or HVDC. Therefore, the devices in series are necessary. When devices are connected in series, device inconsistency and drive inconsistency will cause voltage imbalance of devices [77], [78]. Paralleling large resistance, RC snubber and active drive control are effective methods to solve the problem of voltage sharing and high dv/dt of SiC IGBT devices. Nevertheless, RC snubber needs tradeoff between E_{sw} and snubber loss. Active gate control is complex. In order to utilize these methods effectively, these strategies are implemented in corresponding states of SiC IGBT, as shown in Fig. 16.

First, for the voltage balancing control in the blocking state, resistors with resistance lower than blocking resistance of SiC IGBT are paralleled with device to realize static voltage balancing. Second, RC snubber is used to limit the turn-OFF dv/dt and ensure turn-OFF voltage balancing. Turn-OFF voltage sharing of two series connected SiC IGBT with RC snubber is shown in Fig. 17. Turn-ON voltage balancing is not necessary because the voltage difference is less than the rated voltage. Therefore, the reduction of turn-ON dv/dt can be achieved by AGD.

C. Parallel Connected SiC IGBT

To date, the maximum rated current of a single SiC IGBT device is 32 A due to the limited chip area [45]. However, in HVDC,

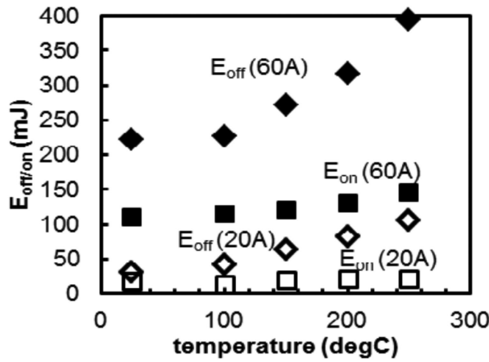


Fig. 18. Comparison of switching loss of single-chip module and three-chip module under different T_j [49].

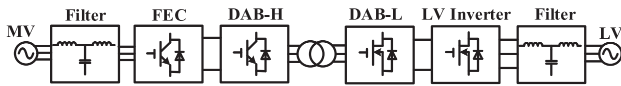


Fig. 19. Schematic of TIPS with 15 kV SiC IGBT and 1.2 kV SiC MOSFET [79].

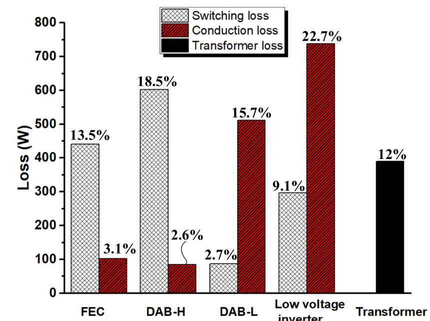


Fig. 20. Loss distribution of 15 kV SiC IGBT and 1.2 kV SiC MOSFET applied in 100 kVA TIPS.

SST, and smart grids, parallel SiC IGBT chips in a module are necessary to handle a higher current (more than 100 A [79]). The current imbalance and oscillation between paralleled chips significantly reduce the current capability of module due to the dispersion of the characteristics of fabricated SiC IGBT devices. The positive temperature coefficient (PCT) of V_f is preferred for paralleled chips. However, the PCT of V_f in reported SiC IGBT is not obvious due to the competition between mobility decreasing and lifetime increasing, as temperature increases. In addition, reasonable internal gate resistor could compensate the inconsistency of SiC IGBT devices and increase the damping during transients, thus improve the paralleling operation.

In addition, the extra loss challenges the paralleled chips. Switching losses of single-chip and three-chip SiC IGBT modules are compared in Fig. 18. The loss of three-chip module is much greater than three times of single-chip module [49]. This is because when the chips are paralleled, the parasitic capacitors of SiC IGBT are also paralleled. Therefore, the increase of input capacitance slows down the gate voltage, which results in rising and falling time of collector current increasing. Similar to input capacitance, increase of miller capacitance and output capacitance result in a slower V_{CE} changing. Finally, the switching loss increases exponentially with the number of parallel chips. Therefore, additional ZVS or RC snubber is expected to limit excessive switching losses. In addition, higher rated current produces a higher voltage overshoot, which is negligible in single-chip test.

D. Medium Voltage Grid Interface

Solid-state transformer gradually replaces the conventional distribution transformer as the interface of medium-voltage grid because of its advantages of lightweight and high efficiency [79], [80]. Transformer-Less Intelligent Power Substation (TIPS) is a noncascade topology based on all-SiC devices, as shown in Fig. 19. As a 13.8 kV to 480 V grid interface, TIPS can realize power conversion greater than 100 kVA. The system includes *LCL* filter, front end converter (FEC) based on SiC IGBT, dual active bridge (DAB) stage for insulating, and low voltage two-level inverter based on SiC MOSFET.

Although the three-level topology reduces the number of devices in series, the design of three-level neutral point clamped (3L NPC) converter is the main challenge of the TIPS system. First, the 3L NPC converter is exposed to high voltage, requiring additional insulation. Conventional issues, such as harmonic current, negative sequence current, precharge of DC bus and imbalance of bus mid-point are still serious. Moreover, unlike the low voltage 3L NPC converter, the fundamental current flowing through converter is small [81]. Therefore, the influence of harmonic current is greater, and harmonic current is more difficult to be extracted. On the other hand, compared with the two-level converter, the number of devices is doubled, worsening the thermal distribution, due to the difference between devices in terms of characteristic, power loss, and cooling conditions [82]. In contrast, compact structure is necessary for low parasitic inductance [83], which is harmful to heat dissipation. In the 3L NPC converter based on SiC IGBT, high frequency transformer should be carefully designed to achieve better tradeoff between size and parasitic capacitance for minimizing the current ringing [84].

It is noteworthy that the efficiency of TIPS with powerful function and space saving is 98% at 1 MVA, which is lower than that of conventional distribution transformer with 99% efficiency [79]. Even if the soft switching technology is used in the DAB, its switching loss accounts for 21% of the total loss, as shown in Fig. 20 [12]. In addition, the ON-state loss of SiC MOSFET used in DAB and low voltage side inverters accounts for 38%. Therefore, it is necessary to further increase the efficiency of TIPS system by reasonably reducing the driving resistance of SiC IGBT or increasing the number of paralleled SiC MOSFET. In addition, for 1 MVA TIPS, higher current SiC IGBT module or paralleling operation is necessary for current up to 100 A conducting.

E. Pulse Power Application

In the pulsed power application, it is expected to replace the high voltage gas switch with the emergence of SiC IGBT. In [13], 24 kV SiC IGBT has been applied to four-stage Marx generator,

which achieves the highest output voltage capability of 32 kV and current capability of 20 A. It delivers 0.66 MW to the load in 10 μs. It is noteworthy that at the end of the pulse, the last stage SiC IGBT withstands a large overvoltage due to the different output impedance of the switching loop, so the necessary voltage derating needs to be considered. Compared with other solid-state switches, such as SiC MOSFET, it has higher pulse current capability. In [85], the peak current capability of 15 kV SiC IGBT is 6.6 times that of 15kV SiC MOSFET. However, due to the inherent bipolar characteristics of SiC IGBT, its switching time limits its short pulsewidth capability, compared with SiC MOSFET. However, the SiC IGBT with drift thickness greater than 200 μm operating at high voltages with low duty cycles is encouraging for pulse power application [86].

In general, the most important points have been discussed in this section. For a better utilization of SiC IGBT in circuit design, other considerations are also critical, which are listed as follows.

1) The characteristics of SiC IGBT are dispersive due to the immature fabrication technology. Therefore, preselection of SiC IGBT with similar characteristics is important to achieve better voltage sharing, current sharing, and thermal distribution.
2) The distributed parasitic capacitance of the system should keep low due to the high d*v*/d*t*. Reasonable active or passive methods for controlling d*v*/d*t* are also effective ways.
3) The cooling conditions should be improved by forced air cooling or water cooling to reach a low T_j, due to the tradeoff between insulation and power dissipation.
4) The type of SiC IGBT could be selected for specific applications, such as n-channel SiC IGBT for boost converter or low side of half bridge, conversely p-channel SiC IGBT for buck converter or high side of half bridge.

VI. Conclusion

As the highest voltage switch, SiC IGBT has attracted wide attention in high voltage transmission, smart grid, and pulse power fields. The SiC IGBTs are still not commercialized due to the intrinsic defects and immature fabrication process. The reported SiC IGBT devices show excellent static and dynamic performance, along with considerable d*v*/d*t* during hard switching, which challenges the power conversion system. Although many solutions are proposed for SiC IGBT, it shows great differences from silicon IGBT and silicon carbide MOSFET. The preliminary attempts in high voltage fields indicate that the promising SiC IGBT would have the prospect to replace Si devices in the future.

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