Letters

A Periodically Refreshed Capacitive Floating Level Shifter for Conditional Switching Applications

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***Abstract*—This letter presents a periodically refreshed capacitive floating level shifter (CFLS) for applications that require a conditional switching signal. The proposed structure can generate a floating signal without additional bias voltage, and all coupling capacitors (CCs) can be simultaneously refreshed. Digital low-dropout (DLDOs) regulators are integrated to show how the leakage current from a CC affects the DLDOs that are driven by conventional and proposed CFLSs. Results are measured according to the temperature and supply voltage. With a 28-nm CMOS process, the proposed CFLS achieves a delay of 8.9 ns including the I/O buffer delay and an energy consumption of 788 fJ per cycle at $V_{\mathrm{DD}} = 0.9$ V.**

***Index Terms*—Capacitively coupled level shifter (LS), conditional switching signal, nonperiodic signal, periodic charge refresh.**

I. Introduction

A FLOATING level shifter (LS) is widely used to sample the voltage with a small ON resistance (R_{ON}) and drive power switches in different supply voltage domains. In particular, for high-voltage (HV) applications such as automobiles, light-emitting diode drivers, and energy harvesting systems with piezoelectric and triboelectric nanogenerators, an LS must be carefully selected to prevent the breakdown of the gate oxide of a transistor. In addition, a small delay and low-power dissipation are required.

A floating LS [1] provides a shifted-up signal with the aid of intermediate lateral double-diffused MOS (LDMOS) transistors that isolate low-voltage devices from the HV. However, a large amount of power is consumed by the shoot-through current (I_{SH}), and the large gate–drain capacitances of the LDMOS transistors result in a low switching speed [2]. Although coupling capacitors (CCs) allow LSs to have a steeper slew rate [3], [4], I_{SH} still remains, and an additional charge pump is required to generate a $2V_{\mathrm{DD}}$ supply domain [4]. Since the power consumed by an LS increases as the highest supply voltage (V_{DDH}) increases, a capacitive floating LS (CFLS) can be a good solution to eliminate I_{SH}. An LS that indirectly uses a CC can be utilized to improve speed by increasing V_{GS} of a transistor in the low-voltage domain [5]. In addition, as shown in Fig. 1, the n-type [6] and p-type [7] CFLSs directly used CCs (i.e., C_1 and C_2) to drive NMOS and PMOS transistors, achieving fast switching speed and low I_{SH}. V_{DD} is the supply voltage for the signal before shifting, and V_{DDH} is the supply voltage for the signal after shifting. The n-type and p-type CFLSs pump up the signal voltage level (i.e., V_{DD}) by V_{DDH} and $V_{\mathrm{DDH}}-V_{\mathrm{DD}}$, respectively. Note that those CFLSs include the two states such as precharging C_1 (φ_1) and driving the output by using C_1 (φ_2). However, if the input signal IN switches nonperiodically, the charge on CCs cannot be stably defined because the conventional CFLSs are synchronized by the signal IN. Therefore, LSs utilizing a CC must consider charge-refreshing operation for wireless sensor network applications that operate nonperiodically [8], [9]. A periodically refreshed LS (PRLS) [10] was proposed to restore the charge on all CCs, making LSs applicable to n-type digital low-dropout (DLDO) regulators, which operate with a conditional switching signal during steady state. However, the prior PRLS is not applicable to HVs that require floating-level signals because only a signal from $2V_{\mathrm{DD}}$ to V_{SS} can be

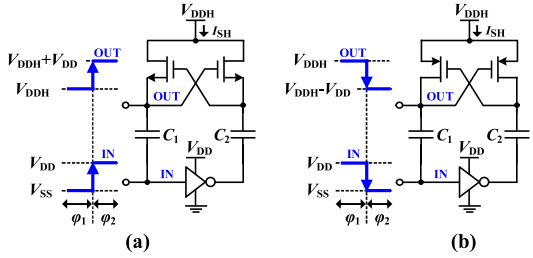

Fig. 1. Structures of (a) n-type [6] and (b) p-type [7] CFLSs.

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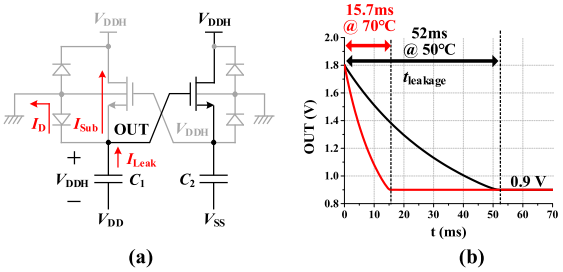

Fig. 2. (a) Leakage current caused by subthreshold (I_{Sub}) and junction leakage (I_D) currents in n-type CFLS. (b) Simulated charge loss of C_1 at the output of an n-type CFLS when $C_1 = 400$ fF, $V_{DD} = V_{DDH} = 0.9$ V, and $T = 50$ and 70 °C.

generated. Therefore, n- and p-type periodically refreshed CFLSs are proposed in this letter to generate the floating signal and refresh all CCs simultaneously. This letter is organized as follows. Section II describes I_{LEAK} existing in CFLSs and introduces the proposed CFLSs. Section III presents the measurement results. Finally, Section IV concludes this letter.

II. Proposed Periodically Refreshed CFLSs

A. Leakage Current of CFLSs

Fig. 2(a) shows the leakage current (I_{LEAK}) of the n-type CFLSs [6]. Because of the subthreshold leakage (I_{Sub}) and junction leakage (I_D) currents of MOSFETs, a conventional CFLS with a nonperiodic switching signal can lose the predefined potential, causing the circuit driven by a CFLS to malfunction. Since I_{sub} and I_D are proportional to the temperature I_{LEAK}, which is the sum of I_{Sub} and I_D, becomes large as the temperature increases. I_{LEAK} is dominated by I_{Sub}. Fig. 2(b) shows the charge loss on the CC in a conventional n-type CFLS when $V_{DD} = V_{DDH} =$ 0.9 V and $C_1 = 400$ fF. At temperatures of 50 and 70 °C, the output voltages of the CFLS are reduced by different values of I_{LEAK}, resulting in discharging times ($t_{leakage}$) from 1.8 to 0.9 V of 52 and 15.7 ms, respectively.

B. Structures of Proposed Periodically Refreshed CFLSs

Fig. 3 shows the structures of the proposed CFLSs. Each LS consists of two CFLS stages, an output stage, and a refreshing stage. As shown in Fig. 1, the conventional n- and p-type CFLSs output the floating signal and refresh the CCs, simultaneously, which is synchronized by the input signal IN. Therefore, if the input frequency (f_{IN}) is very low, the CCs cannot be refreshed, losing the predefined charges. To separate the input signal and the refresh operation, two n-type CFLSs are used for the proposed structure, as shown in Fig. 3(a). When the left-side n-type CFLS is refreshing its CCs, the right-side n-type CFLS outputs a floating signal V_{O3} to V_{GN}. The cross-coupled pair of the output stage using transistors M_{P1}, M_{P2}, M_{N1}, and M_{N2} is used to convert the output voltages V_{O1} and V_{O3} into a single-ended output V_{GN}. If a higher voltage level (i.e., $V_{GN} = V_{DDH} + V_{DD}$) needs to be applied to V_{GN}, M_{P1} and M_{P2} can be used to transfer a higher voltage among V_{O1} and V_{O3} to V_{GN}. Moreover, M_{N1} and M_{N2} are employed to deliver a low-voltage level to V_{GN}

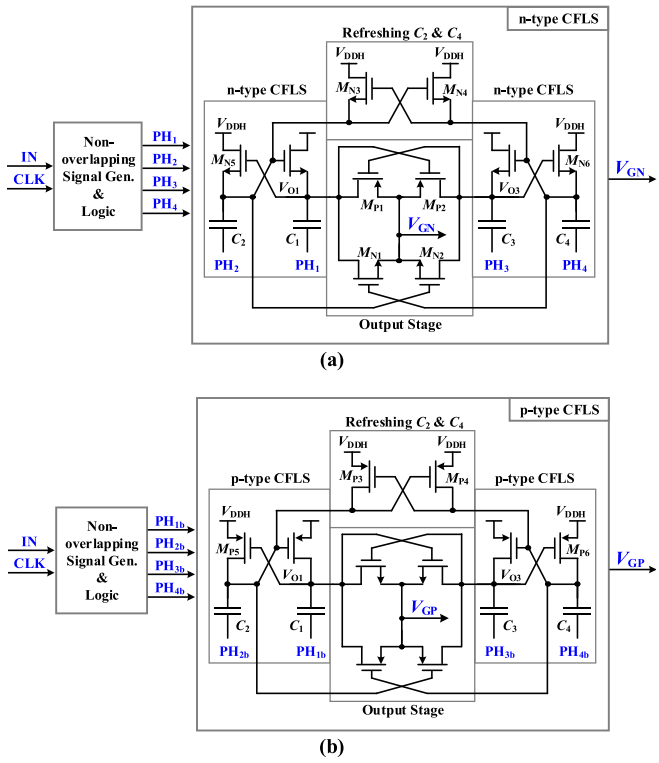

Fig. 3. Structures of the proposed periodically refreshed CFLSs for driving (a) NMOS and (b) PMOS transistors.

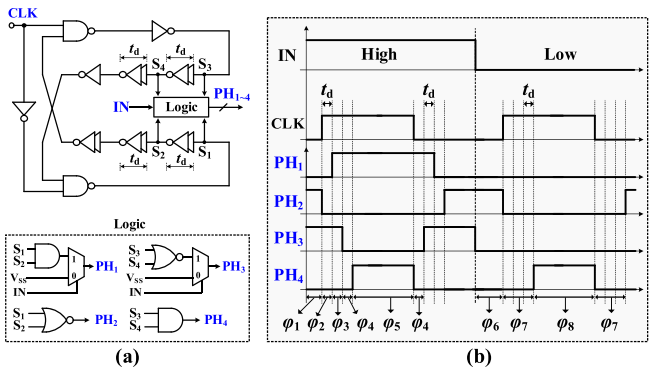

Fig. 4. (a) Nonoverlapping signal generator for the proposed n-type CFLS. (b) Transient waveforms of the signal generator.

(i.e., $V_{GN} = V_{DDH}$). The output stage of the p-type CFLS in Fig. 3(b) is for the same purpose.

The controller for signals PH_1–PH_4, which are required to provide V_{GN} and V_{GP}, is shown in Fig. 4(a). The controller generates the nonoverlapping time t_d to prevent charge loss on all CCs. According to the input signal IN, PH_1 and PH_3 are blocked by multiplexers. When IN is logic "high," the phases are divided into φ_1–φ_5, as shown in Fig. 4(b). When IN is logic "low," phases φ_6–φ_8 are repeatedly used. If $V_{DD} = V_{DDH}$, PH_1 and PH_3 are used to provide $2V_{DD}$ to V_{GN} with the aid of cross-coupled M_{P1} and M_{P2}. In addition, switching PH_1 and PH_3 can simultaneously refresh the charge on C_2 and C_4. However, switching the bottom plates of C_1 and C_3 does not allow their

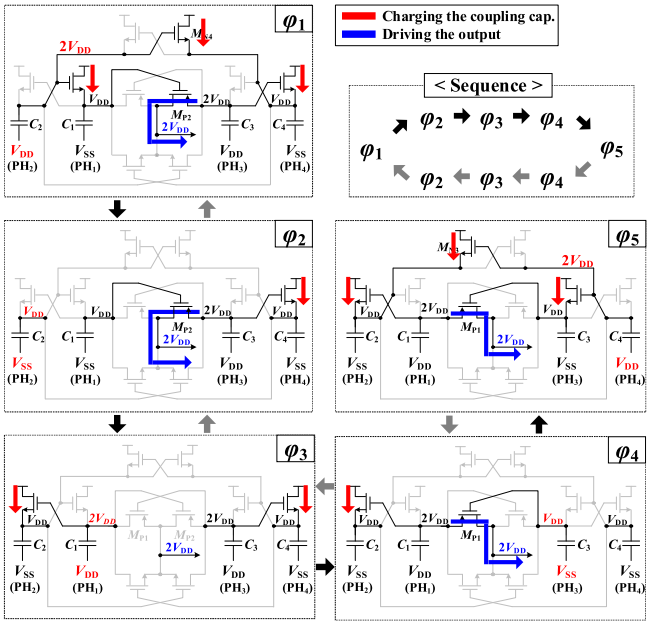

Fig. 5. Detailed operation of the proposed n-type CFLS when the IN is "high."

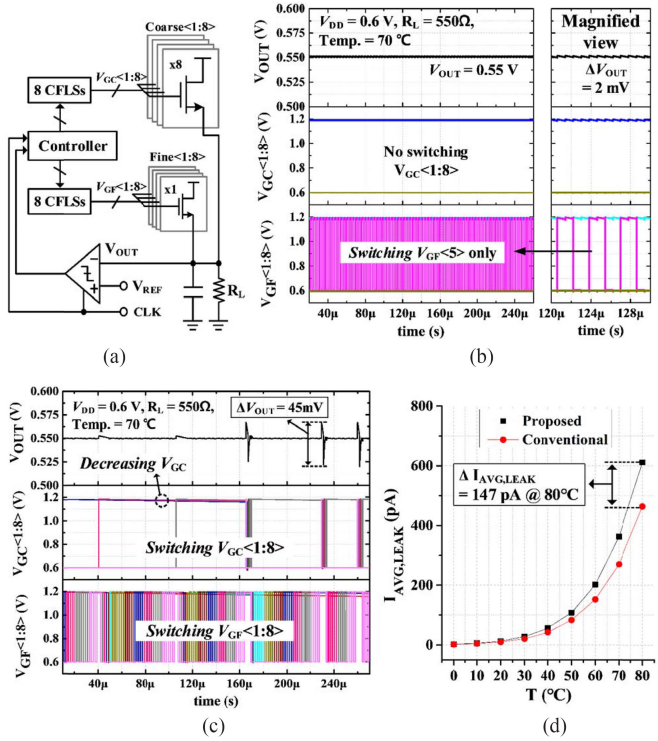

Fig. 6. (a) Block diagram and transient waveforms of NMOS DLDO regulators driven by the (b) proposed and (c) conventional n-type CFLSs when $T = 70$ °C. (d) Simulated $I_{\mathrm{AVG,LEAK}}$ of the CFLSs according to the temperature.

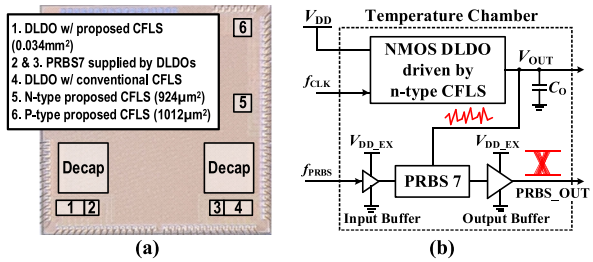

Fig. 7. (a) Die micrograph. (b) Measurement setup.

charge to be refreshed. Therefore, PH_2 and PH_4 are used to restore the charge on C_1 and C_3. Nevertheless, the charge on C_2 and C_4 cannot be refreshed when IN is logic "low" because PH_1 and PH_3 are nonswitching. Thus, additional cross-coupled transistors, M_{N3} and M_{N4}, are used. The operational details are shown in Fig. 5 when IN is logic "high." For the p-type structure, the inverted signals PH_{1b}–PH_{4b} should be applied to operate with the same principle as the n-type structure. It is noted that f_{IN} is limited to half of the clock frequency (f_{CLK}) because the proposed LS pumps the output in the high and low states in one clock cycle. In addition, when the proposed CFLS is applied for a nonperiodic switching application (i.e., $f_{\mathrm{IN}} \ll f_{\mathrm{CLK}}$), the power consumption is dominated by the nonoverlapping signal generator.

To compare the influence of I_{LEAK} in the conventional and proposed CFLSs, NMOS DLDO regulators, which do not switch except for the least significant bit during steady state, were adopted as an application using nonperiodic switching, as shown in Fig. 6. Note that the DLDO uses f_{CLK} of 10 MHz, and f_{CLK} is divided by 32 if there is no switching operation except for one V_{GF} bit. Since the proposed CFLSs can periodically refresh the charge on all CCs, the gate voltage $V_{\mathrm{GF}}<5>$ for the fine loop only switches under conditions where $V_{\mathrm{DD}} = 0.6$ V, $V_{\mathrm{OUT}} = 0.55$ V, $R_{\mathrm{L}} = 550\ \Omega$, and $T = 70$ °C, as shown in Fig. 6(b). However, under the same conditions, the DLDO driven by conventional CFLSs switches not only V_{GF} but also V_{GC}, which is the gate voltage of the coarse loop. As shown in Fig. 6(c), although V_{GC} and V_{GF} decrease owing to I_{LEAK}, V_{OUT} can be maintained by turning other bits ON and OFF, resulting in an output voltage ripple ΔV_{OUT} of 45 mV. As the temperature increases, the frequency of unwanted switching also increases. It should be noted that if the slow refresh rate (i.e., low f_{CLK}) is used for the proposed CFLS, a stable output of DLDO regulator cannot be guaranteed owing to a large V_{OUT} ripple. However, since f_{IN} and f_{CLK} can be separated for the proposed CFLSs, f_{IN} can be very low or even be maintained at dc as long as f_{CLK} is maintained above the frequency that can refresh the CCs.

During t_{leakage}, the simulated average leakage current ($I_{\mathrm{AVG,LEAK}}$) is shown in Fig. 6(d). For the proposed CFLS, the additional I_{LEAK} paths are generated by M_{N1} and M_{N2} of the output stage. Thus, when $T = 80$ °C, $I_{\mathrm{AVG,LEAK}}$ of 611 and 464 pA are obtained for the proposed and conventional n-type CFLSs, resulting in the difference of 147 pA.

III. Measurement Results

Standalone n- and p-type CFLSs and two DLDO regulators driven by the conventional and proposed CFLSs were fabricated by using a 28-nm general-purpose CMOS process, as shown in Fig. 7(a). A 1.8-V I/O n-type MOSFET is used to cover the

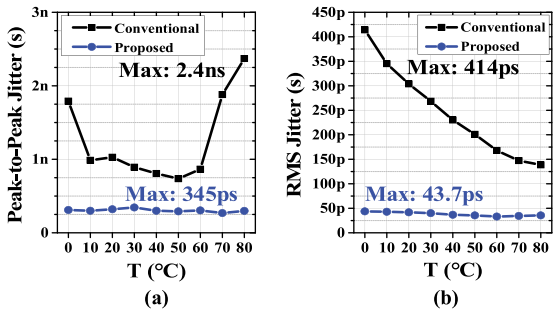

Fig. 8. Measured (a) peak-to-peak and (b) root-mean-square jitters of PRBS-7 supplied by DLDO regulators.

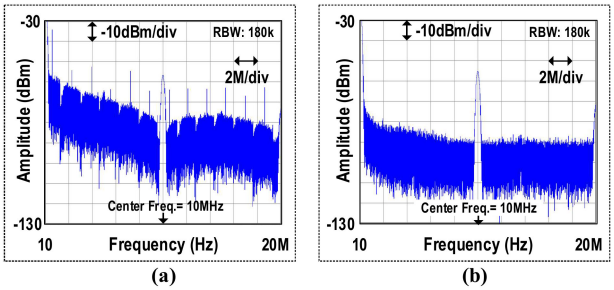

Fig. 9. Measured output power spectra at V_{OUT} of the DLDO regulators driven by the (a) conventional and (b) proposed CFLSs when $T = 30$ °C.

supply voltage range up to 0.9 V, and the n-type proposed CFLS occupies an effective area of 924 μm^2, which includes all CCs with a capacitance of 2.1 pF. Fig. 7(b) shows the measurement setup for comparing the influence of I_{LEAK} in the CFLSs. For this measurement, the jitter is a timing variations of signal edges from PRBS-7 generator, which is caused by V_{OUT} ripple of DLDO regulator (i.e., supply voltage noise). The peak-to-peak and standard deviation values of the timing variations are defined by the peak-to-peak and root-mean-square (rms) jitters, respectively. Fig. 8 shows the measured peak-to-peak and rms jitters when $f_{\mathrm{CLK}} = 10$ MHz, $f_{\mathrm{PRBS}} = 50$ MHz, and $V_{\mathrm{OUT}} = 0.55$ V. The DLDO regulator driven by the proposed CFLS achieves small and flat peak-to-peak jitter compared to the DLDO driven by the conventional CFLS. A large peak-to-peak jitter is obtained at a low temperature because R_{ON} of the power transistors in the DLDO increases as the temperature decreases. In addition, the rms jitter is inversely proportional to the temperature owing to R_{ON}, as shown in Fig. 8(b). As shown in Fig. 9, the DLDO regulator driven by the conventional CFLS has many unwanted frequency components except for $f_{\mathrm{CLK}} = 10$ MHz, which degrades the quality of V_{OUT}. Fig. 10(a) shows the measured transient waveforms of the proposed CFLSs when $f_{\mathrm{IN}} = 1$ MHz and $f_{\mathrm{CLK}} = 4$ MHz under conditions where $V_{\mathrm{DD}} = 0.6$ V and $V_{\mathrm{DDH}} = 0.6$ and 1.5 V for the n- and p-type LSs, respectively. To drive a load capacitance of 100 fF, $C_1 = C_3 = 900$ fF and $C_2 = C_4 = 150$ fF were used, achieving a swing level (i.e., $\Delta V = \Delta V_1 + \Delta V_2$) that is equal to 99% of V_{DD} per clock period. When the signal INB is logic "low," charge is transferred to the outputs V_{GN} and V_{GP}. For a half cycle of f_{CLK}, V_{GN} is pumped by $\Delta V_1 = 0.54$ V, which is 90% of 0.6 V, and the remaining charge

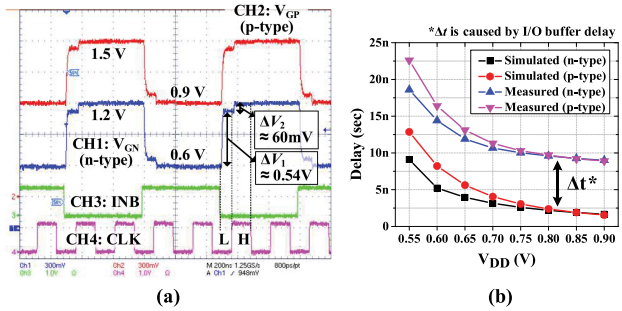

Fig. 10. Measured (a) transient waveforms and (b) time delays of the proposed n- and p-type CFLSs.

TABLE I
PERFORMANCE COMPARISON OF THE CAPACITIVE COUPLED LSS

	JSSC'15 [7]	TCAS-II'16 [5]	ISCAS'17 [3]	This Work	
Process	180 nm	65 nm	180 nm	28 nm	
Type of CC	Directly coupled to output	Indirectly coupled to output	Indirectly coupled to output	Directly coupled to output	
Drivable MOS	PMOS	PMOS & NMOS	PMOS	NMOS	PMOS
Appli-cation	Periodic Signal	Periodic Signal	Periodic Signal	Nonperiodic & Periodic Signals	
V_{DDH} [V]	100	1.0	50	0.55–0.9	0.55–1.8
V_{SSH} [V]	N/A	0.4	45	N/A	N/A
V_{DD} [V]	5	0.2	5	0.55–0.9	
Swing Level	$V_{\mathrm{DDH}} - V_{\mathrm{DD}} \sim V_{\mathrm{DDH}}$	$0 \sim V_{\mathrm{DDH}}$	$V_{\mathrm{DDH}} - V_{\mathrm{DD}} \sim V_{\mathrm{DDH}}$	$V_{\mathrm{DDH}} \sim V_{\mathrm{DDH}} + V_{\mathrm{DD}}$	$V_{\mathrm{DDH}} - V_{\mathrm{DD}} \sim V_{\mathrm{DDH}}$
CC [pF]	5000**	0.4	4	2.1***	
Load [pF]	500	10 Inverters	60	0.1	
Delay @ f_{IN}	0.5 ns @ 500 kHz	12.9 ns @ 5 MHz	1.9 ns* @ 1 MHz	9 ns @ 2.5 MHz	8.9 ns @ 2.5 MHz
Energy/op **** [pJ]	2.5	0.204	242	0.785	0.788

*Simulated result. **Required value for 90.9% of V_{DD} per cycle.
***Required value for 99% of V_{DD} per cycle. ****Energy/operation = Power/f_{IN}.

can be transferred during the next half cycle of f_{CLK}, which provides $\Delta V_2 = 60$ mV to V_{GN}. As shown in Fig. 10(b), there are time differences Δt, between the simulated and measured delays that range from 7.4 to 10.6 ns since the measured delays include the delays of the input and output buffers.

The performance of the proposed CFLSs is compared in Table I. When $V_{\mathrm{DD}} = V_{\mathrm{DDH}} = 0.9$ V, a delay of 9 ns is measured, and an energy consumption (i.e., power/f_{IN}) of 785 fJ is observed for the n-type CFLS. Compared to the LS [7] that directly uses CC to the output, a larger delay is caused by the additional signal generator to provide the bottom plate of the CCs with the signals PH_1–PH_4. In addition, instead of removing I_{SH}, a larger value of CC is required to drive same load capacitance than that in [3]. However, the proposed CFLS including periodic charge refresh can generate a floating signal even with nonperiodic switching signals.

IV. CONCLUSION

This letter has presented n- and p-type CFLSs with periodic charge refresh. The proposed structure can generate a floating signal, and all CCs can be periodically refreshed. Even with a conditional switching signal, the proposed CFLS removes the dependence on I_{LEAK} caused by the temperature variation.

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