A New User-Configurable Method to Improve Short-Circuit Ruggedness of 1.2-kV SiC Power MOSFETs

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***Abstract*—Silicon carbide (SiC) power MOSFETs have been commercialized to replace silicon insulated gate bipolar transistors (IGBTs) in power conversion applications. However, the short-circuit ruggedness of SiC power MOSFETs must be enhanced to match that of Si IGBTs for application in motor drives for electric vehicles. A new, user-configurable method with a series-connected, Si enhancement mode MOSFET (EMM) is demonstrated to improve the short-circuit withstand time of commercially available 1.2-kV SiC power MOSFETs by 86% with a 4.2% increase in ON-resistance and a 13% increase in switching loss. In contrast, operating the 1.2-kV SiC power MOSFET with a reduced gate bias of 15 V produces an 80% improvement in short-circuit withstand time with 31% increase in ON-resistance and a 31% increase in switching loss. It is demonstrated that the drain of the EMM can be used as a sensing node to monitor ON-state current and to detect short-circuit events.**

***Index Terms*—Power MOSFET, programmable control, robustness, short-circuit currents, silicon carbide.**

I. Introduction

SILICON carbide (SiC) power MOSFETs are excellent alternatives to Si insulated gate bipolar transistors (IGBTs) for compact and high-efficiency electric vehicle and industrial motor drive applications due to their low ON-resistance, fast switching capabilities, and high operating temperature range [1]. However, the short-circuit (SC) withstand capability of SiC power MOSFETs, an important requirement for motor drive applications, is much worse than the accepted industry benchmark of 10 μs [2].

The SC capability for a SiC power MOSFET, t_{SC}, is defined as the maximum duration for which it can withstand SC conditions before physical failure. SiC power MOSFETs fail under SC conditions due to self-heating caused by large power dissipation under fault [3]. Such failures can be mitigated by suppressing the peak SC current, which is the same as the device drain saturation current at the dc-bus voltage under fault [4]. Enhancing t_{SC} with device structural changes or by reducing the gate drive voltage requires a trade-off with increase in the ON-resistance and switching losses [5].

A recent invention, named the Baliga short-circuit improvement concept (BaSIC) [6], provides an innovative method to enhance t_{SC} for SiC power MOSFETs with minimum impact on ON-state and switching performance. This technique employs a nonlinear element connected in series with the source electrode of the SiC power MOSFET. The nonlinear element is designed with a low resistance at ON-state current levels and a smaller saturation current than the SiC power MOSFET. Its low ON-state resistance produces minimal impact on the conduction and switching losses, while its lower saturation current enhances the SC time. This concept is analogous to the use of emitter ballast resistors in Si IGBTs to improve SC capability [7]–[10], with a nonlinear element being used in place of the ballast resistor to achieve a better trade-off between ON-state voltage drop and t_{SC}.

The proposed approach has been previously validated using a low breakdown-voltage gate-source-shorted (GSS) Si depletion mode MOSFET (DMM) connected in series with the source of the SiC power MOSFET [11]. It has been experimentally demonstrated that this configuration creates a composite three-terminal MOSFET (CM) (also called BaSIC(DMM) for brevity) that uses the low saturation current of the DMM to suppress the peak SC current in the SiC MOSFET, consequently increasing t_{SC}. The BaSIC(DMM) topology achieves a fixed trade-off between improving t_{SC} and an increase in conduction and switching losses based up on the chosen Si DMM. The trade-off cannot be easily reconfigured by the application engineer because this requires changing the Si DMM device. The BaSIC(DMM) topology has been shown to produce a much superior trade-off between t_{SC} and increase in resistance compared to using a series ballast resistor [12].

An alternate BaSIC topology, called BaSIC(EMM) for brevity, is proposed and demonstrated in this article that utilizes a low breakdown voltage Si enhancement mode MOSFET (EMM) to achieve *user-configurable* t_{SC} enhancement for SiC power MOSFETs. This approach is more flexible because a large number of Si EMM products are commercially available unlike Si DMM devices. In addition, the end user can select (or program) the dc gate bias voltage applied to the Si EMM to achieve a desired value for t_{SC} while trading-off the increase in conduction and switching losses. The same Si EMM can therefore be used to satisfy the requirements for multiple applications.

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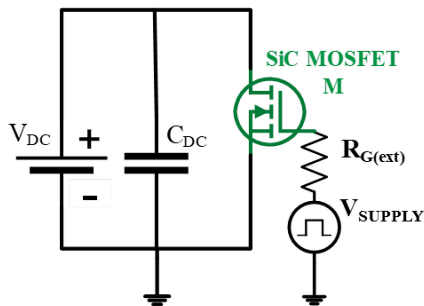

Fig. 1. Schematic for the short-circuit characterization test for a standalone SiC power MOSFET.

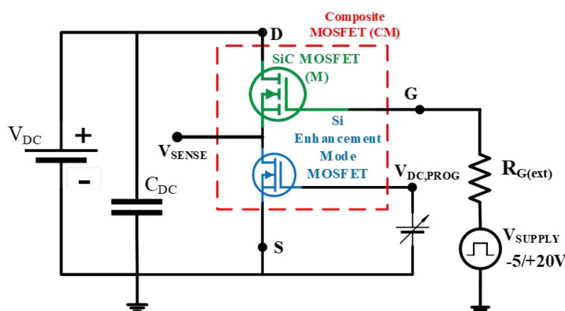

Fig. 2. Schematic for the short-circuit characterization test for the BaSIC(EMM) topology for a 1.2-kV SiC power MOSFET.

Although this topology might draw parallels with active loading in MOSFET amplifiers [13], it is worth pointing out that active load transistors are connected to the drain of the MOSFETs and designed to operate in the saturation mode to maximize amplifier gains and provide stable biasing. In contrast, the series MOSFET used in BaSIC(EMM) approach operates in its linear as well as saturation regions and is located in the gate loop of the SiC power MOSFET.

The schematics for the SC characterization for a standalone SiC power MOSFET (M) and the composite MOSFET (CM) with an Si EMM implementation are shown in Figs. 1 and 2. It is worth emphasizing that the Si EMM operates within the gate loop of the SiC power MOSFET. The largest voltage imposed on it is therefore limited to the gate drive voltage of 20 V typically used for SiC power MOSFETs. Hence, commonly available commercial 30–40 V Si EMMs with low ON-resistance can be used for this configuration. During ON-state and switching operation of the SiC power MOSFET, the Si EMM operates in its linear region with a low ON-resistance, thus, having minimal impact on the performance of the SiC power MOSFET. Under SC conditions, the Si EMM enters its saturation mode at a current level dictated by its dc gate bias. The resulting increase in its drain voltage opposes the gate drive voltage (20 V). The gate-source voltage $V_{\rm GS}$ (SiC) across the SiC power MOSFET is therefore reduced until the saturation current of the SiC power MOSFET *automatically* matches that of the Si EMM. The dc gate bias, $V_{\rm dc,PROG}$, applied to the Si EMM can be *programmed* by the user to control its saturation current under SC conditions to achieve the desired $t_{\rm SC}$. This *user-configured* $t_{\rm SC}$ enhancement method allows one composite MOSFET to be used across different applications with the same power ratings. The composite MOSFET (CM) in the BaSiC(EMM) case forms a four-terminal device including a terminal for the application of a programmable dc gate bias to the Si EMM. In addition, the drain of the Si EMM can be used as a fifth terminal to monitor ON-state current and to detect SC events as demonstrated in this article.

It has been previously reported that improvements in $t_{\rm SC}$ can be achieved by operating SiC power MOSFETs at a lower gate drive voltages. However, this approach produces an increase in the device ON-resistance and switching losses [14]. The trade-offs between $t_{\rm SC}$ enhancement and degradation of $R_{\rm DS,ON}$ and switching performance of SiC power MOSFETs for the two techniques—the BaSIC(EMM) and the use of reduced gate bias—are compared in this article.

II. Devices and Test Methods

A. Devices

Experimental demonstration of the proposed BaSIC(EMM) implementation was performed with the commercially available Wolfspeed 1.2-kV SiC power MOSFET C2M0160120D [15], and the Infineon 40-V Si enhancement mode (EMM) MOSFET IPI70N04S4 [16]. Tests were conducted for seven cases: 1) standalone SiC MOSFET (M) with standard $V_{\rm GS}$(SiC) = 20 V; 2a) composite MOSFET with $V_{\rm dc,PROG}$ = 6 V (labeled CM-6); 2b) composite MOSFET with $V_{\rm dc,PROG}$ = 5.7 V (labeled CM-5.7); 2c) composite MOSFET with $V_{\rm dc,PROG}$ = 5.4 V (labeled CM-5.4); 3a) M with $V_{\rm GS}$ (SiC) = 18 V; 3b) M with $V_{\rm GS}$ (SiC) = 15 V; and 3c) M with $V_{\rm GS}$ (SiC) = 12 V. The reduced gate bias values were chosen to obtain saturation currents in the SiC power MOSFET that were comparable to cases 2a, 2b, and 2c at a dc bias of 800 V. The composite MOSFET configurations were treated like a single device for all the tests.

B. Test Methodology

SC characterization was conducted using the circuits shown in Figs. 1 and 2, by turning the device-under-test (DUT) on at a dc voltage of 800 V using gate pulses of increasing width until physical failure was observed. The SC characterization setup was also used to conduct nondestructive SC tests with 1.5 μs gate pulses at different dc voltages. The peak current for each pulse was extracted as the saturation current and plotted to obtain high-voltage, high-current output characteristics for the different cases. Static characterization was performed using a Keysight B1505A curve tracer. Measured parameters included ON-resistance, threshold voltage, transfer characteristics, breakdown voltage, and device capacitances. Dynamic characterization was performed using clamped inductive load switching tests on a CREE KIT8020-CRD-8FF1217P-1 MOSFET Evaluation Kit. Switching tests were conducted at a dc-bus voltage of 800 V, a switching current of 10 A, and an external gate resistance of 10 Ω. A 150 μH inductor was used as the load with a Wolfspeed 1.2-kV SiC JBS Diode C4D05120A connected across it in antiparallel.

III. Experimental Results

A. High-Voltage High-Current Output Characteristics

The measured high-voltage high-current (HVHC) output characteristics for the different cases are shown in Fig. 3. For

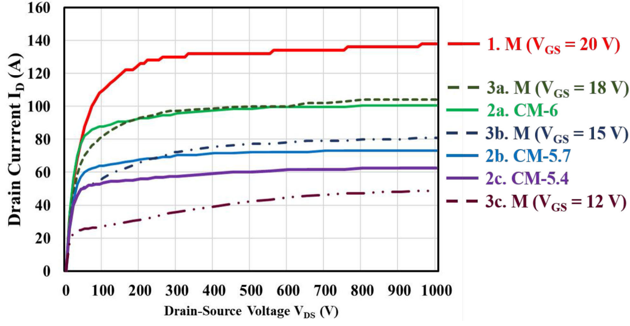

Fig. 3. Measured high-voltage, high-current output characteristics for the BaSIC(EMM) topology and the reduced-gate-bias equivalent cases for the standalone SiC power MOSFET.

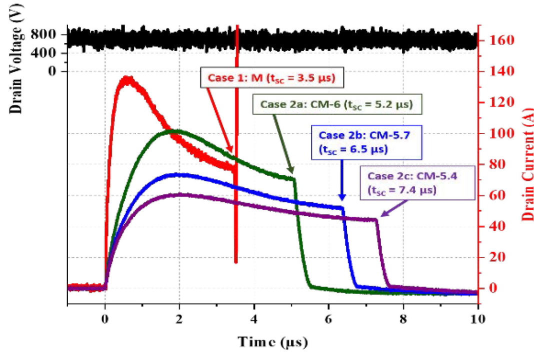

Fig. 4. Measured short-circuit test waveforms for the standalone SiC power MOSFET and BaSIC(EMM) topology.

a dc voltage of 800 V, Case 1 (M) has a saturation current $I_{\mathrm{D,SAT}}$ of 136 A. The dc gate bias values applied to the Si EMM were chosen so that Cases 2a, 2b, and 2c have lower $I_{\mathrm{D,SAT}}$ values of 100, 74, and 60 A, respectively. These results show that the user-configured dc gate bias $V_{\mathrm{dc,PROG}}$ applied to the Si EMM can be selected to suppress $I_{\mathrm{D,SAT}}$ of the SiC power MOSFET to any desired extent. This provides the experimental demonstration of the flexibility of the BaSIC(EMM) topology.

The SiC power MOSFET drain saturation current can also be suppressed by reducing the gate drive voltage. The reduced values for the gate bias voltage were chosen to achieve saturation currents comparable to the BaSIC(EMM) cases so that the two topologies could be compared. Case 3a labeled M ($V_{\mathrm{GS}} = 18$ V) with a gate bias of 18 V has an $I_{\mathrm{D,SAT}}$ of 106 A; Case 3b labeled M ($V_{\mathrm{GS}} = 15$ V) with a gate bias of 15 V has an $I_{\mathrm{D,SAT}}$ of 80 A; and Case 3c labeled M($V_{\mathrm{GS}} = 12$ V) with a gate bias of 12 V has an $I_{\mathrm{D,SAT}}$ of 48 A.

B. Short-Circuit Characterization Tests

The measured SC test waveforms for the standalone SiC MOSFET and the BaSIC(EMM) implementation are shown in Fig. 4. Case 1 (M) has a peak SC current, $I_{\mathrm{SC,PEAK}}$ of 136 A, which reduced to 82 A before failure at 3.5 μs. The peak SC current for case M is equal to the saturation current of the SiC power MOSFET at a drain bias of 800 V and gate drive voltage of 20 V. The current reduces during the SC time due to heating of the device. Case 2a (CM-6) with Si EMM dc gate bias $V_{\mathrm{dc,PROG}} = 6$ V has a $I_{\mathrm{SC,PEAK}}$ of 102 A, which reduced to 70 A before failure at 5.2 μs. Case 2b (CM-5.7) with Si EMM dc gate bias $V_{\mathrm{dc,PROG}} = 5.7$ V has a $I_{\mathrm{SC,PEAK}}$ of 74 A, which reduced to 52 A before failure at 6.5 μs. Case 2c (CM-5.4) with Si EMM dc gate bias $V_{\mathrm{dc,PROG}} = 5.4$ V has a $I_{\mathrm{SC,PEAK}}$ of 62 A, which reduced to 48 A before failure at 7.4 μs. These results provide experimental confirmation that the BaSIC(EMM) topology can be used to increase the SC time by programming the dc gate bias applied to the Si EMM.

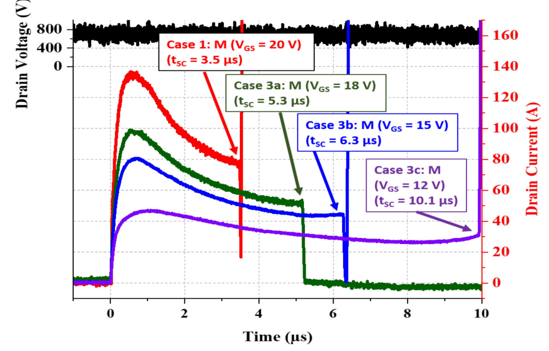

Fig. 5. Measured short-circuit test waveforms for the standalone SiC power MOSFET at different gate drive voltages.

TABLE I
SHORT-CIRCUIT TEST RESULTS

Case	$I_{\mathrm{SC,PEAK}}$ (A)	t_{SC} (µs)	$I_{\mathrm{SC,PEAK}}$ (Norm.)	t_{SC} (Norm.)
1. M ($V_{\mathrm{GS}} = 20$ V)	136	3.5	1	1
2a. CM-6	102	5.2	0.75	1.49
2b. CM-5.7	74	6.5	0.54	1.86
2c. CM-5.4	62	7.4	0.46	2.11
3a. M ($V_{\mathrm{GS}} = 18$ V)	100	5.3	0.74	1.51
3b. M ($V_{\mathrm{GS}} = 15$ V)	80	6.3	0.59	1.8
3c. M ($V_{\mathrm{GS}} = 12$ V)	48	10.1	0.35	2.89

The measured SC waveforms for the standalone SiC MOSFET at different gate bias voltages are shown in Fig. 5. Case 3a with gate bias of 18 V has an $I_{\mathrm{SC,PEAK}}$ of 100 A, which reduced to 52 A before failure at 5.3 μs. Case 3b with gate bias of 15 V has an $I_{\mathrm{SC,PEAK}}$ of 80 A, which reduced to 44 A before failure at 6.3 μs. Case 3c with gate bias of 12 V has an $I_{\mathrm{SC,PEAK}}$ of 48 A, which reduced to 30 A before failure at 10.1 μs. The peak SC current values for each gate bias value correspond to the drain saturation currents at a drain bias of 800 V in Fig. 3.

The results obtained from the SC test results for all the cases are summarized in Table I. It provides absolute and normalized value for the peak SC current and SC time. Using these values, a strong relationship between the SC time and the peak SC current can be observed in Fig. 6. The BaSIC(EMM) topology and the gate bias reduction approach overlap because the heating of the SiC power MOSFET chip is determined by the magnitude of the SC current irrespective of the method used to control its value.

C. Static Characterization Tests

The measured ON-state characteristics for the SiC MOSFET and the composite MOSFET (M) of the BaSIC(EMM) implementations are shown in Fig. 7. A small increase in

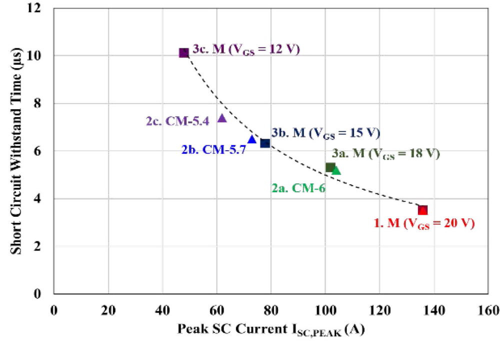

Fig. 6. Relationship between the short-circuit time and the peak short-circuit current using data from all the tested cases. BaSIC(EMM) cases are marked with triangles and the reduced gate bias cases are marked with squares.

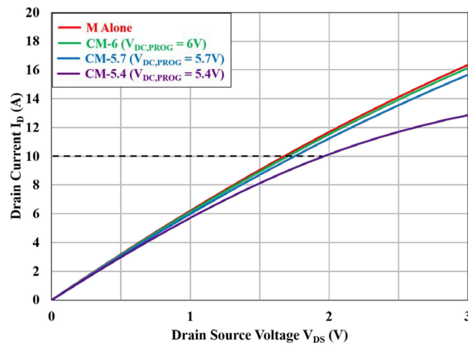

Fig. 7. Measured ON-state characteristics for the standalone SiC power MOSFET and composite MOSFET (M) in the BaSIC(EMM) topologies.

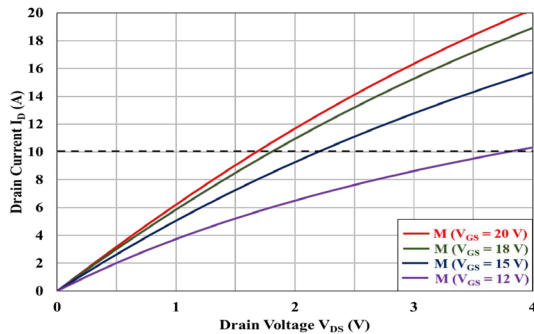

Fig. 8. Measured ON-state characteristics for the standalone SiC power MOSFET at different gate bias voltages.

the ON-resistance is observed for the case of larger dc gate bias $V_{\rm dc,PROG}$ applied to the Si EMM. A greater increase in ON-resistance occurs for the dc gate bias value of 5.4 V with quasi-saturation of the current. This increase in ON-resistance is related to the variation of the Si EMM ON-resistance with gate bias as discussed later in the article.

The measured ON-state characteristics for the SiC MOSFET at different gate bias voltages are shown in Fig. 8. A large increase in the ON-resistance is apparent as the gate bias voltage is reduced due to an increase in the channel resistance within the SiC power MOSFET structure. The ON-resistance values for all the cases at a drain current of 10 A are provided in Table II for comparison.

TABLE II
STATIC CHARACTERIZATION TEST RESULTS

Parameters, Units (Conditions)	1. M (V_{GS} 20V)	2a. CM -6	2b. CM-5.7	2c. CM-5.4	3a. M (V_{GS} 18V)	3b. M (V_{GS} 15V)	3c. M (V_{GS} 12V)
$R_{DS,ON}$, mΩ (V_{GS} = 20V, I_D = 10 A)	168	170	175	195	181	220	380
$R_{DS,ON}$ (Norm.)	1	1.01	1.04	1.17	1.08	1.31	2.26
V_{TH}, V (V_{DS} = 0.1 V, I_D = 1 mA)	3.23	3.29	3.3	3.26	3.23	3.23	3.23
g_M, S (V_{DS} = 10 V, I_D = 10 A)	3.23	3.1	3.1	2.7	3.23	3.23	3.23
BV_{DSS}, V (I_D= 100 μA)	1.58	1.6	1.6	1.6	1.6	1.6	1.6
C_{ISS}, pF (V_{DS} = 1 V, f = 100 kHz)	760	740	732	738	760	760	760
C_{ISS}, pF (V_{DS} = 1 kV, f = 100 kHz)	553	563	549	566	553	553	553
C_{OSS}, pF (V_{DS} = 1 V, f = 100 kHz)	817	802	810	805	817	817	817
C_{OSS}, pF (V_{DS} = 1 kV, f = 100 kHz)	49	49	50	54	49	49	49
C_{RSS}, pF (V_{DS} = 1 V, f = 100 kHz)	250	249	243	256	250	250	250
C_{RSS}, pF (V_{DS} = 1 kV, f = 100 kHz)	3.35	3.33	3.32	3.32	3.35	3.35	3.35

The transfer characteristics were measured for all the cases with a drain bias of 0.1 V. The threshold voltage of about 3.2 V extracted at a drain current of 1 mA was very close for all the cases, as shown in Table II. The breakdown voltage, $BV_{\rm DSS}$, of the composite MOSFET (M) in the BaSIC(EMM) topologies was measured using a gate bias of 0 V. It was found to have the same value of around 1.6 kV for all cases of dc bias applied to the Si EMM because the voltage is supported by the SiC power MOSFET. These results demonstrate that the BaSIC(EMM) topology does not impact the threshold voltage and breakdown voltage.

The measured transfer curves for the standalone MOSFET and composite MOSFET (M) in the BaSIC(EMM) topologies at a drain bias of 10 V are shown in Fig. 9. The transconductance, $g_{\rm M}$, values extracted from this data at a drain current of 10 A is provided in Table II. A reduction of $g_{\rm M}$ is observed with decreasing dc bias, $V_{\rm dc,PROG}$, applied to the Si EMM in the BaSIC(EMM) cases. This change is attributed to the series resistance of the EMM as previously observed with the Si DMM devices [11].

The measured capacitance values for the standalone SiC power MOSFET and composite MOSFET (M) in the BaSIC(EMM) topologies were very close, as shown in Fig. 10. This can be understood by analyzing the internal capacitances shown

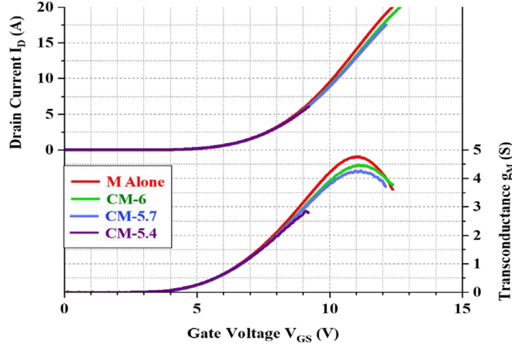

Fig. 9. Measured transfer characteristics for the standalone SiC power MOSFET and composite MOSFET (M) in the BaSIC(EMM) topologies.

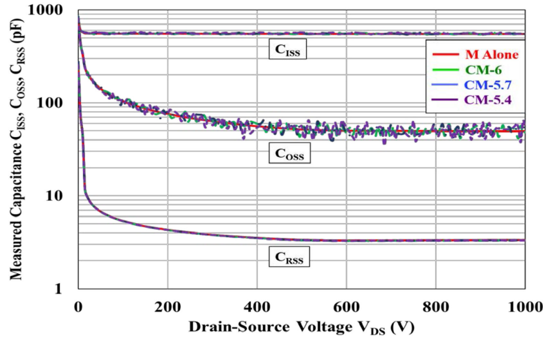

Fig. 10. Measured capacitances of the standalone SiC power MOSFET and the composite MOSFET in the BaSIC(EMM) topology.

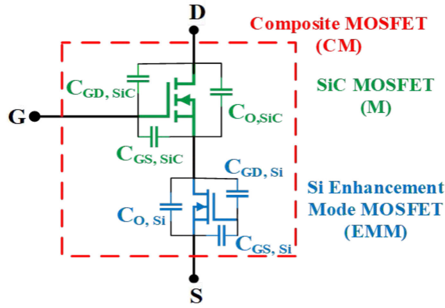

Fig. 11. Schematic of the internal capacitances in the composite MOSFET in the BaSIC(EMM) topology.

in the schematic of Fig. 11 for the composite MOSFET in the BaSIC(EMM) topology.

The input capacitance is measured by creating an external short across the drain-source terminal of the composite MOSFET. This creates two parallel branches—one with $C_{\mathrm{GS,SiC}}$, and the other with a series combination of $C_{\mathrm{GS,SiC}}$ with the output capacitance of the EMM, $C_{\mathrm{O,Si}}$. The input capacitance, C_{ISS} of the composite MOSFET is given by

$$C_{\mathrm{ISS}}\,(\mathrm{CM}) = C_{\mathrm{GD,SiC}} + \frac{C_{\mathrm{GD,SiC}} \times C_{\mathrm{O,Si}}}{C_{\mathrm{GD,SiC}} + C_{\mathrm{O,Si}}}. \quad (1)$$

The EMM operates in the ON-state with a low voltage drop (< 0.2 V) across it under all capacitance test conditions.

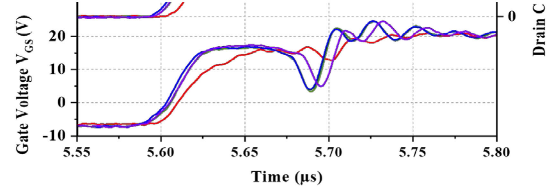

Fig. 12. Measured turn-ON transient for the standalone SiC MOSFET and composite MOSFET in the BaSIC(EMM) topologies.

As a result, it exhibits a high output capacitance (2000 pF) per its datasheet [16]. For an SiC MOSFET drain bias of 1 V, $C_{\mathrm{GD,SiC}}$ has a value of 290 pF, $C_{\mathrm{GS,SiC}}$ has a value of 600 pF, and $C_{\mathrm{O,Si}}$ has a value of 2000 pF per its datasheet [16]. Using these values, a C_{ISS} (CM) of 750 pF is obtained at a drain bias of 1 V in agreement with the measured value given in Table II. For a drain bias of 1000 V, $C_{\mathrm{GD,SiC}}$ has a value of 4 pF, $C_{\mathrm{GS,SiC}}$ has a value of 525 pF, and $C_{\mathrm{O,Si}}$ has a value of 2000 pF per its datasheet [16]. Using these values, a C_{ISS}(CM) of 420 pF is obtained at a drain bias of 1000 V. The measured value of C_{ISS}(CM) at a drain bias of 1000 V was found to be 553 pF.

The output capacitance is measured by applying a dc short across the gate-source terminals of the composite MOSFET. This places $C_{\mathrm{GS,SiC}}$ in parallel with $C_{\mathrm{O,Si}}$. The output capacitance of the composite MOSFET can be expressed as

$$C_{\mathrm{OSS}}\,(\mathrm{CM}) = C_{\mathrm{GD,SiC}} + \frac{C_{\mathrm{DS,SiC}} \times (C_{\mathrm{GS,SiC}} + C_{\mathrm{O,Si}})}{C_{\mathrm{DS,SiC}} + (C_{\mathrm{GS,SiC}} + C_{\mathrm{O,Si}})}. \quad (2)$$

For a drain bias of 1 V, $C_{\mathrm{DS,SiC}}$ has a value of 800 pF per its datasheet [16]. This results in a calculated value of C_{OSS} (CM) of 818 pF in agreement with the measured values provided in Table II. At a drain bias of 1000 V, $C_{\mathrm{DS,SiC}}$ reduces to 50 pF per its datasheet [16]. This results in a calculated value for C_{OSS} (CM) of 52 pF in agreement with the measured values provided in Table II.

The reverse transfer capacitance of the composite MOSFET is the same as that of the SiC power MOSFET

$$C_{\mathrm{RSS}}\,(\mathrm{CM}) = C_{\mathrm{RSS,SiC}}. \quad (3)$$

Its measured values for a dc voltage of 1000 V are given in Table II.

D. Dynamic Characterization Tests

It is important to quantify the impact of the BaSIC(EMM) topology on the turn-ON and turn-OFF losses for the case of the typical inductive load that represents the motor drive applications. Dynamic characterization was therefore performed using a clamped inductive load switching circuit.

The measured drain current and voltage waveforms during the turn-ON and turn-OFF transitions of the standalone MOSFET and the composite MOSFET in the BaSIC(EMM) topologies (Cases 1, 2a, 2b, and 2c) are shown in Figs. 12 and 13. The switching losses E_{ON} and E_{OFF} were obtained by integrating the product of the instantaneous drain voltage and current across the duration of the transient. The measured values for these cases are summarized in

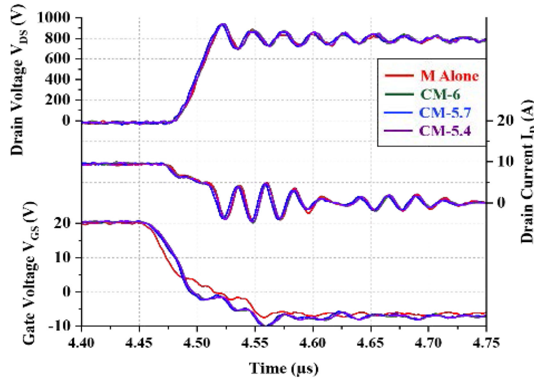

Fig. 13. Measured turn-OFF transient for the standalone SiC MOSFET and composite MOSFET in the BaSIC(EMM) topologies.

TABLE III
CLAMPED INDUCTIVE LOAD SWITCHING TEST RESULTS

Case	E_{ON} (μJ)	E_{OFF} (μJ)	E_{TOT} (μJ)	E_{TOT} (Norm.)
1. M (V_{GS} = 20 V)	314	68	382	1
2a. CM-6	322	65	387	1.01
2b. CM-5.7	368	64	432	1.13
2c. CM-5.4	374	63	437	1.14
3a. M (V_{GS} = 18 V)	346	66	412	1.08
3b. M (V_{GS} = 15 V)	432	68	500	1.31
3c. M (V_{GS} = 12 V)	575	68	643	1.68

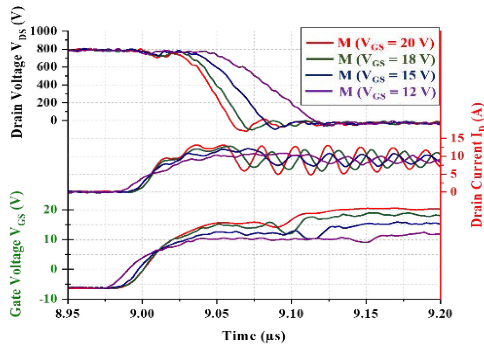

Fig. 14. Measured turn-ON transient for the standalone SiC MOSFET with different gate drive voltages.

Table III. The measured turn-OFF energy loss for the standalone SiC MOSFET and composite MOSFET in the BaSIC(EMM) cases was the same (around 66 μJ). A small increase of less than 20% in the turn-ON switching loss was observed for the CM cases.

The measured drain current and voltage waveforms for the turn-ON and turn-OFF transitions of the standalone MOSFET for the different gate drive voltage are shown in Figs. 14 and 15, respectively. The measured values for these cases are summarized in Table III. The measured turn-OFF energy loss for the standalone SiC MOSFET was the same for all gate drive voltages (around 66 μJ). A large increase of up to 83% in the turn-ON switching loss was observed when the gate bias is reduced.

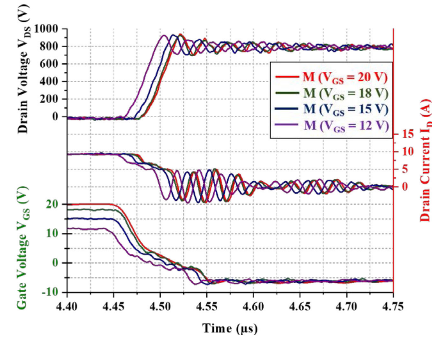

Fig. 15. Measured turn-OFF transient for the standalone SiC MOSFET with different gate drive voltages.

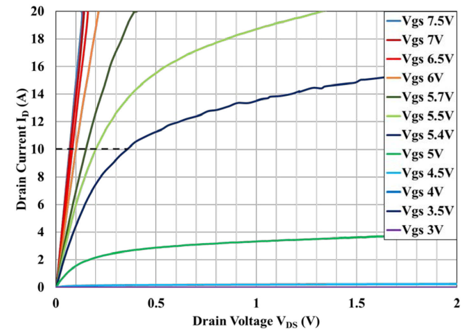

Fig. 16. Measured ON-state characteristics for the Si EMM at different gate bias values ($V_{\rm dc,PROG}$).

IV. DISCUSSION

A. Static Characteristics

The BaSIC(EMM) topology employs a Si EMM connected in series with the SiC power MOSFET to suppress the peak SC current. The ON-resistance of the composite MOSFET in the BaSIC(EMM) topology will be close to that for the SiC power MOSFET if the Si EMM has a low ON-resistance. Si EMM devices with blocking voltages of 30–40 V are commercially available with very low ON-resistances of 5 mΩ. However, this value is achieved at a gate bias of 10 V. This gate bias produces a large saturation current that is not suitable for the BaSIC(EMM) implementation. The ON-resistance of the Si EMM increases when the gate bias is reduced.

The measured ON-state characteristics for the Si EMM device selected for this work are shown in Fig. 16 at various gate bias voltages ($V_{\rm dc,PROG}$). The device remains in its linear region at a drain current of 10 A for $V_{\rm dc,PROG}$ values above 5.5 V with ON-resistance decreasing with increase in the gate bias voltage. However, it enters the quasi-saturation region when $V_{\rm dc,PROG}$ is reduced to 5.4 V, resulting in a much larger ON-resistance.

The ON-resistance $R_{\rm ON}$ (EMM) extracted at $I_{\rm D} = 10$ A for the Si EMM device is plotted in Fig. 17 as a function of its dc gate bias voltage ($V_{\rm dc,PROG}$). It can be seen that the ON-resistance has very low values below 15 mΩ for $V_{\rm GS}$ above 5.6 V but grows to 36 mΩ for a $V_{\rm GS}$ of 5.4 V.

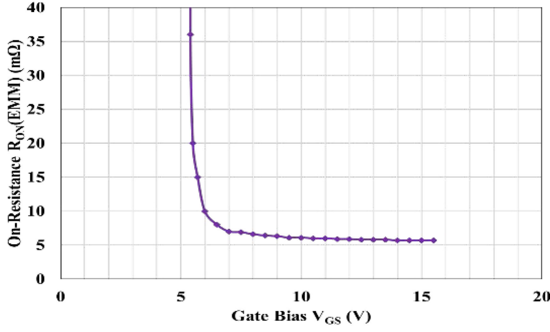

Fig. 17. Measured ON-resistance for the Si EMM at different gate bias values ($V_{\mathrm{dc,PROG}}$).

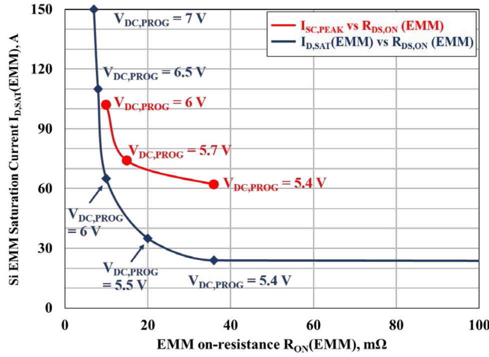

Fig. 18. Trade-off curve for saturation current and $R_{\mathrm{DS,ON}}$ for the Si EMM.

A trade-off curve between reducing the Si EMM saturation current $I_{\mathrm{D,SAT}}$ (EMM) and maintaining a low R_{ON} (EMM) was created, as shown in Fig. 18 by the blue points and line, by using the room temperature values extracted from the Si EMM datasheet. It indicates that the chosen Si EMM for this study is satisfactory for reducing the $I_{\mathrm{D,SAT}}$(EMM) to 65 A with a gate bias of 6 V while obtaining a low ON-resistance of 10 mΩ. However, reducing the $I_{\mathrm{D,SAT}}$(EMM) below 60 A with smaller gate bias significantly increases the ON-resistance for the selected Si EMM device. From Fig. 6, a $t_{\mathrm{SC}} = 10\ \mu$s can be achieved if the peak SC current is reduced to 50 A. From the blue trade-off line in Fig. 18, it can be concluded that a $t_{\mathrm{SC}} = 10\ \mu$s can be obtained with the chosen Si EMM by reducing the $I_{\mathrm{D,SAT}}$ (EMM) to 50 A with a $V_{\mathrm{GS}} = 5.9$ V. However, this is inconsistent with the results shown in Fig. 4.

The inconsistency is created because the Si EMM heats up during the SC event. Its temperature rise, computed by using the adiabatic model used for SC analysis of a power device [17] with $I_{\mathrm{D}} = 40$ A, $V_{\mathrm{DS}} = 5$ V, is about 200 °C after 2 μs. This will reduce the threshold voltage from 3 to 1.5 V according to its datasheet. The saturation current for $V_{\mathrm{GS}} = 5.4$ V will then increase by a factor of 2.6×, in proportion with the change in $(V_{\mathrm{GS}}-V_{\mathrm{TH}})^2$, leading to a value of 62 A, as observed in Fig. 4.

A revised trade-off curve obtained by using the peak SC currents from Fig. 4 is shown in red in Fig. 18. It can be observed that the heating of the Si EMM during the SC event degrades the trade-off curve between I_{SC} and R_{on}. Based on this degraded trade-off curve, a t_{SC} of 10 μs cannot be achieved by using the Si EMM selected for this work because the peak SC current cannot be reduced to 50 A. However, a saturation current of 50 A can be obtained at $V_{\mathrm{GS}} = 10$ V by using the Infineon IRL60HS118 Si Power MOSFET [18] to achieve a $t_{\mathrm{SC}} = 10\ \mu$s. According to its datasheet, the $I_{\mathrm{D,SAT}}$ does not change with temperature up to 175^0 C preventing a rise in the SC current due to heating of the Si EMM. This device has an $R_{\mathrm{DS,ON}} = 13$ mΩ at $V_{\mathrm{GS}} = 10$ V, which is an increase of only 8% over the $R_{\mathrm{DS,ON}}$ of the SiC power MOSFET. It is therefore possible to achieve a $t_{\mathrm{SC}} = 10\ \mu$s using the BaSIC(EMM) approach, although the 6.5 μs reported in this work may be sufficient.

B. Dynamic Characteristics

The rate of change of voltage for a SiC power MOSFET during turn-ON or turn-OFF switching transients is directly affected by the presence of a series resistance R_S [17]

$$\frac{dV_{\mathrm{DS}}}{dt}\,(\text{with } R_S) = \frac{dV_{\mathrm{DS}}}{dt}\,(\text{without } R_S) - \frac{I_{\mathrm{ON}} R_S}{R_G C_{\mathrm{GD}}\,(V_{\mathrm{DS}})} \tag{4}$$

where I_{ON} is the switching current, $C_{\mathrm{GD}}(V_{\mathrm{GS}})$ is the gate-drain capacitance at the drain supply voltage V_{DS}, and R_G is the external gate resistance. The addition of the series resistance from the Si EMM slows down the drain voltage transient during turn-ON, as observed in Fig. 12, which increases the turn-ON energy loss, as shown in Table III. Using a lower gate drive voltage in Cases 3a, 3b, and 3c also increases turn-ON losses. A smaller gate drive voltage reduces the current supplied to charge C_{RSS}(SiC) during the turn-ON transient [17]. This produces longer V_{DS}(SiC) transition times, resulting in an increased switching loss, as shown in Table III.

Switching performance for power MOSFETs can be improved by employing a Kelvin connection at the source [19], [20]. The Kelvin connection decreases the impact of source lead inductances in the package and board. A Kelvin connection can also be used in the BaSIC(EMM) approach by adding an extra lead from the source of the Si EMM device. A low inductance between the source of the SiC power MOSFET and the drain of the Si EMM can be achieved by soldering the drain of the Si EMM to the source of the SiC power MOSFET, producing vertically stacked devices encapsulated in a single case.

C. Sense Node Voltage

The drain terminal of the Si EMM can be used as a sense node (see Fig. 2) to monitor the ON-state current and to detect SC events. The voltage drop across the Si EMM (V_{SENSE}) during ON-state operation is proportional to the current because it operates in the linear region. Monitoring V_{SENSE} allows the determination of the ON-state current flowing through the SiC power MOSFET. The measured waveform of the sense node voltage V_{SENSE} during a double-pulse switching cycle is shown in Fig. 19. V_{SENSE} has a value of about 100 mV at a current of 10 A and about 200 mV at a current of 18 A.

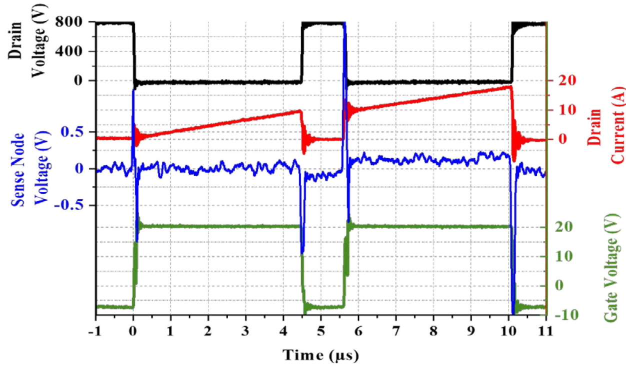

Fig. 19. Measured waveforms for double-pulse test showing the sense voltage behavior during normal operation for the case of composite MOSFET CM-5.7.

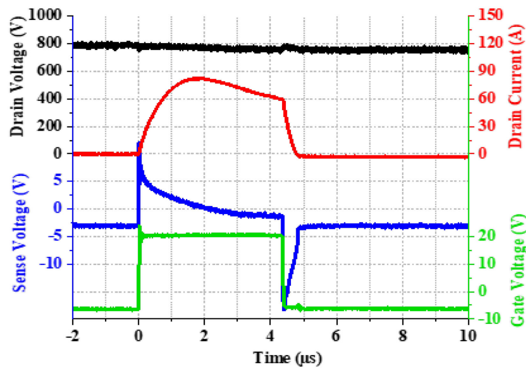

Fig. 20. Measured waveforms including the sense voltage behavior during SC conditions.

During the SC conditions, the EMM enters its current saturation regime. Consequently, the voltage drop across its drain-source terminals increases substantially (from 0.1 V to 5–6 V). The measured waveform of the sense node voltage under an SC pulse is shown in Fig. 20 for the composite MOSFET case CM-6. The sense voltage V_{SENSE} spikes to 10 V after initiating the SC event before reaching 5 V (above its value before the SC event) at 1 μs. The much larger value for V_{SENSE} compared with ON-state values of under 0.2 V can be detected using level crossing logic for fast detection of the SC event and shutting down the gate drive before device failure.

D. SiC Power MOSFET Reliability

The Si EMM operates as a resistance of about 10 mΩ during ON-state and switching operations, with the voltage drop across it opposing the gate drive of the SiC power MOSFET. In high-frequency applications, the SiC power MOSFET drain undergoes a *dv/dt* of about 10 kV/μs during switching transients. Referring to Fig. 11, this *dv/dt* will generate a current through the output capacitance of the SiC power MOSFET. A current of 8.2 A will occur based on a worst case output capacitance of 820 pF (see Table II). The Si EMM operates in its ON-state during normal circuit operation with a resistance of 10 mΩ. The voltage drop produced by the *dv/dt* transient current through the Si EMM is therefore small ($\sim$0.1 V). Consequently, the small voltage spikes across the Si EMM due to circuit *dv/dt* transients are not expected to impact the operation of the SiC MOSFET or its reliability.

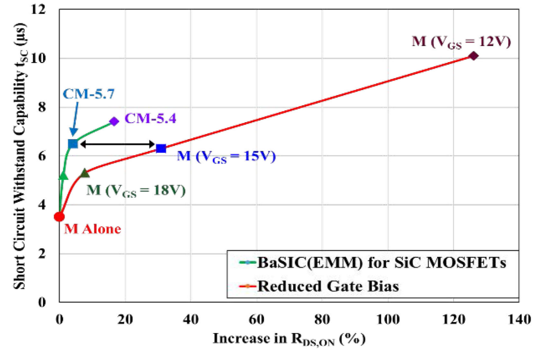

Fig. 21. Trade-off curves for the measured SC withstand time against the measured increase in $R_{\mathrm{DS,ON}}$ for the two methods.

E. SC Performance Trade-Off Curves

From the measured data in Section III, it has been demonstrated that both the BaSIC(EMM) topology and SiC MOSFET gate drive voltage reduction approach can be used to improve the SC time for a 1.2-kV SiC power MOSFET. Both methods were found to produce an increase in ON-state resistance and switching losses. Trade-off curves between increase in SC time and increase in ON-resistance and switching energy loss allow comparing their relative performance.

The trade-off curve between the measured SC time t_{SC} and the measured increase in ON-resistance for the two approaches is plotted in Fig. 21. It is apparent that the BaSIC(EMM) topology produces a much better trade-off curve compared to using a reduced gate bias. In particular, the BaSIC(EMM) topology increases the SC time to 6.5 μs with only 4% increase in ON-resistance, while a similar value for SC time is achieved for a reduced gate bias of 15 V with 31% increase in ON-resistance, as indicated by the black arrow in Fig. 21. The percent increase in ON-resistance is a factor of 8$\times$ smaller for the BaSIC(EMM) case.

The trade-off curve between the measured SC time t_{SC} and the measured total switching loss for the two approaches is plotted in Fig. 22. A much better trade-off curve is again achieved with the BaSIC(EMM) topology compared to the reduced gate bias case. In particular, the BaSIC(EMM) topology increases the SC time to 6.5 μs with only 13% increase in total switching loss while a similar value for SC time is achieved for a reduced gate bias of 15 V with 31% increase in switching loss, as indicated by the black arrow. The percent increase in switching loss is a factor of 2.4$\times$ smaller for the BaSIC(EMM) case.

A comparison between improving the SC capability with the BaSIC(DMM) topology and the reduced gate bias method was previously reported [14]. The BaSIC(DMM) topology utilizes a gate-source-shorted Si depletion-mode-MOSFET in series with the SiC power MOSFET. The performance of this approach was adjusted by paralleling the DMM devices. It was found that the SC time was increased by a factor of 1.65$\times$ with 17% increase

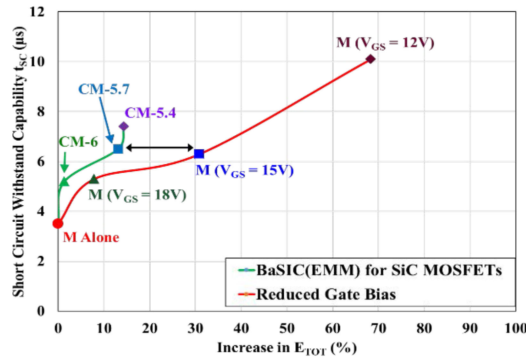

Fig. 22. Trade-off curves for the measured SC withstand time against the measured increase in switching loss for the two methods.

in ON-resistance. The results reported in this article demonstrate that even superior results can be achieved with 1.86× increase in SC time with only 4% increase in ON-resistance with the BaSIC(EMM) topology. In addition, the BaSIC(EMM) topology allows the end user to program the dc gate bias on the Si EMM device to achieve any desired SC time.

V. Conclusion

Experimental data have been presented on the relative performance of two methods to enhance the SC capability of 1.2-kV SiC power MOSFETs. The first method employs a reduced gate drive voltage applied to the SiC power MOSFET. The second method utilizes a novel BaSIC(EMM) topology with a Si enhancement mode MOSFET whose dc gate bias can be configured by the user to reduce the SC current. The BaSIC(EMM) implementation achieved a 1.86× increase in t_{SC} with only 4% increase in ON-resistance and 13% increase in total switching energy loss. In comparison, the reduced gate bias method achieved a 1.8× increase in t_{SC} with a 31% increase in ON-resistance and 31% increase in total switching energy loss.

It was also demonstrated that the BaSIC(EMM) topology can be used to monitor ON-state current levels and to detect SC events by using the Si EMM drain electrode as a voltage sense terminal. The voltage at this terminal remains below 10 V under ON-state, switching, and SC conditions allowing simplified interface with control circuits compared with the commonly used DESAT detection method. Device manufacturers can implement the BaSIC(EMM) topology as a copackaged module containing the SiC power MOSFET and the Si EMM device to simplify implementation in commercial circuit boards.

The BaSIC(EMM) implementation can be scaled to higher current SiC power MOSFET applications. It was demonstrated in this work that a 10-mΩ Si EMM is satisfactory for use with a 10-A SiC power MOSFET. Si EMM devices (e.g., Infineon IRF40SC240 product) with ON-resistance of 0.5 mΩ are commercially available [21]. They could be used to scale up the current to 200 A. SiC modules with high-current handling capability are built using multiple SiC power MOSFET dies packaged in parallel. A Si EMM die with appropriate ON-resistance could be placed in series with each of the SiC dies within the module to enhance the SC ruggedness using the BaSIC topology.

References

[1] B. J. Baliga, "Silicon carbide power devices: A 35 year journey from conception to commercialization," in *Proc. 76th Device Res. Conf.*, Santa Barbara, CA, USA, 2018, pp. 1–2.

[2] A. Bolotnikov *et al.*, "Overview of 1.2 kV – 2.2 kV SiC MOSFETs targeted for industrial power conversion applications," in *Proc. IEEE Appl. Power Elect. Conf. Expo.*, Charlotte, NC, USA, 2015, pp. 2445–2452.

[3] K. Han, A. Kanale, B. J. Baliga, B. Ballard, A. Morgan, and D. C. Hopkins, "A new short circuit failure mechanism for 1.2 kV 4H-SiC power MOSFETs and JBSFETs," in *Proc. 6th IEEE Workshop Wide Bandgap Power Devices Appl.*, Atlanta, GA, USA, 2018, 108–113.

[4] A. Kanale, K. Han, B. J. Baliga, and S. Bhattacharya, "Superior short circuit performance of 1.2 kV SiC JBSFETs compared to 1.2 kV SiC MOSFETs," *Mater. Sci. Forum*, vol. 963, pp. 797–800, Jul. 2019.

[5] X. Huang *et al.*, "Design and fabrication of 3.3 kV SiC MOSFETs for industrial applications," in *Proc. IEEE 6th Int. Symp. Power Semicond. Devices ICs*, Sapporo, Japan, 2017, pp. 255–258.

[6] B. J. Baliga, U.S. Patent Applied and Pending.

[7] Z. J. Shen and S. P. Robb, "Design and modeling of the 600 V IGBT with emitter ballast resistor," in *Proc. 53rd Annu. Device Res. Conf. Dig.*, Charlottesville, VA, USA, 1995, pp. 108–109.

[8] H. Hagino, J. Yamashita, A. Uenishi, and H. Haruguchi, "An experimental and numerical study on the forward biased SOA of IGBTs," *IEEE Trans. Electron Devices*, vol. 43, no. 3, pp. 490–500, Mar. 1996.

[9] C. Yun, S. Kim, Y. Kwon, and T. Kim, "High performance 1200 V PT IGBT with improved short-circuit immunity," in *Proc. 10th Int. Symp. Power Semicond. Devices ICs*, Kyoto, Japan, 1998, pp. 261–264.

[10] P. M. Shenoy, G. M. Dolny, and A. Bhalla, "The influence of body effect on the short-circuit ruggedness of emitter ballasted IGBTs," in *Proc. 13th Int. Symp. Power Semicond. Devices ICs*, Osaka, Japan, 2001, pp. 311–314.

[11] A. Kanale and B. J. Baliga, "Enhancing short circuit capability of 1.2 kV SiC power MOSFETs using a gate-source-shorted Si depletion-mode MOSFET in series with the source," in *Proc. IEEE 13th Int. Conf. Power Elect. Drive Syst.*, Toulouse, France, 2019, pp. 1–6.

[12] A. Kanale and B. J. Baliga, "Comparison of current suppression methods to enhance short circuit capability of 1.2 kV SiC power MOSFETs: A new approach using a series-connected, gate-source-shorted Si depletion-mode MOSFET vs use of a series resistance," in *Proc. 7th IEEE Workshop Wide Bandgap Power Devices Appl.*, Raleigh, NC, USA, 2019, pp. 53–58.

[13] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 6th ed. London, U.K.: Oxford University Press, 2009.

[14] A. Kanale and B. J. Baliga, "Comparison of current suppression methods to enhance short circuit capability of 1.2 kV SiC power MOSFETs: A new approach using a series-connected, gate-source-shorted Si depletion-mode MOSFET vs reduced gate bias operation," in *Proc. 45th Annu. Conf. IEEE Ind. Elect. Soc.*, Lisbon, Portugal, 2019, pp. 51140–5119.

[15] Information on Product webpage, Rev. D, Oct. 2019. [Online]. Available: https://www.wolfspeed.com/c2m0160120d

[16] Information on Product webpage, ver. 01_00, Sep. 2016. [Online]. Available: https://www.infineon.com/cms/en/product/power/mosfet/20v-800v-automotive-mosfet/20v-40v-n-channel-automotive-mosfet/ipi70n04s4-06/

[17] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*, 2nd ed. New York, NY, USA: Springer-Science, 2018.

[18] Information on Product webpage, ver. 03_01, Dec. 2019. [Online]. Available: https://www.infineon.com/cms/en/product/power/mosfet/12v-300v-n-channel-power-mosfet/irl60hs118/

[19] C. G. Stella, M. Laudani, A. Gaito, and M. Nania, "Advantage of the use of an added driver source lead in discrete power MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Fort Worth, TX, USA, 2014, pp. 2574–2581.

[20] V. Crisafulli, "A new package with Kelvin source connection for increasing power density in power electronics design," in *Proc. 17th Eur. Conf. Power Electron. Appl.*, Geneva, Switzerland, 2015, pp. 1–8.

[21] Information on Product webpage, ver. 01_00, Jun. 2019. [Online]. Available: https://www.infineon.com/cms/en/product/power/mosfet/12v-300v-n-channel-power-mosfet/irf40sc240/