A New Single-Input Multioutput Interleaved High Step-Up DC–DC Converter for Sustainable Energy Applications

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***Abstract*—In this article, a new single-input multioutput high step-up dc–dc converter is proposed, which is suitable for sustainable energy applications. Basically, the presented converter consists of an interleaved and a modified single-ended primary inductor converter, which uses coupled-inductor and switched-capacitor-voltage-multiplier techniques. Each stage generates a different output voltage using only one input voltage source and one duty ratio. The output voltage gains are effectively increased at low duty ratios by employing coupled-inductors and voltage multiplier cells. Moreover, because of using low voltage rated MOSFETs, the voltage stresses on power switches are very low. Therefore, the conduction losses are reduced and the conversion efficiency will be improved. In order to lighten the reverse recovery problems of the output diodes, the leakage inductance of the coupled inductors can be beneficial. The maximum efficiency that is achieved by the proposed converter is 97.5% and 96.2%, respectively, for both output loads. The operating principles and steady-state analysis are discussed in detail. Finally, experimental results for a prototype of the proposed topology that is implemented under 24 V for input voltage source, 286 and 390 V, respectively, for both output ports are presented to assess the effectiveness of the proposed converter.**

***Index Terms*—Coupled inductor, high step-up converter, interleaved operation, single-input multioutput (SIMO), voltage multiplier.**

I. Introduction

RECENTLY, applications of sustainable energy sources such as photovoltaics, wind, and fuel cells have largely increased and so many researchers investigate on these topics. Green energies have lots of benefits such as cleanness, being silent, usable in small and large scales, not necessity of import from other regions, and so on [1], [2]. However, these energies have some restrictions like low level of output voltage and high input current ripple [3], [4]. Therefore, high step-up dc–dc converters are needed to operate as an interface between the renewable sources with low voltage and the output loads, which will lead to high voltage gain [5].

Conventional boost converters can raise the output voltage gain with high duty ratios, although the achieved voltage gain is forced by the parasitic components as the forward voltage drop ($V_{\rm FD}$), rectifier diodes' ON-state resistance (r_D), and also the equivalent series resistance (ESR) of capacitors and inductors. Furthermore, owing to strong switching and output diode reverse recovery losses, the efficiency is drastically reduced [6], [7]. To develop the voltage gain and conversion ratio as well as eliminate and or make the mentioned problems lower, a few high step-up converters have been presented that can be noted [8]–[11]. The recommended converter in [8] without employing any magnetic devices such as transformer can increase the output voltage gain, but due to using high number of switches to boost the voltage level, its structure is complicated. In [9] a high step-up converter has been proposed. In this structure, a classic single-ended primary inductor converter (SEPIC) has been integrated with an extended switched capacitor (SC) converter, which improves the output voltage gain, but owing to no inductor at the input side, the input current ripple is almost high. Moreover, the value of duty ratio is far up, which increases power losses and cuts the efficiency down. A switched-capacitor-inductor passive stage has been utilized to grow the voltage gain, which has been proposed in [10]. However, the input current is discontinuous, so it is not possible to boost the output voltage. A high voltage gain dc–dc converter employing SC and a dual switch has been recommended in [11]. High output voltage gain at a low duty ratio is the leading benefit of this converter, but the normalized voltage stress on the output diodes is pretty high, which affects the efficiency. Other types of converters are mainly combination of the mentioned structures.

High-frequency transformers as isolated converters can be a selection in renewable energy applications, but the obtained high output voltage gain as a result of high leakage inductance increases the voltage stress on power devices [12]–[15].

Recently, nonisolated high step-up dc–dc converters are used very much. Broadly speaking, nonisolated converters have simple structure and compact size. The means on the literature are categorized in two sections: noncoupled inductor means including cascade, SC, and voltage lift techniques; and coupled

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inductor means [16]–[19]. In this article, the coupled inductor means are studied.

The coupled-inductor converters are really helpful to get high step-up voltage gain. However, because of the leakage inductance in their structure, there is a high voltage spike on active power switches at turn-OFF intervals. As a result, a clamp circuit is required to recycle the leakage energy. The clamp technique is able to accomplish soft switching for active switches and enhance the efficiency [20]. The presented topologies in [21] and [22] have been integrated with Dickson multiplier cell and capacitor-diode, respectively. However, owing to the mentioned reasons, both converters have low efficiency as well as pulsating input current will cause electromagnetic interference difficulties, especially in [22], because of high number of active power switches, the structure and its control are complicated. In some cases, the input current ripple is low, but the current stress path through the components at high power levels is almost high, which leads to a decrease in the efficiency [23], [24]. Normally, the interleaving technique is an appropriate way to reduce the input current ripple [25].

In this article, a new interleaved high step-up dc–dc converter with single-input multioutput (SIMO) is proposed, which is a suitable topology for high step-up applications in renewable energy systems. In the topology of the introduced converter, there are two outputs belonging to an interleaved and a SEPIC converter. Both of them by employing coupled-inductor and voltage-multiplier techniques produce high level of output voltage. The proposed converter has continuous input current with low ripple due to use of interleaved connection. By employing low voltage rated MOSFETs with low conduction resistor, the power losses are decreased and following that the efficiency will be improved. Generally, it can be said that the purpose of the converter is to create multiple ports at the output by increasing the power level and reducing losses on the semiconductors. Therefore, the proposed topology is a good candidate for renewable energy applications.

II. Topology of the Proposed Converter and Operational Principles

A. Converter Topology

The proposed SIMO interleaved high step-up dc–dc converter is shown in Fig. 1. Overall, in the configuration of the interleaved part, two coupled inductors as parallel-input and series-output along with a linking voltage multiplier cell to one of the output loads are connected to each other. The parallel-input connection plays the role of an energy storage and a transfer device, whereas the series-output connection and the voltage multiplier cell are used to achieve high voltage gain at low duty ratios. Moreover, the output voltage gain of the SEPIC stage is improved by adopting a coupled-inductor and two voltage multiplier modules.

As explained, the utilized three coupled-inductors store and release the energy into capacitors and output loads R_{L1} and R_{L2}. According to these coupled inductors, the magnetizing and leakage inductors are named as L_{m1}, L_{m2}, L_{m3} and L_{k1}, L_{k2}, L_{k3}, respectively. The diodes D_7 and D_8 along with the secondary windings of two input coupled inductors and also the SCs C_{o21} and C_{o22} form a voltage multiplier module. In addition, there is another voltage multiplier pack, which includes two voltage multipliers as D_3, C_3, D_4, C_4 and the coupled inductor of the SEPIC part. This coupled inductor with the capacitor C_1 and the diode D_2 make a clamp circuit to recycle its leakage energy. The diodes D_1, D_5, and D_6 are used to transfer the energy to the output capacitors C_{o24}, C_{o23}, and C_{o1}, respectively. The power switches S_1 and S_2 operate based on interleaved method with 180° phase shift and the same duty ratio in a switching period. The duty ratio of the switches (D) must be greater than 0.5 in order to work in step-up mode.

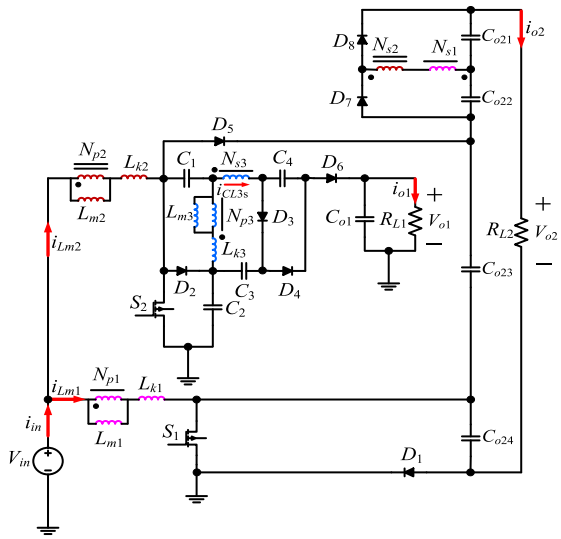


Fig. 1. Circuit configuration of the proposed converter.

B. Operation Modes

The suggested converter has ten operation modes in a switching period and it is analyzed under continuous conduction mode (CCM). Figs. 2 and 3 show the operation modes of the proposed converter. Moreover, the key waveforms under CCM during a switching period are presented in Fig. 4. In order to study operation modes simply, some assumptions are considered as follows.

1) The employed power components are totally assumed ideal. Thus, the efficiency will be 100%.
2) The input voltage is a dc source.
3) All capacitors and inductors are large enough with no fluctuations in the voltage of capacitors and the current inductors.
4) Turns ratio of the CL_3 in the SEPIC stage is $n_1 = N_{s3}/N_{p3}$.
5) For input coupled inductors, their turn's ratios are equal as $n_2 = N_{s1}/N_{p1} = N_{s2}/N_{p2}$.

Mode 1 [t_0–t_1]: At the beginning of this mode, the switch S_1 is turned ON under zero current switching (ZCS), whereas the switch S_2 is in the ON-state as well. The inductors L_{k3}, L_{m3} and the capacitor C_1 are charged by C_2. Secondary side current of the CL_3 (i_{CL3s}) and the capacitor C_3 charge the capacitor C_4 through the diode D_4. The current i_{Lk1} grows

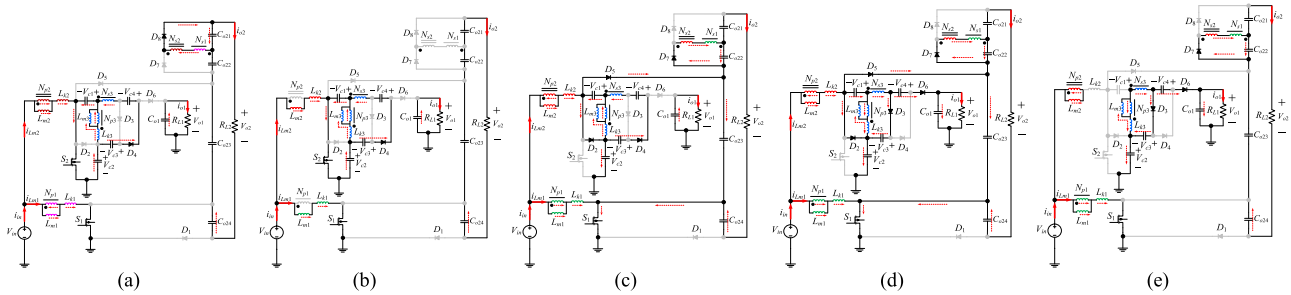


Fig. 2. Operation modes of the proposed converter under CCM. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5.

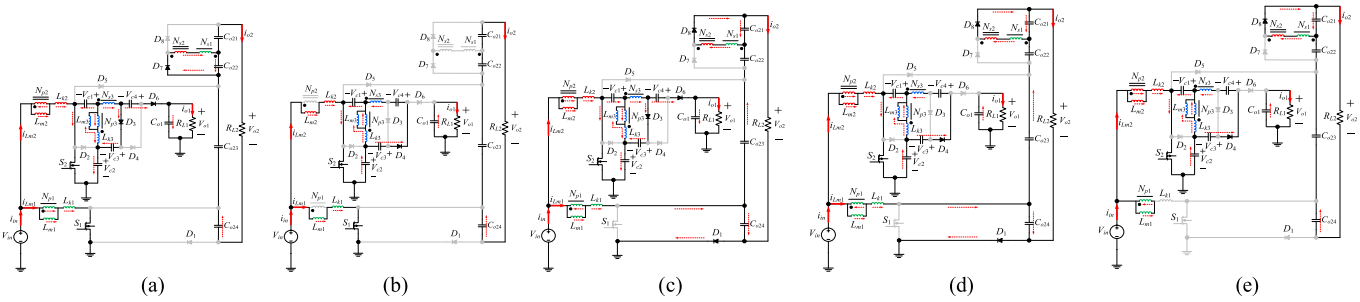


Fig. 3. Operation modes of the proposed converter under CCM. (a) Mode 6. (b) Mode 7. (c) Mode 8. (d) Mode 9. (e) Mode 10.

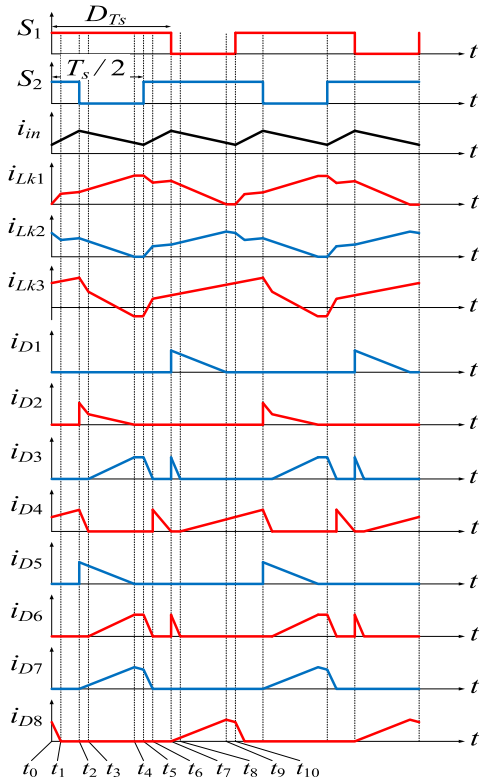


Fig. 4. Key waveforms of the proposed converter under CCM.

rapidly, but its increase rating is controlled and restricted by L_{k1}. The energy stored in L_{m1} is transferred to the load side and charge C_{o21} through the diode D_8 if $i_{Lk1} < i_{Lm1}$. Fig. 2(a) shows the equivalent circuit of this mode.

Mode 2 [t_1–t_2]: In this mode at t_1, both switches S_1 and S_2 are conducting. Thus, the output diodes are turned OFF, and the loads are just charged by output capacitors, as shown in Fig. 2(b). The magnetizing inductors L_{m1} and L_{m2} and the leakage inductors L_{k1} and L_{k2} are charged linearly by the input voltage source. Similar to mode 1, C_3 charges the capacitor C_4 via D_4 and also the capacitor C_2 charges L_{k3}, L_{m3}, and C_1. Therefore, the following equations can be written for current and voltage of capacitors:

$$i_{C1} = i_{Lm3} + (n_1 + 1)i_{D4} = -i_{C2} \tag{1}$$

$$i_{C4} = i_{D4} = -i_{C3} \tag{2}$$

$$V_{C4} = V_{C3} + (n_1 + 1)(V_{C2} - V_{C1}). \tag{3}$$

The voltage across L_{m3} equals

$$V_{Lm3} = V_{C2} - V_{Lk3,m2} - V_{C1} \tag{4}$$

where $V_{Lk3,m2}$ is the voltage across L_{k3} during mode 2. The voltage and current equations of L_{k3} are described as

$$\begin{cases} V_{Lk3,m2} = \frac{i_{Lk3}(t_2) - i_{Lk3}(t_1)}{DT_s} L_{k3} \\ i_{Lk3} = i_{Lm3} + n_1 i_{D4}. \end{cases} \tag{5}$$

Mode 3 [t_2–t_3]: At the beginning of this mode, S_2 is turned OFF, which causes to conduct the diodes D_2, D_5, and D_7, as shown in Fig. 2(c). The energy stored in L_{m2} is moved to the load side and charges the capacitor C_{o22} via the diode D_7. The leakage inductor L_{k2} is discharged into the capacitors C_2 and C_{o23} through the diodes D_2 and D_5, respectively. The voltage stress on S_2 is clamped by C_{o23}. The capacitor C_3 charges the capacitor C_4 via D_4. The magnetizing inductor L_{m3} and the capacitor C_1 are fed by the leakage inductor L_{k2}. In other words,

the energy stored in L_{k3} is recycled to C_1 through the diode D_2. Thus, the following equations can be used:

$$i_{D2} = i_{Lk2} + i_{Lk3} - i_{CL3s} - i_{D5} \tag{6}$$

where i_{CL3s} is the secondary side current of CL_3 and is expressed as

$$\begin{cases} i_{CL3s} = -i_{D4} \\ i_{CL3s} = (i_{Lm3} - i_{Lk3})/n_1 \end{cases} \tag{7}$$

$$i_{Lk3} = \frac{1}{L_{k3}} \int_{t_2}^{t_3} \left(-V_{C1} + \frac{V_{C3} - V_{C4} - V_{C1}}{n_1} \right) dt. \tag{8}$$

Due to low value of L_{k3} and its high negative voltage, the slope of its current must be high. Therefore, this mode will be too small.

Mode 4 [t_3–t_4]: In this mode, the current of magnetizing inductor L_{m3} is larger than the current of leakage inductor $L_{k3}(i_{Lk3} < i_{Lm3})$, so based on (7) the current direction of the coupled inductor is altered and D_3 is turned ON. The diode D_6 is also turned ON and sent the energy stored in C_4 to the output load of SEPIC stage. The diode D_2 still keeps recycling the energy stored in L_{k3} to C_1. The following equations can be written for the currents flowing through the capacitors and the diodes:

$$i_{C1} = -(i_{Lk2} - i_{D2} - i_{D5}) \tag{9}$$

$$i_{C4} = -i_{D6} = i_{Co1} - i_{o1} = i_{C2} - i_{Lk2} \tag{10}$$

$$i_{D2} = i_{Lk2} + i_{Lm3} - i_{D5} - (n_1 + 1)(i_{D3} + i_{D6}). \tag{11}$$

As shown in Fig. 2(d), in the proposed structure, C_3 is parallel with both sides of the coupled inductor (CL_3), although in many common voltage multiplier converters, the secondary side of coupled inductors is merely parallel with capacitors. As a result, in the introduced converter, the voltage of capacitor C_3 is grown and increases V_{o1}. The magnetizing inductor L_{m2} charges the capacitor C_{o22}, whereas the inductors L_{m1} and L_{k1} are fed by the input source. At the end of this mode, i_{Lk2} reduces to zero and when it accurately becomes zero, the diode D_5 is turned OFF as well. The following equations are obtained in this mode of operation:

$$V_{Lk2} = V_{\text{in}} - V_{C2} \tag{12}$$

$$V_{Lm3} = -V_{C1} - V_{Lk3,m4} \tag{13}$$

where $V_{Lk3,m4}$ is the voltage of L_{k3} during mode 4 and is obtained by

$$\begin{cases} V_{Lk3,m4} = \frac{i_{Lk3}(t_4) - i_{Lk3}(t_3)}{d_4 T_s} L_{k3} \\ i_{Lk3} = i_{Lm3} + (-n_1 i_{D3}). \end{cases} \tag{14}$$

In recent equation, $d_4 T_s$ is the length of mode 4

$$V_{C3} = (n_1 + 1)V_{C1} + n_1 V_{Lk3,m4} \tag{15}$$

$$V_{o1} = V_{C2} + V_{C3} + V_{C4} \tag{16}$$

$$V_{o2} = V_{Co21} + V_{Co22} + V_{Co23} + V_{Co24}. \tag{17}$$

Mode 5 [t_4–t_5]: At the beginning of this mode, i_{Lk2} diminishes to zero and makes the diodes D_2 and D_5 turned OFF. The capacitor C_1 is open circuit as well. Therefore, there are not any reverse recovery problems for the diodes D_2 and D_5, as shown in Fig. 2(e). The capacitor C_4 is discharged to R_{L1}. In addition, the capacitor C_3 is fed analogous with mode 4 because of being parallel with both sides of CL_3. The capacitor C_2 is charged by the recycled energy of the leakage inductor L_{k3}. According to Fig. 2(e), the current of S_1 equals the summation of i_{Lm1} and i_{Lm2}. Thus, the following equations can be written for this mode:

$$i_{CL3s} = i_{Lk3} = \frac{i_{Lm3}}{n_1 + 1} \tag{18}$$

$$i_{S1} = i_{Lm1} + i_{Lm2}. \tag{19}$$

Mode 6 [t_5–t_6]: In this mode, the switch S_2 is turned ON under ZCS and the leakage inductor L_{k2} is charged by the input source, whereas the switch S_1 is in the ON-state as well, as shown in Fig. 3(a). Thus, the current of L_{k2} is increased. Furthermore, the current of the leakage inductor L_{k3} is grown quickly and its equation is obtained by

$$i_{Lk3} = \frac{1}{L_{k3}} \int_{t_5}^{t_6} \left(V_{C2} - V_{C1} + \frac{V_{o1} - V_{C1} - V_{C4}}{n_1} \right) dt. \tag{20}$$

Owing to high voltage of L_{k3} and low inductance, its current slope will get upward. As a result, the length of this mode is extremely small.

The energy stored in the magnetizing inductor L_{m2} is still transferred to the output side and charges the capacitor C_{o22} through the diode D_7 if $i_{Lk2} < i_{Lm2}$. i_{D7} is going to zero and it is limited by L_{k1} and L_{k2}, losses of which get lightened. When i_{D7} becomes zero completely, this mode is finished.

Mode 7 [t_6–t_7]: In this mode, S_1 and S_2 are in ON-state and no energy is transferred to the output loads. As shown in Fig. 3(b), this mode is precisely similar with mode 2. Therefore, it is avoided repeating it.

Mode 8 [t_7–t_8]: The switch S_1 is turned OFF under ZCS, whereas S_2 is in ON-state. As shown in Fig. 3(c), the diodes D_1, D_3, D_6, and D_8 are turned ON. The magnetizing inductor L_{m1} sent its energy to the output side and charges the capacitor C_{o21} through D_8. The current i_{Lk1} is reduced because of charging C_{o24}. The capacitors C_1 and C_4 transmit their energy to the load, but C_2 and C_3 are charged. The inductors L_{m2} and L_{k2} are storing energy during this mode.

Mode 9 [t_8–t_9]: Based on Fig. 3(d), the diodes D_3 and D_6 are switched OFF, which make the capacitors C_3 and C_4 discharged and charged, respectively. The energy of C_{o24} is supplied by L_{k1}. The energy of L_{m1} is transferred to the output side. L_{k3}, L_{m3}, and C_1 are charged during this mode.

Mode 10 [t_9–t_{10}]: During this mode, the current of L_{k1} becomes zero and the diode D_1 is turned OFF as well, which is shown is Fig. 3(e). The magnetizing inductor L_{m1} is still released its energy to charge of C_{o21} and the output load R_{L2}. The inductors L_{m2} and L_{k2} consume total energy of V_{in}. It means that the current of S_2 equals the summation of the currents flowing through L_{m1} and L_{m2}. Thus

$$i_{S2} = i_{Lm1} + i_{Lm2}. \tag{21}$$

At the end of this mode, one switching period is completed, meaning the switch S_1 is turned ON and the next switching cycle is started.

III. Steady-State Analysis

In order to simplify the steady-state analysis of the introduced topology under CCM, the operation modes 1, 3, 6, and 8 are neglected because they are very small intervals. In this section, both voltage gains of the proposed converter are calculated and then, voltage stress on power devices is obtained.

A. Voltage Gain of the SEPIC Stage

The voltage of the capacitors C_1 and C_2 is achieved by using volt-second balance on the inductors

$$V_{C1} = \frac{D}{1-D}V_{\text{in}} - DV_{Lk3,m2} - \left(\frac{n_1}{n_1+1}\right)\left(d_4 + \frac{(1-D-d_4)}{1-D}\right)V_{Lk3,m4} \quad (22)$$

$$V_{C2} = \frac{V_{\text{in}}}{1-D} - \left(\frac{n_1}{n_1+1}\frac{(1-D-d_4)}{1-D}\right)V_{Lk3,m4}. \quad (23)$$

By applying volt-second balance on the leakage inductor L_{k3} and ignoring turn-OFF and turn-ON modes of S_2 meaning modes 3 and 6, respectively, the following equations are achieved:

$$V_{Lk3,m2}DT_s + V_{Lk3,m4}d_4T_s = 0 \quad (24)$$

$$V_{Lk3,m2} = -\frac{d_4}{D}V_{Lk3,m4}. \quad (25)$$

By substituting (22) and (25) in (15), the voltage of C_3 is computed as follows:

$$V_{C3} = \frac{(n_1+1)D}{1-D}V_{\text{in}} + d_4V_{Lk3,m4} - \left(\frac{1-D-d_4}{1-D}\right) \times n_1V_{Lk3,m4} + n_1V_{Lk3,m4}. \quad (26)$$

The voltage of the capacitor C_4 is obtained by using (3), (15), (22), and (23) as

$$V_{C4} = \frac{(n_1+1)}{1-D}V_{\text{in}} - \left(\frac{1-D-d_4}{1-D}\right)n_1V_{Lk3,m4} + n_1V_{Lk3,m4}. \quad (27)$$

By replacing (23), (26), and (27) in (16), we obtain

$$V_{o1} = M_1V_{\text{in}} + \left(\left[-\frac{(1-D-d_4)}{1-D}\right]\left[\frac{n_1}{n_1+1} + 2n_1\right] + d_4 + 2n_1\right)V_{Lk3,m4} \quad (28)$$

$$M_1 = \frac{V_{o1}}{V_{\text{in}}} = \frac{n_1+2+(n_1+1)D}{1-D} \quad (29)$$

where M_1 is the voltage gain of the SEPIC stage of the proposed converter.

B. Voltage Gain of the Second Stage

The two input coupled inductors are assumed identical and then, their coupling coefficient (k) will be equal obviously. Therefore, based on this fact $L_{m1} = L_{m2} = L_m$, $L_{k1} = L_{k2} = L_k$, and $k = L_m/(L_m + L_k)$.

The voltage of capacitors C_{o23} and C_{o24} is similar to the traditional boost converters

$$V_{Co23} = V_{Co24} = \frac{V_{\text{in}}}{1-D}. \quad (30)$$

According to the operation modes and (30), the voltage of capacitors C_{o21} and C_{o22} is expressed as

$$V_{Co21} = N_{s2} - N_{s1} = n_2kV_{Co24} = \frac{n_2k}{1-D}V_{\text{in}} \quad (31)$$

$$V_{Co22} = N_{s1} - N_{s2} = n_2kV_{Co23} = \frac{n_2k}{1-D}V_{\text{in}}. \quad (32)$$

By replacing (30)–(32) in (17), the second stage voltage gain of proposed converter M_2 is obtained when $L_k << L_m$ as

$$M_2 = \frac{V_{o2}}{V_{\text{in}}} = \frac{2n_2+2}{1-D}. \quad (33)$$

C. Voltage Stress on Power Devices

The voltage stress on power components such as switches, diodes, and capacitors is achieved based on operation modes and voltage gains. Hence, the voltage across switches and diodes is given by

$$V_{S1} = V_{S2} = \frac{V_{\text{in}}}{1-D} = \frac{V_{o2}}{2n_2+2} \quad (34)$$

$$V_{D1} = V_{D2} = \frac{V_{o2}}{2n_2+2} \quad (35)$$

$$V_{D3} = V_{D4} = V_{D6} = \frac{(n_1+1)}{1-D}V_{\text{in}} = \frac{(n_1+1)V_{o1}}{n_1+2+D(n_1+1)} \quad (36)$$

$$V_{D5} = V_{Co23} + V_{Co24} = \frac{V_{o2}}{n_2+1} \quad (37)$$

$$V_{D7} = V_{D8} = V_{Co21} + V_{Co22} = \frac{n_2V_{o2}}{n_2+1}. \quad (38)$$

The voltage stress on capacitors is computed by

$$V_{C1} = \frac{D}{1-D}V_{\text{in}} = \frac{DV_{o1}}{n_1+2+D(n_1+1)} \quad (39)$$

$$V_{C2} = \frac{V_{\text{in}}}{1-D} = \frac{V_{o1}}{n_1+2+D(n_1+1)} \quad (40)$$

$$V_{C3} = \frac{(n_1+1)D}{1-D}V_{\text{in}} = \frac{(n_1+1)DV_{o1}}{n_1+2+D(n_1+1)} \quad (41)$$

$$V_{C4} = \frac{(n_1+1)}{1-D}V_{\text{in}} = \frac{(n_1+1)V_{o1}}{n_1+2+D(n_1+1)}. \quad (42)$$

IV. Design Guidelines of the Proposed Converter

In this section, the utilized power devices are designed in order that the introduced converter works appropriately. It is evident that there are some drawbacks when the proposed converter operates in discontinuous conduction mode (DCM) such as low dynamic response, high current stress on inductors according to the value of frequency, and low output voltage

TABLE I
COMPARISON OF THE PROPOSED CONVERTER WITH SOME OTHER STRUCTURES

Converter Topology	Voltage Gain	Voltage Stress on Switch	Voltage Stress on Diodes	Input Current Ripple/magnitude [%]	Number of Devices				Efficiency (%)	Cost [$]
					Switch	Diode	Capacitor	Coupled Inductor		
Proposed Converter	$\frac{n_1+2+(n_1+1)D}{1-D}$	$\frac{V_{o1}}{n_1+2+(n_1+1)D}$	$\frac{(n_1+1)V_{o1}}{n_1+2+D(n_1+1)}$	low/1.2%	2	8	8	3	97.5	$38.30
	$\frac{2n_2+2}{1-D}$	$\frac{V_{o2}}{2(n_2+1)}$	$\frac{n_2V_{o2}}{n_2+1}$						96.2	
[2]	$\frac{n+1}{1-D}$	$\frac{V_o}{n+1}$	$\frac{nV_o}{n+1}$	low/4%	1	3	3	1	94	$32.46
[4]	$\frac{n+1}{1-D}$	$\frac{V_o}{n+1}$	$\frac{nV_o}{n+1}$	low/5%	1	3	3	1	96	$45.88
[6]	$\frac{1+nD}{1-D}$	$\frac{V_o}{1+nD}$	$\frac{nV_o}{1+nD}$	high/21%	1	4	1	1	91.7	$29.85
[18]	$\frac{1+2n+nD}{1-D}$	$\frac{V_o}{1+2n+nD}$	$\frac{nV_o}{1+2n+nD}$	low/12.8%	1	5	5	1	93.2	$41.94
[19]	$\frac{2+nD}{1-D}$	$\frac{V_o}{2+nD}$	$\frac{V_o(n+1)}{2+nD}$	high/25%	1	3	6	1	92	$47.72
[21]	$\frac{1+n(1+D)}{1-D}$	$\frac{V_o}{1+n(1+D)}$	$\frac{nV_o}{1+n(1+D)}$	low/18%	1	4	3	1	91	$30.99
[23]	$\frac{n+2+(n+1)D}{1-D}$	$\frac{V_o}{n+2+D(n+1)}$	$\frac{(n+1)V_o}{n+2+D(n+1)}$	low/10%	1	4	4	1	93.5	$34.14

gain. Hence, the performance of the suggested topology in CCM is more improved than DCM. As a result, its components are designed under CCM.

A. Design of Inductors

The proposed converter operates in CCM when half of all the current ripples of inductors become less than their average current values. Based on this fact, by assuming $I_{Lm}\ I_{\rm in}/2$, both input inductors ($L_{m1}=L_{m2}=L_m$) are obtained by

$$L_m=\frac{DV_{\rm in}}{\Delta i_{Lm}f_s}. \tag{43}$$

The average current of L_{m3} is computed by applying ampere-second balance on the capacitor C_1 as

$$I_{Lm3}=(n_1+1)I_{o1} \tag{44}$$

$$L_{m3}=\frac{DV_{\rm in}}{\Delta i_{Lm3}f_s} \tag{45}$$

where Δi_{Lm3} and f_s are the ripple of the inductor L_{m3} and the switching frequency, respectively.

B. Design of Capacitors

By neglecting ESR of capacitors, the amounts of capacitors are expressed as

$$C_1\geq\frac{1}{2}\frac{V_{o1}D^2}{(1-D)\Delta V_{C1}R_{L1}f_s} \tag{46}$$

$$C_2\geq\frac{1}{2}\frac{V_{o1}D}{(1-D)\Delta V_{C2}R_{L1}f_s} \tag{47}$$

$$C_3\geq\frac{1}{2}\frac{(n_1+1)V_{o1}D^2}{(1-D)\Delta V_{C3}R_{L1}f_s} \tag{48}$$

$$C_4\geq\frac{1}{2}\frac{(n_1+1)V_{o1}D}{(1-D)\Delta V_{C4}R_{L1}f_s} \tag{49}$$

where ΔV_C is the voltage ripple of capacitors. The values of output capacitors are calculated by

$$C_{o1}\geq\frac{DV_{o1}}{\Delta V_{Co1}f_sR_{L1}} \tag{50}$$

$$C_{o2}=4C_{o21}\geq\frac{DV_{o2}}{\Delta V_{Co2}f_sR_{L2}}. \tag{51}$$

C. Restrictions of Turns Ratios

Turn ratio is a very significant parameter in nonisolated converters due to its effect on semiconductors. For the presented topology, there are two turns ratios that using (29) and (33) are expressed as

$$n_1\geq\frac{V_{o1}(1-D)}{V_{\rm in}(1+D)}-\frac{2+D}{1+D} \tag{52}$$

$$n_2\geq\frac{V_{o2}}{2V_{\rm in}}(1-D)-1. \tag{53}$$

V. COMPARISON STUDIES

In order to describe the performance of the proposed converter, it should be compared with some other topologies. Table I lists the features of the proposed converter and a few of the similar structures. It is apparent from the information supplied that the input current of the introduced converter is in CCM and it has low ripple. Thus, the voltage gain and efficiency are increased. Consequently, it will be more appropriate for renewable energy applications. The comparison is provided in similar conditions as far as possible. Based on Table I, the input current ripple of the proposed converter is low compared to other topologies, which is nearly 1%. In terms of the total cost, although the proposed converter is high-priced, because of using passive elements with lower rating it is able to transfer high levels of power with low power losses. Furthermore, the presented system has a good reliability and it can be used for different applications as well as in comparison with other topologies,

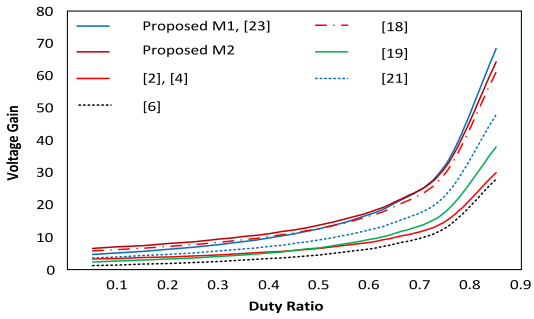


Fig. 5. Voltage gain of the proposed converter in comparison with similar topologies.

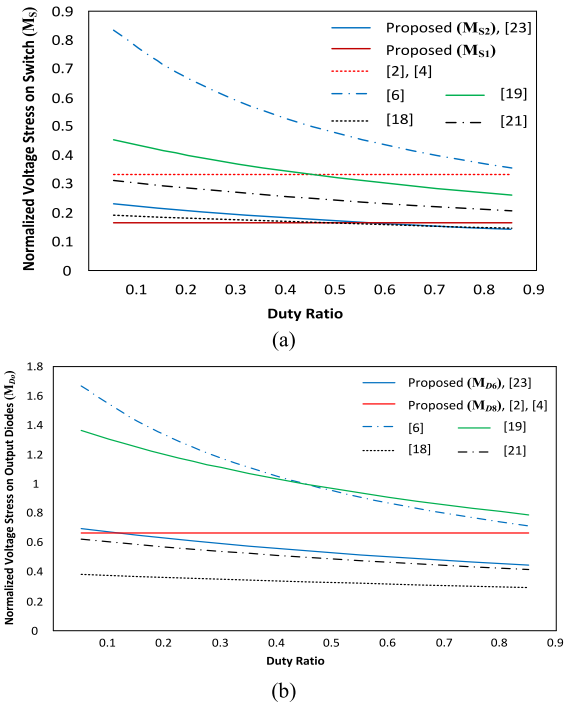


Fig. 6. Variations of normalized voltage stress on (a) power switches and (b) diodes.

the proposed converter has improved efficiency despite that converters with high number of components usually have lower efficiency. As a result, flexibility of the suggested topology is more than the others from the commercial viewpoint.

In Fig. 5, the voltage gains of all the converters are seen. As shown in this figure, the first output voltage gain of the proposed topology (M_1) is similar to the suggested converter in [23], and is greater than the others at high duty ratios. Afterward, the second voltage gain (M_2) has higher value and is slightly greater than the output voltage gain presented in [18]. The voltage stress variations on power switches and diodes are shown in Fig. 6(a) and (b), respectively. Based on Fig. 6(a), the normalized voltage stresses on both power switches are almost identical, but M_{S2} the normalized voltage stress under the effect of M_1 has the lowest value like [23]. The normalized voltage stress under the effect of M_2 (M_{S1}) has a little higher value than M_{S2}, but it is approximately equal to M_{S1}. Therefore, the low voltage stress on switches causes low switching losses and high efficiency.

TABLE II
SPECIFICATIONS OF THE IMPLEMENTED PROTOTYPE

Parameter	Value
Input voltage (V_{in})	24V
Output voltages (V_{o1} & V_{o2})	286V & 400V
Output powers (P_{o1} & P_{o2})	300W & 380W
Duty ratio (D)	0.64
Switching frequency (f_s)	40kHz
Turns ratio of coupled-inductors (n_1 & n_2)	(1&2)/Ferrite core EE 55/28/21
Magnetizing inductors (L_{m1}=L_{m2} & L_{m3})	640μH & 1920μH
Leakage inductors	1.5μH
Capacitors (C_1, C_2, C_3, C_4)	330μF/200V
Output capacitors (C_{o1} & C_{o21}= ⋯ =C_{o24})	470μF/450V & 330μF/250V)
Diodes	MUR1560
Power switches	IRFP260

A glance at Fig. 6(b) provided reveals that the normalized voltage stress on one of the output diodes of the proposed converter using $M_1(M_{D6})$ is the same as the proposed topology in [23], although it is not the lowest one; it is a bit greater than the proposed converter in [21]. By employing M_2, the normalized voltage stress on D_8, the second output diode of the proposed converter (M_{D8}) is higher than M_{D6}, whereas it is lower than the presented converters in [6] and [19]. As a result, the small voltage stress on output diodes reduces the reverse recovery problems and conduction losses and also increases the efficiency in both output ports.

Generally, a multioutput system has less efficiency. However, in the proposed converter, the efficiency in both outputs is high because according to the mentioned issues, the voltage stress on power components is very lower than V_{o1} and V_{o2}. Thus, the proposed topology has low power losses and acceptable performance on gain enhancement technology overall.

VI. EXPERIMENTAL RESULTS

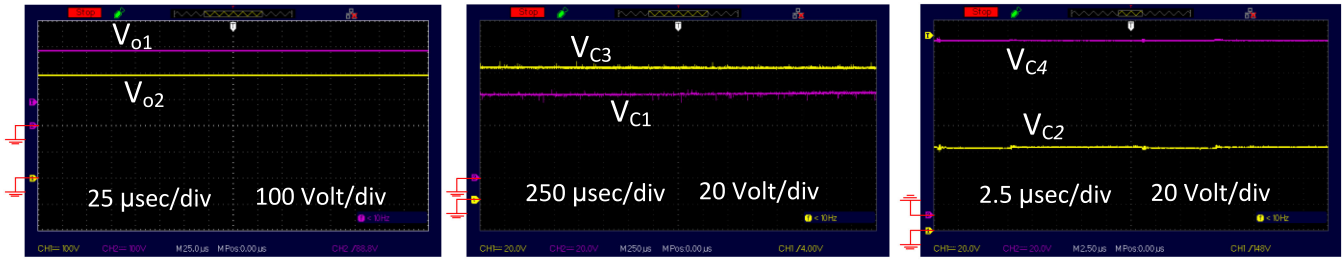
A. Specifications of Components and Converter

In order to evaluate the theoretical studies and performance of the proposed SIMO converter, a prototype with 300 W for load 1 and 380 W for load 2 is carried out in laboratory. Table II illustrates the values of the employed power elements for the prototype version.

The presented converter boosts the input voltage with amount of 24–286 V in load side 1 (V_{o1}) and 390 V in load side 2 (V_{o2}), respectively. Based on the design considerations, both power switches have the same duty ratios, which is chosen 0.64. In addition, in order to decrease the passive devices' volume, the value of switching frequency will be 40 kHz. A microcontroller ATMEGA16 is used to generate two pulse signals for the power switches. All diodes are MUR1560, which have low forward voltage drop ($V_{\rm FD}$) as well as the two power switches have low ON-state resistance ($R_{dS\text{-on}}$) for small voltage stress; in this case, the selected switches are IRFP260. All three utilized coupled inductors are ferrite cores EE 55/28/21 with 0.2 mm air gap.

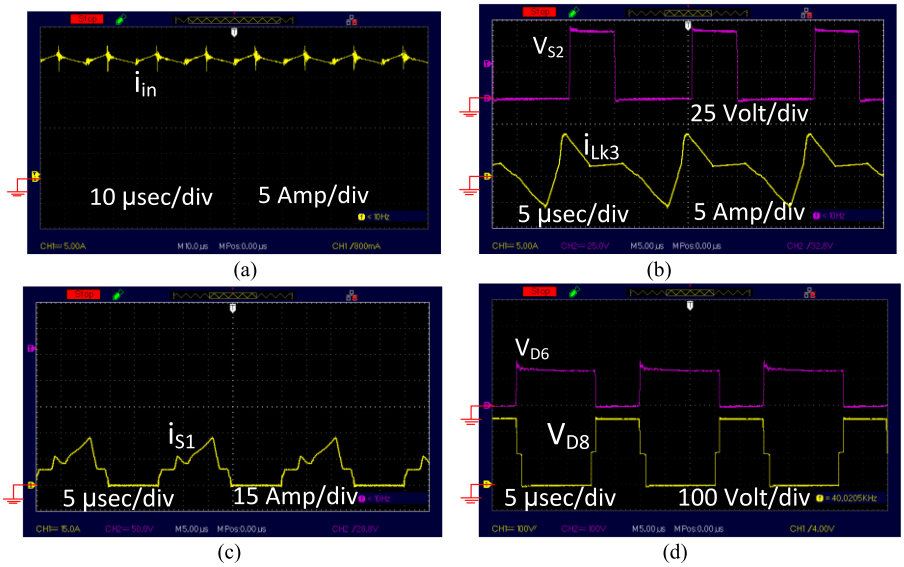
B. Set-Up Results

Fig. 7(a) presents the output voltage for two loads. According to this figure, the output voltage of the SEPIC part is about 285.6 V, whereas for the second stage, the output voltage is almost 390 V with very low fluctuations. Furthermore, the



(a) (b) (c)

Fig. 7. (a) Output voltages. (b) Voltage of capacitors C_1 and C_3. (c) Voltage of capacitors C_2 and C_4.



(a) (b) (c) (d)

Fig. 8. (a) Input current of the proposed converter. (b) Voltage of S_2 and the current of L_{k3}. (c) Current of S_1. (d) Voltage across diodes D_6 and D_8.

voltage of capacitors C_1 and C_3 is shown in Fig. 7(b), whereas Fig. 6(c) describes the voltage of capacitors C_2 and C_4. These capacitors all are named as mid-capacitors. Based on Fig. 6(b) and (c), the voltage across capacitors C_1, C_2, C_3, and C_4 is 43.3 V with 5.7% ripple, 67.5 V with 3.3% ripple, 82.7 V with 3.3% ripple, and 131.6 V with 0.6% ripple, respectively. The voltage ripples of all four capacitors are extremely low. In other words, their voltage is almost constant. The input current of the proposed converter is illustrated in Fig. 8(a), which equals about 27.4 A and has a ripple of 1.2%. In Fig. 8(b), the current of the leakage inductor L_{k3} is seen. The maximum point of it is almost 8 A. Also, the voltage of S_2 is 68 V approximately and it is the same as the voltage of S_1, which is indicated in Fig. 8(b) too. Fig. 8(c) shows the current passing through the power switch S_1, which is about 27 A and is identical with the input current. The voltage across output diodes D_6 and D_8 is illustrated in Fig. 8(d).

According to this figure, the voltage of D_6 is about 135 V, whereas the voltage of D_8 is almost 255 V; both parameters are smaller than V_{o1} and V_{o2}, respectively. Based on the theoretical and experimental results, the input current ripple of the proposed topology is very low due to using interleaved technique. In addition, the voltage stress on semiconductors is small, which causes the proposed converter has low losses and high efficiency. As a result, according to the mentioned issues, the proposed system has suitable operation for high step-up applications. Fig. 9 illustrates the laboratory prototype of the proposed converter.

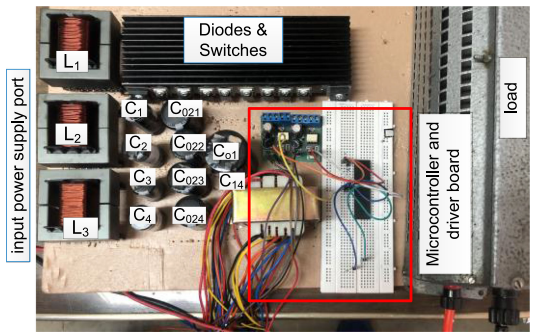


Fig. 9. Laboratory prototype of the proposed converter.

VII. Conclusion

In this article, a new SIMO high step-up dc–dc converter was presented. The suggested converter is suitable for sustainable energy applications. The proposed converter has ten operation

modes in a switching cycle, which were theoretically analyzed in mathematical. Afterward, two different voltage gains were obtained for two output ports and then all parameters were designed using them. In order to ensure that the proposed converter has good qualifications, it was compared with some similar topologies. Finally, a prototype of the recommended converter was constructed under 300 and 380 W to assessment of its work and relevant experimental results were presented as well. According to theoretical and experimental results, the proposed converter has low input current ripple (1.2%), low voltage stress on power components, low power losses, high gain, and high efficiency (97.5% and 96.2%). Therefore, this topology can be a satisfactory structure for applications of sustainable energies.

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