A New Approach to Model Reverse Recovery Process of a Thyristor for HVdc Circuit Breaker Testing

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***Abstract*—In the HVdc circuit breaker testing process, a thyristor is used to generate high current for the testing purpose. However, the reverse recovery process (RRP) of a thyristor can induce a significant overvoltage problem, which jeopardizes the reliable operation. It is important to model the RRP of a thyristor. The existing modeling methods usually omit the stray inductances in the circuit, which cannot describe the hard-switching process accurately. Therefore, this article proposes a novel method to model the RRP, considering the stray inductances. There are mainly three original contributions. First, the physical mechanism of the RRP is analyzed, describing the internal charge behavior and dividing the RRP into two stages. Second, this article provides a novel trigonometric exponential (TE) model of the thyristor voltage and current with analytical equations. Third, the extraction method of model parameters is also provided based on external circuit parameters and thyristor characteristics. In order to verify the proposed modeling method, a 1 kV/830 A IGBT-based circuit breaker is implemented with a thyristor to initialize the current. The experimental results show that the negative peak voltage induced by the RRP is as high as 4.26 kV, and the proposed TE model can precisely predict the overvoltage with a relative error of 7.51%.**

***Index Terms*—DC breaker, reverse recovery process (RRP), thyristors.**

I. Introduction

COMPARED with the traditional ac grids, the flexible dc transmission technology has a significant technical advantage in the integration and long-distance transmission of renewable energy [1], [2]. However, the low resistance of the transmission system could lead to a rapid rising fault current in the flexible dc grid. When overhead lines are implemented, the probability of temporary faults at the dc side will be significantly increased. Therefore, fast and reliable removal strategies of faults should be provided [3].

High-voltage dc circuit breakers (HVdc CBs) with fast response speed are effective in fault protection and have been steadily applied in flexible dc power grid projects [4]–[7]. For example, the Zhoushan 200-kV five-terminal grid and the Nan'ao 160-kV three-terminal grid have installed HVdc CBs [8], [9]. The Zhangbei 500 kV grid will be equipped with 16-HVdc CBs with different topologies [10].

Conducting the current interruption test for HVdc CBs is an indispensable part of the CBs development because the most important function of HVdc CBs is to clear the rising-current fault as quickly as possible to protect the power grid. For example, the 500-kV hybrid dc circuit breaker and its semiconductors need to turn OFF a pulse fault current up to 25 kA. Therefore, it is necessary to establish a high-current and high-reliability testing platform to validate the turn-off feature of HVdc CBs.

Due to the high current capability, thyristors have been widely applied in pulse power units [11]–[12], thyristor controlled series compensation [13], high-voltage dc converter valves [14], [15], and high-current rectifiers for ac motors [16], [17]. They are also being used in the HVdc CBs applications. For example, the current interruption test circuit requires a thyristor to control the testing process [18], [19], and the forced commutation unit of HVdc CBs requires thyristors to achieve zero current switching [20], [21].

This article aims to address a common issue in HVdc CBs. It focuses on the overvoltage caused by the reverse recovery process (RRP) of a thyristor in the current interruption test circuit. The circuit is defined in the standard MIL-STD-750D [22], which contains a thyristor and an *LC* resonance. In HVdc CBs, the overvoltage could cause a potential dielectric breakdown, resulting in aging and damages of semiconductor devices. In addition, it increases the power losses of the turn-OFF process, lowering efficiency. Therefore, it is necessary to model the RRP of a thyristor and accurately estimate the overvoltage, which can be used to guide the component selection and calculate the turn-OFF losses. Moreover, it can be further extended to analyze the inverter side commutation failure and the dynamic voltage distribution of the HVdc valve [14], [23].

Recently, the exponential function based model has been widely used to describe the RRP of a thyristor [24]– [26]. The

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current of a thyristor is generally fitted based on the empirical formula, which is simple but lacks accuracy. Waldmeyer and Backlund [27] and Chokhawala and Carroll [28] proposed a scant hyperbolic model. It creates a nicely rounded current peak, which matches some particular measurements. However, the time constant is not provided. In Zhang *et al.* [29], a thyristor is treated as a time-varying resistor, and its resistance is fitted into a logistic curve, which reflects the reverse recovery characteristics of a thyristor. But this model relates to external circuit parameters and needs to be retuned for different parameters.

In addition, Shenai [30]– [32] adopted the finite element analysis method to simulate the PPR of a thyristor. It usually requires physical parameters and geometric structures, such as the doping profile and ambipolar lifetime, which are challenging to acquire from the manufacturer. Ma *et al.* [33]–[35] proposed a lumped charge model based upon Linvill's lumped parameter approach and the standard charge method to describe the dynamic change of the internal charge during the RRP, maintaining simplicity for the fast simulation. Nevertheless, the impact of the external circuit on the RRP is not considered. In contrast, Yue *et al.* [36] analyzed the effect of the external circuit on the RRP based on experiments. However, the proposed analytical current expression does not consider external circuit parameters, such as inductance.

Therefore, this article proposed a novel method to model the RRP of a thyristor in the HVdc CBs test circuit, which accurately predicts the overvoltage issue. The innovative contributions of this article are summarized in three aspects.

First, the physical mechanism of the RRP is analyzed as the reference to divide the RRP into multiple stages. Different stages correspond to different processes of the charge behavior inside the thyristor. For each stage, the equivalent *RC* parameters are extracted separately to maintain the accuracy to describe the RRP.

Second, the trigonometric exponential (TE) model is proposed to describe the transient process, which also includes the external inductance. The inductance resonates with the equivalent capacitance and directly affects the current varying rate. This article clearly validates that the inductance should be considered to predict the overvoltage more accurately.

Third, based on the proposed TE model, the parameter extraction method is also provided in detail, in order to find the equivalent parameter values in different stages. For a specific thyristor, a low-power experiment can be conducted to acquire the *V-I* curve during RRP. Then, the parameter extraction method can be applied to establish the thyristor model, which can be further used to predict the overvoltage in different high-power scenarios.

An experimental prototype is implemented to realize a current interruption test circuit. Experimental results validate that the proposed model can accurately predict the overvoltage up to 4.26 kV, and the relative error is within 7.51%.

II. Physical Mechanism of RRP

A. Testing Circuit for HVdc Circuit Breaker

In an HVdc CB, an IGBT submodule is usually used as the switching device, which consists of an IGBT and a snubber capacitor C_s. To study the response of a circuit breaker to a rising-current fault, it is necessary to conduct the current interruption experiment, as shown in Fig. 1 [37]. The working principle is based on an *LC* resonant circuit controlled by the thyristor and IGBT. In Fig. 1(a), the function of each device is explained as follows:

1) capacitor bank C_m is precharged as the dc power source;
2) inductor L_m resonates with C_m to generate rising-current;
3) thyristor triggers the rising process of the current;
4) IGBT works as the main body of a circuit breaker;
5) metal oxide varistor (MOV) is used to limit the voltage across the IGBT module within its restriction voltage $V_{\rm res}$.

According to Fig. 1(b), the working process of the testing circuit is explained as follows.

1) Initially, the capacitor bank C_m is precharged to the desired value, which could be as high as a few kilovolts.
2) At T_1, turn ON the IGBT, and pay attention that there is no current flowing in the circuit as the thyristor is not ON.
3) At T_2, turn ON the thyristor, and the current in the circuit starts to rise.
4) At T_3, the current reaches the peak value in the ON-state stage. Turn OFF the IGBT to test its fault protection performance, and the current starts to decrease and charge the snubber capacitor of IGBT. When V_{Cs} exceeds the MOV operating voltage, the current commutates to MOV until the voltage reaches the limit $V_{\rm res}$.
5) At T_4, the current decreases to zero, the thyristor starts to turn OFF, the RRP begins, the IGBT voltage remains $V_{\rm res}$ until the snubber capacitor is discharged.
6) In Fig. 1(a), the thyristor works in a hard-switching mode with no parallel snubber, so there is a significant overvoltage during the RRP, which is the primary focus of this article.

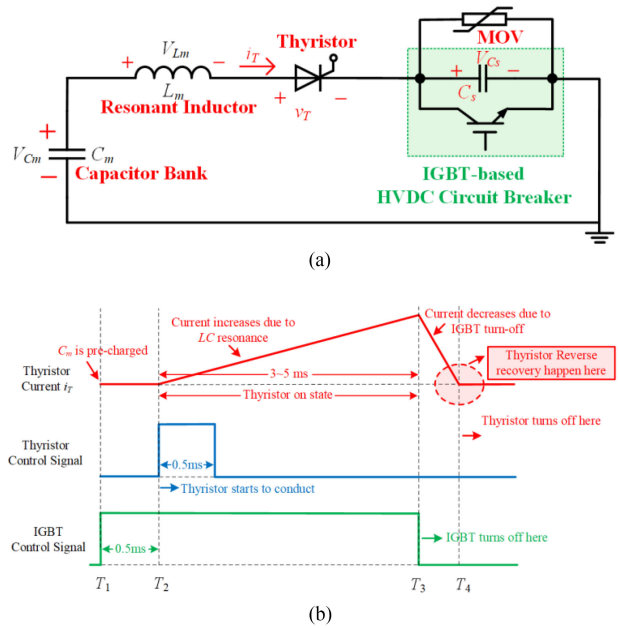


Fig. 1. Current interruption circuit and control of testing an HVdc circuit breaker. (a) Schematic of current-interruption circuit for HVdc circuit breaker. (b) Time sequencing of control signals to show working principle.

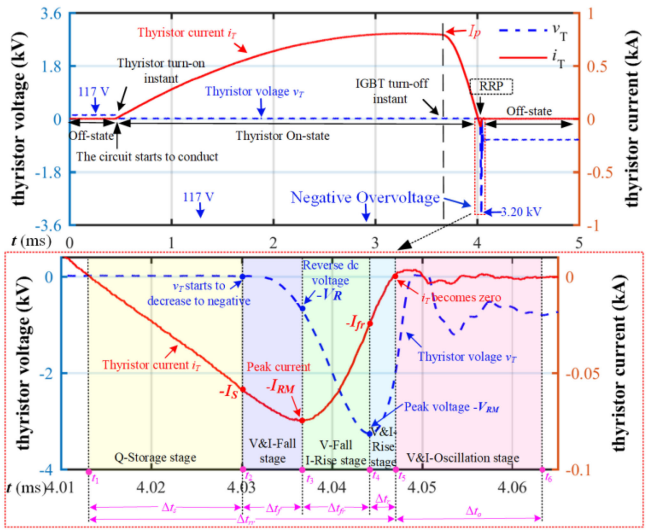


Fig. 2. Example of measured voltage and current waveforms during RRP.

TABLE I
DEFINITION OF SPECIFIED PARAMETERS IN FIG. 2

i_T	Thyristor current	V_{RM}	Peak voltage during RRP
I_s	Current at the end of Q-storage	Δt_s	Duration of Q-storage stage
I_p	Peak current during on-state	Δt_f	Duration of V&I-fall stage
I_{RM}	Peak current during PPR	Δt_{fr}	Duration from $-I_{RM}$ to $-V_{RM}$
I_{fr}	Current at the end of V-fall I-rise	Δt_r	Duration from $-V_{RM}$ to I_r
v_T	Thyristor voltage	Δt_{rr}	Entire RRP $\Delta t_{rr}=\Delta t_s+\Delta t_f+\Delta t_{fr}+\Delta t_r$
V_R	Input reverse dc voltage	Δt_o	Duration V&I-oscillation stage

B. Working Principle of the Thyristor RRP

Based on Fig. 1(a), a prototype of the HVdc circuit breaker is implemented to conduct the current interruption experiment. The measured waveforms are shown in Fig. 2, which is consistent with the analysis in Fig. 1(b). The details of the RRP are also presented in an enlarged figure, which clearly shows the negative overvoltage problem of the thyristor.

In Fig. 2, the transient process is divided into five stages: Q-storage stage, V&I-fall stage, V-fall I-rise stage, V&I-rise stage, and V&I oscillation stage. The specified currents and voltages are also illustrated, and their definitions are provided in Table I. The working process during the RRP of the thyristor is described as follows.

1) At t_1, i_T Gradually Decreases to Zero. The Junction J_1 Dominates, and the Thyristor Enters the "Q-Storage Stage": The thyristor is a four-layer p-n-p-n device consisting of three p-n junctions (J_1, J_2, and J_3) [38]. In the normal ON-state, there is a high concentration of free carriers in the *N*-drift region, maintaining a low ON-state voltage drop of the thyristor.

During RRP, the equivalent internal circuit of the thyristor is shown in Fig. 3, which is also consistent with the testing circuit in Fig. 1(a).The MOV voltage is limited as V_{Cs}, and the capacitor C_m voltage is V_{Cm}. Comparing the polarity of voltages in Fig. 1(a), and 3, the equivalent voltage source during RRP is

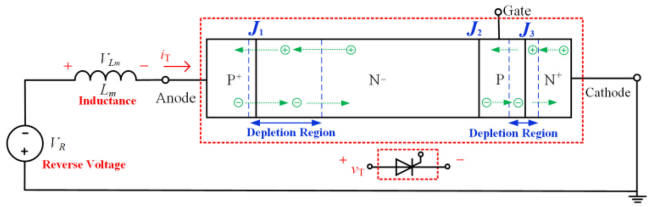


Fig. 3. Equivalent internal circuit of a thyristor during the RRP.

defined as V_R, which is given by

$$V_R = V_{Cs} - V_{Cm}. \tag{1}$$

After t_1, there are still a large number of minority carriers, and the concentration is higher than the thermal equilibrium concentration. The p-n junctions are still in a forward bias state, and the ON-state voltage drop is still very low.

In this process, the current i_T reversely increases with a constant rate di_T/dt, which is determined by external circuit parameters (e.g., V_R and L_m).

The junction J_1 dominates this process. The reverse current begins to remove the carriers in the N-region. Since the doping concentration of the P^+ region is much higher than that of the N- region, the hole injected from P^+ to N- is much more than the electron from N- to P^+, meaning the reverse current is mainly caused by the hole in N- region. The difference in concentration between the P and N- regions is small, so the junction J_2 contributes less to the reverse current. The period from t_1 to t_2 is a charge storage process for the N-region. It is called "Q-storage stage". The duration time is defined as Δt_s.

2) At t_2, i_T Continues to Decrease. The Junctions J_1 and J_3 Dominate to Form Space Charge Regions, Causing the Voltage v_T to Decrease. The Thyristor Enters the "V&I-Fall Stage": As shown in Fig. 3, when the reverse current i_T flows, extra charges are extracted from the depletion regions of J_1 and J_3, forming the space charge regions. As the space charge region increases, the thyristor gradually recovers the reverse blocking capability and the external impedance increases. Then, the rate di_T/dt decreases. Since v_T decreases, the process is defined as "V&I-Fall stage," and the duration time is defined as Δt_f.

3) At t_3, di_T/dt is Zero, Current i_T Reaches the Peak Value $-I_{RM}$, and the Thyristor Undertakes the Reverse Voltage $-V_R$. The Thyristor Enters the "V-Fall I-Rise Stage": After t_3, the junction J_2 starts to dominate the process, and additional holes accumulate in the N-region. The reverse current i_T starts to increase from a negative value back to zero. According to Fig. 3, the thyristor voltage v_T is expressed as

$$v_T(t) = -V_R - L_m \cdot di_T/dt. \tag{2}$$

It clearly shows that the voltage stress of the thyristor is determined by three factors: the voltage V_R, the inductance L_m, and the current varying rate di_T/dt. The voltage across the inductor L_m also contributes to the thyristor voltage. In this process, the current varying rate di_T/dt increases, resulting in a high voltage across the inductance and the peak voltage V_{RM} across the thyristor at the end of this stage. Since v_T is falling

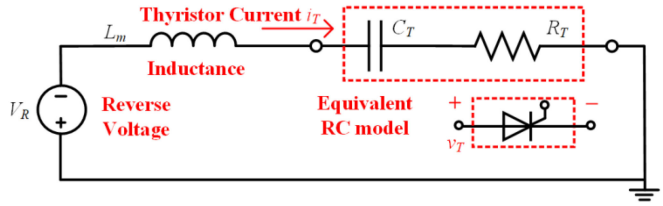


Fig. 4. Equivalent *RC* model of a thyristor during the RRP.

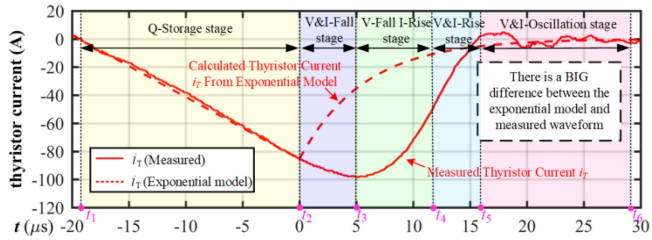


Fig. 5. Comparison of the measured current with the exponential model.

while i_T is rising, this process is defined as the "V-Fall I-Rise stage." The duration time is Δt_{fr}, which is from $-I_{\rm RM}$ to $-V_{\rm RM}$.

4) At t_4, v_T Reaches Peak Value $-V_{RM}$, and it Reaches $-I_{fr}$, the Thyristor Enters the "V&I-Rise Stage": After t_4, additional holes continue accumulating in the N-region, v_T starts to increase, and i_T still increases in this stage. v_T could also be expressed by (2). Due to both v_T and i_T rising in this stage, this process is defined as "V&I-Rise stage," and the duration time is Δt_r.

5) At t_5, the Thyristor Current i_T Reaches Zero. The Thyristor Reaches the Reverse Blocking State, and the RRP Ends. The Thyristor Enters the "V&I-Oscillation Stage": After t_5, the oscillation of v_T is due to the resonance between L_m and the parasitic capacitance. It is called "V&I-oscillation stage." In Fig. 2, the oscillation is much smaller than the peak voltage $V_{\rm RM}$. Then, the time interval Δt_o is not considered as part of the RRP to simplify the analysis.

To summarize, the total reverse recovery time is defined as $\Delta t_{rr} = \Delta t_s + \Delta t_f + \Delta t_{fr} + \Delta t_r$. In Fig. 2, it needs to be clarified that Δt_{rr} is from time t_1 to time t_5. The calculation range of reverse recovery charges Q_{rr} is from t_1 to t_5.

The above working mechanism clearly shows that the external inductance L_m affects both the thyristor voltage and current during the RRP. Therefore, it is vital to study the impact of L_m and investigate the analytical expressions.

III. TE Model

A. Model Description

In this section, the analytical expressions for each stage are provided to model the RRP as follows:

Q-Storage stage [t_1–t_2]: The thyristor does not have the reverse blocking capability, and the current varying rate di_T/dt remains unchanged. This stage is also called the linear stage, and i_T is expressed as

$$i_T(t) = -k\,(t - t_1)\,, t_1 < t < t_2 \tag{3}$$

where $k = di_T/dt$ represents the initial current descent rate and is determined by the external circuit parameters. At the end of this stage, the reverse current is expressed as $-I_s = -k\Delta t_s$.

Other stages [t_2–t_5]: The thyristor restores the reverse blocking capability, which is essentially the dynamic change of the depletion layer charge of a thyristor. In this process, the thyristor can be modeled as an equivalent capacitance C_T in series with a resistance R_T, as shown in Fig. 4.

According to KVL, the voltages can be given by

$$L_m \cdot di_T/dt + R_T i_T + v_{CT} + V_R = 0. \tag{4}$$

1) Exponential Model: Previously, in Revankar and Srivastava [24]–[26], the inductance L_m is usually neglected. The total stored charge of the thyristor is defined as q_T, and the relationship could be given by

$$i_T = dq_T/dt, V_{CT} = q_T/C_T. \tag{5}$$

Then, (4) is simplified as

$$dq_T/dt + q_T/\tau_T + V_R/R_T = 0 \tag{6}$$

where $\tau_T = R_T \times C_T$ indicates the minority carrier lifetime. Also, τ_T relates to the recombination process of the p-n junction and is affected by the current magnitude and junction temperature [36]. By Solving (6), i_T is calculated as below, which clearly shows that i_T is in an exponential form

$$i_T(t) = -I_s \cdot e^{-t/\tau_T}, t_2 < t < t_6. \tag{7}$$

For the example waveform in Fig. 2, the exponential model of the current can be derived. The work of Revankar and Srivastava [24] is used to extract the parameters, and the current equation is expressed as

$$i_T(t) = -I_s \cdot e^{-\frac{t}{\Delta t_s/(1.5\times\ln 10)}}, t_2 < t < t_6. \tag{8}$$

From (8), the exponential waveform of the current is shown in Fig. 5, which is compared with the measurement. It clearly shows a significant difference, which means that the conventional exponential model is not suitable to describe the thyristor current i_T during the RRP. Then, it is necessary to study a more accurate modeling method.

2) TE Model: In this article, the inductance L_m is considered. Substituting (5) into (4), the circuit is described as follows:

$$L_m \cdot \frac{d^2 q_T}{dt^2} + R_T \frac{dq_T}{dt} + \frac{q_T}{C_T} + V_R = 0. \tag{9}$$

Assuming that an underdamped condition, i.e.,

$$\sqrt{\frac{1}{L_m C_T}} > \frac{R_T}{2L_m}. \tag{10}$$

Then, solving (9), the current i_T is calculated as follows:

$$i_T(t) = C_1 e^{-At}\cos(Bt) + C_2 e^{-At}\sin(Bt) \tag{11}$$

where

$$\tau_L = \frac{L_m}{R_T}, A = \frac{1}{2\tau_L}, B = \sqrt{\frac{1}{L_m C_T} - \tau_L^2}. \tag{12}$$

In (11) and (12), C_1, C_2, A, and B relate to practical circuit parameters, which will be provided in the following section. Then, the equivalent parameters C_T and R_T of a thyristor could be calculated based on A and B.

It clearly shows that, when L_m is considered, i_T is in a TE form. It means that the thyristor current has an oscillation trend during an exponential decay process. It will affect the current waveform and the corresponding overvoltage of a thyristor in RRP. Therefore, (11) is named as a TE model. It needs to be emphasized that this TE model is more accurate than the conventional exponential model in (7), which will be verified by the following section.

B. Parameters Extraction Method

According to the previous analysis, the RRP is described by (3) and (11). Moreover, multiple parameters that need to be determined in the proposed TE model, which are explained below.

1) Q-Storage Stage [t_1, t_2]. k and I_s: In the Q-storage stage, k and I_s need to be decided. The current varying rate k is determined by the external circuit. The reverse current I_s relates to the duration time Δt_s. Therefore,

$$k = di_T/dt = V_R/L_m. \tag{13}$$

According to Revankar and Srivastava [24], Δt_s relates to the characteristic of the thyristor. The relationship between k and Δt_s will be studied in the following section, which will be able to provide Δt_s for any given external circuit parameters.

2) V&I-Fall Stage [t_2, t_3]. A_1, B_1, C_{11}, and C_{21}: During the RRP in Fig. 3, the size of the depletion layer varies in different stages. Then, the equivalent capacitance C_T and resistance R_T in Fig. 4 also change in different stages. In the V&I-fall stage, the equivalent parameters are defined as C_{T1} and R_{T1}. Correspondingly, the parameters in (11) are defined as A_1, B_1, C_{11}, and C_{21}. Therefore, the circuit model is described as follows:

$$\begin{aligned} i_T(t) = {} & C_{11}e^{-A_1(t-t_2)}\cos\left[B_1\left(t-t_2\right)\right] \\ & + C_{21}e^{-A_1(t-t_2)}\sin\left[B_1\left(t-t_2\right)\right], t_2 < t < t_3. \end{aligned} \tag{14}$$

At t_2, the initial conditions are $i_T(t_2) = -I_s$ and $i'_T(t_2) = k$. Based on (14), the parameters are given by

$$C_{11} = -I_s, C_{21}B_1 - C_{11}A_1 = -k. \tag{15}$$

At the end of this stage, $i_T(t_3) = -I_{\rm RM}$ and $i'_T(t_3) = 0$. Therefore

$$C_{11}e^{-A_1\Delta t_f}\cos\left(B_1\Delta t_f\right) + C_{21}e^{-A_1\Delta t_f}\sin\left(B_1\Delta t_f\right) = -I_{\rm RM} \tag{16}$$

$$\begin{aligned} & \left[\left(C_{21}B_1 - C_{11}A_1\right)\cos\left(B_1\Delta t_f\right)\right. \\ & \left. - \left(C_{11}B_1 + C_{21}A_1\right)\sin\left(B_1\Delta t_f\right)\right]e^{-A_1\Delta t_f} = 0. \end{aligned} \tag{17}$$

There are four independent equations from (15)–(17) for four unknown parameters: A_1, B_1, C_{11}, and C_{12}. After calculation, the current $I_{\rm RM}$ at the end of this stage could be expressed below:

$$I_{\rm RM} = -C_{11}e^{-A_1\Delta t_f}\cos\left(B_1\Delta t_f\right) - C_{21}e^{-A_1\Delta t_f}\sin\left(B_1\Delta t_f\right). \tag{18}$$

3) V-Fall I-Rise Stage [t_3, t_4]. A_2, B_2, C_{12}, and C_{22}: In the V-Fall I-Rise stage, i_T also follows the form of (11)

$$\begin{aligned} i_T(t) = {} & C_{12}e^{-A_2(t-t_3)}\cos\left[B_2\left(t-t_3\right)\right] \\ & + C_{22}e^{-A_2(t-t_3)}\sin\left[B_2\left(t-t_3\right)\right], t_3 < t < t_4. \end{aligned} \tag{19}$$

At t_3, the initial conditions are $i_T(t_3) = -I_{\rm RM}$, $i'_T(t_3) = 0$. Then, substituting into (19), it can be simplified as follows:

$$C_{12} = -I_{\rm RM}, C_{22}B_2 - C_{12}A_2 = 0. \tag{20}$$

At t_4, the current is defined as $i_T(t_4) = -I_{fr}$. According to Fig. 2 and Table I, there is $\Delta t_{fr} = t_4 - t_3$. Then, it is simplified as follows:

$$\begin{aligned} & C_{12}e^{-A_2\Delta t_{fr}}\cos\left(B_2\Delta t_{fr}\right) + C_{22}e^{-A_2\Delta t_{fr}}\sin\left(B_2\Delta t_{fr}\right) \\ & \quad = -I_{fr}. \end{aligned} \tag{21}$$

At t_4, v_T reaches the peak value, which means $v'_T(t_4) = 0$. Then, from the definition in (2), $i''_T(t_4) = 0$. Therefore

$$\begin{aligned} & \left(A_2^2C_{12} - 2A_2B_2C_{22} - B_2^2C_{12}\right)\cos\left(B_2\Delta t_{fr}\right) \\ & \quad + \left(A_2^2C_{22} + 2A_2B_2C_{12} - B_2^2C_{22}\right)\sin\left(B_2\Delta t_{fr}\right) = 0. \end{aligned} \tag{22}$$

Then, A_2, B_2, C_{12}, and C_{22} could be obtained from (20)–(22). Moreover, $-I_{fr}$ is expressed as

$$\begin{aligned} I_{fr} = {} & -C_{12}e^{-A_2\Delta t_{fr}}\cos\left(B_2\Delta t_{fr}\right) \\ & - C_{22}e^{-A_2\Delta t_{fr}}\sin\left(B_2\Delta t_{fr}\right). \end{aligned} \tag{23}$$

At t_4, the peak value of v_T is defined as $-V_{RM}$. Then, according to (2), $V_{\rm RM}$ is given by

$$\begin{aligned} V_{RM} = {} & V_R + L_m e^{-A_1\Delta t_{fr}}\left[\left(C_{22}B_2 - C_{12}A_2\right)\cos\left(B_2\Delta t_{fr}\right)\right. \\ & \left. - \left(C_{12}B_2 + C_{22}A_2\right)\sin\left(B_2\Delta t_{fr}\right)\right]. \end{aligned} \tag{24}$$

4) V&I-Rise Stage [t_4, t_5]. A_3, B_3, C_{13}, and C_{23}: In the V&I-Rise stage, i_T also follows the form of (11):

$$\begin{aligned} i_T(t) = {} & C_{13}e^{-A_3(t-t_4)}\cos\left[B_3\left(t-t_4\right)\right] \\ & + C_{23}e^{-A_3(t-t_4)}\sin\left[B_3\left(t-t_4\right)\right], t_4 < t < t_5. \end{aligned} \tag{25}$$

At t_4, the initial conditions are $i_T(t_4) = -I_{fr}$ and $v_T(t_4) = -V_{RM}$. Then, substituting into (25), it can be simplified as follows:

$$C_{13} = -I_{fr}, C_{23}B_3 - C_{13}A_3 = (V_{RM} - V_R)/L_m. \tag{26}$$

At t_4, v_T reaches a peak value, which means $v'_T(t_4) = 0$. Then, from the definition in (2), there is $i''_T(t_4) = 0$. Therefore,

$$\left(A_3^2C_{13} - 2A_3B_3C_{23} - B_3^2C_{13}\right) = 0. \tag{27}$$

At t_5, there is $i_T(t_5) = 0$. According to Fig. 2 and Table I, there is $\Delta t_r = t_5 - t_4$. Then, it is simplified as follows:

$$C_{13}e^{-A_3\Delta t_r}\cos\left(B_3\Delta t_r\right) + C_{23}e^{-A_3\Delta t_r}\sin\left(B_3\Delta t_r\right) = 0. \tag{28}$$

Furthermore, A_3, B_3, C_{13}, and C_{23} could be calculated from (26)−(28).

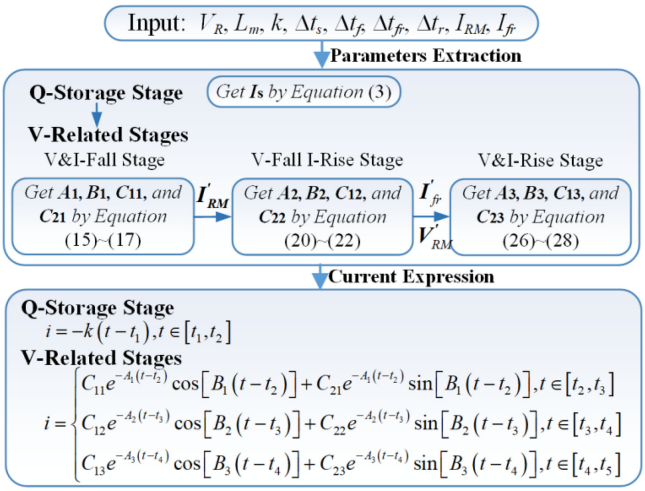


Fig. 6. Flowchart of the proposed modeling methodology of a thyristor RRP based on the TE model.

TABLE II
EXTRACTED PARAMETERS FROM WAVEFORMS IN Fig. 2

L_m (mH)	V_R (V)	k (A/μs)	Δt_s (μs)	Δt_f (μs)	Δt_{fr} (μs)	Δt_r (μs)	I_{RM} (A)	I_{fr} (A)
0.24	781.5	3.26	18.80	4.92	2.78	2.89	74.91	24.30

TABLE III
EXTRACTED TE MODEL IN THE V&I-FALL STAGE WHEN $k = 3.26$ A/μs

A_1	B_1	C_{11}	C_{21}
-7.26×10^4	9.30×10^4	-65.10	12.57

5) Summary of Parameter Extraction Process: The proposed modeling method is presented as a flowchart in Fig. 6. In a practical application, circuit parameters, such as the reverse dc voltage V_R and the inductance L_m, need to be measured, which can provide the current varying rate k. Then, an experiment can be conducted to measure the time-related parameters (Δt_s, Δt_f, Δt_{fr}, Δt_r) and current-related parameters (I_{RM}, I_{fr}). Based on the TE model in Fig. 6, the thyristor current i_T, and equivalent parameters during the RRP can be acquired.

IV. PREDICTION OF OVERVOLTAGE BASED ON THE TE MODEL

A. Parameter Extraction Through Experiments

1) Parameter Extraction With $k = 3.26$ A/μs (Based on Fig. 1): The circuit breaker in Fig. 1 is used as an example to show the parameter extraction method. The circuit parameters are designed as $L_m = 0.24$ mH and $V_R = 781.5$ V. In this example, the current varying rate $k = 3.26$ A/μs. The experimental waveforms are shown in Fig. 2. Then, according to Fig. 2, the parameters related to the RRP are extracted, as shown in Table II.

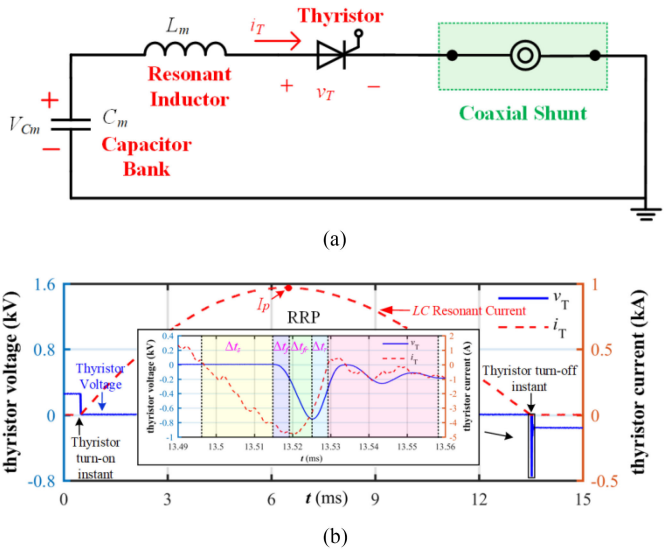
Substituting Table II into the modeling process in Fig. 6, the proposed TE model of the RRP can be derived. Then, the equivalent parameters need to be acquired to describe the current equation. The parameters in different stages are shown in Tables III, IV, and V, respectively. The tables clearly show that the thyristor parameters vary in different stages, which is caused by the change of the depletion layer of the thyristor.

TABLE IV
EXTRACTED TE MODEL IN THE V-FALL I-RISE STAGE WHEN $k = 3.26$ A/μs

A_2	B_2	C_{12}	C_{22}
4.15×10^4	1.84×10^5	-74.91	-16.88

TABLE V
EXTRACTED TE MODEL IN THE V&I-RISE STAGE WHEN $k = 3.26$ A/μs

A_3	B_3	C_{13}	C_{23}
2.41×10^5	3.86×10^5	-24.30	11.91



(a)

(b)

Fig. 7. *LC* resonant circuit based RRP testing circuit and experimental results. (a) Schematic of an *LC* resonant circuit with a coaxial shunt. (b) Experimental waveforms of the thyristor current and voltage.

2) Parameters Extraction With Various k (Based on Fig. 7): In the proposed modeling process in Fig. 6, time-related parameters (Δt_s, Δt_f, Δt_{fr}, and Δt_r) and current-related parameters (I_s, I_{RM}, and I_{fr}) are used as inputs. However, these parameters also relate to the current varying rate k, which is determined by the inductance L_m and voltage V_R. Therefore, it is necessary to extract parameter values and establish the RRP model for various k.

In order to be able to tune the value of k, an *LC* resonant circuit [22], [39] with a thyristor is used in the experiment, and the circuit topology is shown in Fig. 7(a). A coaxial shunt is used to measure the current. The thyristor voltage rating is 4.8 kV, and the current rating is 1.0 kA. The typical experimental waveforms are shown in Fig. 7(b). The working process is explained below.

1) The capacitor C_m is precharged to an initial voltage.
2) Trigger the thyristor to conduct the current.
3) C_m and L_m form a resonance. The thyristor current i_T starts to increases and then decreases.
4) At the zero-crossing point, the thyristor naturally turns OFF, and the RRP occurs.

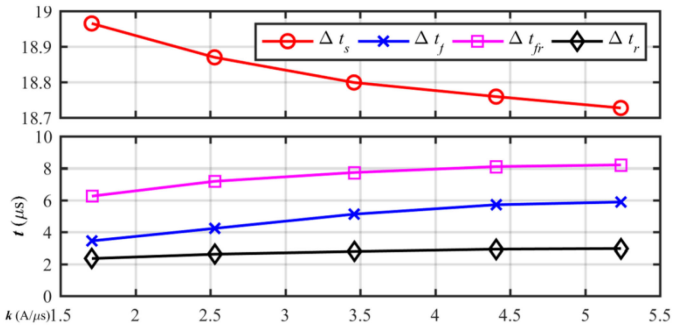


Fig. 8. Measured time-related parameters (Δt_s, Δt_f, Δt_{fr}, Δt_r) at different current varying rate k.

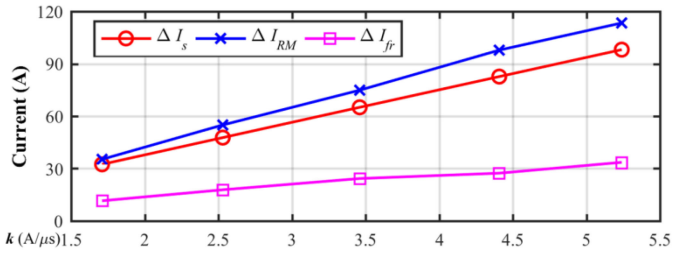


Fig. 9. Measured current-related parameters (I_s, $I_{\rm RM}$, I_{fr}) at different current varying rate k.

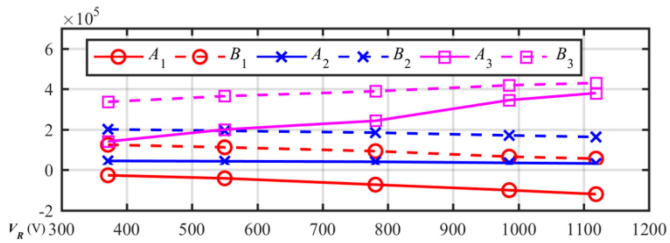


Fig. 10. Extracted parameters A_1, B_1, A_2, B_2, A_3, and B_3 at different V_R.

During experiments, the initial voltage on the capacitor C_m is changed to tune the current varying rate k. The experimental waveforms are recorded. Then, the time-related parameters and current-related parameters are measured at different k as shown in Figs. 8 and 9, respectively.

For time-related parameters, Fig. 8 shows that, as k increases, Δt_s decreases, but Δt_f, Δt_{fr}, and Δt_r increase. For current-related parameters, Fig. 9 shows that I_s, I_{RM}, and I_{fr} increase linearly with k. Through curve fitting, parameters are estimated as a function of k, which is shown below

$$\begin{cases} I_s = 18.6k + 0.64 \\ I_{\rm RM} = 22.28k - 2.00, I_{fr} = 5.98k + 2.19. \end{cases} \tag{29}$$

After input parameters are acquired, the process in Fig. 6 is further used to extract the modeling parameters (A_1, B_1, A_2, B_2, A_3, and B_3), as shown in Fig. 10, which indicates a linear relationship with V_R. It is because the reverse voltage V_R can change the depletion region inside the thyristor during RRP, as described in Section II-B. Then, parameters could be estimated

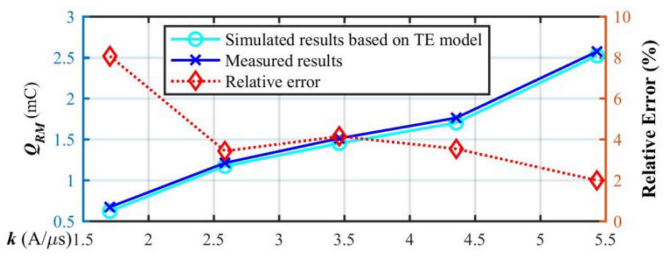


Fig. 11. Comparison of calculated and measured reverse recovery charge Q_{rr} at different current varying rate k.

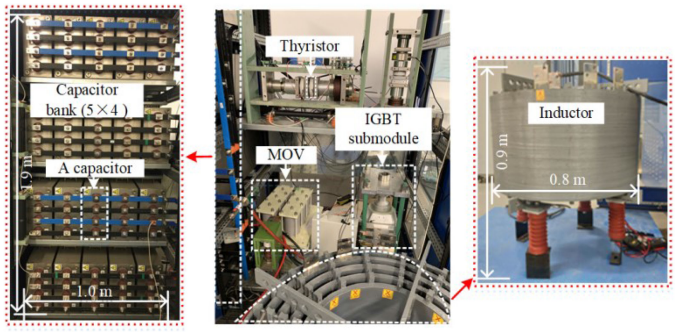


Fig. 12. Experimental prototype of an HVdc circuit breaker testing platform.

TABLE VI
CIRCUIT PARAMETERS IN THE HVDC BREAKER TESTING PLATFORM OF Fig. 12

Inductance L_m	*DC Capacitor* C_m	*MOV Voltage* V_{res}	*IGBT snubber* C_s
0.24mH, 0.416mH, 0.813mH	20 mF	781.5V, 983.0 V	220 μF

as a function of V_R, which could be given by

$$\begin{cases} A_1 = -126.63V_R + 2.45 \cdot 10^4, B_1 = -94.868V_R + 1.62 \cdot 10^5 \\ A_2 = -16.96V_R + 5.20 \cdot 10^4, B_2 = -50.71V_R + 2.21 \cdot 10^5 \\ A_3 = 322.17V_R + 1.65 \cdot 10^4, B_3 = 124.65V_R + 2.93 \cdot 10^5. \end{cases} \tag{30}$$

Moreover, based on the established TE model in Fig. 6, the accumulated charge Q_{rr} during the RRP could be calculated. The calculation result is also compared with measurements at different values of k, as shown in Fig. 11. The relative error between calculations and measurements is within 4%, which also validates the effectiveness of the proposed TE model.

B. Overvoltage Prediction in Practical Testing Systems

1) Prototype Implementation of HVdc Testing Platform: An HVdc circuit breaker testing platform is implemented, as shown in Fig. 12, following the circuit schematic in Fig. 1, and circuit parameters in Table VI.

The capacitor bank C_m is selected as 20 mF. In this high-power platform, the capacitor's current rating is as high as 25 kA, and the voltage rating is up to 5 kV. According to Fig. 1(a), the inductor L_m resonates with the capacitor C_m, which defines the resonant frequency. In practical testing, the resonance should

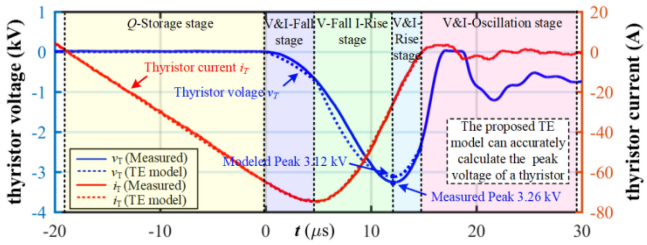


Fig. 13. Comparison of measured waveforms with the proposed TE model.

TABLE VII
COMPARISON OF MEASUREMENTS AND CALCULATIONS FROM THE TE MODEL

	Q_{rr} (mC)	V_{RM} (kV)
Calculation from TE Model	1.71	3.12
Measurement	1.71	3.26

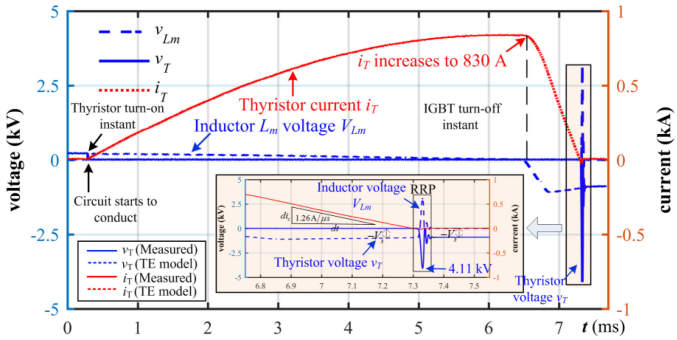


Fig. 14. Experimental waveforms of an HVdc circuit breaker with parameters as $V_R = 983$ V, $L_m = 0.813$ mH, and $k = 1.21$ A/μs.

provide at least 3 ms for the control unit to respond [18], [19], [40], [41], which provides the inductance range. In this design, L_m has three values, 0.24 mH, 0.416 mH, and 0.813 mH, for different testing conditions. It needs to be emphasized that L_m is the resonant inductance in the breaker testing circuit, which is different from the transmission line inductance in a practical HVdc system. The MOV is selected to achieve a constant voltage across the IGBT, and its restriction voltage V_{res} can be selected as two values, 781.5 and 983.0 V. Besides, the snubber capacitor C_s is selected to be 220 μF, and the thyristor is the one tested in Section IV-A.

In the testing process, the capacitor bank C_m is precharged, and control signals for the thyristor and IGBT follow Fig. 1(b). After the thyristor turns ON, the current i_T increases based on the resonance between C_m and L_m, when i_T reaches the peak value, the IGBT turns OFF, and i_T starts to decrease and charge the snubber capacitor C_s. After C_s is charged to the restriction voltage of the MOV, it is clamped to $V_{\rm res}$. In the *LC* resonance, when i_T reaches the peak, C_m is fully discharged, which means V_{Cm} is usually very small. Then, based on (1), V_R is approximately equal to $V_{\rm res}$.

2) Overvoltage Prediction With k = 3.26 A/μs: In this example, the parameter values follow Table II, in which $V_R = 781.5$ V, $L_m = 0.24$ mH, and $k = 3.26$ A/μs.

According to Fig. 1, the thyristor voltage v_T can be derived from i_T, and the expression is provided in (2), which relates to V_R and the current varying rate di_T/dt. Based on the extracted parameters in Tables III–V, the proposed TE model can be calculated from Fig. 6. The comparison between calculated waveforms from the proposed TE model and measurements are shown in Fig. 13.

Fig. 13 shows that the proposed TE model agrees well with the measured waveforms. A detailed comparison of the critical parameters is provided in Table VII. It shows that the proposed TE model can accurately provide the peak current $I_{\rm RM}$, reverse recovery charge Q_{rr}, and the peak voltage $V_{\rm RM}$. In the experiment, the capacitor C_m is precharged to 117 V, but the induced peak voltage during the RRP is as high as 3.26 kV, which validates the overvoltage issue. In addition, Table VII shows the relative error of the estimated $V_{\rm RM}$ is only 4.29%.

A comparison of the TE model results in Fig. 13 with the conventional exponential model results in Fig. 5 shows that this article is a good improvement in previous studies. It contributes to predicting the overvoltage issue in the RRP of thyristors accurately.

3) Overvoltage Prediction With Various k: In this example, V_R and L_m are selected to different values to predict the overvoltage issue with various k.

When $V_R = 983$ V, $L_m = 0.813$ mH, and $k = 1.21$ A/μs, the measured waveforms are shown in Fig. 14. The capacitor C_m is precharged to 235 V. The maximum current is as high as 830 A, when the IGBT turns OFF. According to Fig. 14, during the RRP of a thyristor, there is an obvious overvoltage that can jeopardize the safe operation in the HVdc circuit breaker testing. Therefore, it is important to predict the overvoltage at different conditions.

Analysis in Section-III (especially Fig. 6) could be used to establish the current equation i_T. Then, voltage v_T can be calculated. The detailed procedure is explained as follows:

1) calculate the current varying rate $k = di_T/dt = V_R/L_m$;
2) use the proposed TE model in (3) and (11) to get the general expressions of the current and voltage;
3) use the extraction method in (29) to get I_s and (30) to get A_1, A_2, A_3, B_1, B_2, and B_3;
4) calculate (C_{11}, C_{21}), (C_{12}, C_{22}), and (C_{13}, C_{23}) based on (15), (20), and (26), respectively;
5) substitute parameters as input to the design methodology in Fig. 6 to acquire the specific expressions of the current and voltage with all the necessary parameters and coefficient;
6) predict peak current and voltage based on the acquired equations.

In this example, $V_R = 983$ V. When L_m is 0.416 or 0.813 mH, k is 2.35 A/μs or 1.21 A/μs, respectively. Then, according to the procedure above, parameters A_1, A_2, A_3, B_1, B_2, and B_3 are calculated in Table VIII, and parameters (C_{11}, C_{21}), (C_{12}, C_{22}), and (C_{13}, C_{23}) are shown in Table IX. Then, the proposed TE model can be derived from Fig. 6.

When $V_R = 983$ V, $L_m = 0.416$ mH, and $k = 2.35$ A/μs, the comparison of the proposed TE model and the measurement is

TABLE VIII
PARAMETERS A_1, A_2, A_3, B_1, B_2, AND B_3 FOR DIFFERENT L_m

L_m (mH)	*Storage Stage*	*V&I-Fall Stage*		*V-Fall I-Rise Stage*		*V&I-Rise Stage*	
	I_s	$A_1(\times 10^5)$	$B_1(\times 10^4)$	$A_2(\times 10^4)$	$B_2(\times 10^5)$	$A_3(\times 10^5)$	$B_3(\times 10^5)$
0.416	46.42	-1.00	6.89	3.53	1.71	3.34	4.16
0.813	24.09	-1.00	6.89	3.53	1.71	3.34	4.16

TABLE IX
PARAMETERS (C_{11}, C_{21}), (C_{12}, C_{22}), AND (C_{13}, C_{23}) FOR DIFFERENT L_m

L_m (mH)	*V&I-Fall*		*V-Fall I-Rise*		*V&I-Rise*	
	C_{11}	C_{21}	C_{12}	C_{22}	C_{13}	C_{23}
0.416	-46.42	32.96	-53.78	-11.08	-16.37	9.90
0.813	-24.09	17.52	-28.09	-5.79	-8.56	2.03

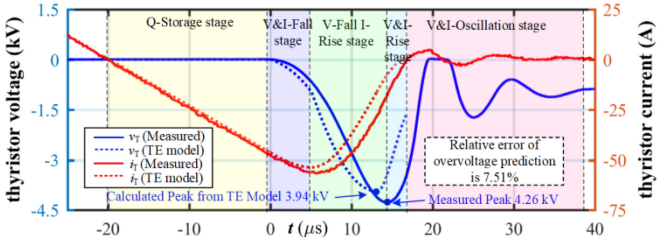


Fig. 15. Comparison of predicted and measured waveforms when $V_R = 983$ V, $L_m = 0.416$ mH, and $k = 2.35$ A/μs.

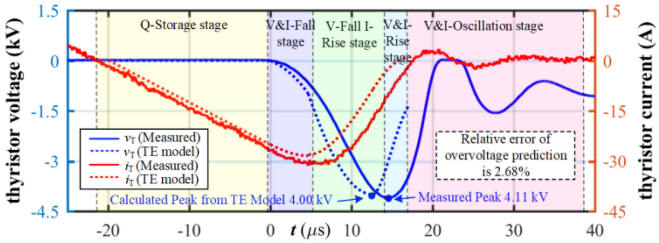


Fig. 16. Comparison of predicted and measured waveforms when $V_R = 983$ V, $L_m = 0.813$ mH, and $k = 1.21$ A/μs.

shown in Fig. 15. The measured peak voltage is 4.26 kV, and the predicted peak voltage is 3.94 kV, resulting in a relative error of 7.51%.

When $V_R = 983$ V, $L_m = 0.813$ mH, and $k = 1.21$ A/μs, the comparison of the proposed TE model and the measurement is shown in Fig. 16, which is also the enlarged figure of Fig. 14. The measured peak voltage is 4.11 kV, and the predicted peak voltage is 4.00 kV, resulting in a relative error of 2.68%.

Furthermore, the precharge voltage of the capacitor varies to realize different reverse voltage V_R and current varying rate k. When $L_m = 0.416$ and 0.813 mH, the above procedure is used to derive the proposed TE model and predict the overvoltage V_{RM}. Meanwhile, experiments are conducted to measure the overvoltage at different conditions. Then, the comparison of the predicted with measured voltages is shown in Table X. It clearly shows that the proposed TE model is accurate to predict the overvoltage, and the relative error is limited within 7.51% at different conditions.

TABLE X
PREDICTION OF OVERVOLTAGE V_{RM} AT DIFFERENT L_m AND k CONDITIONS

L_m (mH)	k (A/μs)	Simulated (kV)	Measured (kV)	Relative Error (%)
0.416	0.66	1.29	1.37	5.84
	1.32	2.30	2.44	5.73
	2.35	3.94	4.26	7.51
0.813	0.54	1.59	1.66	4.22
	1.14	3.45	3.52	1.99
	1.21	4.00	4.11	2.68

V. CONCLUSION AND FUTURE WORK

This article proposed a TE model to describe the RRP of a thyristor in an HVdc circuit breaker testing platform based on a general *LC* resonance circuit. The modeling methodology was presented in detail, showing the analytical equations and the parameter extraction method from the current and voltage waveforms of a thyristor during the RRP. Given the external conditions of the reverse voltage V_R and inductance L_m, the proposed TE model was effective in predicting the overvoltage of a thyristor. A 1 kV/830 A dc circuit breaker prototype was implemented, and experiments showed that the proposed TE model could accurately predict the overvoltage up to 4.26 kV, and the relative error was within 7.51%.

In future work, there are two directions. First, the RRP of parallel-connected thyristors will be investigated in order to achieve high-current interruption capability. The interaction of multiple thyristors and their equivalent models will be studied. Second, the proposed modeling method will be applied in more applications in HVdc circuit breakers. For example, it can be used to predict the overvoltage issue in the forced commutation unit of the circuit breaker during the RRP, which will contribute to maintaining the reliable and safe operation of circuit breakers. To summarize, it is expected that the achievements of overvoltage modeling in this article will promote the application of HVdc power system in the future.

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