A Method to Balance Dynamic Current of Paralleled SiC MOSFETs With Kelvin Connection Based on Response Surface Model and Nonlinear Optimization

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***Abstract*—Multichip SiC power modules with Kelvin-source connection are popular in applications with large capacity and high switching frequency. However, dynamic current imbalance among paralleled dies due to asymmetric layout limits the available capacity. Thus, this article proposes a method to mitigate the mismatched dynamic current by adjusting the connection points of bonding wires and copper traces. The response surface models and nonlinear constrained optimization algorithms are introduced for the first time to help determine the optimized positions for the connection points. By this method, the dynamic current imbalance can be well suppressed under various working conditions. Besides, the method is cost-efficient and well compatible with the conventional manufacturing technologies because there need no additional efforts but some modifications on bonding wires. At first, the optimization guidelines are obtained after analyzing the mechanism of dynamic current imbalance among paralleled SiC MOSFETs with Kelvin-source connection. Based on the optimization guidelines and response surface models of parasitic inductance, the dynamic current sharing problem can be transformed into a nonlinear constrained optimization issue in mathematics. According to the solution of the mathematic problem, the optimized positions for connection points of bonding wires and copper traces can be determined. Finally, some simulations and experiments are conducted to verify the effectiveness of the proposed method.**

***Index Terms*—Asymmetric layout, dynamic current sharing, multichip SiC power modules, nonlinear constrained optimization, response surface model.**

I. Introduction

A. Illustration of the Problem

SiC MOSFETs are promising devices for high-capacity applications, such as motor drivers of electric vehicles, photovoltaic inverters, and solid-state transformers, due to their high block voltage, high switching frequency, low ON-resistance, and excellent thermal performance [1], [2]. However, the rated current of a single die for the state-of-the-art SiC MOSFETs is limited by 150 A, which is not sufficient for some applications with high capacity [3]–[5]. Parallel operation of SiC MOSFETs is a good way to improve the overall current capacity. However, imbalanced current among paralleled dies is inevitable because of asymmetric layout, mismatched device parameters, and different cooling conditions. Unbalanced current can further result in mismatched power losses and unbalanced junction temperature, which means mismatched degradation rate and thermal-mechanical stress for paralleled dies. Then the reliability and stability of the multichip power modules may be challenged. In practice, the multichip power modules are always de-rated to avoid catastrophic damage of imbalanced current [6]. In order to fully utilize the capacity of each paralleled die and enhance the reliability of multichip power modules, it is necessary to suppress current imbalance among paralleled SiC MOSFET dies in multichip power modules.

The current imbalance in multichip power modules consists of static and dynamic current imbalance. In [7], it is pointed out that the static current of paralleled SiC MOSFETs can be self-balanced due to the positive temperature coefficient of ON-resistance (R_{on}). However, the dynamic current tends to be more unbalanced because of negatively temperature-dependent threshold voltage (V_{th}), which could lead to thermal runaway for the paralleled SiC MOSFETs in applications with high switching frequency. These results suggest that the dynamic current sharing should be seriously discussed while the static current sharing needs less analysis because of the self-balanced ability.

To effectively mitigate the mismatched dynamic current, the mechanism of dynamic current imbalance should be comprehensively understood. In [8] and [9], the influences of mismatched device parameters and asymmetric layout on dynamic current sharing performance are investigated by theoretical analysis and experiments. Besides, some statistic methods are adopted to analyze the mechanism of current imbalance among paralleled SiC MOSFETs in [10] and [11]. In these works, it is figured out that the threshold voltage of dies and the distribution of parasitic inductance can greatly affect the dynamic current sharing performance.

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The dynamic current imbalance resulting from the deviations of device parameters can be well limited by chip preselection. In [12], a new criterion is proposed to characterize the spread of device parameters and a hierarchical cluster algorithm is developed to screen multiple devices for better dynamic current sharing performance in parallel operation of SiC MOSFETs. And a linear regression model for screening SiC MOSFETs to minimize transient current imbalance is presented in [13]. Thus, this article turns to discuss about the dynamic current sharing issues associated with asymmetric layout.

B. Review on Previous Methods and Description of the Proposed Method

There have been some methods to mitigate dynamic current imbalance among paralleled chips in previous works, which can be divided into two categories: active methods, and passive methods.

The active methods need accurate measurement on unbalanced dynamic current and separate gate control for each paralleled chip. In [14] and [15], the time delay of gate drive signal is adjusted based on the detected signals from differential current transformer to promote dynamic current sharing. In [16], a cost-efficient master–slave control method is presented to reduce unbalanced current with single master gate driver and several amplifiers. All the active methods are effective to improve dynamic current sharing performance for paralleled discrete SiC MOSFETs. However, it is difficult to apply these methods to multichip power modules because there is not enough room to insert current sensors into the modules. Though some compact Rogowski coil current sensors are developed, they are still too bulk to be inserted into the power modules [17]. For some point field detectors of small size, the cross coupling of magnetic field in the power modules will greatly affect the accuracy of current measurement, which could further mislead the behaviors of gate drivers in active methods [18]. In addition, the separate control of gate drive is complicated and expensive for multichip power modules with plenty of paralleled dies in each switching position.

The passive methods always focus on inserting external components or optimizing the layout to compensate for the mismatches of paralleled branches. First, there are some methods to insert magnetic components into paralleled branches for better dynamic current sharing performance. In [19], the drive-source resistors and coupled power source inductors are adopted to suppress dynamic current imbalance. Similarly, in [20], a differential mode choke is employed to promote dynamic current sharing for paralleled discrete SiC MOSFETs. In [21], some ultramini negatively coupled inductors are used to balance the dynamic current among two paralleled SiC MOSFET dies. In the abovementioned methods, the manufacturing process of inserted magnetic components will be much complicated when more than two chips are in parallel. Thus, it is difficult to apply these methods to multichip SiC power modules. Besides, the total cost will be increased.

Second, there are some methods by modifying the layout of direct bonding copper substrates (DBC) to balance dynamic current. Several layout schemes are proposed to achieve symmetric power loops for better dynamic current sharing performance in [22]–[24]. Besides, some methods are proposed to optimize the layout of drive loop for better dynamic current sharing performance in [25] and [26]. All abovementioned methods to improve dynamic current sharing by optimizing layout focus on modifying the copper traces on DBC. And there are few discussions about the optimization of the bonding wires.

In [27], only the length of bonding wires is adjusted to compensate for mismatched parasitic inductance for better dynamic current sharing performance. The length of the copper traces between bonding wires of adjacent dies is not adjusted. Besides, the Kelvin-source connection is not considered in [27]. Inspired by this method, this article proposes a more flexible method to balance dynamic current among paralleled SiC MOSFET dies with Kelvin-source connection. Specifically, the positions of the connection points for power source bonding wires and copper traces are adjusted to balance the dynamic current. In the proposed method, the length of bonding wires and the length of copper traces between power source bonding wires of adjacent dies are optimized simultaneously to balance dynamic current. Thus, this method is of more degree of freedom. Besides, the response surface models and nonlinear optimization algorithms are introduced for the first time to help determine the optimal positions for connection points of bonding wires and copper traces.

The specific procedures of the proposed method are as follows. First, the optimization targets of various parasitic inductances are obtained by investigating the mechanism of dynamic current imbalance among paralleled SiC MOSFETs with Kelvin-source connection. Then the response surface models of the parasitic inductance for bonding wires and copper traces are built up based on the parametric analysis by finite element method (FEM). Further, the analytical expressions of the response surfaces can be approximately obtained by numerical fitting. According to the optimization targets of parasitic inductance and analytical expressions of all response surfaces, the dynamic current sharing problem is transformed into a nonlinear constrained optimization issue, which can be easily solved by mathematic software. Based on the solution of the nonlinear optimization problem, the optimized positions for connection points of bonding wires and copper traces can be determined to improve dynamic current sharing performance.

The rest of this article is arranged as follows. Section II summarizes the optimization targets for various parasitic inductances by analyzing the mechanism of dynamic current imbalance among paralleled SiC MOSFETs with Kelvin-source connection. Section III discusses about the response surface models of parasitic inductance for bonding wires and copper traces. Based on these models, Section IV illustrates how to transform the dynamic current sharing issue into a nonlinear constrained optimization problem. And a specific optimized case is given by solving the nonlinear constrained optimization problem with mathematic software. In Section V, some simulations and experiments are conducted to verify the effectiveness of the proposed method. Finally, Section VI concludes the article.

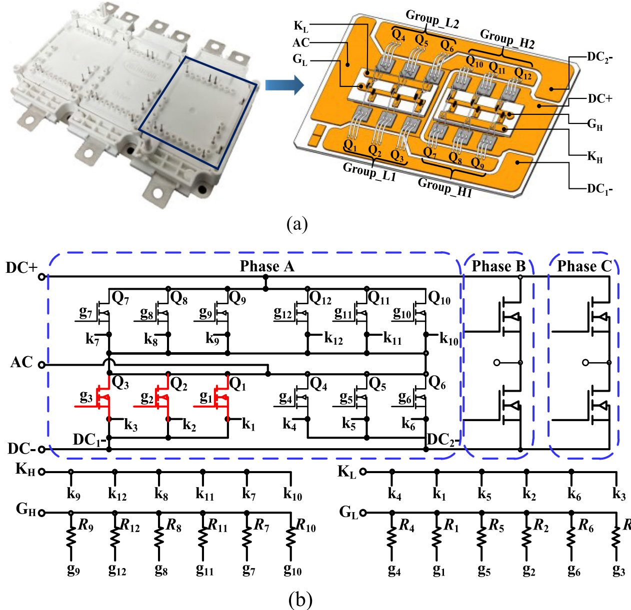


Fig. 1. Schematic of the baseline SiC power module. (a) Configuration of the baseline power module and inside view of one phase leg. (b) Topology.

II. Mechanism of Layout Dominated Dynamic Current Imbalance

A. Configuration of Baseline SiC Power Modules

The configuration of the baseline SiC power module is shown in Fig. 1, whose layout and terminals are similar to the commercial HybridPACK Drive power modules from Infineon [28]. As is shown in Fig. 1, each phase leg comprises twelve SiC MOSFET dies. Each switching position consists of six paralleled dies, which are divided into two groups located in the DBC symmetrically. Considering the symmetry of the overall layout, it is feasible to evaluate the overall current sharing performance of the multichip power module by investigating the imbalanced current among dies in one of the groups. Thus, this article just discusses about the unbalanced dynamic current among dies in Group_L1 [seen in Fig. 1(a)], which are marked by red lines in Fig. 1(b).

B. Guidelines to Mitigate Dynamic Current Imbalance in Multichip SiC Power Modules With Kelvin-Source Connection

The qualitative switching waveforms of SiC MOSFETs are depicted in Fig. 2 [29]. Dynamic current imbalance mainly occurs in the shadow areas. During these intervals, the SiC MOSFETs operate in saturation regions, which can be modeled as current sources controlled by gate-source voltage (v_{gs}). The drain-source parasitic capacitance (C_{ds}) can be neglected as is discussed in [30]. The gate-source capacitance (C_{gs}) is dynamically in parallel with gate-drain capacitance (C_{gd}). Thus, the dynamic circuit model for the paralleled dies in Group_L1 can be built up as shown in Fig. 3, where C_{iss} is equal to the sum of C_{gs} and C_{gd}. This article just focuses on the unbalanced dynamic current resulting from asymmetric layout and all the device parameters for various dies are regarded to be equal.

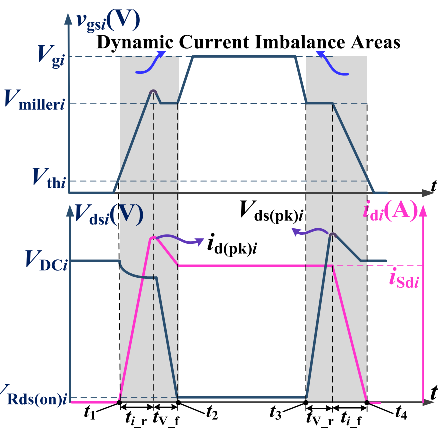


Fig. 2. Qualitative switching waveforms of SiC MOSFETs.

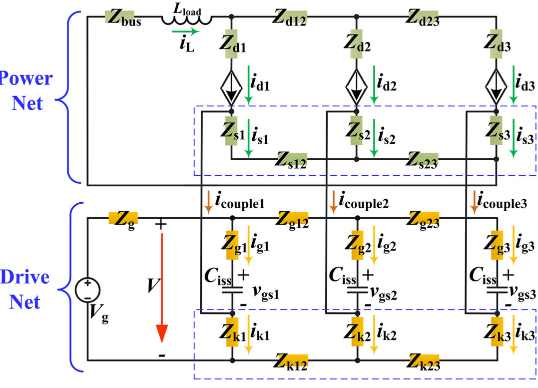


Fig. 3. Dynamic circuit model for paralleled dies in Group_L1 of the baseline power module.

As is shown in Fig. 3, the dynamic circuit model consists of power net and drive net. Applying Kirchhoff Voltage Law (KVL) to the nets circled by blue dash line, there are

$$\begin{cases} (Z_{s1} + Z_{s12})\, i_{s1} - Z_{s2} i_{s2} + Z_{k2} i_{k2} + Z_{k12}\,(i_{k2} + i_{k3}) \\ \quad - Z_{k1} i_{k1} = 0 \\ Z_{s2} i_{s2} + Z_{s23}\,(i_{s1} + i_{s2}) - Z_{s3} i_{s3} + (Z_{k3} + Z_{k23})\, i_{k3} \\ \quad - Z_{k2} i_{k2} = 0. \end{cases} \tag{1}$$

Balanced dynamic current among paralleled dies means that

$$i_{d1} = i_{d2} = i_{d3} \tag{2}$$

According to the saturation model of SiC MOSFETs, the drain current of paralleled dies can be expressed as

$$\begin{cases} i_{d1} = g(v_{gs1} - V_{th})^2 \\ i_{d2} = g(v_{gs2} - V_{th})^2 \\ i_{d3} = g(v_{gs3} - V_{th})^2 \end{cases} \tag{3}$$

where g and V_{th} are transconductance coefficient and threshold voltage of paralleled SiC MOSFET dies, respectively [20]. The transconductance coefficient, g, can be further expressed as

$$g = \frac{\mu_n C_{OX} Z_{CH}}{2 L_{CH}} \tag{4}$$

where μ_n is the majority-carrier mobility. C_{OX} is the gate oxide capacitance per unit area, $C_{OX} = \varepsilon_{OX}/t_{OX}$. ε_{OX} is the dielectric constant of the silicon dioxide. t_{OX} is the thickness of the gate oxide. Z_{CH} and L_{CH} are channel width and length, respectively.

Based on (2) and (3), balanced dynamic current also suggests that

$$v_{gs1} = v_{gs2} = v_{gs3}. \tag{5}$$

According to the characteristics of capacitance, there are

$$\begin{cases} v_{gs1} = \frac{i_{g1}}{sC_{iss}} \\ v_{gs2} = \frac{i_{g2}}{sC_{iss}} \\ v_{gs3} = \frac{i_{g3}}{sC_{iss}}. \end{cases} \tag{6}$$

By (5) and (6), it can be deduced that

$$i_{g1} = i_{g2} = i_{g3} = i_g \tag{7}$$

when the dynamic currents of paralleled SiC dies are balanced.

In practice, it is desirable to decouple power net and drive net, which means $i_{\text{couple},n}$ (n = 1, 2, and 3) is equal to zero. Otherwise, some current in the power net may go through the drive net, which may overheat the drive source bonding wires [31]. If the drive net is fully decoupled with the power net, there are

$$\begin{cases} i_{dn} = i_{sn} \\ i_{kn} = i_{gn} \end{cases} \quad (n = 1, 2, 3). \tag{8}$$

By (2), (7), and (8), it can be concluded that

$$\begin{cases} i_{s1} = i_{s2} = i_{s3} = i_s \\ i_{k1} = i_{k2} = i_{k3} = i_k. \end{cases} \tag{9}$$

Take (9) into (1), it can be derived that

$$\begin{cases} (Z_{s1} + Z_{s12} - Z_{s2})\, i_s + (Z_{k2} + 2Z_{k12} - Z_{k1})\, i_k = 0 \\ (Z_{s2} + 2Z_{s23} - Z_{s3})\, i_s + (Z_{k3} + Z_{k23} - Z_{k2})\, i_k = 0. \end{cases} \tag{10}$$

To satisfy (10) at all the time, it is required that

$$\begin{cases} Z_{s1} + Z_{s12} - Z_{s2} = 0 \\ Z_{s2} + 2Z_{s23} - Z_{s3} = 0 \end{cases} \tag{11}$$

$$\begin{cases} Z_{k2} + 2Z_{k12} - Z_{k1} = 0 \\ Z_{k3} + Z_{k23} - Z_{k2} = 0. \end{cases} \tag{12}$$

Applying KVL to the drive net, it can be expressed that

$$\begin{cases} v_{gs1} = V - Z_{g1}i_{g1} - Z_{k1}i_{k1} \\ v_{gs2} = V - Z_{g12}(i_{g2} + i_{g3}) - Z_{k12}(i_{k2} + i_{k3}) \\ \qquad -Z_{g2}i_{g2} - Z_{k2}i_{k2} \\ v_{gs3} = v_{gs2} + Z_{g2}i_{g2} + Z_{k2}i_{k2} - (Z_{g23} + Z_{g3})\, i_{g3} \\ \qquad - (Z_{k3} + Z_{k23})\, i_{k3}. \end{cases} \tag{13}$$

By (5), (7), (9), and (11)–(13), there are

$$\begin{cases} (2Z_{g12} + Z_{g2} - Z_{g1})\, i_g = 0 \\ (Z_{g23} + Z_{g3} - Z_{g2})\, i_g = 0. \end{cases} \tag{14}$$

To satisfy the equations in (14) at the switching transients, there should be

$$\begin{cases} 2Z_{g12} + Z_{g2} - Z_{g1} = 0 \\ Z_{g23} + Z_{g3} - Z_{g2} = 0. \end{cases} \tag{15}$$

Then the specific requirements on various impedances in the baseline multichip SiC power module to balance the dynamic current of paralleled SiC MOSFETs with Kelvin-source connection can be described by (11), (12), and (15).

In conventional multichip power modules, the impedances mentioned in (11), (12), and (15) mainly result from the bonding wires and copper traces on DBC. Thus, it is feasible to adjust the bonding wires for better dynamic current sharing performance. The impedance in (11), (12), and (15) can be further written as

$$Z_X = R_X + sL_X \tag{16}$$

where R_X is the equivalent series resistance, L_X is the parasitic inductance and s is the Laplace operator. At the switching intervals, the parasitic inductance dominates the impedance, which means that $|sL_X| \gg |R_X|$. Thus, equation (16) can be approximately expressed as

$$Z_X \approx sL_X. \tag{17}$$

By (17), equations (11), (12), and (15) can be rewritten as

$$\begin{cases} L_{s1} + L_{s12} - L_{s2} = 0 \\ L_{s2} + 2L_{s23} - L_{s3} = 0 \end{cases} \tag{18}$$

$$\begin{cases} L_{k2} + 2L_{k12} - L_{k1} = 0 \\ L_{k3} + L_{k23} - L_{k2} = 0 \end{cases} \tag{19}$$

$$\begin{cases} 2L_{g12} + L_{g2} - L_{g1} = 0 \\ L_{g23} + L_{g3} - L_{g2} = 0. \end{cases} \tag{20}$$

Equations (18), (19), and (20) describe the optimization targets of the power source, drive source, and gate parasitic inductance, respectively, when the device parameters for dies are equal. As is discussed in [32], the unbalanced dynamic current is more sensitive to the mismatched power source parasitic inductance than the mismatched gate and drive source parasitic inductance. Hence, this article focuses on optimizing the power source parasitic inductance to balance dynamic current. Specifically, the connection points of power source bonding wires and copper traces are adjusted to suppress dynamic current imbalance in SiC power modules with Kelvin-source connection.

III. Response Surface Model of Parasitic Inductance

Response surface model can help develop the relationship between selected design parameters and the chosen response [33]. By this method, this article tries to figure out the relationship between critical geometric parameters and parasitic inductance. The analytical expressions of the response surfaces can be obtained by numerical fitting to help evaluate the parasitic inductance in power modules. In conventional power modules, the parasitic inductance mainly results from the bonding wires and copper traces on DBC. Therefore, this section separately

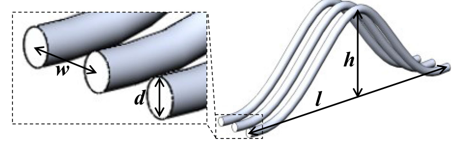


Fig. 4. Schematic of paralleled bonding wires.

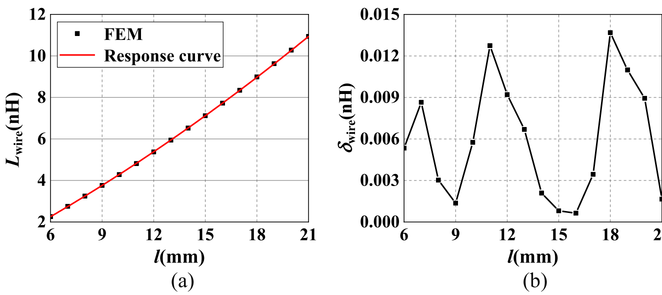


Fig. 5. (a) Response curve of parasitic inductance for bonding wires. (b) Errors of the numerical fitting in (21).

discusses about the response surface models of the parasitic inductance from bonding wires and copper traces.

A. Response Surface Model for the Parasitic Inductance of Bonding Wires

The maximum diameter of commercial bonding wires is no more than 500 μm so the current capacity of single bonding wire is limited. In order to increase the current capacity, several bonding wires are always paralleled. Some geometric parameters are marked in Fig. 4, which determine the three-dimensional model of paralleled bonding wires.

In practice, it is inconvenient to frequently change the diameter (d) and arc height (h) of bonding wires. The number of paralleled bonding wires and the distance between adjacent bonding wires (w) are constrained by the source areas of SiC MOSFET dies. Thus, only the distance between two terminals of bonding wires, l, is selected as the design parameter and the total parasitic inductance of paralleled bonding wires is chosen as the response. Some other geometric parameters, h, w, and d are set to 3.5 mm, 1 mm, and 250 μm, respectively. And three paralleled bonding wires are employed for each SiC MOSFET die. The total parasitic inductance (L_{wire}) of paralleled bonding wires with various l can be calculated by FEM. Specifically, the parasitic inductance is extracted by ANSYS Q3D when the extraction frequency is 200 MHz. The results are in Fig. 5(a).

The response surface degrades into a curve because there is just one design parameter. Then the analytical expression of the response curve can be obtained by numerical fitting, which can be written as

$$L_{wire}(l) = 0.006391l^2 + 0.4063l - 0.4134. \quad (21)$$

The errors of the numerical fitting in (21), δ_{wire}, can be calculated by

$$\delta = |L_{\text{FIT}} - L_{\text{FEM}}| \quad (22)$$

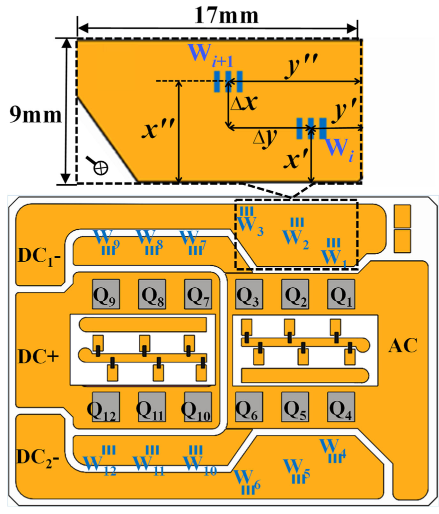


Fig. 6. Schematic of DBC layout and the placement of dies.

where L_{FIT} and L_{FEM} are the parasitic inductance calculated by the fitting equation and FEM, respectively. The results are shown in Fig. 5(b).

B. Response Surface Model for the Parasitic Inductance of Copper Traces on DBC

In this article, the thickness of the copper traces on DBC is 0.3 mm. The DBC layout and the placement of dies are determined (seen in Fig. 6). The connection points of power source bonding wires and copper traces are marked by W_1 to W_{12}. For clear illustration, the copper trace, which W_1, W_2, W_3, and the terminal DC_1- are located in, is discussed in detail as an instance. The parasitic inductance of the copper traces between adjacent connection points affect the dynamic current sharing performance. The parasitic inductance of copper traces between the terminal DC_1- and the connection points W_3 contributes to the total loop inductance, which influences the voltage spike at turn-OFF transients. Thus, the response surface models of the parasitic inductance for the two parts are discussed in detail.

The overall shape of the copper trace is fixed. Therefore, the parasitic inductance between adjacent connection points depends on their positions on the copper trace. There are four parameters (x', y', Δx, Δy) determining the positions of adjacent connection points, W_i and $W_{i+1} (i = 1 \text{ or } 2)$, on the copper trace as is shown in Fig. 6.

The parasitic inductance between adjacent connection points is extracted when Δx and Δy are fixed and x' and y' are varied. The results are shown in Fig. 7. It can be seen that the parasitic inductance varies when adjacent connection points with fixed relative position move to the edge of the copper trace. However, the variation of the parasitic inductance is less than 10.9%. Besides, the connection points are always located in the central region of the copper trace in practice. Thus, the variation of the parasitic inductance is neglected. Then the response surface model for the parasitic inductance of copper traces between adjacent connection points can be built up with only two design parameters, Δx and Δy. And the response surface model of the

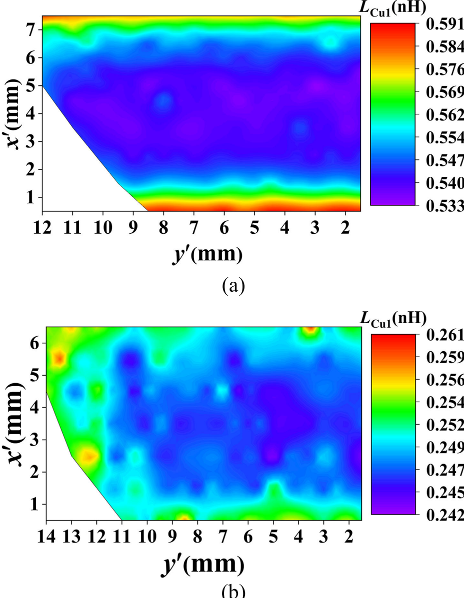


Fig. 7. Parasitic inductance between W_i and W_{i+1} at various x' and y' when (a) $\Delta x = 1$ mm, $\Delta y = 4$ mm and (b) $\Delta x = 2$ mm, $\Delta y = 3$ mm.

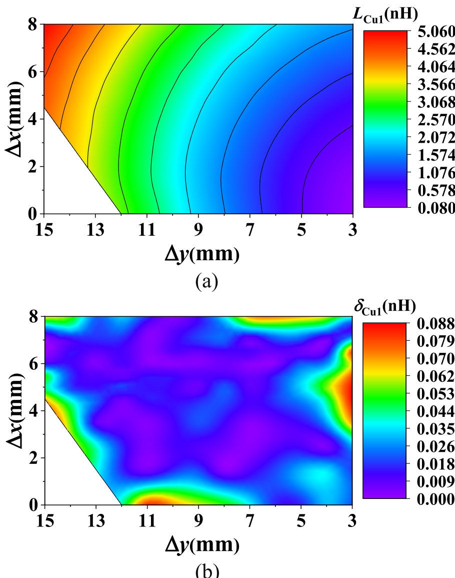


Fig. 8. (a) Response surface for parasitic inductance of copper traces between adjacent connection points. (b) Errors of the numerical fitting in (23).

parasitic inductance between W_1 and W_2 is regarded to be the same as that of the parasitic inductance between W_2 and W_3. The response surface is shown in Fig. 8(a). Then the analytical expression of the response surface can be approximately obtained by numerical fitting, which can be expressed as

$$L_{Cu1}(\Delta x, \Delta y) = 0.01289\Delta y^2 - 0.01234\Delta x\Delta y + 0.02149\Delta x^2 + 0.1424\Delta y + 0.06034\Delta x - 0.4289. \quad (23)$$

The errors of the numerical fitting in (23), δ_{Cu1}, can be calculated by (22) as well. The results are shown in Fig. 8(b).

The response surface of the parasitic inductance for the copper traces between W_3 and DC_1- to the selected design parameters,

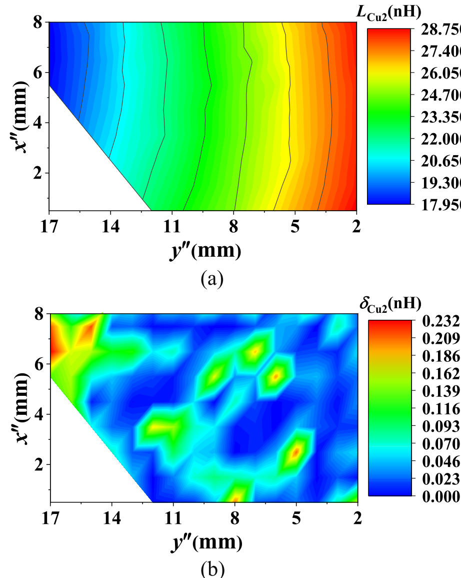


Fig. 9. (a) Response surface for the parasitic inductance of copper traces between W_3 and DC_1-. (b) Errors of the numerical fitting in (24).

x'' and y'', can also be obtained with similar method [seen in Fig. 9(a)]. The mathematic expression of the response surface can be expressed as

$$L_{Cu2}(x'', y'') = -0.0001873y''^2 - 0.01048x''y'' + 0.02717x''^2 - 0.6116y'' - 0.214x'' + 29.59. \quad (24)$$

The errors of the numerical fitting in (24), δ_{Cu2}, can also be calculated by (22). The results are shown in Fig. 9(b).

IV. Mathematic Description of the Dynamic Current Sharing Problem

A. *Transformation of Dynamic Current Sharing Problems Into Nonlinear Constrained Optimization Issues*

The specific requirements on parasitic inductance for balanced dynamic current have been derived in Section II as shown in (18), where L_{si} and L_{sij} $(i, j = 1, 2, 3 \text{ and } j > i)$ mainly result from the bonding wires and copper traces, respectively. Based on the response surface models in Section III, the equations in (18) can be transformed into equations consisting of the design parameters. Considering the limitations of the design parameters resulting from manufacturing process and the shape of copper traces, the problem to determine appropriate values for design parameters can be described as a nonlinear constrained optimization issue. The details are presented in the following.

First, a Cartesian coordinate is established as shown in Fig. 10. The positions of Q_i and W_i can be noted by their central points, whose coordinate values are noted as (X_{0i}, Y_{0i}) and (x_i, y_i), respectively. Then all the selected design parameters mentioned in Section III can be represented by these coordinate values. The X_{0i} and Y_{0i} are constant considering that the positions of dies are fixed. Then the selected design parameters can be directly represented by some functions of x_i and y_i $(i = 1, 2, \text{and } 3)$. For bonding wires, one terminal is connected with the dies and another terminal is connected with the copper traces. Thus, the

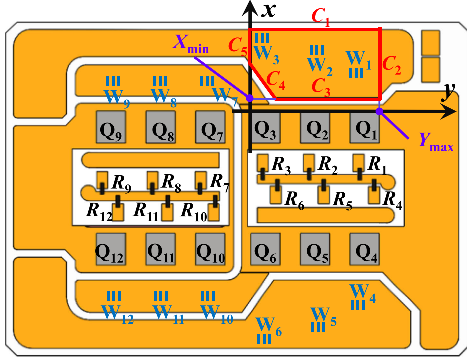


Fig. 10. Schematic of the Cartesian coordinate.

selected design parameter, l, can be written as

$$l = \sqrt{(x_i - X_{0i})^2 + (y_i - Y_{0i})^2} \quad (i = 1, 2, 3). \tag{25}$$

For the copper trace between adjacent connection points, the selected design parameters, Δx and Δy, can be expressed as

$$\begin{cases} \Delta x = |x_{i+1} - x_i| \\ \Delta y = |y_{i+1} - y_i| \end{cases} \quad (i = 1, 2) \tag{26}$$

For the copper trace between the terminal DC_1– and W_3, the selected parameters, x'' and y'', can be represented by

$$\begin{cases} x'' = |x_3 - X_{\min}| \\ y'' = |y_3 - Y_{\max}|. \end{cases} \tag{27}$$

where $X_{\min}$ is the x-coordinate value of the crossing point for the line, C_3, and x-axis; and $Y_{\max}$ is the y-coordinate value of the crossing point for the line, C_2, and y-axis.

Taking (25) into (21), the parasitic inductance resulting from power source bonding wires of Q_i (L_{si}) can be mathematically expressed as a function of the coordinates of connection points, which is

$$L_{si} = L_{\text{wire}}(l) = f_1(x_i, y_i)(i = 1, 2, 3). \tag{28}$$

By (23) and (26), the L_{sij} can also be written as a function of the coordinates of connection points, which can be written as

$$\begin{aligned} L_{sij} &= L_{Cu1}(\Delta x, \Delta y) \\ &= f_2(x_i, x_j, y_i, y_j) \quad (i, j = 1, 2, 3 \text{ and } i \neq j). \end{aligned} \tag{29}$$

Based on (28) and (29), (18) can be rewritten as

$$\begin{cases} F_1(x_1, x_2, y_1, y_2) = 0 \\ F_2(x_2, x_3, y_2, y_3) = 0. \end{cases} \tag{30}$$

Equations in (30) can be further converted into one equation, which is

$$F = |F_1(x_1, x_2, y_1, y_2)| + |F_2(x_2, x_3, y_2, y_3)| = 0. \tag{31}$$

In order to balance the dynamic current among paralleled dies in multichip power modules, the positions of W_1, W_2, and W_3 should be adjusted to change the values of x_1, x_2, x_3, y_1, y_2, and y_3 until the equation in (31) is satisfied. From another perspective, the dynamic current sharing performance can be improved by selecting proper values for the parameters, x_1, x_2, x_3, y_1, y_2, and y_3, to minimize the value of the function, F. Then the issue of mitigating switching current imbalance can be mathematically represented by a nonlinear constrained optimization problem, whose target function is F in (31). The aim is to obtain the minimum point of F under some constrained conditions. Then the optimized wire bonding scheme can be determined according to the minimum points of F to achieve excellent dynamic current sharing performance. The constrained conditions depend on the shape of copper traces and the manufacturing techniques. All the connection points should be located in the region circled by red line as shown in Fig. 10. In the Cartesian coordinate shown in Fig. 10, the boundaries of the region can be mathematically expressed as

$$\begin{cases} C_1 : x = X_{\max} \\ C_2 : y = Y_{\max} \\ C_3 : x = X_{\min} \\ C_4 : y = kx + b \\ C_5 : y = Y_{\min} \end{cases} \tag{32}$$

where $X_{\min}$, $X_{\max}$, $Y_{\min}$, $Y_{\max}$, b, and k are equal to 2, 11, 0, 17, 7.67 mm, and –2.377, respectively. In addition, to avoid the crossing of bonding wires, there should be

$$y_j - y_i > \Delta Y (j > i) \tag{33}$$

where ΔY is the allowed minimum difference of y-coordinate value for adjacent connection points, which is set as 1.5 mm.

When the bonding wires in power source are modified, the total parasitic inductance in power source should keep almost constant to avoid greatly increasing of voltage overshoot and switching losses. Thus, one more constrained condition is introduced, which can be expressed as

$$\Delta L \leq \Delta L_{\max} \tag{34}$$

where ΔL is the increment of the parasitic inductance from the source of Q_3 to the terminal DC_1– after adjusting the bonding wires and $\Delta L_{\max}$ is the allowed maximum value of ΔL, which is set as 2 nH in this case.

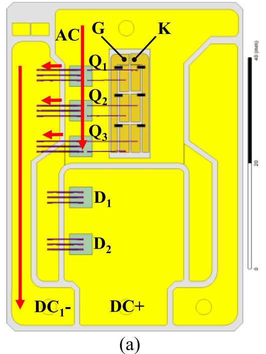
By now, the switching current sharing problem is transformed into a nonlinear constrained optimization issue, whose target function is shown in (31) and the constrained conditions are summarized in (32)–(34).

B. Numerical Solution and the Corresponding Optimized Wire Bonding Scheme

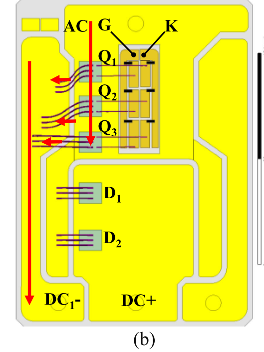
The abovementioned nonlinear constrained optimization issue can be solved by "interiorpoint" optimization algorithm, which can be easily realized by the numerical calculation software, MATLAB. Based on the solution, the optimized positions of W_1, W_2, and W_3 can be determined. The specific values of x_1, x_2, x_3, y_1, y_2, and y_3 for the initial and optimized power modules are listed in Table I. Then the three-dimension models of the initial and optimized power modules are built up (seen in Fig. 11). The SiC MOSFETs in high side switch are replaced by SiC diodes for simplification.

TABLE I
COORDINATE VALUES OF CONNECTION POINTS

	Initial Values	Optimized Values
x_1	5.8mm	4.0mm
x_2	5.8mm	6.7mm
x_3	5.8mm	8.5mm
y_1	15.8mm	12.7mm
y_2	8.9mm	5.8mm
y_3	2.0mm	2.2mm



(a)



(b)

Fig. 11. Three-dimensional models of the (a) initial and (b) optimized baseline power modules.

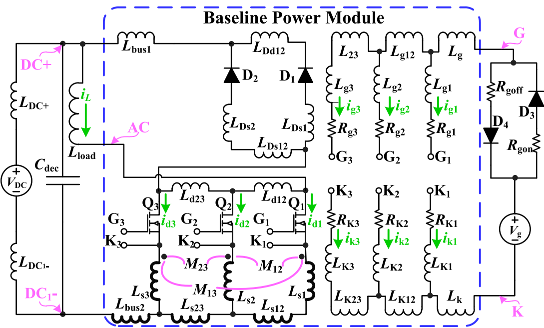


Fig. 12. Circuit model of the double pulse tester for the initial and optimized power modules.

TABLE II
VALUES OF POWER SOURCE PARASITIC INDUCTANCE

	Initial (FEM)	Optimized (FEM)	Optimized (Ideal)
L_{s1}	3.281nH	2.978nH	2.712nH
L_{s2}	3.281 nH	4.092 nH	3.984 nH
L_{s3}	3.281 nH	4.616 nH	4.667 nH
L_{s12}	0.959 nH	1.122 nH	1.257 nH
L_{s23}	0.963 nH	0.265 nH	0.349 nH
L_{bus2}	19.885 nH	19.420 nH	18.89 nH
M_{12}	0.317 nH	0.297 nH	0 nH
M_{23}	0.317 nH	0.722 nH	0 nH
M_{13}	0.121 nH	0.138 nH	0 nH

V. SIMULATION AND EXPERIMENT VERIFICATIONS

A. Indexes for Current Sharing Performance Evaluation

To evaluate the dynamic current sharing performance of the initial and optimized power modules, some indexes are defined. The maximum unbalanced turn-ON and turn-OFF current among paralleled dies are defined as

$$\begin{cases} \Delta i_{\text{on}} = \max\left[\max\left(\left|i_{d1}(t) - i_{d2}(t)\right|\right), \max(\left|i_{d2}(t)\right.\right. \\ \qquad \left.\left. - i_{d3}(t)\right|), \max\left(\left|i_{d1}(t) - i_{d3}(t)\right|\right)\right] \quad t \in [t_1, t_2] \\ \Delta i_{\text{off}} = \max\left[\max\left(\left|i_{d1}(t) - i_{d2}(t)\right|\right), \max(\left|i_{d2}(t)\right.\right. \\ \qquad \left.\left. - i_{d3}(t)\right|), \max\left(\left|i_{d1}(t) - i_{d3}(t)\right|\right)\right] \quad t \in [t_3, t_4] \end{cases} \tag{35}$$

where t_1, t_2, t_3, and t_4 are marked in Fig. 2. The total switching losses for Q_i can be expressed as

$$E_{Si} = \int_{t_1}^{t_2} i_{di}(t) \times v_{dsi}(t)dt + \int_{t_3}^{t_4} i_{di}(t) \times v_{dsi}(t)dt \; (i = 1, 2, 3). \tag{36}$$

The maximum unbalanced total switching losses among dies in multichip power modules are written as

$$\Delta E_S = \max\left[E_{S1}, E_{S2}, E_{S3}\right] - \min\left[E_{S1}, E_{S2}, E_{S3}\right]. \tag{37}$$

The total switching losses of the power module are

$$E_{\mathrm{T}} = E_{\mathrm{S1}} + E_{\mathrm{S2}} + E_{\mathrm{S3}}. \tag{38}$$

B. Simulation Verifications

The circuit model of the double pulse tester for the power module is shown in Fig. 12. The proposed method focuses on optimizing the power source parasitic inductance marked by black bold line in Fig. 12. In this method, some errors of the response surface models and numerical fitting can make the parasitic self-inductance away from the desired values to some degree. Besides, the mutual inductance among conductors is neglected. The errors and mutual inductance among conductors may affect the performance of the proposed method.

Based on the three-dimensional model in Fig. 11, the accurate parasitic self-inductance in the initial and optimized module can be extracted by FEM. The mutual inductance among conductors can also be extracted by FEM. In Fig. 11, it can be seen that the direction of the current in bonding wires is almost normal to the direction of the current in copper traces in the initial and optimized power module. Thus, only the mutual inductance among power source bonding wires are considered. The ideal parasitic self-inductance in the optimized module can be calculated according to the optimized coordinate values of connection points and numerical fitting equations. All mutual inductance in the ideal optimized power module is neglected. The results above are listed in Table II. It can be seen that there are some variations between the accurate parasitic inductance extracted by FEM and the ideal parasitic inductance calculated by response surface models and numerical fitting equations. This may degrade the performance of the optimized method.

Then the dynamic current sharing performance in all cases can be evaluated by simulations under conditions in Table III. The simulation results in Fig. 13 suggest that the optimized method can well suppress the dynamic current imbalance in the power modules. Some modelling errors and the neglecting of the mutual inductance can indeed degrade the performance of the proposed method. However, compared with the initial power module, the unbalanced dynamic current can still be greatly mitigated by the optimized method.

TABLE III
SIMULATION CONDITIONS

Parts	Values
V_{DC}	500V
V_g	17V/-1.8V
C_{dec}	100nF
L_{load}	37μH
I_{load}	105A
R_{gon}, R_{goff}	4.1Ω/8.2Ω
R_{g1}, R_{g2}, R_{g3}	1.8Ω
R_{k1}, R_{k2}, R_{k3}	1.8Ω
D_1, D_2	S6305(1200V/50A)
Q_1, Q_2, Q_3	S4102(1200V/98A)

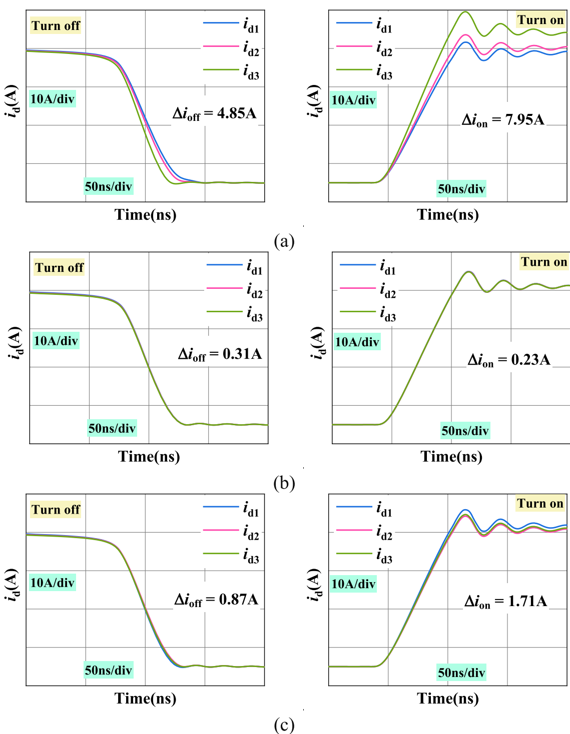


Fig. 13. Simulation waveforms of drain current at turn-OFF and turn-ON transients. (a) Initial power module. (b) Ideal optimized power modules. (c) Real optimized power module.

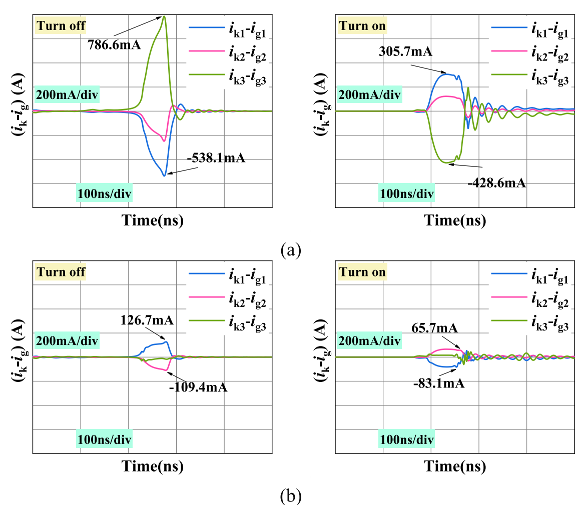


Fig. 14. Differential current between drive source and gate for paralleled dies in (a) the initial and (b) the real optimized power modules.

TABLE IV
DEVICE PARAMETERS OF DIES IN PROTOTYPES

	Initial power module			Optimized power module		
	Q_1	Q_2	Q_3	Q_1	Q_2	Q_3
V_{th} (V)	4.0316	4.0386	4.0388	4.0403	4.073	4.0403
R_{on} (mΩ)	30.9	31.2	31.6	34.1	33.8	34.0
g(A/V^2)	1.8690	1.8685	1.8681	1.8655	1.8651	1.8656

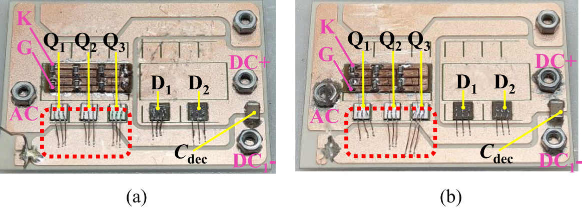


Fig. 15. Overviews of the (a) initial and (b) optimized baseline power modules.

It is desirable that the i_{kn} is equal to i_{gn} (n = 1, 2, 3), which suggests that the drive loop is fully decoupled with the power loop. In this section, the differential currents between drive source and gate for paralleled dies are extracted to evaluate the coupling degree between drive loop and power loop (see in Fig. 14). It can be seen that the maximum differential current between drive source and gate for paralleled dies in the optimized module fall by a factor of six and five at turn-OFF and turn-ON transients, respectively, compared to counterparts in the initial power module. The results suggest that the optimized method can help decouple the drive loop with the power loop.

In general, the simulation results suggest that the proposed method can effectively suppress the unbalanced switching current and decouple the drive loops with power loops for paralleled dies in the multichip SiC power modules with Kelvin-source connection.

C. Experiments Verifications

The SiC MOSFETS (S4102) and SiC Schottky diodes (S6305) from ROHM are employed as paralleled dies and free-wheeling diodes, respectively. The dies are preselected by Agilent 1505 to avoid mismatches of device parameters. The parameters of dies in the prototypes are shown in Table IV. In the experiments, the bonding wires are realized by manual operation with a simple wire bonding machine. Then two baseline power modules are fabricated (see in Fig. 15). For commercial automatic wire bonding machines, the accuracy for the placement of bonding wires is ±5 μm, which can better realize the optimized wire bonding scheme [34]. In other words, the proposed method is well compatible with the manufacturing technologies for the mass production of power modules.

A test bench is built up (see in Fig. 16) to evaluate the performance of the two baseline modules. The current sensors are Rogowski coils (30 MHz/120 A) from PEM, whose maximum error caused by undesired noises is 0.3 A [35, 36]. The consistency of the two Rogowski coils, CWT1 and CWT2, is

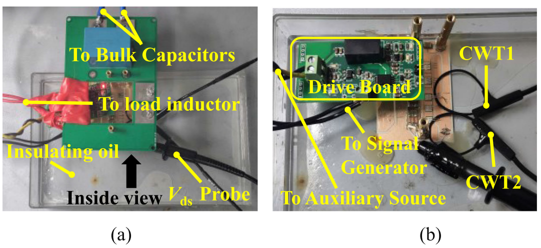


Fig. 16. Experimental test rig. (a) Top view of the test rig. (b)Inside view of the test rig.

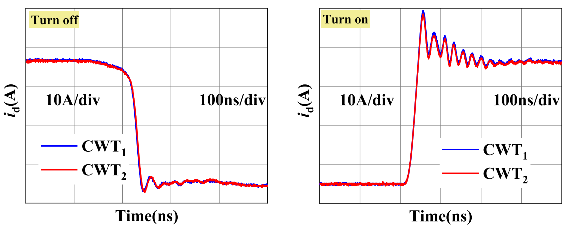


Fig. 17. Verification of the consistency of the two Rogowski coils by measuring the current of Q_3 in the initial power module.

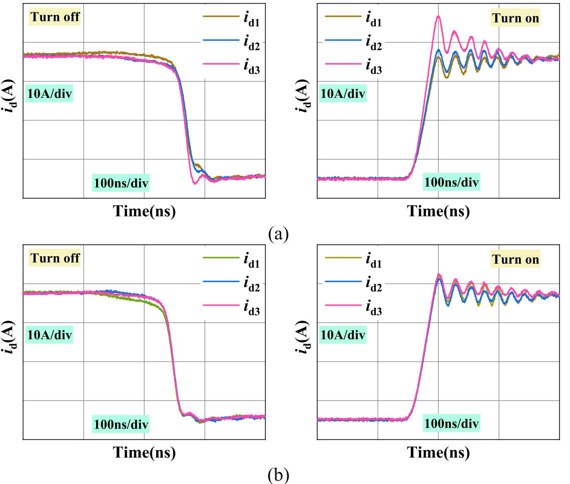


Fig. 18. Experimental waveforms of drain current at turn-OFF and turn-ON transients for the (a) initial and (b) optimized baseline power modules.

verified by measuring the current of Q_3 in the initial power module. The results suggest the Rogowski coils are of good consistency as is shown in Fig. 17. The power modules are placed into a tank filled with oil rather than encapsulated by silica gel for the convenience of current measurement. The bus voltage is limited at 300 V to avoid the partial discharge. Though the bus voltage of 300 V is lower than the practical bus voltage for SiC MOSFETs, the test results are representative. The switching current waveforms are depicted in Fig. 18 when the load current (I_L) is 105 A, $R_{\rm gon}$ is 4.1 Ω and $R_{\rm goff}$ is 8.2 Ω.

To comprehensively evaluate the performance of the proposed method, extensive experiments are conducted when I_L increases from 30 to 105 A, the $R_{\rm gon}$ is 3.1, 4.1, or 6 Ω and the $R_{\rm goff}$ is 6.2, 8.2, or 12 Ω. The $\Delta i_{\rm on}$ and $\Delta i_{\rm off}$ are extracted as is shown in Fig. 19. All the results above suggest that the dynamic current imbalance can be well suppressed in the optimized module.

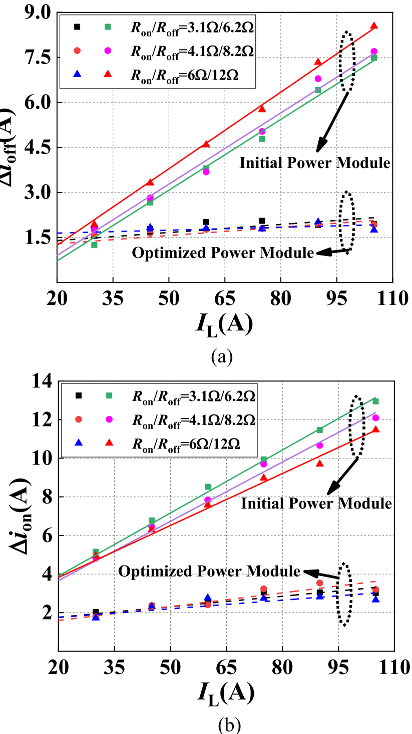


Fig. 19. (a) $\Delta i_{\rm off}$ and (b) $\Delta i_{\rm on}$ in the initial and optimized baseline power modules under conditions with various load current and drive resistance.

The effect of the optimized method on the total switching loss imbalance is also investigated when the I_L is 105 A. To comprehensively investigate the effect of the proposed method on unbalanced total switching losses, the ΔE_S and E_T of the initial and optimized power modules are extracted when various $R_{\rm gon}$ and $R_{\rm goff}$ are employed (see in Tables V and VI). For parallel operation of SiC MOSFETs, larger branch parasitic inductance always result in smaller turn-ON losses ($E_{\rm on}$) but more turn-OFF losses ($E_{\rm off}$) for the SiC MOSFET in the branch [32]. Thus, when the layout is asymmetric, the unbalanced $E_{\rm on}$ can be compensated by unbalanced $E_{\rm off}$ to some degree. When the $R_{\rm goff}$ and $R_{\rm gon}$ are properly selected, the unbalanced $E_{\rm on}$ and unbalanced $E_{\rm off}$ can well compensate for each other to achieve small unbalanced total switching losses even though the layout is much asymmetric. In these cases, the optimized method can hardly reduce the unbalanced total switching losses further. In the cases listed in Table V, when $R_{\rm gon}$ is fixed, the $|\Delta E_{S({\rm optimized})}-\Delta E_{S({\rm initial})}|$ is related to $R_{\rm goff}/R_{\rm gon}$. When $R_{\rm goff}/R_{\rm gon}$ is close to a specific value, which is approximately between 2.33 and 2.46, the compensation effect between unbalanced $E_{\rm on}$ and $E_{\rm off}$ will be more significant to decrease the $|\Delta E_{S({\rm optimized})}-\Delta E_{S({\rm initial})}|$. The specific value of the special $R_{\rm goff}/R_{\rm gon}$ will be researched in the future. When the $R_{\rm gon}$ is fixed at 3.1 or 4.1 Ω and the $R_{\rm goff}$ increases from 6.2 to 12 Ω, the $R_{\rm goff}/R_{\rm gon}$ is first close to and then far away from the special value. Thus, the $|\Delta E_{S({\rm optimized})}-\Delta E_{S({\rm initial})}|$ decreases first and then increases with $R_{\rm goff}$. When the $R_{\rm gon}$ is 6 Ω and the $R_{\rm goff}$ increases from 6.2 to 12 Ω, the $R_{\rm goff}/R_{\rm gon}$ is close to the special value all the time. Thus, the $|\Delta E_{S({\rm optimized})}-\Delta E_{S({\rm initial})}|$

TABLE V
MAXIMUM UNBALANCED TOTAL SWITCHING LOSSES FOR THE INITIAL AND OPTIMIZED POWER MODULES WITH VARIOUS DRIVE RESISTANCE

	R_{gon}=3.1Ω R_{goff}=6.2Ω	R_{gon}=3.1Ω R_{goff}=8.2Ω	R_{gon}=3.1Ω R_{goff}=12Ω	R_{gon}=4.1Ω R_{goff}=6.2Ω	R_{gon}=4.1Ω R_{goff}=8.2Ω	R_{gon}=4.1Ω R_{goff}=12Ω	R_{gon}=6Ω R_{goff}=6.2Ω	R_{gon}=6Ω R_{goff}=8.2Ω	R_{gon}=6Ω R_{goff}=12Ω
R_{goff} / R_{gon}	2.00	2.65	3.87	1.51	2.00	2.93	1.03	1.37	2.00
$\Delta E_{S(Initial)}$ (μJ)	38.17	25.34	85.33	48.61	29.86	74.62	70.50	51.75	63.28
$\Delta E_{S(Optimized)}$ (μJ)	21.29	25.08	47.21	22.58	30.37	54.83	24.81	30.90	55.36
($\Delta E_{S(Optimized)} - \Delta E_{S(Initial)}$) (μJ)	– 16.88	– 0.26	– 38.12	– 26.03	+0.51	– 19.79	– 45.69	– 20.85	– 7.92

TABLE VI
TOTAL SWITCHING LOSSES OF THE INITIAL AND OPTIMIZED POWER MODULES WITH VARIOUS DRIVE RESISTANCE

	R_{gon}=3.1Ω R_{goff}=6.2Ω	R_{gon}=3.1Ω R_{goff}=8.2Ω	R_{gon}=3.1Ω R_{goff}=12Ω	R_{gon}=4.1Ω R_{goff}=6.2Ω	R_{gon}=4.1Ω R_{goff}=8.2Ω	R_{gon}=4.1Ω R_{goff}=12Ω	R_{gon}=6Ω R_{goff}=6.2Ω	R_{gon}=6Ω R_{goff}=8.2Ω	R_{gon}=6Ω R_{goff}=12Ω
$E_{T(Initial)}$(μJ)	2702.40	2989.05	3651.05	2942.30	3228.95	3890.95	3434.49	3721.15	4383.14
$E_{T(Optimized)}$ (μJ)	2738.96	3124.22	3728.31	2973.62	3358.88	3962.97	3437.88	3823.14	4427.23
$\frac{E_{T(Optimized)} - E_{T(Initial)}}{E_{T(Initial)}} \times 100\%$	+1.4%	+4.5%	+2.1%	+1.1%	+4.0%	+1.9%	+0.1%	+2.7%	+1.0%

just decreases with $R_{\rm goff}$. It can be seen that the ΔE_S of the optimized module decrease a lot compared with the ΔE_S of the initial module in most cases while, in some special cases, the ΔE_S almost keeps constant when the optimized method is employed. Thus, the optimized method can generally mitigate the unbalanced total switching losses. The E_T in the optimized power module just increases a little compared to that in the initial power module, which suggests the optimized method will not decrease the efficiency of the power modules.

VI. CONCLUSION

This article proposes a method to balance dynamic current in multichip SiC power modules with Kelvin-source connection. Specifically, the connection points of power source bonding wires and copper traces are optimized to suppress dynamic current imbalance. The response surface models of the parasitic inductance and nonlinear constrained optimization algorithms are combined together for the first time to help determine the optimized positions of connection points. The proposed method is cost-efficient and well compatible with the traditional manufacturing technologies of multichip power modules because there need not be additional efforts except some modifications on the bonding wires. The simulation results indicate that the method can help decouple the power loop and drive loop. Both simulation and experimental results verify that the proposed method can well suppress the dynamic current imbalance in the multichip SiC power modules with Kelvin-source connection under condition with various load current and drive resistance.

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