Sawtooth Carrier-Based PWM Methods With Common-Mode Voltage Reduction for Symmetrical Multiphase Two-Level Inverters With Odd Phase Number

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***Abstract*—The increased phase number of multiphase systems enables us to exploit more degrees of freedom, such as the shape of phase carriers in pulsewidth modulation (PWM). The sawtooth carrier-based PWM (SCPWM) techniques are proposed in this article to reduce common-mode voltage (CMV) in both the peak-to-peak amplitude and the changing frequency, and it can be easily extended to symmetrical multiphase two-level inverters with any odd phase number. Theoretical analysis reveals that the switching between mirror-symmetrical carriers within one phase narrows the range of the sum of switching states in all phases, which leads to the reduction of CMV amplitude. Meanwhile, the overlapping of sawtooth carriers' straight edges among different phases slows down the change of the sum of switching states, which results in the decrease of CMV changing frequency. Moreover, the effects of voltage harmonics injection and switches' dead-time settings on the CMV reduction performance under the proposed SCPWM techniques are investigated. Finally, the experiment results in a five-phase induction machine and multiphase RL loads verify the improved CMV performance and the extensibility of the proposed SCPWM methods.**

***Index Terms*—Common-mode voltage (CMV), multiphase voltage-source inverter (VSI), pulsewidth modulation (PWM), sawtooth carrier.**

I. Introduction

MULTIPHASE drive systems are gaining increasing popularity due to their advantages of enhanced reliability, reduced torque ripple, and decreased power rating in each phase over the traditional three-phase counterparts [1]. Accordingly, multiphase machines are attracting growing attention in safety-critical and/or high-power applications. Due to their high reliability and high efficiency, a five-phase interior permanent magnet machine was designed for hybrid electric vehicles [2]. In 2017, Yanzhou Dongfang Company developed a 6-kV nine-phase induction motor drive system for the application of underground coal mining [3]. A 1.1-MW nine-phase PMSM was developed as a traction motor for an ultrahigh-speed elevator, and the feasibility and validity of the drive system were demonstrated at the world's tallest elevator test tower of that time [4]. As for the 15-phase motors, they are gaining increasing applications in electric ship propulsion systems, such as the type 45 destroyer and Queen Elizabeth aircraft carrier of the U.K. Royal Navy commissioned in 2009 and 2017, respectively. Additionally, a 35-kW 15-phase induction motor drive system was suggested to be applied in the CNC (computer numerical control) machining application [8].

Common-mode voltage (CMV) is one of the side effects in drive systems fed by pulsewidth-modulated (PWM) inverters. The high-amplitude and high-frequency CMV would not only lead to bearing damages [9]–[11] but also bring about undesirable electromagnetic interference (EMI) problems [12], [13]. The bearing damages caused by CMV are mainly due to the dv/dt-induced bearing currents and electric discharge machining (EDM) currents. The dv/dt current flowing through the bearing accelerates the insulation aging, and it flows whenever the shaft voltage, which is a replica of CMV, undergoes a change [10]. The EDM current is accompanied by the oil film dielectric breakdown, and it is generated whenever the shaft voltage buildup across the stray capacitance exceeds the breakdown limit of the thin lubricant around the bearings [11]. Moreover, the CMV changing frequency, which refers to the frequency of voltage steps, in other word, the equivalent frequency of the time during the voltage slope of the CMV, relates to the switching frequency, and the EMI emissions deteriorate with the increasing changing frequency of CMV [14]. Therefore, all the three factors, including the step-value, the amplitude, and the changing frequency are important performance indicators of CMV. Since the step-value is inherently reduced to $V_{\rm dc}/m$ in the multiphase two-level inverters, this article concentrates on the reduction of CMV in the amplitude and changing frequency.

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To reduce the CMV, both hardware and software solutions have been proposed over the past few decades. In most of the hardware cases, passive or active CMV filters are added to the inverter [15], [16], which inevitably increase the size and substantial cost of the system. By contrast, the software solutions gain more popularity, which aim to reduce the CMV by improving the PWM methods.

Most of the CMV-reducing PWM methods belong to the modified SVPWM type, which are realized by selecting those voltage space vectors that give out very low or even zero CMV.

Modified SVPWM methods for five-phase two-level inverters were proposed in [17] and [18], which can reduce the peak-to-peak CMV by 40% or 80%. Nevertheless, the effect of voltage vectors on multiple subspaces need to be considered, which makes the computation burden of SVPWM growing exponentially as the phase number increases. A generic CMV-elimination SVPWM technique was proposed in [19], which simplifies the computation complexity to make it convenient to be extended to any multiphase occasion. Unfortunately, this method is only suitable for multiphase multilevel occasions, where extra voltage levels and redundant voltage vectors can be utilized. In fact, regardless of the type of ac machines and the number of phases, the most common voltage-source inverter (VSI) for multiphase applications is still the two-level type [20]. Chen *et al.* [21] proposed a generalized PWM method with minimum CMV for multiphase two-level VSIs with any odd phase number m, which suppresses the CMV to only two minimum levels, and therefore, achieves a CMV reduction rate of 80% and 85% for the five-phase and seven-phase two-level inverters, respectively. However, this kind of PWM aims at sinusoidal output voltage on RL loads, without considering the harmonic characteristics of multiphase machines [22], [23]. Besides, only the CMV amplitude is reduced, while the CMV changing frequency remains the same as conventional PWM methods.

Alternatively, the carrier-based PWM (CPWM) methods better suit the multiphase occasions, because they are independent of the phase number and can be naturally extended to any multiphase VSI [24]. By modifying the two modulating waves for each phase, CMV-reduction CPWM methods were proposed for a five-phase VSI [25]. But the coupled inductor is required in the inverter, which turns it to be a three-level topology. Triangle carriers with a uniform phase lag of $2\pi/m$ are employed in the phase-shifted sinusoidal PWM (PS-SPWM) [26], where the CMV could be completely eliminated in symmetrical inverters with an even phase number. However, for the inverters with odd phase numbers, the CMV reduction effect of PS-SPWM is undermined as the modulation index increases. Xiong *et al.* [27] proposed a reduced CMV carrier-based modulation (RCMV-CBM) for the five-phase inverter with RL loads, where the opposite triangle carriers are applied to the second and fourth largest modulating waves. Though the peak-to-peak value of CMV is reduced by 80%, the changing frequency of CMV remains the same. Besides, experiments in [27] were conducted on RL loads, while further verifications on multiphase machines are lacking. Recently, triangle carriers were suggested in [28] to reduce both the amplitude and the changing frequency of CMV, but the proposed PWM method only applies to asymmetrical dual-three phase inverters.

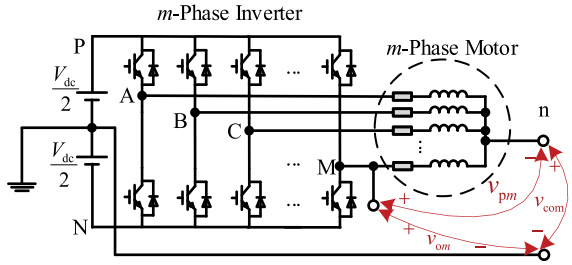

Fig. 1. CMV of an m-phase two-level inverter.

Because of easier extensibility to general multiphase cases, this article concentrates on the CPWM methods. Considering that the CMV can be completely eliminated in symmetrical multiphase inverters with even phase number using PS-SPWM, this article proposes modified CPWM methods for symmetrical multiphase two-level inverters with odd phase numbers. Additionally, this article analyzes the effects of low-order phase voltage harmonic injection and switches' dead time on CMV reduction of the proposed PWM methods.

The organization of this article is as follows. Section II analyzes the CMV of an m-phase two-level inverter. Then, the conventional CPWM, RCMV-CBM [27], and two proposed sawtooth carrier-based PWM (SCPWM) methods with CMV reduction are introduced and compared in Section III. Section IV discusses the effects of carrier switching on the output phase current. Then, the effects of harmonic injection and switches' dead time on CMV under SCPWM methods are discussed in Sections V and VI, respectively. Experiment results on a five-phase induction machine (IM) and multiphase RL loads in Section VII verify the theoretical analysis. Finally, Section VIII concludes the article.

II. CMV of Multiphase Inverter

Usually, the CMV refers to the potential difference buildup across the entire load with respect to the earth ground. In this article, the CMV is defined as the voltage $v_{\rm com}$ between the motor neutral point and the midpoint of the inverter's dc-link bus, which is shown in Fig. 1. Moreover, v_{oi} and v_{pi} are the output voltage and phase voltage of the ith phase, respectively. The relationship among these three voltages can be expressed as

$$v_{\rm com} = \frac{1}{m}\sum_{i=1}^{m} v_{oi} \tag{1}$$

$$v_{pi}(t) = v_{oi}(t) - v_{\rm com}(t). \tag{2}$$

Assuming $S_i \in \{0, 1\}$ denotes the switching states of the ith two-level VSI leg, then $\sum_{i=1}^{m} S_i = 0, 1, 2, \ldots, m$ corresponds to the $\sum_{i=1}^{m} v_{oi} = (-m/2)V_{\rm dc},\ (-m/2+1)V_{\rm dc},\ (-m/2+2)V_{\rm dc},\ \ldots, (m/2)V_{\rm dc}$, which finally results into $v_{\rm com} = (-1/2)V_{\rm dc},\ (-1/2+1/m)V_{\rm dc},\ (-1/2+2/m)V_{\rm dc},\ \ldots, (1/2)V_{\rm dc}$, respectively. Therefore, for the m-phase two-level inverter, $(m+1)$ possible values of $\sum_{i=1}^{m} S_i$ lead to $(m+1)$ possible levels of $v_{\rm com}$.

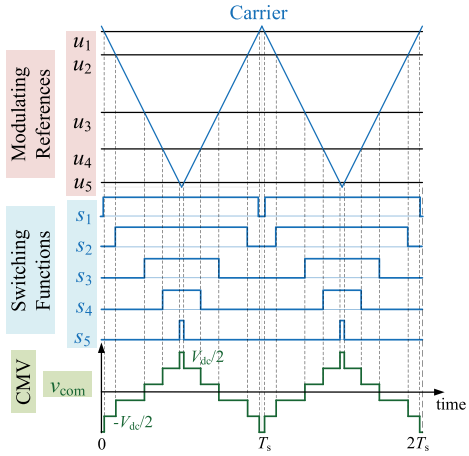

Fig. 2. Switching states and CMV of a five-phase VSI under conventional CPWM.

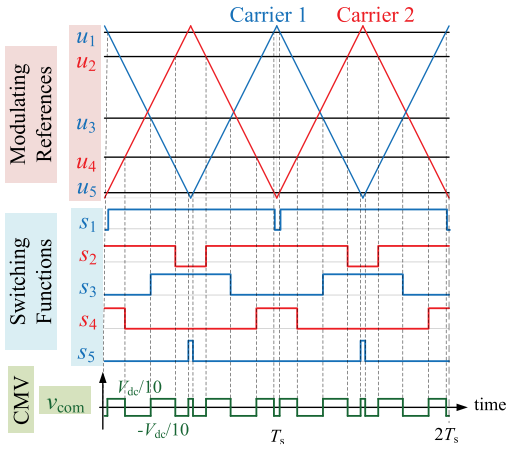

Fig. 3. Switching states and CMV of a five-phase VSI under RCMV-CPWM.

III. CPWM With CMV Reduction

A. Conventional CPWM

In the conventional CPWM, all the phases employ the same triangle carrier. Taking the five-phase system as an example, the switching patterns are shown in Fig. 2, where u_1 to u_5 stand for the maximum to minimum modulation references, and s_1 to s_5 stand for the respective switching states. All the switching pulses are distributed around center, and the sum of the switching states varies from 0 to 5. Therefore, the CMV waveform has six levels. Obviously, when extended to a general m-phase inverter, the CMV waveform has $m+1$ levels, with the sum of switching patterns varying from 0 to m.

B. Reduced CMV Carrier-Based Modulation

Considering that the sum of switching states corresponds to the level of CMV, we can reduce the CMV amplitude by limiting the sum of switching states in a narrow range. If triangle waves with opposite phase positions were applied to specific phases and the distribution of switching pulses would be double-sided rather than central, this provides the possibility to recombine the switching pulses.

Extending RCMV-CBM to general m-phase occasions, the reference values for m phases are sorted from high to low, and marked as u_1 to u_m. Then, two reference groups are divided according to the odd or even subscript. Normal triangle carriers marked in black are applied for the phases in the first group, while opposite triangle carriers marked in red are applied in the second group. By recombining the double-sided or central switching states, the sum of switching states can be fixed at two values of $(m-1)/2$ and $(m+1)/2$, and therefore, the CMV is suppressed two levels of $(-1/2m)V_{\rm dc}$ and $(1/2m)V_{\rm dc}$. As shown in Fig. 3, taking the five-phase case as an example, opposite triangle carriers are applied to the second group composed of u_2 and u_4, so the distributions of u_2 and u_4 are double-sided. As a result, the sum of five switching pulses varies between the values of 2 and 3, which means that the CMV is suppressed to two levels of $(-1/10)V_{\rm dc}$ and $(1/10)V_{\rm dc}$.

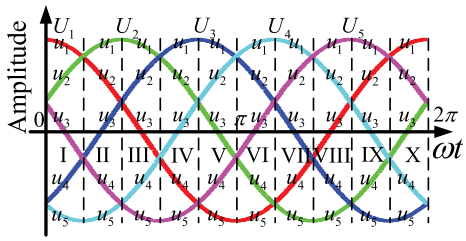

Fig. 4. Ten sectors of the five-phase sinusoidal modulation waves.

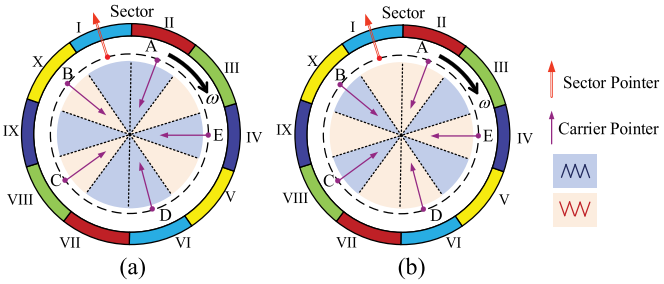

Fig. 5. Carriers in one fundamental period for the five-phase system under RCMV-CBM of (a) Type I and (b) Type II.

For the kth phase in a general symmetrical m-phase inverter, the sinusoidal modulating reference is expressed as follows, where $U_{\rm o}$ and ω are the amplitude and angular speed of the sinusoidal reference voltage, respectively:

$$U_k = U_{\rm o} \cdot \cos\left(\omega t + \frac{2\pi \cdot (k-1)}{m}\right) \quad (k = 1, 2, 3, \ldots, m). \tag{3}$$

Because the sinusoidal modulating wave is time-varying in reference value, the sorted u_1 to $u_{\rm k}$ do not correspond to U_1 to U_k of the natural order. For an m-phase system, the relationship between reference values of m phases can be divided into $2m$ sectors during each fundamental period. For the five-phase case shown in Fig. 4, each fundamental period can be divided into ten sectors. Consequently, for a specific phase, the applied triangle carrier might change as its located sector varies. Fig. 5 illustrates

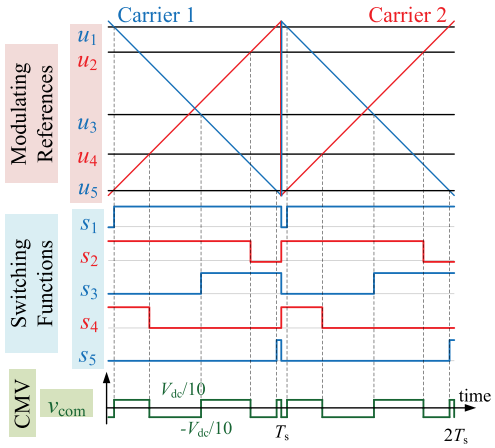

Fig. 6. Switching states and CMV of a five-phase VSI under SCPWM-1 of Type I.

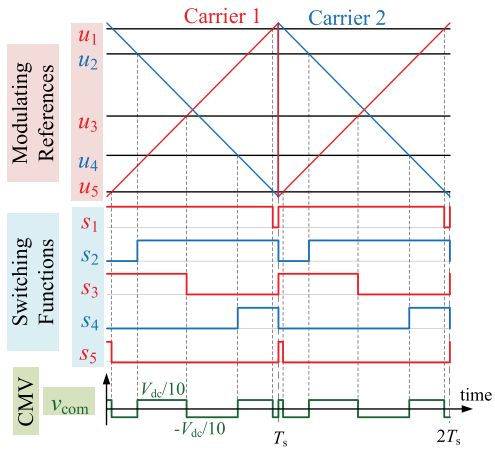

Fig. 7. Switching states and CMV of a five-phase VSI under SCPWM-1 of Type II.

the applied carrier of each phase in different sectors. The outer circumference corresponds to a fundamental period, and the sector pointer and carrier pointer rotate around the center of the circle at the angular speed ω. The sector pointer indicates the current sector among all the ten sectors in Fig. 4, and the carrier pointer indicates the kind of carrier adopted for the respective stator phase in the current sector. As shown in Fig. 5, under RCMV-CBM in the five-phase case, the carrier for each phase changes eight times during a fundamental period. The adoption of triangle carriers in Fig. 5(a) corresponds to Fig. 3. However, if the triangle carriers for the two groups are exchanged, as shown in Fig. 5(b), the same CMV reduction effect can still be obtained.

C. Sawtooth Carrier-Based PWM-1

The sawtooth carrier has a straight edge, which enables the coincidence of switching times in different phases, and therefore, provides the possibility of reducing the CMV changing frequency. In the proposed SCPWM-1, which is evolved from RCMV-CBM, the left-slanting and right-slanting sawtooth carriers are employed to replace the normal and opposite triangle carriers. Similar to RCMV-CBM, SCPWM-1 is applicable to any m-phase occasion, with left-slanting and right-slanting sawtooth carriers employed for two reference groups, respectively.

For the five-phase case, the switching patterns and respective CMV waveform are shown in Fig. 6, where three left-slanting and two right-slanting carriers (Type I) are employed. Clearly, the CMV changes only six times under SCPWM-1 during one switching cycle, which is lower than ten times under RCMV-CBM in Fig. 3. When extended to general m-phase occasions, it can be obtained that the CMV changes $(m + 1)$ times under SCPWM-1, compared with $2m$ times under conventional CPWM and RCMV-CBM methods, which employ triangle carriers.

D. Sawtooth Carrier-Based PWM-2

The change of carrier for one phase during a fundamental period inevitably deteriorates the output voltage (current) distortion of the CPWM, which will be discussed in Section IV.

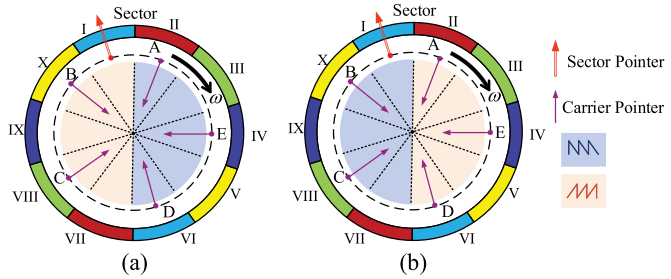

Fig. 8. Carriers in one fundamental period for the five-phase system under SCPWM-2 of (a) Type I and (b) Type II.

Actually, two left-slanting and three right-slanting carriers in Fig. 7 can result in the same CMV amplitude and frequency as those three left-slanting and two right-slanting carriers in Fig. 6. Providing that different types of sawtooth carriers were adopted for the references with odd and even subscripts, the same CMV performance in peak-to-peak amplitude and changing frequency would be achieved.

In the proposed SCPWM-2, Types I and II of SCPWM-1 are alternately adopted when the sector changes, and similar CMV performance can be achieved as that of SCPWM-1. What is more, the carrier for each phase changes only two times during one fundamental period under SCPWM-2, as shown in Fig. 8. In contrast, the number of carrier change times is eight under SCPWM-1, which is the same as RCMV-CBM shown in Fig. 5. Therefore, the proposed SCPWM-2 method manages to reduce the carrier change times by 75%. It can be derived that when extended to the general m-phase case, the carrier for one phase changes only two times under SCPWM-2, compared with $2m - 2$ times under SCPWM-1. The optimization of carrier changing times will effectively improve the quality of output phase current, which will be illustrated in Section IV.

It should be noted that SCPWM-2 also has two types of carrier selections depending on which kind of sawtooth carriers is applied first, as shown in Fig. 8(a) and (b). Section VI will discuss which kind is better, considering the dead-time effects and the rotating directions.

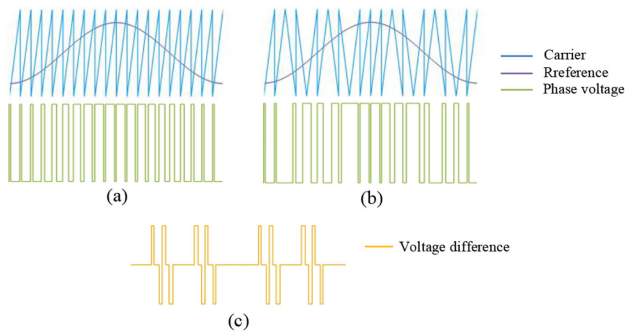

Fig. 9. Waveforms of (a) conventional SCPWM, (b) SCPWM-1, and (c) their difference.

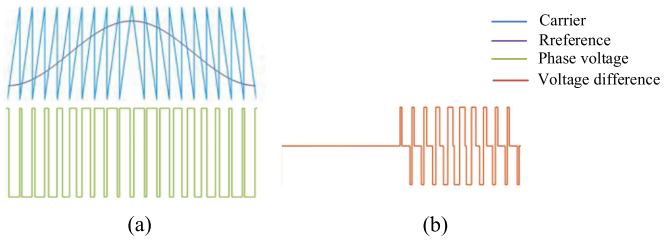

Fig. 10. Waveforms of (a) SCPWM-2 and (b) its difference from conventional SCPWM.

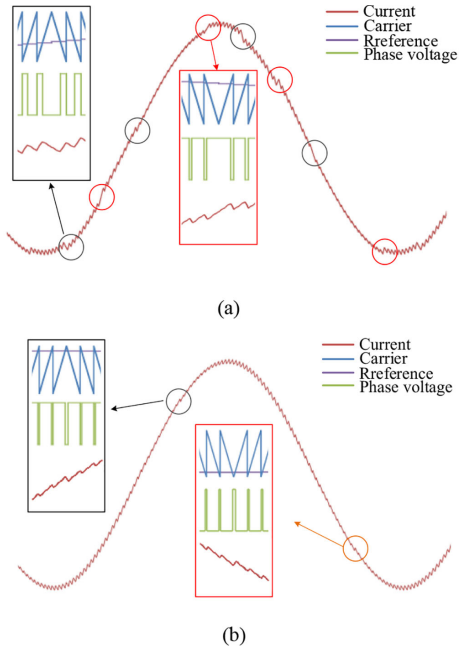

Fig. 11. Changes of sawtooth carriers and their impacts on phase current under (a) SCPWM-1 and (b) SCPWM-2.

IV. Effects of Carrier Switching on the Output Current

The PWM aims to generate a series of switched pulses that have the same volt-second average as the modulation reference waveform in any of the switching cycles. However, unwanted harmonics are contained in these switched voltage pulses, which will finally lead to the distortion of the output current from the desired sinusoidal waveform. In motor drive applications, low-order phase voltage harmonics account more for the distortion of phase current than the high-order ones.

According to the double Fourier integration analysis of the phase voltage expressions under naturally and regularly sampled PWM methods [29], the naturally sampled PWM is the most ideal in terms of low-order harmonics, and any modification from the naturally sampled PWM would unavoidably increase the low-order baseband harmonics.

The naturally sampled SCPWM refers to the conventional CPWM in Fig. 2 that employs only one kind of sawtooth carrier. However, the proposed SCPWM-1 and SCPWM-2 have switches between the left- or right-slanting sawtooth carriers during a fundamental period shown in Figs. 5 and 8. As shown in Fig. 9, the phase voltage of SCPWM-1 in Fig. 9(b) can be regarded as the superposition of the waveform in Fig. 9(c) over the phase voltage of the ideal naturally sampled SCPWM in Fig. 9(a). Therefore, the characteristics of the injected waveform in Fig. 9(c) decide the low-order baseband harmonics of SCPWM-1. Obviously, the waveform in Fig. 9(c) contains redundant harmonics, especially the fourth order. The injected waveform for SCPWM-2 is shown in Fig. 10(b), and its low-order harmonics would be lower than those in Fig. 9(c) because of reduced carrier switch times and better symmetry.

Phase current waveforms of the two SCPWM methods are further compared in Fig. 11, where the black box indicates that the switch from right- to left-slanting sawtooth carriers would lead to a triangle carrier with upward angle, while the red box indicates a triangle carrier with downward angle generated by the switch from left- to right-slanting sawtooth carriers. Actually, the change of the sawtooth carriers in neighboring cycles leads to a triangle carrier that lasts for two switching cycles. This deterioration of phase current can be identified from the black and red boxes in Fig. 11, where the current ripples during the two carrier-switch cycles are obviously larger than those during normal sawtooth cycles. Fortunately, by optimizing the carrier-switch patterns, the SCPWM-2 has only two carrier-switch transients in a fundamental period, and therefore, its current waveform is relatively smoother than that under SCPWM-1, which has eight carrier-switch transients. Therefore, the SCPWM-2 outweighs SCPWM-1 in the total harmonic distortion (THD) of the output phase current.

V. Effects of Harmonics on CMV Reduction

For multiphase machines, the injection or suppression of harmonics in phase current is usually required to optimize the operation [30], [31]. The regulation of current harmonics is achieved by the injection of corresponding voltage harmonics in the VSIs. Therefore, it is necessary to investigate the effects of voltage harmonic injection on the CMV performance of our proposed SCPWM methods.

In these three CMV-reduction CPWM techniques (RCMV-CBM, SCPWM-1, and SCPWM-2), the reference values are sorted from high to low in each sector, and marked as u_1 to u_m, complying with $u_i \geq u_{i+1}\,(i = 1, 2, \ldots, m-1)$, as shown in Fig. 4. Then, according to the odd or even subscript,

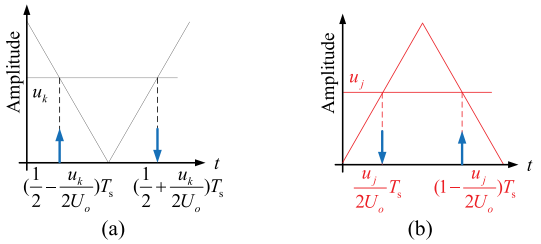

Fig. 12. Rising and falling edges for the (a) normal and (b) opposite triangle carriers.

two reference groups are divided, which employ two mirror symmetrical carriers during the modulation. In this way, the rising and falling edges of the phase output voltage are alternated, and therefore, the amplitude of CMV is suppressed, as shown in Figs. 3, 6, and 7. The rising and falling edges for different triangle carriers are shown in Fig. 12, and the alternation of rising and falling edges under sorted references calls for expressions (4) and (5), where $k = 1, 3, 5, \ldots, m-2$. Both of the two inequalities can be simplified into (6). It can be proved that the inequality (6) is also required in CMV-reduction PWM methods when employing symmetrical sawtooth carriers

$$\left(\frac{1}{2}-\frac{u_k}{2U_o}\right)T_s < \left(\frac{u_{m-k}}{2U_o}\right)T_s < \left(\frac{1}{2}-\frac{u_{k+2}}{2U_o}\right)T_s \quad (4)$$

$$\left(\frac{1}{2}+\frac{u_{k+2}}{2U_o}\right)T_s < \left(1-\frac{u_{m-k}}{2U_o}\right)T_s < \left(\frac{1}{2}+\frac{u_k}{2U_o}\right)T_s \quad (5)$$

$$U_o - u_k < u_{m-k} < U_o - u_{k+2}. \quad (6)$$

With injected harmonics, the reference voltage for the kth phase can be expressed as follows, where σ_γ and φ_γ are the injection ratio and phase lag of the γ^{th} harmonic compared to the fundamental wave, respectively:

$$U_k' = U_k + U_o \cdot \sum_{\gamma=3,5,7,\ldots,(m+1)/2} \sigma_\gamma \cdot \cos\left(\gamma\left(\omega t + \frac{2\pi\cdot(k-1)}{m}\right)+\varphi_\gamma\right) \quad (k=1,2,3,\ldots,m). \quad (7)$$

If the injection of harmonics breaks the inequality of (6), the rising or falling edges of phase voltages will be consecutive and the CMV reduction effect would be undermined. Considering that there are $2m$ sectors and $(m-3)/2$ possible harmonics for an m-phase system, it is rather complicated to check whether the inequality (6) holds in each sector. Therefore, offline numerical computation is suggested to find the feasible ranges of σ_γ and φ_γ that ensure the CMV reduction effect of CPWM techniques. The flowchart is shown in Fig. 13, where ε stands for the step-value of the circular computation and f is the result function defined as follows:

$$f\left[\left(\sigma_3,\sigma_5,\ldots,\sigma_{(m+1)/2}\right),\left(\varphi_3,\varphi_5,\ldots,\varphi_{(m+1)/2}\right)\right] = \begin{cases} 1 \text{ (inequality (6) holds)} \\ 0 \text{ (inequality (6) does not hold).} \end{cases} \quad (8)$$

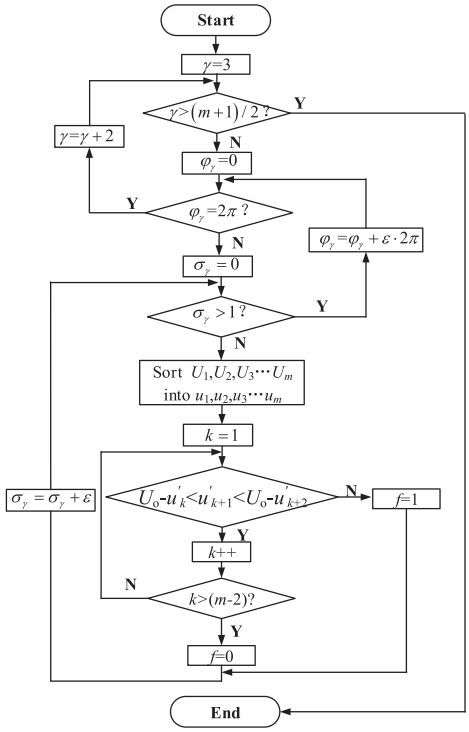

Fig. 13. Flow chart to find the CMV-reduction feasible region with injected harmonics.

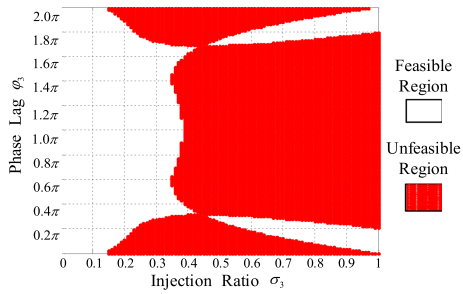

Fig. 14. CMV-reduction feasible and unfeasible regions with third harmonic injection for five-phase VSIs.

In the five-phase case, the result function $f(\sigma_3, \varphi_3)$ is plotted in Fig. 14. This figure tells that under modified CPWM techniques with injected third-harmonic reference voltage, if the operating point (σ_3, φ_3) locates in the feasible region, the CMV would be successfully suppressed to two levels; otherwise, the CMV would have more than two levels and CMV reduction effect would be undermined.

VI. Dead-Time Effects on CMV

All the preceding sections talk about the CMV in ideal conditions, where the output voltage waveform of the phase leg is supposed to be the same as its respective PWM waveform. Because the nonideal turn-ON and -OFF transients exist in the ON/OFF transient states of the switching devices, the dead-time protection is required to avoid the shoot-through of the upper and lower switches. However, the loads of multiphase inverters

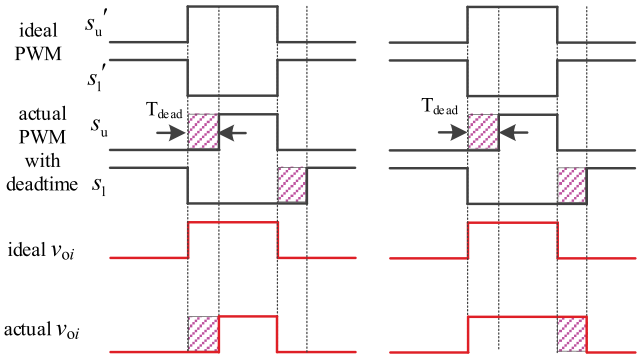

Fig. 15. Dead-time effects on the output voltage of the phase leg when the phase current (a) $i_p > 0$ and (b) $i_p < 0$.

usually present inductive characteristics, which indicates that the phase current lags behind the phase voltage, and therefore, the freewheeling effects due to the dead-time should not be neglected.

As shown in Fig. 15, the ideal PWM waveforms of upper and lower switches complement perfectly. When the dead time is added to the PWM before the switch turning ON, the complementary relationship breaks, and the switching ON moments of upper and lower are staggered. When the phase current $i_p > 0$, freewheeling exists in the antiparallel diode of the lower switch, and the step-up/down of the v_{oi} is decided by the switching ON/OFF of the upper switch, which is shown in Fig. 15(a). On the contrary, when the phase current $i_p < 0$, freewheeling exists in the antiparallel diode of the upper switch, and the step-up/down of the v_{oi} is decided by the switching ON/OFF of the lower switch, which is shown in Fig. 15(b). Therefore, the waveform of output voltage is not the same as the ideal PWM signal, and the actual CMV would be affected.

Taking the SCPWM-2 as an example, in the normal switching cycles without carrier changing, the ideal and actual CMV waveforms are shown in Fig. 16. In these two cycles, the modulation references $u_A > u_E > u_B > u_D > u_C$, which corresponds to the Sector X in Fig. 4. The inductive characteristic of the motor load supports the assumption that i_A, $i_E > 0$ and i_B, i_C , $i_D < 0$. According to Fig. 15, when the phase current is positive, the output phase voltage depends on the driving pulses of the upper switch S_{u_i} and vice versa. When the modulating references meet the sawtooth carriers, switching actions will occur. On the hypotenuse of the carrier, because the modulation references are different, their respective switching moments are different. Hence, these dead-time delays on phase voltages would not overlap, and they would be reflected as the delays of low or high voltage level in the CMV, shown in the red dashed circles pointed by red arrows in Fig. 16. Obviously, these dead-time delays would not affect the amplitude or the changing times of the CMV. However, on the vertical edge of the carrier, switching actions of different phase legs occur simultaneously, regardless of the modulation reference values. Phase legs adopting left-slanting sawtooth carriers would turn OFF the upper switch and turn ON the lower one, while phase legs adopting the right-slanting sawtooth carriers would turn ON the upper switch and turn OFF

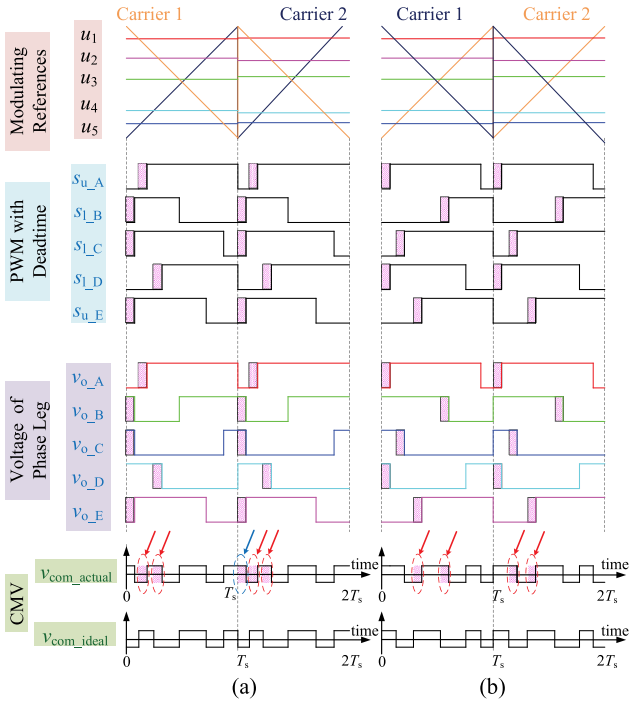

Fig. 16. Dead-time effects on CMV during the normal switching cycles with carrier selection patterns of (a) Type I and (b) Type II.

TABLE I
DEAD-TIME DELAY TYPES UNDER SCPWM-2 AT THE VERTICAL EDGE MOMENTS OF SAWTOOTH CARRIERS

Phases	Carrier Slanting Type	Switching Pulse		Voltage Depends on	Dead-time Delay Type
		S_{u_i}	S_{l_i}		
A	Left	$1 \to 0$	$0 \to 1$	S_{u_A}	–
B	Right	$1 \to 0$	$0 \to 1$	S_{l_B}	step down
C	Left	$1 \to 0$	$0 \to 1$	S_{l_C}	step down
D	Right	$0 \to 1$	$1 \to 0$	S_{l_D}	–
E	Right	$0 \to 1$	$1 \to 0$	S_{u_E}	step up

the lower one. According to the switching actions of SCPWM-2, the dead-time delay types can be listed in Table I. As the effects of the step-up and step-down types can cancel each other out, the combined delay effect of all the five phases is one step-down delay, shown in the blue dashed circles pointed by blue arrows in Fig. 16(a). When the left- and right-slanting sawtooth carrier groups are exchanged, the step-up delay in phase A and step-down delay in phase D will be neutralized, and therefore, there does not exist dead-time effects on the CMV at vertical edge moments in Fig. 16(b). However, even if the dead-time effect in the blue circle exists in Fig. 16(a), it would reflect as the delay of existing CMV voltage level, without affecting the CMV amplitude or the changing times.

In the carrier-changing cycles, the ideal and actual CMV waveforms are shown in Fig. 17, where Fig. 17(a) and (b) correspond to the transients from Sections X to I in Fig. 8(a) and (b), respectively. At the hypotenuses, dead-time effects are reflected

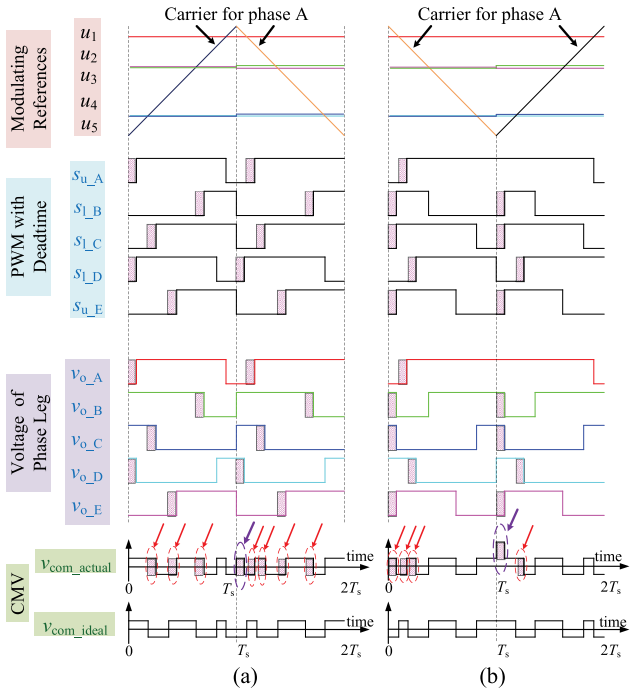

Fig. 17. Dead-time effects on CMV during the carrier-changing switching cycles with carrier selection patterns of (a) Type I and (b) Type II.

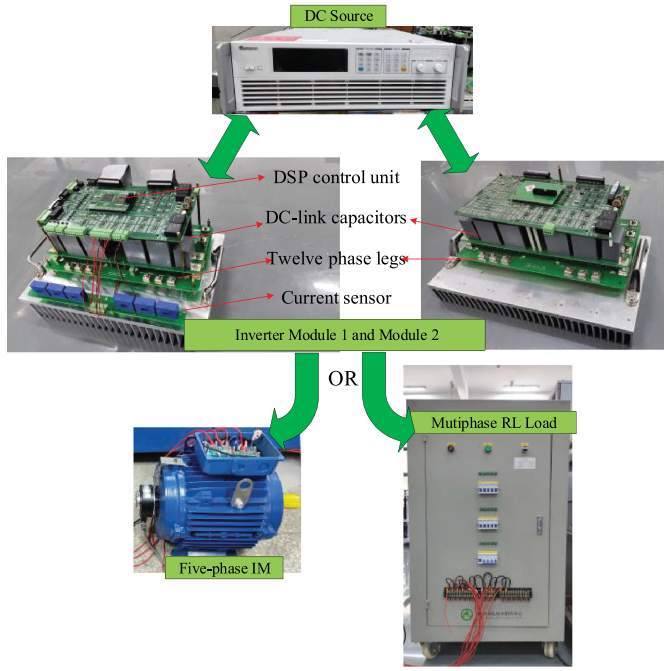

Fig. 18. Photograph of the experimental platform.

as the delays of voltage levels of the CMV in the red circles of Fig. 17, without affecting the amplitude or changing times of CMV, which are much the same to those in Fig. 16. However, because the carrier type changes for phase A at the end of the former cycle, a normal or opposite triangle carrier is created in Fig. 15, which lasts for two switching cycles. Consequently, the vertical carrier edge for phase A disappears in these two cycles, which avoids the instantaneous switching actions of phase A legs at the end of former cycle or the beginning of the latter cycle. Hence, the combined dead-time effect at the vertical edge moments only depends on phases B, C, D, and E. Applying similar analysis as Table I, it can be figured out that there is only one step-down in output voltage of phase D in Fig. 17(a), which will be reflected as a dead-time CMV spike in the purple circle. While at the vertical edge moments in Fig. 17(b), there are two step-down and one step-up delays, whose combined effect is also reflected as a dead-time CMV spike in the purple circle. However, the spikes in Fig. 17(a) and (b) have different effects on CMV. The spike in Fig. 17(a) is superimposed to the lower voltage level, so it only affects the changing times of CMV, while the spike in Fig. 17(b) is superimposed to the higher voltage level, and therefore, it affects both the amplitude and changing times of CMV. As for the carrier-changing transients for other phases, similar results can also be deduced. Considering that each CMV spike causes two voltage steps which are included into the former and latter switching cycles separately, the voltage steps of CMV in each switching cycle is still six times without the affection of dead time.

To summarize, though the two different selections of the carrier patterns in Fig. 8 have similar dead-time delay effects on CMV during normal switching cycles, they lead to different dead-time spike effects during the carrier-changing cycles. For the clockwise rotation in Fig. 8, which corresponds to the positive sequence of A-B-C-D-E, the type I carrier selection outweighs type II, because of no additional effects on CMV amplitude. On the contrary, for the counterclockwise rotation corresponding to the negative sequence of A-E-D-C-B, the type II carrier selection would be preferred, which does not increase the levels of CMV in this condition.

VII. Experiment Results

In the experiment, a multiphase inverter prototype with 12 phase legs is built. The controller of the whole inverter is a digital signal processor (DSP TMS320F28377), which has at most 12 independent PWM signals to drive the independent phase legs. It should be pointed out that the proposed PWM methods can also be implemented by analog circuits. The motor load is a five-phase IM, manufactured by rewinding the stator coils of a traditional three-phase machine with 30 slots, whose model is Y-132S-2. By diving stator phase windings into five stator phases with $2\pi/5$ electrical angle between adjacent phases, the number of slots per pole per phase is three. The RL load has 15 branches, and each branch is the series connection of a 10-Ω resistor and a 50-mH inductance. The photograph of the experimental platform is shown in Fig. 18 and parameters for the experiments are listed in Table II.

A. Comparison of Four CPWMs Under Rotor Field Oriented Control (RFOC)

In this section, the five-phase IM was driven at 3000 r/min under the RFOC, where closed-loop controllers for both the fundamental and third-harmonic currents are included [32]. For

TABLE II
PARAMETERS FOR THE EXPERIMENTS

Machine Parameters				Converter Parameters	
P_N	4 kW	L_{m1}	203.3 mH	$f_{\text{switching}}$	10k Hz
R_s	1.554 Ω	L_{ls}	14.8 mH	T_{dead}	1 uS
R_r	1.582 Ω	L_{lr}	7.6 mH	V_{dc}	200 V
p_n	1				

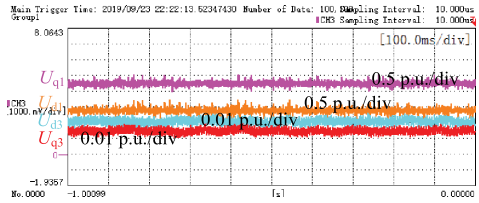

Fig. 19. Fundamental and third harmonic voltage references of the five-phase VSI.

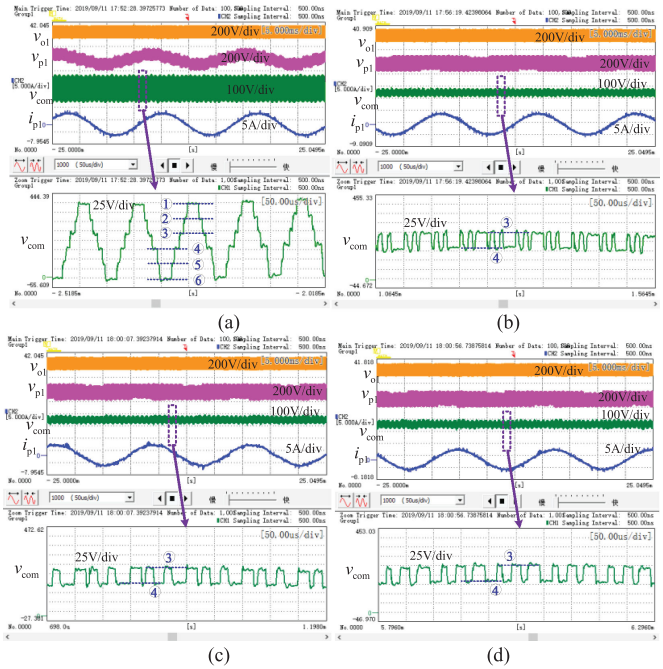

Fig. 20. Experiment results of CMV and phase current in five-phase RFOC drive case under (a) conventional CPWM, (b) RCMV-CBM, (c) SCPWM-1, and (d) SCPWM-2.

this five-phase IM with distributed stator windings, most of the electromechanical energy conversion occurs on the fundamental plane, and therefore, the third harmonic in phase current is suppressed to zero to improve the operation efficiency.

The fundamental and third-harmonic voltage references are shown in Fig. 19, and then, the operating point C can be calculated, which is ($\sigma_3 = 0.0169$, $\varphi_3 = 0.372\pi$). Obviously, the point C locates in the CMV-reduction feasible region of Fig. 14. Fig. 20 shows the waveforms of CMV v_{com}, along with the output voltage v_{o1}, phase voltage v_{p1}, and phase current i_{p1} of phase A. Clearly, the CMV has six levels under conventional

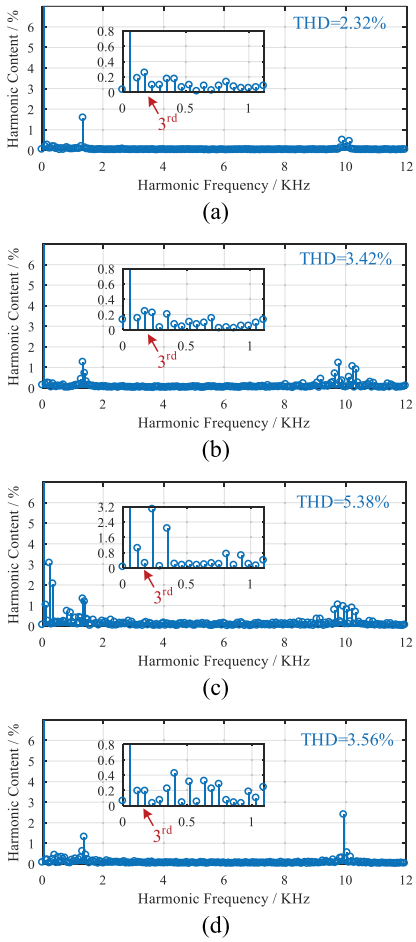

Fig. 21. FFT analysis of experiment phase current in five-phase RFOC drive case under (a) conventional CPWM, (b) RCMV-CBM, (c) SCPWM-1, and (d) SCPWM-2, with magnified view of harmonics lower than the 20th order.

CPWM in Fig. 20(a), while it decreases to two levels under the three modified CPWM methods in Fig. 20(b)–(d). In particular, $v_{\text{com-pp}}$ decreases from 200 V to about 50 V, which corresponds to the 80% reduction rate in the theoretical analysis. Additionally, the CMV changes six times during one switching cycle under the two SCPWM methods in Fig. 20(c) and (d), which is 40% less than ten times in Fig. 20(a) and (b).

The fast Fourier transform (FFT) analysis in Fig. 21 demonstrates that the three modified CPWM methods lead to higher phase current THD than the conventional CPWM, and SCPWM-2 achieves about the same THD as RCMV-CBM, which is better than SCPWM-1. Detailed analysis demonstrates that the third harmonic of the five-phase IM can be suppressed to less than 0.3% under the RFOC for all the four kinds of PWM methods. Moreover, the frequent switching of carriers under SCPWM-1 leads to obvious low-order harmonics, especially the fourth and sixth components, which is about 3.2% and 2.1%, respectively. These low-order harmonics seriously deteriorate the THD of the phase current. With the optimization of carrier switching times, SCPWM-2 manages to suppress the fourth and sixth harmonics to less than 0.5%. Obviously, the decrease of carrier switching times leads to better low-order harmonic performance

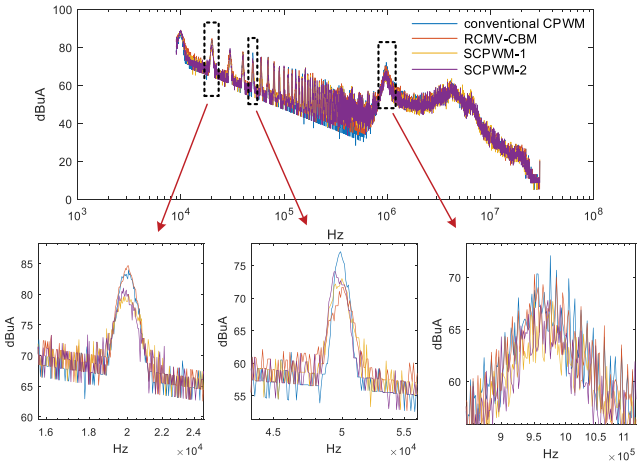

Fig. 22. Conducted CM EMI test results under four kinds of CPWM methods.

TABLE III
COMPARISON OF CONDUCTED CM EMI PEAK VALUES IN DIFFERENT FREQUENCY RANGES

Frequency Range / kHz	Peak Value / dBuA			
	Conventional CPWM	RCMV-CBM	SCPWM-1	SCPWM-2
19—21	84.00	84.66	80.01	81.03
49—51	77.13	71.67	73.01	74.05
150—200	68.74	68.59	69.30	69.11
200—300	63.11	63.37	62.32	62.51
300—500	59.93	60.89	59.63	59.09
500—1000	72.08	70.28	67.68	67.79
1×10^3—2×10^3	69.87	67.20	64.55	64.86
2×10^3—4×10^3	62.44	61.92	63.31	61.78
4×10^3—1×10^4	61.06	61.00	63.61	60.62
1×10^4—2×10^4	34.41	34.65	35.86	37.62
2×10^4—3×10^4	27.48	28.68	26.81	27.16

of SCPWM-2 than SCPWM-1, which complies with the analysis in Section IV. However, the harmonics of SCPWM-2 are still larger than the conventional CPWM, which results in higher THD of SCPWM-2 than conventional CPWM.

According to the standard DO-160E [33], the conducted CM EMI under four different PWM methods was measured, where the two line impedance stabilization networks (LISNs: NNBM 8126 A890, 0.1–150 MHz, 600 V, 100 A) were connected in series with dc power and the inverters to isolated dc power noise. Moreover, the copper sheet of 2000 × 1200 × 0.50 mm was utilized to provide the common grounding for the inverter and electrical machinery shell. With EMI receiver Rohde-Schwarz ESL 3 utilized, the conducted CM EMI test can be carried out to get accurate frequency spectrum characteristic in a frequency range of 10 kHz–30 MHz. The EMI test results are shown in Fig. 22. It can be found that the EMI differences of the four PWM methods mainly exist in peak values of three frequency ranges. From the detailed comparison listed in Table III, we can find that the modified CPWM methods generally achieve lower EMI peak values than the conventional CPWM. In particular, the two SCPWM methods attenuate the EMI peak values by

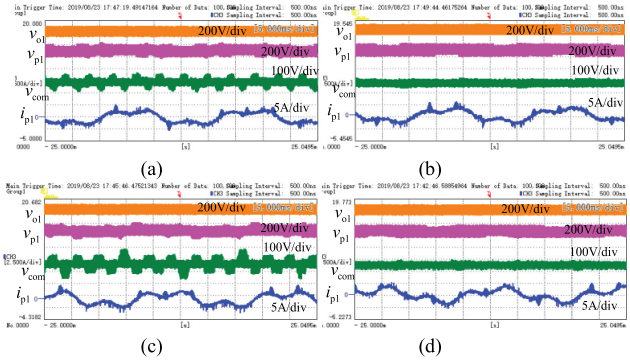

Fig. 23. Experiment results of CMV in five-phase drive case under SCPWM-2 at operating points of (a) A, (b) B, (c) C, and (d) D.

about 3 dBμA in the first two frequency ranges, and more than 4 dBμA in the third high-frequency range corresponding to the zoomed-in subfigures in Fig. 22. Compared with the conventional CPWM, the proposed SCPWM-2 always presents better EMI performance in Table III except for two frequency ranges. In the first range of 150–200 kHz, SCPWM-2 is only 0.37 dBμA worse than the conventional method. In the range of 10–20 MHz, though the EMI peak value of SCPWM-2 is 3.21 dBμA higher than that of conventional method, the EMI values of this frequency range are relatively much lower than those of other frequency ranges.

B. Harmonic Effects on CMV Under SCPWM-2

Because all the three CMV-reduction PWM methods, which are RCMV-CBM, SCPWM-1M and SCPWM-2, rely on the inequality (6), they are affected by the harmonic injection to the same extent. In this section, experiments were conducted under SCPWM-2 when the third harmonic is injected into the phase voltage of the five-phase IM under RFOC. Experimental results at four operating points of A ($\sigma_3 = 0.2$, $\varphi_3 = 0$), B ($\sigma_3 = 0.2$, $\varphi_3 = 0.2$), C ($\sigma_3 = 0.3$, $\varphi_3 = 0$), and D ($\sigma_3 = 0.3$, $\varphi_3 = 0.4\pi$) are shown in Fig. 23(a)–(d), respectively. With different injected third harmonics, the CMV waveforms expand to four levels in Fig. 23(a) and (c), while still being suppressed to two levels in Fig. 23(b) and (d). These results comply with the theoretical analysis in Section IV that the suppression of CMV is deteriorated at the working points of red areas in Fig. 14, because the inequality (6) is broken by the inappropriate harmonic injection. Because inductances on the harmonic planes are usually much lower than those in fundamental planes [34], [35], even low harmonic ratio in the phase voltage would lead to high harmonic content in the phase current, which can be validated in i_{p1} waveform of Fig. 23. More experimental results at different operating points, along with A, B, C, and D, are listed in Fig. 24, which partly verify the correctness of Fig. 14 in Section IV.

C. Dead-Time Effects on CMV Under SCPWM-2

To better observe and verify the dead-time effects, the dead-time of PWM signals in this section is set at 5 μs, while the five-phase IM is rotating at 3000 r/min. Though the dead

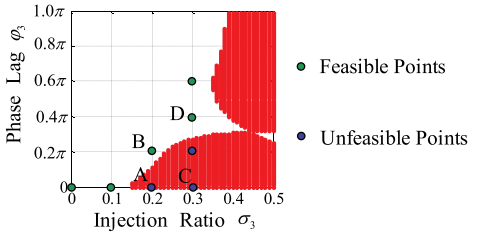

Fig. 24. Experiment verification of feasible and unfeasible points.

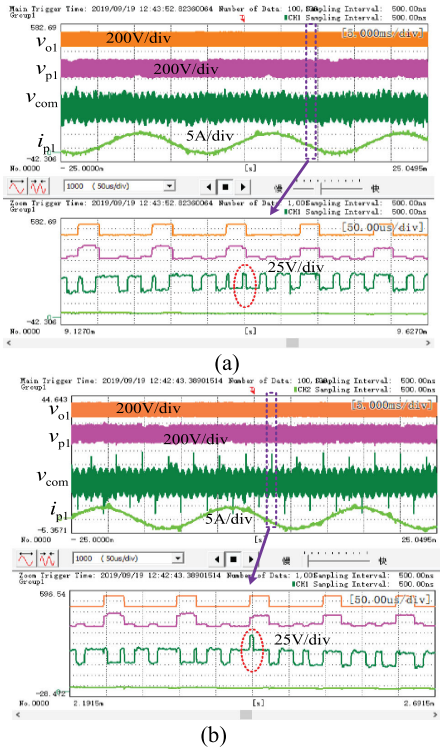

Fig. 25. Dead-time effects on CMV under SCPWM-2 with carrier selection patterns of (a) Type I and (b) Type II.

time leads to CMV spikes in Fig. 25(a), it does not increase the CMV peak-to-peak amplitude. However, dead-time-induced CMV spikes in Fig. 25(b) increase the CMV waveforms to four voltage levels, which increases the CMV amplitude by 100% compared to Fig. 25(a). The results in these two subfigures comply with the theoretical analysis in Section VI that the carrier selection method type I outweighs type II in suppressing peak values of CMV for the machine rotating clockwise with positive sequence. Additionally, we can find that there are ten CMV spikes in each fundamental cycle of about 20 ms, which correspond to two times of carrier changes for each of the five phases. Even with these CMV spikes, the CMV number of voltage steps is still six during each switching cycle in these two subfigures, which verifies the analysis in Section VI.

D. Extension of SCPWM-2 to Other Multiphase Occasions

To verify the extensibility and validity of the proposed PWM methods in other multiphase occasions, experiments were conducted in 7-phase, 9-phase, and 11-phase cases with RL loads.

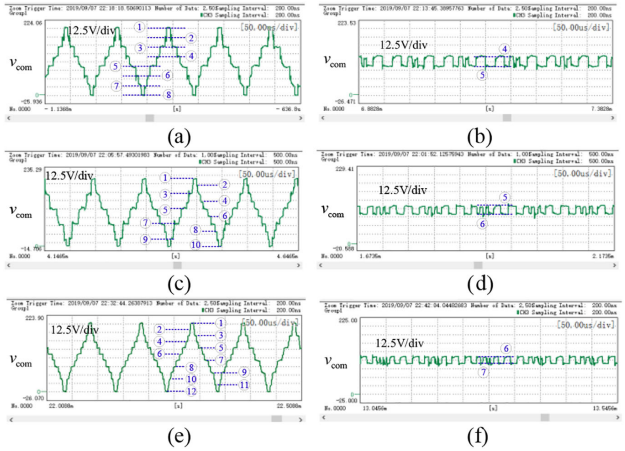

Fig. 26. Experiment results of CMV under conventional CPWM and proposed SCPWM-2 in (a) and (b) 7-phase, (c) and (d) nine-phase, and (e) and (f) 11-phase cases.

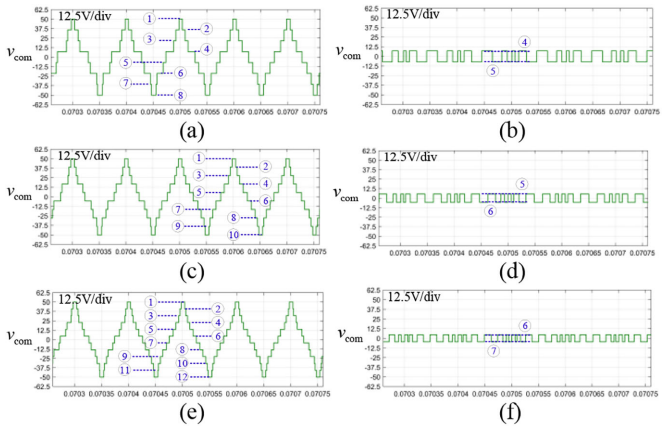

Fig. 27. Simulation results of CMV under conventional CPWM and proposed SCPWM-2 in (a) and (b) 7-phase, (c) and (d) 9-phase, and (e) and (f) 11-phase cases.

For each phase of the RL loads, the resistance R is 10 Ω and the inductance L is 50 mH. The parameters of the converter are the same as those in Table II, except that the voltage of dc bus is changed into 100 V.

Due to the limited size of this article, only testbench CMV results of SCPWM-2 against the conventional CPWM were shown in Fig. 26. Obviously, the CMV has eight levels in the 7-phase case, ten levels in the 9-phase case, and 12 levels in the 11-phase case under conventional CPWM, but is reduced to only two levels in all the multiphase cases under the proposed SCPWM-2 method. Along with the reduction of CMV amplitude, the SCPWM-2 manages to reduce the CMV changing times per switching cycle from 14 to 8 in the 7-phase case, from 18 to 10 in the 9-phase case, and from 22 to 12 in the 11-phase case. It should be pointed out that in the experiment results of CMV under conventional CPWM, some CMV levels are not distinguishable. For example, in Fig. 26(c), only six clear CMV levels can be seen at first and then it becomes ten. It is because of the fact that in the period closing to the beginning and ending of one sector, for a nine-phase system, four group references are

TABLE IV
COMPARISON OF CMV PERFORMANCE UNDER TWO CPWM METHODS WHEN EXTENDED TO 7-, 9- AND 11-PHASE CASES

	Conventional CPWM			SCPWM-2		
Multiphase Cases	7	9	11	7	9	11
CMV Amplitude (%)	100%	100%	100%	14.3%	11.1%	9.1%
CMV Changing Frequency (%)	100%	100%	100%	57.1%	55.6%	54.5%

very close and therefore, four special CMV levels are short-lived and only six levels can be seen clearly. The simulations were also conducted under the same conditions by MATLAB/Simulink to verify the correctness of the experimental results. The simulation results were shown in Fig. 27, which are consistent with the experimental results.

The improvement of CMV performance with multiphase RL loads is tabulated in Table IV, which comply with the theory analysis in Section III that the proposed SCPWM-2 could reduce the CMV amplitude and changing frequency by $(m-1)/m$ and $(m-1)/2m$, respectively.

VIII. CONCLUSION

In this article, the SCPWM methods are proposed to improve the CMV performance of multiphase two-level inverters. The following conclusions can be derived.

1) The SCPWM methods can not only reduce the CMV amplitude like the other CMV-reduction PWM methods, but also reduce the CMV changing frequency.
2) These carrier-based SCPWM methods can be easily extended to any multiphase inverter with odd phase number m, achieving the reduction of CMV amplitude and frequency by $(m-1)/m$ and $(m-1)/2m$, respectively.
3) With appropriate injection ratio and phase lag in the feasible regions, the injection of harmonics in the voltage references does not deteriorate the CMV reduction effect of SCPWM.
4) The CMV spikes are generated by the dead time of switching devices under SCPWM, but their effects on CMV peak-to-peak amplitude can be avoided by selecting the proper carrier selection pattern.
5) The SCPWM methods deteriorate the THD of output current. Though SCPWM-2 achieves better output current THD than SCPWM-1 by carrier changing optimization, it is still worse than the conventional CPWM.

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