Resonant *LLC* DC–DC Converter Employing Fixed Switching Frequency Based on Dual-Transformer With Wide Input-Voltage Range

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***Abstract*—In this article, a dual-transformer-based *LLC* resonant converter is proposed, which is a hybrid combination of a full-bridge and half-bridge *LLC* circuits. The output voltage is regulated through fixed-frequency phase-shift pulsewidth modulation control scheme, whereas the switching frequency is equal to the resonant frequency, which helps to design the magnetic components. The turns-ratio design of the two transformers is analyzed by the current stress and power distribution of both transformers with two different cases. The proposed converter is capable of realizing soft switching over wide input-voltage and whole load range. Finally, a prototype converter of 1 kW is built and the experiments are conducted under wide input-voltage and full load range. The experimental results show that the proposed converter can achieve high efficiency throughout the full load range.**

***Index Terms*—DC-DC power converters, pulsewidth modulation (PWM), transformers, zero voltage switching (ZVS).**

I. Introduction

In RECENT years, renewable energy resources (RES) are widely adopted to save energy and protect the environment. The intermittent nature of these resources brings many challenges related to high efficiency, wide voltage ranges, and multifunctions. In many applications, such as renewable energy systems, electrical vehicle chargers, telecommunication power supplies, and light-emitting diode (LED) drivers, dc–dc power converters are required to operate with a wide voltage range as they provide a regulated and stable output [1]–[3]. Therefore, dc–dc power converter with high efficiency over a wide voltage range is a key for these applications. Among various dc–dc power converter topologies, isolated dual active converters (DAB) are the most attractive due to their simplicity and inherent features, such as galvanic isolation, high power applications, soft switching, and high efficiency [4]–[6]. In recent research studies, many control schemes are suggested for isolated DAB dc–dc converters. The simplest and mostly used control topology for DAB dc–dc converter is phase-shift angle control.

The phase-shift control-based dc–dc converters have a wide zero-voltage-switching (ZVS) range and maximum efficiency at unity voltage gain. However, at wide input-voltage range, the converter suffers from high circulating losses, limited ZVS range, and low efficiency. To deal with these issues, researchers have proposed various dc–dc converter topologies with different control schemes [7]–[11]. But all these topologies and control techniques are complicated and cannot solve all the problems.

Resonant *LLC* dc–dc converter is another topology of isolated dc–dc converter. The *LLC* resonant converters have achieved prevalent attention for the above-mentioned applications as it is capable of achieving ZVS for switches and zero current switching (ZCS) for diodes. This causes high power density and high efficiency [12]–[14]. Generally, *LLC* resonant converter operates with variable-frequency control (VFC) to regulate the output voltage. In VFC control, the switching frequency f_s is varied to achieve the desired voltage gain. Therefore, in such applications where the input-voltage range is low, the f_s range is narrow. But, a wide input-voltage range needs wide variation range of f_s , which brings certain issues such as, electromagnetic compatibility, high conduction losses, and low efficiency [15]–[17].

To narrow the f_s range in wide voltage gain applications, various control schemes have been proposed for *LLC* converters [18]–[20]. A hybrid modulation scheme based on asymmetric pulsewidth modulation (APWM) and frequency modulation (FM) [21] is proposed to narrow the frequency range of *LLC* resonant converter. The proposed modulation scheme is switched from FM to APWM in hold-up time to get high converter gain. However, the dc offset current caused by APWM affects the size of magnetic elements, which reduces the power density of the converter. A semiactive variable-structure rectifier for *LLC* resonant converter [22] is proposed to achieve wide output voltage with variable frequency, where PWM controls are employed for primary and secondary side, respectively. But, the control is complicated and two extra switches are required to get the variable structure at secondary side. To achieve wide output voltage and narrow frequency range, VFC and phase-shift control are implemented in the interleaved *LLC* resonant converter [23]. The converter employs VFC for high output voltage, whereas

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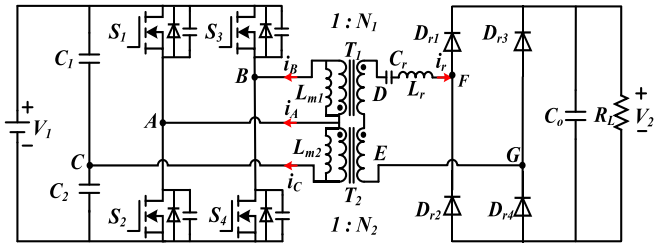

Fig. 1. Proposed topology of dual-transformer-based *LLC* converter.

the phase-shift control is used for the low output voltage. The implementation of these schemes is complex and difficult.

To overcome the problems associated with VFC *LLC* resonant converters, fixed-frequency with different control topologies are proposed in [24]–[27]. A fixed frequency PWM control-based converter topology [28] is proposed to regulate the output voltage and to simplify the design of the converter. However, an extra bidirectional ac switch is used at the secondary side of transformer, which suffers from hard switching and hence, reduces efficiency. A very interesting topology for series resonant converter is proposed in [29] and [30]. These converters consist of two transformers and two full-bridges (FBs) sharing one common leg, which is a combination of six switches (insulated-gate bipolar transistor (IGBTs) and MOSFETs), at the primary side of transformer. A fixed-frequency PWM implementing series resonance in discontinuous conduction mode (DCM) is applied to control the conduction period of the two FB bridges. Due to the resonance, all the main switches can achieve ZCS which is preferred for the switches IGBTs. However, the switching frequency of IGBTs is limited.

To improve the performance of *LLC* resonant dc–dc converter in a wide input-voltage range, a fixed-frequency *LLC* resonant converter using two transformers is proposed in this article. The topology of the proposed converter is a combination of a half-bridge (HB) and an FB *LLC* converter sharing one leg. Thus, only four active switches are needed. To improve the power density of the converter, SiC MOSFETs are used instead of IGBTs and thus, the switching frequency can be designed very high and the power density of the converter can be high as well. The output voltage is regulated by the fixed-frequency phase-shift PWM control, where the switching frequency is equal to the resonant frequency, which facilitates the design of magnetic elements. In addition, all the main active switches can achieve ZVS over the entire full load range, which significantly decreases the switching loss and improves the efficiency.

The rest of the article is organized as follows. The proposed topology and its working principle are given in Section II. The proposed converter design and its analysis are discussed in Section III. In Section IV, simulation with modulation strategy is illustrated. The experimental results are given in Section V. Finally, the article is concluded in Section VI.

II. Topology and Working Principle

A. Proposed Converter Topology

The topology of the proposed resonant converter is given in Fig. 1. The proposed converter is a hybrid combination of two bridges, an FB and an HB, whereas these two bridges share the same leg A (S_1/S_2). The FB circuit is a combination of switches

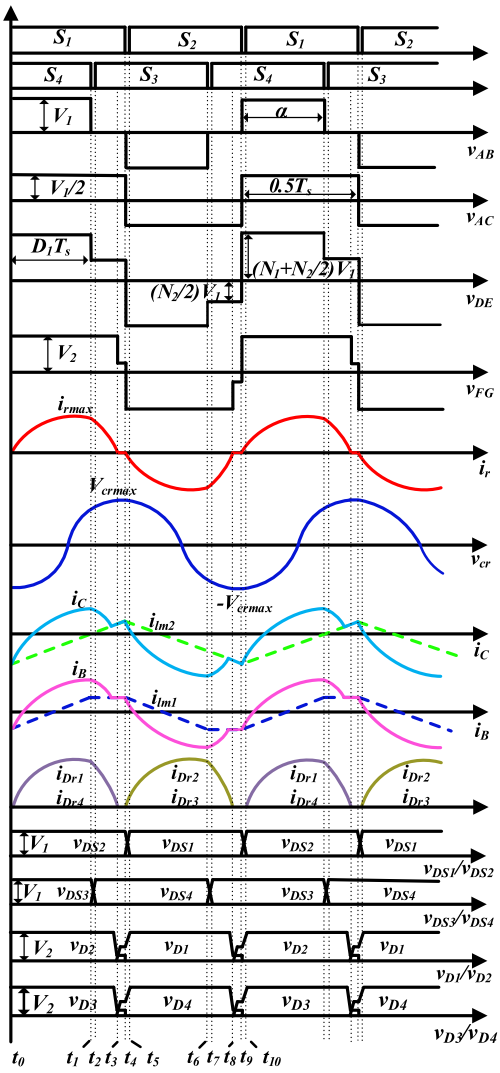

Fig. 2. Steady-state waveforms.

is composed of switches S_1, S_2 and capacitors C_1 and C_2 with transformer T_2. L_{m1} and L_{m2} are the magnetizing inductors of T_1 and T_2, respectively, and v_{AB} and v_{AC} are the primary-side voltages across L_{m1} and L_{m2}, respectively. The primary sides of both transformers are connected in parallel, whereas the secondary sides are connected in series. v_{DE} is secondary-side voltage and v_{FG} is the FB rectifier voltage. The *LC* resonant tank (L_r, C_r) is at secondary along with the FB rectifier (D_{r1}–D_{r4}) and the output filter capacitor (C_o).

The HB is uncontrolled so that it always operates with 50% duty cycle, therefore, the peak voltage of T_2 (v_{AC}) is always $\pm V_1/2$, and the duty cycle (D_1) of FB is controlled by the phase-shift angle (α) between A and B legs, hence, the voltage across T_1 (v_{AB}) is PWM controlled, as shown in Fig. 2. The range of D_1 is from $D_{1\max}$ to $D_{1\min}$. The input-voltage variation of the converter is from $V_{1\min}$ to $V_{1\max}$, which shows that when input-voltage value is $V_1 = V_{1\min}$, the duty ratio of FB is equal to $D_{1\max}$ and the resonant converter works in HB–FB mode, whereas the converter operates as an HB-*LLC* resonant converter as the duty ratio of FB is equal to $D_{1\min}$. The turns ratio of T_1 and T_2 are selected carefully to achieve the desired output voltage

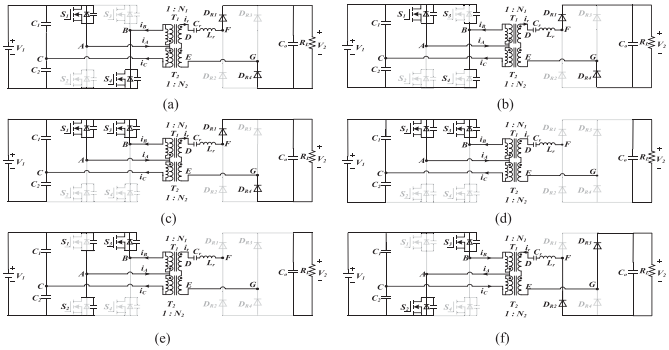

Fig. 3. Operation stages.

B. Steady-State Operation and Working Modes of the Converter

The steady-state behavior of the proposed converter is analyzed and shown in Fig. 2, where i_r is the resonant tank current, and i_B and i_C are the primary-side currents of T_1 and T_2, respectively. All the four switches (S_1–S_4) are driven with fixed 50% duty ratio. The duty cycle D_1 of transformer T_1 is regulated by phase-shift angle (α), which depends on the voltage gain and the load. The case $0< D_1 < 0.5$ is explained, and the key waveforms are presented in Fig. 2, where a four-level voltage of v_{DE} is observed when $0< D_1 < 0.5$. The following assumptions are made for steady-state analysis of the converter:

1) all the active switches *(S_1–S_4)* are ideal and the dead time between gate signals is neglected;
2) the output capacitor C_o is large enough and the output voltage is constant;
3) C_1 and C_2 are large enough, therefore the voltage ripple can be neglected, and voltage across each capacitor is half of the input;
4) the parasitic capacitors of C_{oss1}–C_{oss4} of the all switches S_1–S_4 have equal capacitance.

There are five working stages in each half-switching period ($0.5T_S$), as shown in Fig. 2, whereas the waveforms are symmetrical in one cycle. Therefore, only a half-cycle is discussed, and the corresponding equivalent circuit diagrams are shown in Fig. 3.

Stage 1 *(t_0–t_1) [see Fig. 3(a)]:* Before t_0, S_2 and S_4 conduct, at t_0, S_1 is turned ON and S_2 is turned OFF. Both S_1 and S_4 conduct together from t_0 to t_1. During this stage, v_{AB} is equal to the input voltage V_1 and v_{AC} is equal to $V_1/2$. At the secondary side of two of the transformers, v_{DE} is equal to $(N_1+ N_2/2)V_1$ and v_{FG} is equal to V_2. The resonant current i_r starts increasing in the positive direction and the rectifier diodes D_{r1} and D_{r4} start conducting. The voltage across S_2 and S_3 (v_{DS2}, v_{DS3}) is equal to the applied input voltage and the voltage across diode D_{r3} and D_{r2} (v_{D3}, v_{D2}) is equal to the output voltage V_2. The equivalent circuit of this mode is given in Fig. 3(a), and the resonant current and voltage are expressed as

$$\begin{cases} i_r(t) = i_r(t_0)\cos(\omega_r(t-t_1)) \\ \qquad +\frac{v_{DE}-v_{cr0}-v_{FG}}{Z_r}\sin(\omega_r(t-t_1)) \\ v_{cr}(t) = (v_{DE}-v_{cr0}-v_{FG}\cos(\omega_r(t-t_1)) \\ \qquad +Z_r(i_r(t_0)\cos(\omega_r(t-t_0)) \end{cases} \tag{1}$$

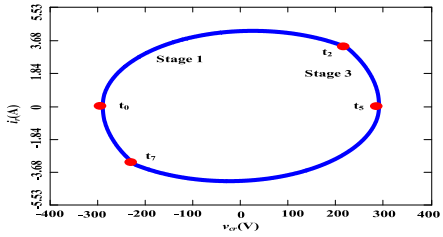

Fig. 4. Steady-state trajectory.

where

$$v_{DE} = \left(N_1 + \frac{N_2}{2}\right)V_1, \quad v_{FG} = V_2, \quad Z_r = \sqrt{\frac{L_r}{C_r}}.$$

Stage 2 *(t_1–t_2) [see Fig. 3(b)]:* At time t_1, S_4 is turned OFF. Current i_B is the sum of resonant current referred to the primary side of T_1 and its magnetizing current (i_{lm1}), and this current starts to charge/discharge the junction capacitor of S_4/S_3 switches. After the voltage across drain–source (v_{DS3}) of S_3 is zero, the body diode of S_3 conducts and hence, the ZVS is obtained for S_3.

Stage 3 *(t_2–t_3) [see Fig. 3(c)]:* At t_2, S_3 is switched ON with ZVS. In this subinterval, V_{AB} is equal to 0, and the converter operates in HB mode. The resonant tank input voltage V_{DE} is now equal to $N_2V_1/2$ only, and the resonant current i_r starts decreasing. At the end of this stage (t_3), i_r reaches zero and, i_C and i_B equal the magnetizing currents i_{lm2} and i_{lm1}, respectively. i_r and V_{cr} in this subinterval are given by

$$\begin{cases} i_r(t) = i_r(t_1)\cos(\omega_r(t-t_3)) \\ \qquad +\frac{v_{DE}-v_{cr1}-v_{FG}}{Z_r}\sin(\omega_r(t-t_3)) \\ v_{cr}(t) = (v_{DE}-v_{cr1}-v_{FG})\cos(\omega_r(t-t_3)) \\ \qquad +Z_r(i_r(t_1)\cos(\omega_r(t-t_3)) \end{cases} \tag{2}$$

where

$$v_{DE} = \left(\frac{N_2}{2}\right)V_1 \quad v_{FG} = V_2 \quad Z_r = \sqrt{\frac{L_r}{C_r}}.$$

Stage 4 *(t_3–t_4) [see Fig. 3(d)]:* From t_3 to t_4, i_r is zero, and i_B and i_C are equal to the magnetizing currents i_{lm1} and i_{lm2}, respectively, whereas the diodes D_{r1} and D_{r4} currents are zero and stop conducting. In this time period, the converter operates in DCM and the load is only supplied by the output capacitor. The currents i_C and i_B can be expressed as in

$$\begin{cases} i_B(t) = i_{lm1}(t-t_4) \\ i_C(t) = i_{lm2}(t-t_4). \end{cases} \tag{3}$$

Stage 5 *(t_4–t_5) [see Fig. 3(e) and (f)]:* S_1 is turned OFF at t_4. During this stage, as i_r is zero, i_A is only equal to the sum of the magnetizing currents of the two transformers ($i_{lm1} + i_{lm2}$). Current i_A begins to charge/discharge S_1/S_2 junction capacitors in the dead time and drain–source voltage of S_2 (V_{DS2}) starts falling. At the end of this period, V_{DS2} is zero and S_2 body diode begins to conduct. S_2 is ready for ZVS ON.

Fig. 4 shows the steady-state trajectory curve of the resonant tank current and resonant voltage, where the different stages in one half-cycle are mentioned. In stage 1, the converter is operating in FB–HB mode, whereas in stage 3, the converter is working in only HB mode.

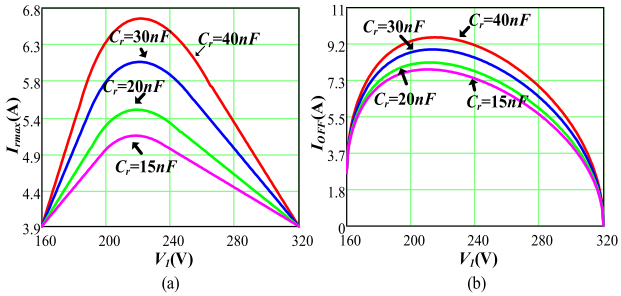

Fig. 5. Different resonant capacitor value versus (a) resonant peak current and (b) S_3 and S_4 turn-OFF current.

III. Converter Design and Performance Analysis

A. Resonant Tank Parameters

The average value of the resonant current during complete half-switching period is equal to the load current. During the positive half-cycle of resonant current i_r, the resonant capacitor voltage v_{cr} increases from $-v_{cr\max}$ to $+v_{cr\max}$ as shown in Fig. 2. Therefore, the total charge q on the resonant capacitor increases, which is related to the output current. The average resonant current $i_r(\text{avg})$ and the maximum resonant capacitor voltage $v_{cr\max}$ can be give as in the following:

$$\begin{cases} i_r(\text{avg}) = \frac{1}{\frac{1}{2}T_s}\int_0^{\frac{T_s}{2}} i_r(t)dt = \frac{P_o}{V_o} \\ V_{cr\max} = \frac{P_o}{4V_o f_r C_r} \end{cases} \tag{4}$$

where P_o and V_o are the output power and voltage, respectively, C_r is the resonant tank capacitance and f_r is the resonant frequency. As can see from (4), at heavy load, the resonant capacitor voltage $v_{cr\max}$ will be higher. To prevent capacitive switching and hard switching, the maximum voltage across resonant capacitor $v_{cr\max}$ should be lower than the output voltage (V_o) at the maximum rated power. Therefore, the required minimum C_r is calculated by

$$C_{r\min} > \frac{P_{o\max}T_s}{4{V_o}^2} \tag{5}$$

where $P_{o\max}$ is 1.2 times the rated power P_o ($P_o = 1\,\text{kW}$) for overload operation requirement, output voltage $V_o = 400\,\text{V}$ and $T_s = 1/f_r$ ($f_r = 106\,\text{kHz}$). To ensure that $v_{cr\max}$ is lower than V_o, substituting the given specification, one can obtain the minimum resonant capacitance value $C_{r\min} > 17.69\,\text{nF}$. For the optimal value of C_r, the peak resonant current and turn-OFF current of S_3 and S_4 are taken into account. Higher peak current will lead to increase in conduction losses; however, the switching loss of S_3 and S_4 are mainly due to the high turn-OFF current. Fig. 5 shows the resonant peak current and turn-OFF current for switches S_3/S_4 at rated power with different resonant capacitor C_r values. According to Fig. 5(a), the peak resonant current increases with high C_r value. Similarly, the turn-OFF current, as shown Fig. 5(b), is higher at larger resonant capacitor value. It can be noted from Fig. 5, that at $C_r = 15\,\text{nF}$, resonant current has the lowest peak value and also, S_3 and S_4 have the lowest turn-OFF current; however, this value is lower than the minimum required value $C_{r\min}$. Therefore, C_r is selected $C_r = 20\,\text{nF}$ for the proposed converter. As mentioned above that the proposed converter operates at resonant frequency, once C_r is decided, the resonant inductor L_r can be obtained by using the resonant frequency formula.

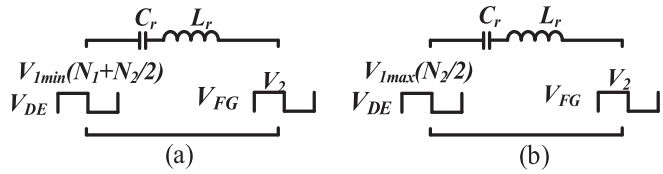

Fig. 6. Resonant tank input and output voltage. (a) $V_1 = V_{1\min}$. (b) $V_1 = V_{1\max}$.

B. Transformer Turns Ratio Selection

For the proposed converter, the range of D_1 is 0–0.5, the input-voltage variation is 160–320 V, and output voltage is 400 V. According to the input-voltage range, the turns ratio of both transformers (N_1 and N_2) are designed such that when input-voltage value is $V_1 = V_{1\min}$, the duty ratio of FB is equal to $D_{1\max} = 0.5$ and, the input and output voltage of the *LC* tank are ensured to be the same as can be seen in Fig. 6. Similarly, at input voltage $V_1 = V_{1\max}$, D_1 is equal to $D_{1\min} = 0$. Therefore, the voltage across transformer T_1 is zero at $D_{1\min} = 0$ and only T_2 contributes to the output voltage; hence, in this case, the converter works as a conventional HB-*LLC* converter. Therefore, the turns ratio for two transformers are obtained from (6) and (7), where $G_{\max}$ and $G_{\min}$ are the maximum and minimum voltage gain: V_2/V_1, respectively

$$\frac{N_2}{2} = G_{\min} \tag{6}$$

$$N_1 + \frac{N_2}{2} = G_{\max}. \tag{7}$$

C. Current Stress of the Two Transformers

By substituting $G_{\min} = 400/320$ and $G_{\max} = 400/160$ into (6) and (7), the turns ratio is calculated: $N_1 = 5/4$ and $N_2 = 5/2$ for case A. It is worth noting that the value of N_1 has significant impact on the efficiency of the converter since it can affect the peak and turn-OFF currents of the switches. Increasing the value of N_1 will result in the increase of peak current and high turn-OFF current of leg A switches S_3/S_4 as well as transformer T_1 current, whereas the current of T_2 will decrease. However, it has very small effect on the peak and turn-OFF currents of leg A (i_A) switches S_1 and S_2, because i_A current is the summation of both transformers T_1 and T_2 currents with their corresponding magnetizing currents. Also, another case B is analyzed and compared with the case A. For case B, the same turns ratio for T_1 and T_2 is selected from (6) by equating $N_1 = N_2$, which means that the current in both transformers are the same. In this case, the same turns ratio can be calculated: $N_1 = N_2 = 10/6$.

Fig. 7 shows the comparison of the rms resonant current $(i_{r\text{RMS}})$ and the two transformers' primary-side rms currents (I_{T1} and I_{T2}) in both cases. Fig. 7(a) shows that for the whole input-voltage range, the $i_{r\text{RMS}}$ current in case B, where $N_1 = N_2 = 10/6$, is of higher value than that in case A. Similarly, the primary-side rms current of T_1 is higher in case B than in case

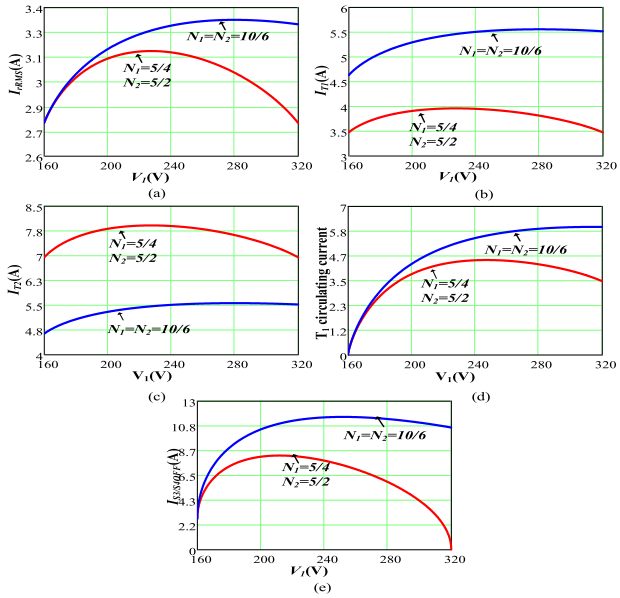

Fig. 7. Comparison of both cases regarding (a) resonant rms current, (b) T_1 primary, (c) T_2 primary rms current, (d) rms circulating current of T_1, and (e) rms current S_3/S_4 turn-OFF current.

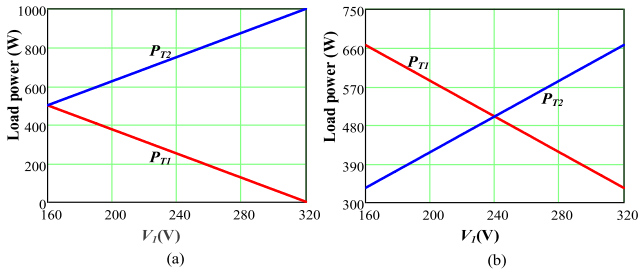

Fig. 8. Comparison of power distribution of two transformers: (a) case A; and (b) case B.

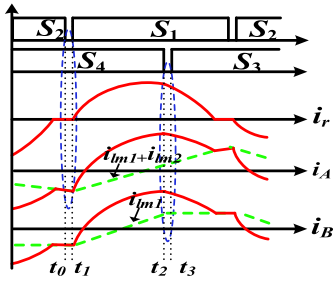

Fig. 9. ZVS condition for the switches.

A, as shown in Fig. 7(b), whereas T_2 primary-side rms current is higher in case A compared to case B, as can be seen in Fig. 7(c).

The optimal operating mode for the proposed converter is at the situation where $D_1 = 0.5$, because in this mode, the converter is operating in CCM and the circulating current in T_1 does not exist. However, when D_1 is less than 0.5, the T_1 transformer has circulating current which can be seen in the time period $[t_2$–$t_3]$ in Fig. 2. The comparison of the rms value of this circulating current in both cases are presented in Fig. 7(d). As shown in Fig. 7(d), as the input voltage is pretty close to $V_{1\min}$, the rms circulating current of T_1 is almost the same in both cases. Consequently, as the input voltage V_1 increases, the rms value of circulating current of T_1 is increased and rms value of this current is higher in case B compared to case A. Furthermore, comparison of the turn-OFF current of S_3/S_4 switches is illustrated in Fig. 7(e); in case B, the switching losses would be higher than that in case A, because the turn-OFF current of the S_3/S_4 switches is significantly high in case B, as shown in Fig. 7(e).

D. Power Distribution of the Two Transformers

The power transfer of the two transformers is expressed in (8), and the comparison of the power transfer of the transformers in both cases are shown in Fig. 8

$$\begin{cases} P_{T1} = \frac{2}{T_s}\int_0^{DT_s}[N_1 V_1 i_r(t)]dt \\ P_{T2} = \frac{2}{T_s}\int_0^{t_3}\left[\frac{N_2 V_1}{2} i_r(t)\right]dt \end{cases} \tag{8}$$

where P_{T1} and P_{T2} are transformers T_1 and T_2 transferred power, respectively. As can be seen in Fig. 8, as the input voltage increases, P_{T1} decreases, whereas P_{T2} increases. It is illustrated from Fig. 8(b) that the maximum power delivered by the two transformers to the load is almost the same in case B. However, T_2 has higher maximum power rating in case A, as shown in Fig. 8(a). It means that the core size of T_2 in case A is higher compared with that needed in case B, similarly, T_1 core size is reduced in case A as required for case B. Using area-product (AP) method, the core size for the two transformers can be calculated according to the maximum power transfer by T_1 and T_2 in both cases. The sum of the total size of the two transformers in both cases is approximately the same.

E. ZVS Realization of the Converter Switches

In this section, ZVS for the two legs A and B switches are discussed in detail. For the two legs A and B, the ZVS conditions are different. ZVS current of switches S_3 and S_4 of the leg B depends on the sum of transformer T_1 magnetizing current (i_{lm1}) and the load current. As can be seen from Fig. 9, the current i_B is maximum at time interval $(t_2$–$t_3)$ when S_3/S_4 is switched, and is enough to be used for achieving ZVS in the dead time. However, the worst condition for S_3/S_4 is when $D_1 = 0$ at very light load, because the magnetizing current is zero as the voltage across transformer T_1 is zero and ZVS is lost in this mode. This condition occurs only in case A, where D_1 can reach zero; however, in case B, S_3/S_4 switches always achieve ZVS as D_1 will always be higher than zero.

Switches of left-side leg A (S_1/S_2) of the converter depends only on the sum of two magnetizing currents. As shown in Fig. 9, that at time $(t_0$–$t_1)$, S_1/S_2 is switched, i_r is DCM and equal to zero at this time interval; hence, the current of leg A is equal to the sum of both magnetizing currents $(i_{lm1} + i_{lm2})$ of the two transformers. This current should be large enough to charge/discharge of the junction capacitors of the power switches. The ZVS limits for the switches S_1 and S_2 can be described as in

$$i_{lm1} + i_{lm2} \geq \frac{2V_1 C_{oss}}{t_d} \tag{9}$$

TABLE I
PERFORMANCE AND ECONOMIC COMPARISON

Topology	Dual-bridge LLC converter [26]	Two transformers LLC converter [13]	Dual-transformer-asymmetrical dual-bridge converter [11]	Proposed dual-transformer LLC converter
No. of MOSFETs	6	6	6	4
No. of diodes	2	8	4	4
Transformers	1 (large)	2 (small)	2 (small)	2 (small)
Modulation	PWM	FM	Phase-shift	PWM
Soft Switching	ZVS and ZCS	ZVS and ZCS	ZVS and ZCS	ZVS and ZCS
Voltage Gain	Wide	Wide	Low	Wide
Maximum power	480W	250W	1000W	1000W
cost	medium	higher	high	high
Full-load efficiency	94.1%	97.7%	95.35%	95.2%

where t_d is the dead time between S_1 and S_2, and $C_{\rm oss}$ is the parasitic capacitance of the power MOSFETs. Fig. 9 indicates that $i_{lm1} + i_{lm2}$ has reached the maximum value before S_1 turns ON and the resonant current starts to increase when S_1 is turned ON. According to (9), the ZVS condition for S_1 and S_2 switches is calculated as

$$\frac{V_1}{8L_{m1}}(D_1T_s) + \frac{V_1T_s}{8L_{m2}} \geq \frac{2V_1\mathrm{C}_{oss}}{t_d} \tag{10}$$

where L_{m1} and L_{m2} are the magnetizing inductance of transformers T_1 and T_2, respectively. As can be seen from (10), S_1 and S_2 can easily achieve ZVS when $D_1 > 0$. However, when D_1 is equal to zero, the voltage across L_{m1} would be zero and hence, i_{lm1} will also be zero, therefore, i_{lm2} should be large enough to achieve ZVS for S_1 and S_2. The desired L_{m2} value for T_2 transformer can be derived using

$$L_{m2} \leq \frac{t_dT_s}{16C_{\rm oss}}. \tag{11}$$

Moreover, the converter is always operating at resonant frequency and, at $0 < D_1 < 0.5$, the converter operates in DCM, thus, ZCS can be easily accomplished for the FB rectifier diodes.

F. Comparison With Other Converters

The performance and economic comparison of the proposed converter with previous converters is given in Table I. As can be seen from Table I, dual-bridge *LLC* converter [26] has medium cost due to the use of one transformer, however, the number of MOSFETs switches is more than the proposed converter and also the power rating is pretty low. The other two converters [11] and [13] used two transformers topology, similar to the proposed converter. The full-load efficiency of [13] is higher but the converter cost is higher compared to others due to more number of switches used and also, the output power is low. The converter of [11] and the proposed converter have the same high power rating, however, the voltage gain of [11] is narrow and also, the active switches are more than the proposed converter.

TABLE II
KEY PARAMETERS FOR BOTH CONVERTERS

System parameters	Variable frequency LLC converter	Proposed LLC converter
Input side voltage (V_1)	160-320V	160-320V
Output side voltage (V_2)	400V	400V
Transformer T1 turns ratio (N_1)	3:5	4:5
Transformer T2 turns ratio (N_2)	None	2:5
Resonant inductor (L_r)	56.48μH	112.2 μH
Resonant capacitor (C_r)	39.92nF	20nF
Magnetizing inductor (L_m)	84.71μH	240μH for T1, 139μH for T2
Output power (P_{out})	1000W	1000W
Resonant frequency (f_r)	106kHz	106kHz
Switching frequency (f_s)	78~149 kHz	106kHz
Transformer core T_1	EE-EE42/21/20	EE-EE41/17/42
Transformer core T_2	None	EE-EE41/21/15
Primary side MOSFETs (S_1-S_4)	C3M0065090J	C3M0065090J
Output side diodes (D_{r1}-D_{r4})	C3D10060G	C3D10060G

G. Efficiency Comparison With the Variable-Frequency LLC Converter

For the efficiency comparison, a frequency control *LLC* converter is designed. The specifications for the frequency *LLC* converter and the proposed converter are listed in Table II. Table II shows that the switching frequency for the proposed converter is 106 kHz, however the switching frequency range for the variable-frequency converter is 78–149 kHz.

To compare the efficiency of both topologies, the conduction loss, switching loss, and core loss of both the converters are considered.

The total conduction loss for the two converters could be calculated by

$$\begin{aligned} P_{\rm con\_loss} &= 2V_FI_{av} + \sum_{i=1}^{n=4} R_{ds\_\rm on}{I_{Si}}^2 + {I_{Lr\_\rm rms}}^2(R_{\rm trans\_pri1}{N_1}^2 \\ &\quad + R_{\rm trans\_pri2}{N_2}^2 + R_{\rm trans\_sec1} + R_{\rm trans\_sec2}) \end{aligned} \tag{12}$$

where V_F is the diode forward voltage, I_{av} is the average current of diodes, $R_{ds\_\rm on}$ is the conduction resistance of switches, I_{si} is the rms current of switch S_i, $I_{Lr\_\rm rms}$ is the rms resonant current, and $R_{\rm trans\_pri}$ and $R_{\rm trans\_sec}$ are the primary- and secondary-side winding resistances of transformers.

ZVS-ON is considered for both converters in the whole range of voltage. Therefore, only the turn-OFF loss of primary-side switches is considered. Therefore, the switching loss of the proposed converter can be calculated by

$$P_{\rm switch\_loss} = \sum_{i=1}^{n=4} \int_0^{t_{fi}} v_{DSi}(t)i_{DSi}(t)dt \tag{13}$$

where $v_{DSi}(t)$ is the drain-to-source voltage of the switch and $i_{DSi}(t)$ is the drain current in the process of turn-OFF for the switch S_i. The value of t_{fi} could be obtained from datasheets.

ZCS in the proposed converter can be achieved in the whole range of voltage. Whereas for variable-frequency *LLC* converter, the turn-OFF loss of the output-side diodes needs to be considered when the voltage gain is less than one. Therefore, the turn-OFF

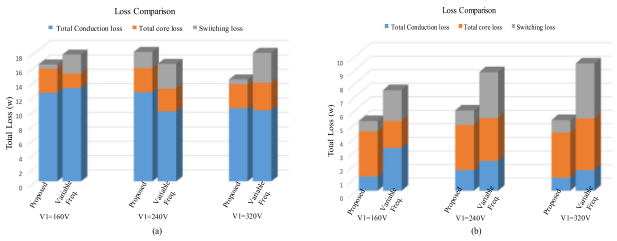

Fig. 10. Total loss comparison at (a)1000 W and (b)100 W.

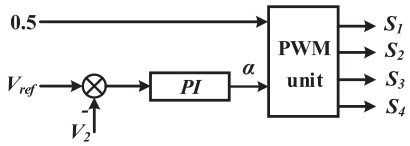

Fig. 11. Phase-shift PWM control for the proposed converter.

loss for the variable-frequency converter can be found by

$$P_{\text{switch\_loss}} = \begin{cases} \sum_{i=1}^{n=4} \int_0^{t_{fi}} v_{DSi}(t) i_{DSi}(t) dt & V_1 < 240\,\text{V} \\ \sum_{i=1}^{n=4} \int_0^{t_{fi}} v_{DSi}(t) i_{DSi}(t) dt + & V_1 > 240\,\text{V} \\ \sum_{i=5}^{n=8} \int_0^{t_{fi}} v_{ACi}(t) i_{ACi}(t) dt & \end{cases} \tag{14}$$

where $v_{ACi}(t)$ is the anode to cathode voltage of diode and $i_{ACi}(t)$ is the current at turn-OFF for the diode D_{ri}.

The magnetic loss of transformers could be approximated by Steinmetz empirical formula

$$P_{\text{tmag\_loss}} = C_m {f_s}^{\alpha} {B_m}^{\beta} V_{e-\text{trans}} \tag{15}$$

where C_m, α, and β are coefficients and $V_{e-\text{trans}}$ is the volume of the transformer.

Fig. 10 shows the comparison of the total loss of both topologies at 1 and 0.1 kW. Fig. 10(a) shows that at 1 kW (full load), the conduction loss is dominant in both converters because of the high rms current in the whole input voltage. The VFC *LLC* converter has lower losses at $V_1 = 240$ V at full load as shown in Fig. 10(a), because this is the optimal operating point for the variable-frequency *LLC* converter as the switching frequency is approximately equal to the resonant frequency. Whereas the proposed converter losses are lower at $V_1 = 160$ V and $V_1 = 320$ V, as the proposed converter has low circulating current and low switching loss.

In the case of 100W load the variable-frequency converter has very high conduction and very high switching loss as compared to the proposed converter. This contribute the overall loss of the variable-frequency converter, as shown in Fig. 10(b). Therefore, it can be concluded that the proposed converter provides better performance in whole load in terms of overall efficiency compared to the variable-frequency *LLC* converter.

IV. Control Strategy and Simulation of the Proposed Converter

The phase-shift angle (α) PWM control strategy is implemented to regulate the output voltage and the block diagram of the closed-loop control is shown in Fig. 11. As can be seen in Fig. 11, α is controlled through PI regulator and based on the α value, the PWM unit generates the corresponding gate driving signals for the switches. This control strategy is pretty simple and easy to be implemented as compared to other complicated approaches for wide ZVS range under wide input-voltage range.

TABLE III
List of Key Parameters

System parameters	Case A	Case B
Input side voltage (V_1)	160 – 320V	
Output side voltage (V_2)	400V	
Transformer T_1 turns ratio (N_1)	4:5	6:10
Transformer T_2 turns ratio (N_2)	2:5	6:10
Magnetizing inductance (L_{m1})	240 µH	
Magnetizing inductance (L_{m2})	139 µH	
Resonant inductor (L_r)	112.1 µH	
Resonant capacitor (C_r)	20nF	
Rated output power	1kW	
Resonant frequency (f_r)	106kHz	
Primary side capacitance (C_1 and C_2)	20 µF	
Primary side MOSFETs (S_1-S_4)	C3M0065090J	
Output side diodes (D_{r1}-D_{r4})	C3D10060G	
Output Capacitance (C_o)	33.6 µF	

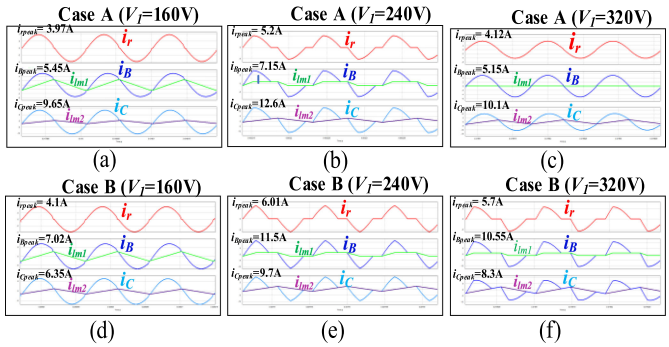

Fig. 12. Simulation results with different input voltages.

The simulation of the proposed converter is carried out by PSIM software. The parameters used for the simulation are the same as listed in Table III. The resonant parameters (L_r and C_r) have the same value in both cases (A and B), whereas cases A and B have different turns ratios (N_1 and N_2) for the two transformers. The simulation results are shown in Fig. 12. It can be seen from simulation results that the peak resonant current and turn-OFF currents of S_3 and S_4 are lower in case A than those in case B. Consequently, the simulations results are almost the same as discussed in theoretical analysis.

V. Experimental Results

A. Hardware Specifications

A 1-kW laboratory prototype was developed to experimentally verify the performance of the proposed converter. The specifications of the designed converter are listed in Table III and a photograph of the hardware is shown in Fig. 13. For the control unit, digital signal processor (DSP) controller TMS320F28335 from Texas Instruments (TI) is used and drive chip Si8233 is used. All the primary-side switches are SiC MOSFETs C3M0065090J, and the secondary-side FB rectifier diodes are type C3D10060G.

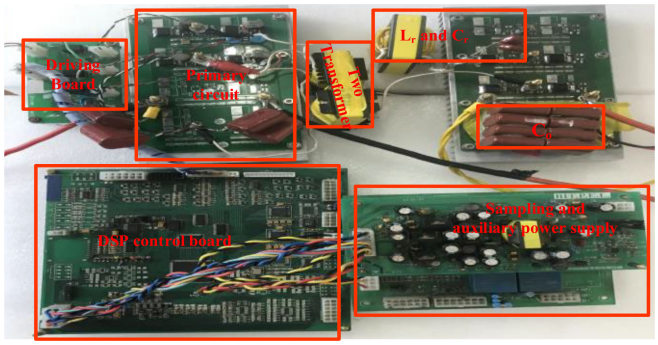

Fig. 13. Photograph of the experimental prototype.

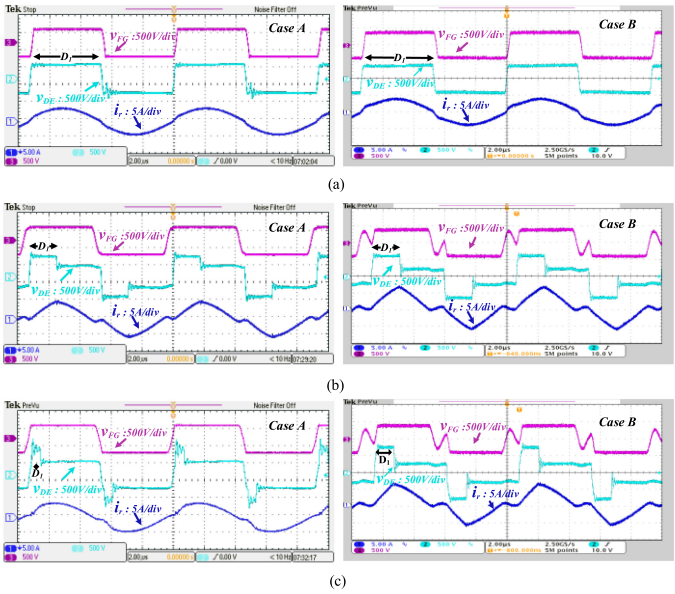

Fig. 14. Experimental waveforms of the two cases at 1 kW output power. (a) $V_1 = 160$ V. (b) $V_1 = 240$ V. (c) $V_1 = 320$ V.

B. Experimental Waveforms

Fig. 14 shows the experimental waveforms of the proposed converter prototype in the two cases with full load (1 kW). V_{DE} is the resonant tank input voltage at secondary side and V_{FG} is the tank output voltage. i_r is the resonant current at secondary side. From Fig. 14(a), it can be seen in both cases A and B, that when $V_1 = 160$ V, the V_{DE} and V_{FG} are square waveforms and i_r is pretty close to a sinusoidal wave. The value of duty cycle (D_1) is maximum (0.5) at this input voltage. Fig. 14(b) shows the experimental waveform of the two cases when $V_1 = 240$ V. As V_1 increases, the duty cycle of FB converter decreases and the peak of resonant current increases. It can be seen that in case B, the peak of the resonant current and turn-OFF current is higher as compare to case A. Similarly, the duty cycle of FB in case A is approaching zero when $V_1 = 320$ V and the resonant current has lower peak as compared to case B as shown in the experimental waveform of Fig. 14(c). It demonstrates that as the input voltage V_1 increases, the transformer T_2 of the HB circuit supplies more power to the output load. Also, the experimental waveforms at low load ($P_o = 0.1$ kW) of these two cases are shown in Fig. 15.

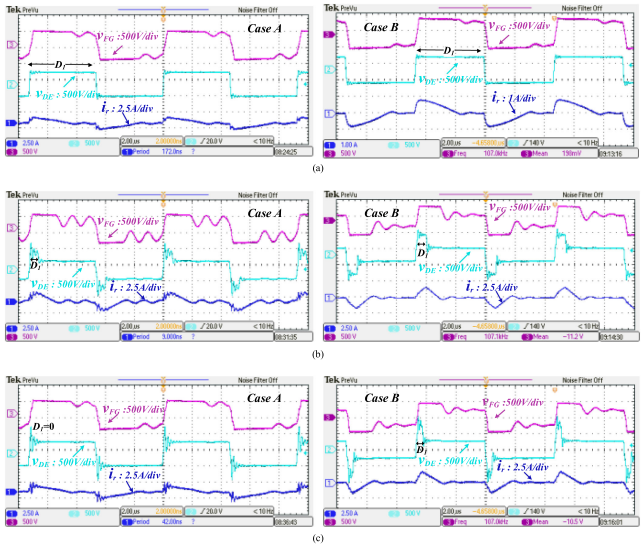

Fig. 15. Experimental waveforms at 0.1 kW output power. (a) $V_1 = 160$ V. (b) $V_1 = 240$ V. (c) $V_1 = 320$ V.

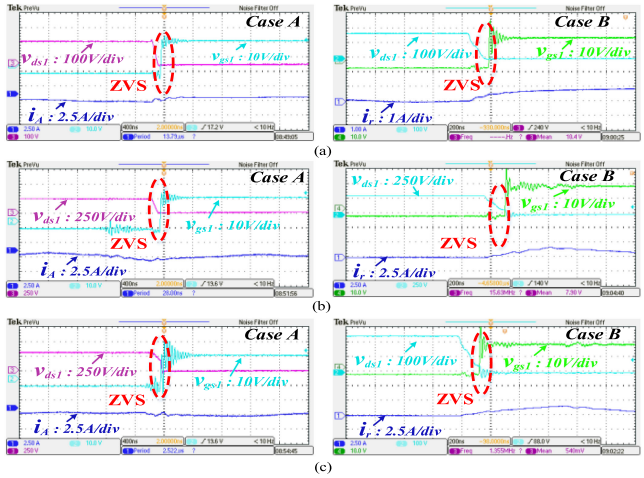

Fig. 16. ZVS waveforms for S_1 switch of the two cases A and B at 100 W. (a) $V_1 = 160$ V. (b) $V_1 = 240$ V. (c) $V_1 = 320$ V.

The amplitude of the resonant current i_r decreases as the output power reduced.

As discussed in the previous section, ZVS for heavy load is easy to achieve, therefore, ZVS of switches S_1 and S_3 in both cases under light load (0.1 kW) is captured and shown in Figs. 16 and 17, respectively. The drain-to-source voltage (V_{DS}), gate-to-source voltage (V_{GS}), resonant current (i_r), and leg A and leg B currents (i_A, i_B) are shown in Fig. 16. ZVS for S_1 in both cases can be observed through experimental waveforms for light load under the whole input-voltage range. In Fig. 17, ZVS of switch S_3 in the two cases is shown. It can be noted in Fig. 17(c) case A that ZVS is lost for S_3 when $V_1 = 320$ V, because $D_1 = 0$ and, voltage across T_1 transformer is zero; hence, i_{LM1} is zero. Meanwhile, in case B, the duty cycle $D_1 > 0$, therefore, S_3 is turned-ON with ZVS.

In order to verify the dynamic behavior of the proposed *LLC* converter, load transient experiments have been carried out for the two cases. The experimental waveforms of the load changing

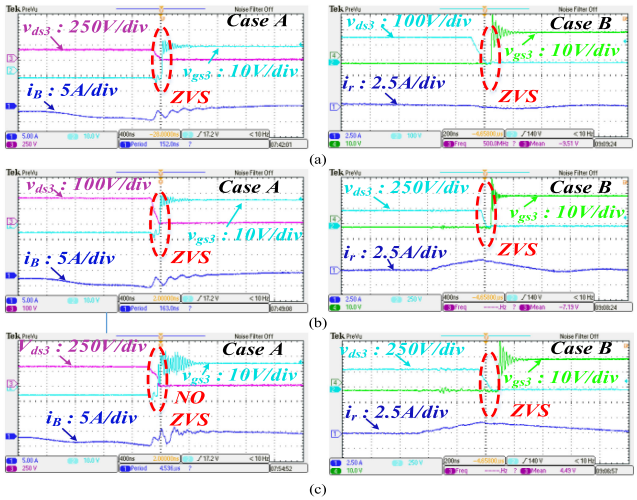

Fig. 17. ZVS waveforms for S_3 switch of the two cases A and B at 100 W. (a) $V_1 = 160$ V. (b) $V_1 = 240$ V. (c) $V_1 = 320$ V.

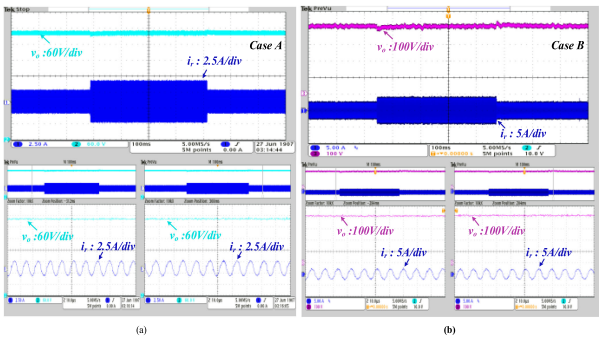

Fig. 18. Waveform of load step change from full load to half load. (a) Case A. (b) Case B.

between 0.5 and 1 kW are presented in Fig. 18. It can be seen from Fig. 18 that in both cases, the switching of load from half to full load is smooth and the output voltage changes only a little bit in facing. It shows that the proposed resonant converter has very good dynamic response.

The converter efficiency in cases A and B at different loads and different input voltages are plotted in Fig. 19. The two cases A and B have the maximum efficiency at $V_1 = 160$ V, because at this input voltage, the duty cycle $D_1 = 0.5$ and the circulating losses do not exist in the converter. From the efficiency graph in Fig. 19(b), it can be seen that when $V_1 = 240$ V, the case B efficiency is lower than that in case A; it is because case B has higher peak and RMS current when input voltage increases. However, when $V_1 = 320$ V, both cases have lower efficiencies. The circulating time period at $V_1 = 320$ V in case A is wide, as can be seen from the experimental results in Fig. 14, due to D_1 being approximately equal to zero. Consequently, in case B, at maximum input voltage, the high turn-OFF current and circulating current cause a reduction in efficiency. Therefore, as can be seen from the efficiency curve in Fig. 19(c), when $V_1 = 320$ V, both cases A and B have lower efficiency at full load as compared to lower input voltage. From the efficiency graph it can be concluded that under the whole input-voltage range, case A has better performance in terms of overall converter efficiency.

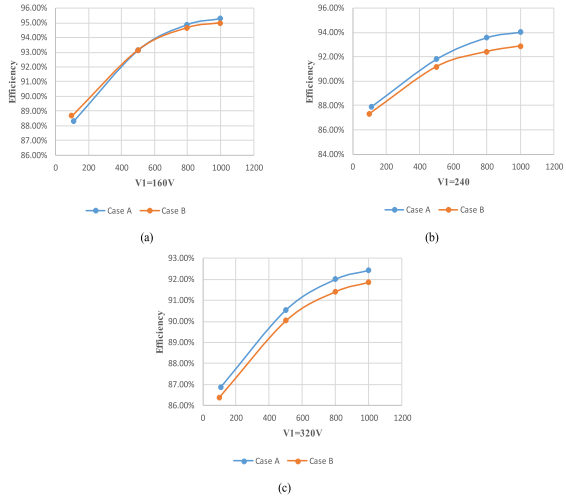

Fig. 19. Efficiency of cases A and B at different input voltages.

VI. Conclusion

In this article, a dual-transformer-based hybrid *LLC* resonant converter for wide input-voltage applications is proposed. The proposed converter is a hybrid combination of FB and HB circuits. It operates with fixed resonant frequency where a simple phase-shift PWM control is adopted to regulate the output voltage, which helps to simplify the magnetic components' design. For optimal design of turns ratio of the two transformers, two cases with different turns ratio have been examined and compared. The effect of resonant capacitor over the peak resonant current and the switches' turn-OFF currents are also described. A 1-kW prototype is designed and tested to verify the characteristics of the proposed converter. The steady-state and dynamic performance of the prototype are tested and the experimental results are presented. ZVS for the primary switches is also tested and verified under full load and whole input-voltage ranges. It is found that the proposed dual-transformer-based resonant *LLC* converter provides high efficiency for wide input-voltage applications.

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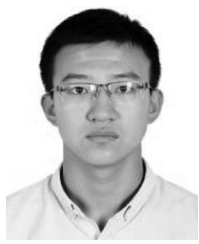

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