Physics-Based Modeling of Parasitic Capacitance in Medium-Voltage Filter Inductors

Hongbo Zhao, *Student Member, IEEE*, Dipen Narendra Dalal, *Student Member, IEEE*, Asger Bjørn Jørgensen, Jannick Kjær Jørgensen, Xiongfei Wang, *Senior Member, IEEE*, Szymon Bęczkowski, Stig Munk-Nielsen, *Member, IEEE*, and Christian Uhrenfeldt, *Member, IEEE*

***Abstract*—This article proposes a general physics-based model for identifying the parasitic capacitance in medium-voltage (MV) filter inductors, which can provide analytical calculations without using empirical equations and is not restricted by the geometrical structures of inductors. The elementary capacitances of the MV inductor are identified, then the equivalent capacitances between the two terminals of the inductor are derived under different voltage potential on the core. Further, a three-terminal equivalent circuit, instead of the conventional two-terminal equivalent circuit, is proposed by using the derived capacitances. Thus, the parasitic equivalent capacitance between the terminals and the core are explicitly quantified. Experimental measurements for parasitic capacitances show a good agreement with the theoretical calculations.**

***Index Terms*—Filter inductors, medium-voltage (MV), parasitic capacitance, physics-based modeling, three-terminal equivalent circuit.**

I. Introduction

With the recent advancements of the Silicon Carbide (SiC) technology, the blocking voltage of SiC metal–oxide–semiconductor field-effect transistor (MOSFET) devices has been increased to 10 and 15 kV [1], which brings several benefits to the medium-voltage (MV) power converters, such as a simpler circuit topology [2], [3], and lower turn-ON and turn-OFF switching energy dissipation than in Si devices [4].

Due to the faster switching behavior (higher dv/dt) of SiC MOSFET devices, the parasitic capacitances of MV converter systems are of significant concern [5]. The adverse effects of the parasitic capacitances on the converter operation are recently revealed, e.g., the transient heatsink grounding current [6], the drain current oscillations caused by power modules [7]–[9], and the common-mode current in the gate drivers [10], [11]. It has been shown that the parasitic capacitance of MV filter inductors can bring large spikes to the drain current and the load current [12], [13], which can be three times larger than the nominal load current [13], and consequently deteriorate electromagnetic interference issues [14] and accelerate the aging of the power modules [15].

The modeling and analysis of the parasitic capacitances in the MV converter filters have also attracted increasing attention. The physics-based modeling methods, which are based on the geometrical structures of inductors, are widely applied to calculate the parasitic capacitance of the filter inductors. Those methods can be broadly categorized into two groups, i.e., finite element methods (FEM) and analytical modeling methods.

The FEM models have better accuracy than the analytical models. In those models, the commonly used FEM-based software, e.g., ANSYS and COMSOL, are first used to extract the parasitic electrical parameters of components by means of a two-dimensional or a three-dimensional computer-aided design (CAD) tool [16], and then, the *RLC* matrix can be exported at certain frequencies [17]. Although convenient, this method has two restrictions, i.e., it is time-consuming if the components have complex structures and it is hard to derive design-oriented insights that can map the geometrical parameters to parasitic *RLC* parameters.

It is, therefore, of interest to develop the analytical modeling methods for calculating the parasitic capacitance of inductors, which is computationally more efficient and applicable for the model-based design and optimization when compared with the FEM-based alternatives [18]. Analytical modeling methods are capable of fully characterizing the capacitive couplings in inductors. Two approaches have been reported to derive the analytical models.

The first approach is based on the energy-conservation modeling [18]–[22], which is developed by assuming the equal voltage drops across the windings and using the energy-conservation law. A relative capacitance of the two adjacent planes between the two terminals of inductors can be derived, which is, however, dependent on the capacitance when the two adjacent planes are completely disconnected [19]. The empirical equations are, therefore, widely used for deriving the capacitance when the two adjacent planes are disconnected [19]–[22]. Yet, the empirical equations are not precise when the geometrical structure of inductors is complex, and hence, it is important to compensate for the errors. For that purpose, an improved model with equivalent relative permittivity is recently reported in [18]. However,

Manuscript received January 9, 2020; revised May 3, 2020; accepted June 8, 2020. Date of publication June 16, 2020; date of current version September 4, 2020. This work was supported by MV-BASIC Project funded by the Department of Energy Technology of Aalborg University, KK Wind Solutions, and Siemens Gamesa. Recommended for publication by Associate Editor Y.-M. Chen. *(Corresponding author: Xiongfei Wang.)*

The authors are with the Department of Energy Technology, Aalborg University, 9220 Aalborg, Denmark (e-mail: hzh@et.aau.dk; dnd@et.aau.dk; abj@et.aau.dk; jkj@et.aau.dk; xwa@et.aau.dk; sbe@et.aau.dk; smn@et.aau.dk; chu@et.aau.dk).

Color versions of one or more of the figures in this article are available online at https://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2020.3003157

the improved model is still not a general modeling method for inductors with a complex geometric structure.

The second method is based on the lumped-circuit modeling, which is, in theory, based on the charge-conservation law and the equivalent circuit network [23]–[28]. The circuit network is composed of multiple capacitances, where each capacitance can be theoretically calculated based on the charge-conservation law and the geometrical structure [23]. Although intuitive, the computational burden of this approach increases with the rising complexity of the equivalent circuit network. In case that the geometrical structure of the inductor winding is simple, the explicit analytical equation of overall capacitance between the two terminals of the inductor can be readily derived, based on the symmetry of the circuit without considering inductive effects [23]. However, when the geometrical structure is complex, or the inductive effects are considered, it is difficult to simplify the circuit network into the explicit analytical equations. It is, therefore, necessary to solve the circuit by using matrix-based calculators [27] and circuit-based simulators [28].

A common restriction of the previous analytical models is the two-terminal circuit assumption, which is merely valid for calculating the parasitic capacitance of inductors with a floating core. Yet, the same does not apply to inductors with a grounded core, since the inductor should be represented by a three-terminal equivalent circuit. The IEEE Std. C57.12.01 requires to ground the frame and core of the high-power dry-type transformers [29] such that the extra common-mode current injectioncan be observed [30], and thus the couplings between terminals and core cannot be neglected. Although there are no specific standards on the grounding requirements for high-power filter inductors, their frame and core are usually grounded in practice due to the safety requirements. Especially for the MV inductors, the potential of the core can float with high value if not grounded, due to the high voltages at the dc link and ac grid side.

Two major challenges can, therefore, be identified from the prior art, which are summarized as follows.

1) The energy-conservation modeling is constrained by the accuracy of the used empirical equations, while the lumped-circuit modeling is limited by the computational burden.
2) The two-terminal equivalent circuit is inadequate for modeling inductors with grounded cores, where the capacitive couplings between two terminals and the ground cannot be overlooked.

To address these challenges, this article proposes a physics-based modeling approach, where instead of directly using empirical equations as in [19], the inductor is modeled first as a circuit network of elementary capacitances, which are then lumped as total capacitances between inductor terminals by using the energy-conservation principle. Thus, a more general and computationally efficient modeling procedure than the conventional approaches is obtained. Further, based on the lumped capacitances of inductors, a three-terminal equivalent circuit, considering three different core potentials, is developed, which not only enables us to characterize the capacitive couplings between terminals and ground when the core is grounded but can also be readily adapted to inductors with floating cores. The calculations of the parasitic capacitance of the researched inductor by using the proposed modeling method have been verified experimentally.

II. Capacitive Couplings in MV Inductors

An MV filter inductor is given as an example in this article. The MV inductor is designed for a 5 kHz two-level voltage source converter based on SiC MOSFETs with 4.16 kV line-to-line voltage and 6 kV dc-link voltage.

Two U-type amorphous cores are used for the magnetic loop with a 2 mm air gap in between. Due to the high inductance of the required filter inductor, the dual windings are designed with a three-layer structure, which can increase the power density of the filter inductor. There are 63 turns in each layer. With 189 turns of a single winding, a 30 mH inductance is achieved with the dual windings. The inductor is designed to the rated RMS current of 8 A.

Three schematics of the MV inductor are shown in Fig. 1 to illustrate the physical structure. Fig. 1(a) is the CAD model of the designed MV 30 mH inductor. Fig. 1(b) is the horizontal cross-sectional view of the designed inductor. Fig. 1(c) is the vertical cross-sectional view of one of the dual windings of the designed inductor. As can be seen, some spacers are added between the two adjacent layers to provide an extra distance for reducing the equivalent parasitic layer-to-layer capacitance. Bobbins are added between the inner layer and core for insulating the core and windings. The key parameters of the physical structure of the inductor are listed in Table I.

The values for the relative permittivity of the materials are listed in Table II, which are identified from the datasheet.

The cables for windings are selected as DAMID 200 [31]. The coating material of the cables is THEIC-modified polyester. The bobbins are selected as UI/120/41 for c-type cores [32]. The material of bobbin is Durethan BKV 30 H3, which is based on polyamide 6 with 30% glass-reinforced [33]. The spacers between the two adjacent layers are manufactured by using the same material as bobbins. The relative permittivity of polyester is between 2.8 and 4.5 [34]. Therefore, the average value of 3.7 is used in this article.

The capacitive couplings in this inductor are identified as follows.

1) The turn-to-turn capacitive coupling contributed by the voltage potential difference between two neighbor turns in the same layer.
2) The layer-to-layer capacitive coupling resulted from the voltage potential difference between two neighbor turns at different layers.
3) The layer-to-core capacitive coupling caused by the voltage potential differences between the inner layer and the core.
4) The winding-to-winding capacitive coupling resulted from the voltage potential differences between the two windings.

III. Conventional Analytical Modeling Methods

This section reviews two commonly used analytical modeling methods, and the constraints for calculating the parasitic capacitance of the researched MV filter inductor are highlighted.

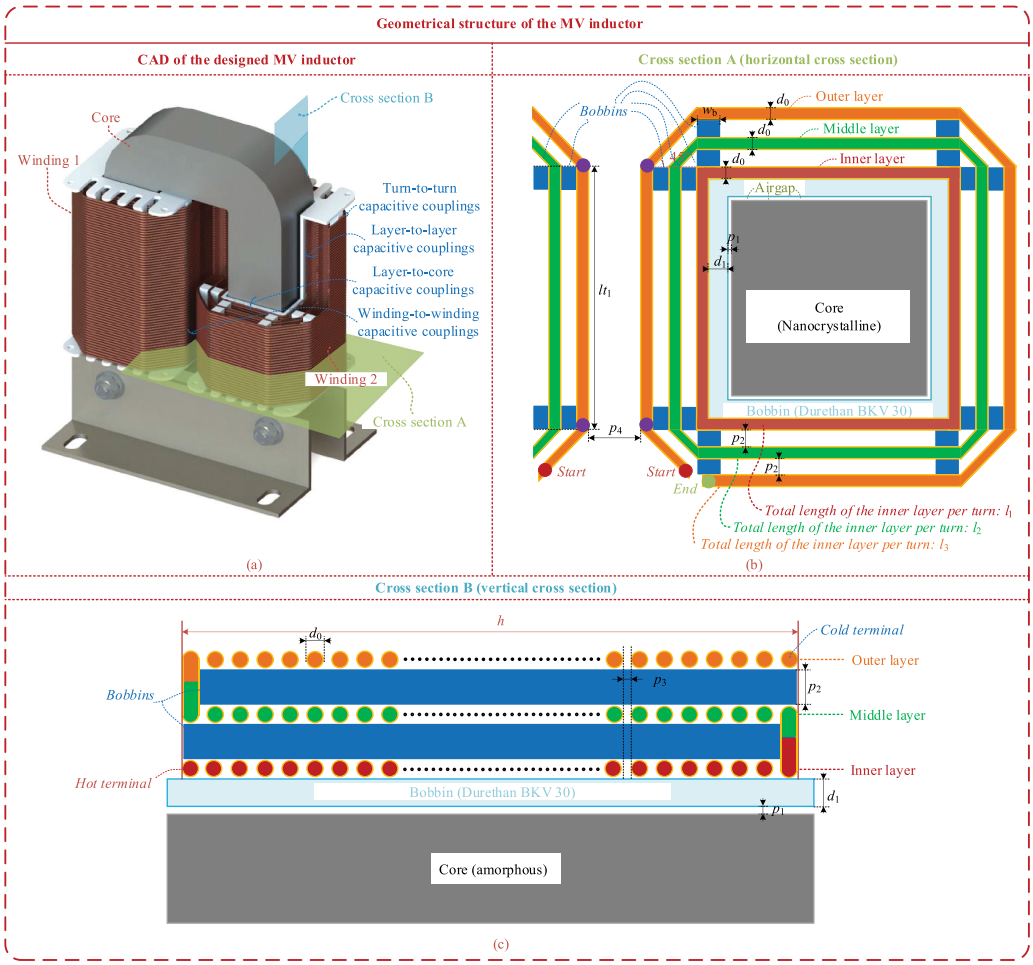


Fig. 1. Schematics for deriving geometrical parameters of the MV inductor. (a) CAD model and capacitive couplings. (b) Cross section A (horizontal cross section). (c) Cross section B (vertical cross section).

A. *Lumped-Circuit Modeling Method*

Based on [23]–[26], the lumped-circuit modeling method is used for characterizing the parasitic capacitance of the researched inductor.

The turn-to-turn, layer-to-layer, and winding-to-winding capacitive couplings can be decomposed into elementary turn-to-turn capacitances since all of them can be represented by the voltage potential difference between the two turns. The bobbins (spacers) can be used between the two adjacent layers, and hence, the elementary turn-to-turn capacitance with and without bobbins needs to be considered, respectively. In contrast, the layer-to-core capacitive coupling is composed of multiple elementary turn-to-core capacitances. Since the bobbins are always used in high-power inductors, only the elementary turn-to-core capacitance with bobbins is derived.

Therefore, three elementary capacitances of the researched MV inductor are developed, which are given in Fig. 2. r_c and r_0 are the radii of the conductor and turn including coating. p and p_c are the lengths of the air gap between two turns for calculating elementary turn-to-turn and turn-to-core capacitance. l_{b1} and l_{b2} are the thickness of the two different bobbins. Θ is the elementary angle.

In Fig. 2, $C_c(\theta)$ is the elementary coating capacitance, $C_{g1}(\theta)$, $C_{g2}(\theta)$, and $C_{g3}(\theta)$ are the elementary air capacitances. $C_{b1}(\theta)$ and $C_{b2}(\theta)$ are the elementary bobbin capacitances, and C_{core} is the elementary core capacitance.

The derived equations for representing the elementary turn-to-turn capacitances without bobbins $C_{\text{ele\_turn-to-turn}}$ of Fig. 2(a) are shown as follows:

$$dC_c(\theta) = \frac{\varepsilon_r \varepsilon_0}{\text{In}\frac{r_0}{r_c}} d\theta \qquad dC_{g1}(\theta) = \frac{\varepsilon_0 r_0}{p + 2r_0(1-\cos\theta)} d\theta$$
$$\frac{1}{dC_{\text{ele\_turn-to-turn}}(\theta)} = \frac{1}{dC_c(\theta)} + \frac{1}{dC_{g1}(\theta)} + \frac{1}{dC_c(\theta)} \quad (1)$$

where, ε_0 and ε_r are the permittivity of vacuum and coating, respectively. Therefore, the integrated elementary capacitance $C'_{\text{ele\_turn-to-turn}}$ between two neighbor turns in Fig. 1(a) can be represented as the following equation, where the integrated angle is from $[-\pi/2, \pi/2]$ [24]:

$$C'_{\text{ele\_turn-to-turn}} = \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} dC_{\text{ele\_turn-to-turn}}(\theta) \quad (2)$$

TABLE I
KEY PARAMETERS OF THE MV INDUCTOR

Description	Symbol	Value
Diameter of the cable	d_0	1.4 mm
Length of the air gap between the bobbin and core	p_1	0.75 mm
Thickness of the bobbins between the inner layer and core	d_1	2 mm
Length of the air gap between two adjacent layers	p_2	5.7 mm
Average length of the air gap between two turns in the same layer	p_3	0.45 mm
Height of the windings	h	11.9 cm
Width of the spacers between two adjacent layers	w_b	4.8 mm
Length of the outer layer per turn	l_1	24.7 cm
Length of the middle layer per turn	l_2	22.2 cm
Length of the inner layer per turn	l_3	19.7 cm
Average length of per turn for three layers	l	22.2 cm
Average length of the air gap between the two windings	p_4	3 mm
Number of turns of per layers	n	63
Number of layers	m	3
Number of the winding	w	2
Total inductance	L	30 mH
Equivalent inductance per turn	L_1	0.079 mH

TABLE II
RELATIVE PERMITTIVITY OF THE MATERIAL

Description	Symbol	Value
The permittivity of the bobbins [33]	ε_b	4.0
The permittivity of the coating of cables [34]	ε_r	3.7 (average value)
The permittivity of vacuum [35]	ε_0	8.82×10^{-12} F/m

Similarly, the integrated elementary turn-to-turn capacitance with bobbins $C'_{\text{ele\_turn-to-turn\_wb}}$ and turn-to-core capacitance $C'_{\text{ele\_turn-to-core\_wb}}$ are derived.

By using the integrated elementary capacitance, the equivalent circuit of the parasitic capacitive couplings of the researched inductor can be constructed as

$$\begin{cases} \dfrac{1}{dC_{\text{ele\_turn-to-turn\_wb}}(\theta)} = \dfrac{2}{dC_c(\theta)} + \dfrac{2}{dC_{g2}(\theta)} + \dfrac{1}{dC_{b1}(\theta)} \\ C'_{\text{ele\_turn-to-turn\_wb}} = \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} dC_{\text{ele\_turn-to-turn\_wb}}(\theta) \end{cases} \tag{3}$$

$$\begin{cases} \dfrac{1}{dC_{\text{ele\_turn-to-core\_wb}}(\theta)} = \dfrac{1}{dC_c(\theta)} + \dfrac{1}{dC_{g2}(\theta)} + \dfrac{1}{dC_{b2}(\theta)} \\ \qquad\qquad + \dfrac{1}{dC_{g3}(\theta)} \\ C'_{\text{ele\_turn-to-core\_wb}} = \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} dC_{\text{ele\_turn-to-core\_wb}}(\theta). \end{cases} \tag{4}$$

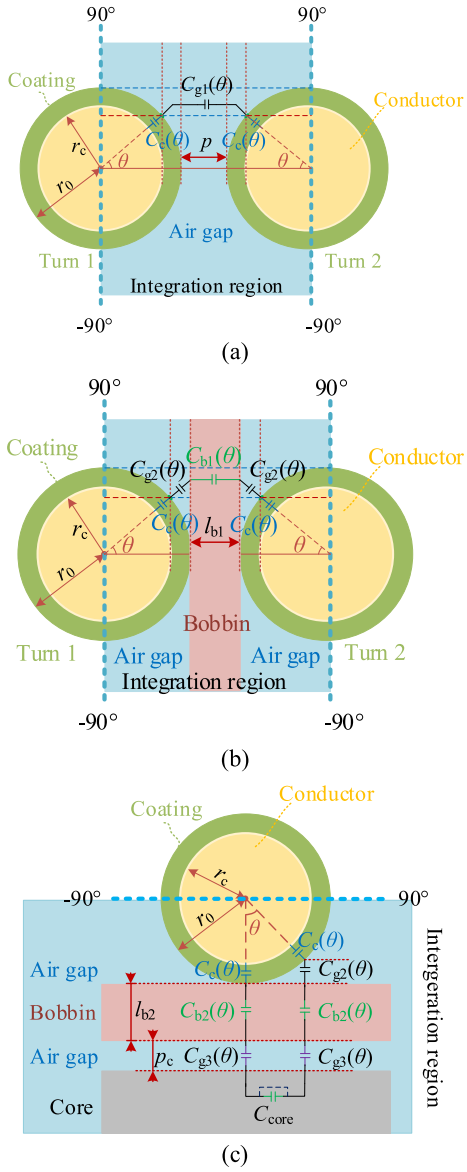


Fig. 2. Elementary capacitances of the researched inductor. (a) Turn-to-turn capacitance without bobbins. (b) Turn-to-turn capacitance with bobbins. (c) Turn-to-core capacitance.

However, the explicit analytical equation of the parasitic capacitance cannot be identified in this application, since the mathematical induction methods reported in [23]–[25] are only valid for the inductors with simple geometrical structures, where the researched MV inductor has a three-layer and double-winding structure.

B. Energy-Conservation Modeling Method

The parasitic capacitance between two adjacent planes can also be described by using the stored electrical-field energy [18]–[22]. The voltage potential on the plane is assumed to be linearly distributed.

Using this theory, the lumped turn-to-turn capacitance of m-layer cable with n-turns per layer, which is presented in Fig. 3, can be derived as (5) for two windings. V_1 is the voltage potential

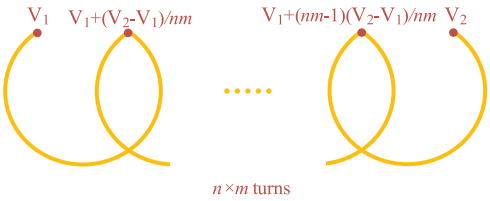


Fig. 3. Schematic of multiple turns within a winding.

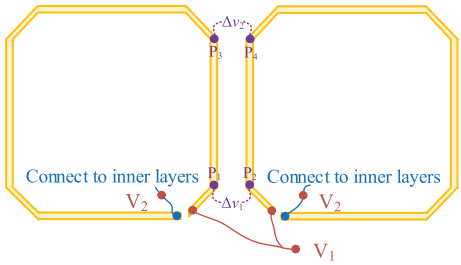


Fig. 4. Schematic of the two windings.

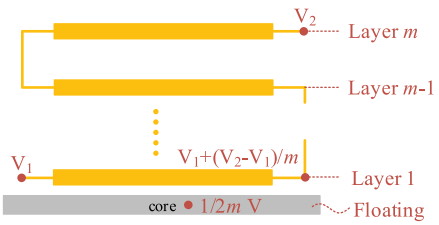


Fig. 5. Schematic of multiple layers and a core within a winding.

at the first turn, where V_2 is the voltage potential at the last turn. n is the number of turns in one layer, m is the number of layers

$$C_{\text{eq\_turn-to-turn}} = 2 \times \frac{nm-1}{(nm)^2} \times C_{\text{eq\_turn-to-turn\_dis}} \quad (5)$$

where $C_{\text{eq\_turn-to-turn\_dis}}$ is the capacitance between two adjacent turns when disconnected. The detailed derivations are attached in Appendix A.

In Fig. 4, the lumped winding-to-winding capacitance is addressed, where the equation is presented in (6). In this case, only the region within $P_1P_2P_3P_4$ is assumed to store the electrical field energy between the two windings.

$$C_{\text{eq\_winding\_to\_winding}} = \frac{(\Delta v_1^2 + \Delta v_2^2 + \Delta v_1 \Delta v_2)}{3nm(\text{V}_2 - \text{V}_1)^2} C_{\text{eq\_winding-to-winding\_dis}} \quad (6)$$

where $C_{\text{eq\_winding-to-winding\_dis}}$ is the capacitance between the two adjacent windings of P_1P_3 and P_2P_4 when disconnected. The voltage potential between $P1$ and $P2$ is Δv_1, where the voltage potential between $P3$ and $P4$ is Δv_2. The detailed derivations are attached in Appendix B.

Similarly, the lumped layer-to-layer capacitance, shown in Fig. 5, is derived as

$$C_{\text{eq\_layer-to-layer}} = \frac{4(m-1)}{3m} \times C_{\text{eq\_layer-to-layer\_dis}} \quad (7)$$

where $C_{\text{eq\_layer-to-layer\_dis}}$ is the capacitance between the two adjacent layers when disconnected. The detailed deviations are attached in Appendix C.

Finally, the lumped layer-to-core capacitance between the inner layer and core shown in Fig. 5 is calculated as the following equation for the two windings, where the core is assumed to be floating in this case:

$$C_{\text{eq\_layer-to-core1}} = \frac{1}{12m^2} \times C_{\text{eq\_layer-to-core\_dis}} \quad (8)$$

where $C_{\text{eq\_layer-to-layer\_dis}}$ is the intermediate capacitance between the inner layer and core. The detailed derivations are attached in Appendix D.

The total lumped capacitance can be calculated as the sum of (5)–(8). Generally, the intermediate capacitance $C_{\text{eq\_turn-to-turn\_dis}}$, $C_{\text{eq\_winding-to-winding\_dis}}$, $C_{\text{eq\_layer-to-layer\_dis}}$, and $C_{\text{eq\_layer-to-core\_dis}}$ can be derived by using the empirical equations in [19].

However, the empirical equations will introduce significant errors when the geometrical structure of the inductors is complex since it is not a general solution for deriving the intermediate capacitances. Besides, this method is derived based on the assumption that the core is floating. Therefore, it cannot characterize the parasitic coupling between terminals and ground when the core is grounded.

IV. Proposed Analytical Modeling Method

The step-by-step modeling processes of the proposed analytical modeling method are given in Fig. 6.

In Fig. 6, Steps 1)–4) can be obtained by using the previous modeling methods introduced in Section III. The processes of Steps 5)–9) are given in detail as follows.

A. Step 5) Deriving the Intermediate Lumped Capacitances When Adjacent Planes Are Disconnected

Fig. 7(a) is the equivalent circuit of the capacitive coupling between the two neighbor turns with elementary capacitance and inductance, where the two neighbor turns are assumed to be disconnected. The equivalent circuit in Fig. 7(a) is simplified as (b). The impedance of the submodule is given as the following equation:

$$Z_{\text{AB}} = j\omega L_{\text{ele\_turn-to-turn}} + \frac{1}{j\omega C_{\text{eq\_turn-to-turn\_wb\_dis}}}. \quad (9)$$

For frequencies much smaller than the characteristic frequency, the submodule is simplified into a single capacitor, which is given as

$$Z_{\text{AB}} \approx \frac{1}{j\omega C_{\text{eq\_turn-to-turn\_wb\_dis}}} \quad f \ll \frac{1}{2\pi\sqrt{2L_{\text{ele\_turn-to-turn}} C_{\text{eq\_turn-to-turn\_wb\_dis}}}}. \quad (10)$$

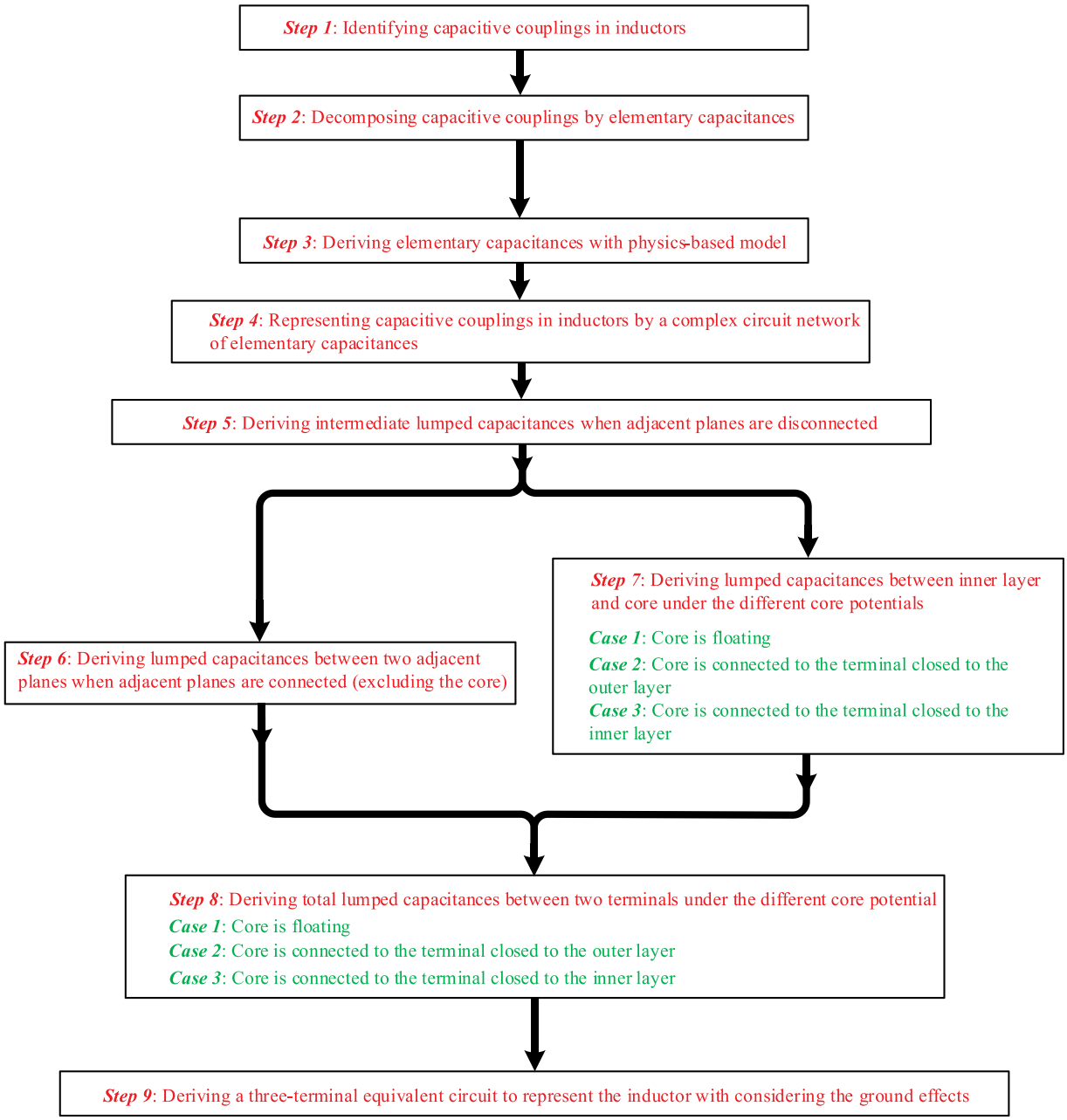


Fig. 6. Flowchart for the proposed physics-based modeling method.

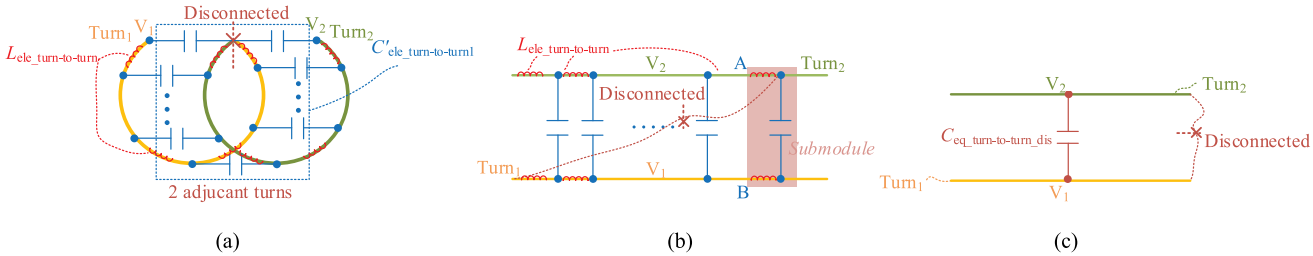


Fig. 7. Parasitic capacitance between two neighbor turns. (a) Equivalent circuit. (b) Simplification of the equivalent circuit. (c) Equivalent circuit when the frequency is much smaller than the characteristic frequency.

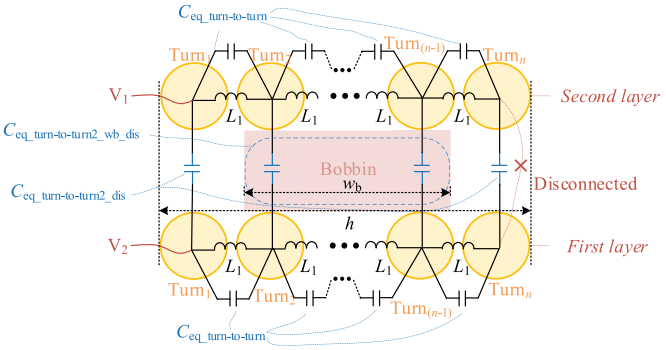


Fig. 8. Equivalent circuit of the parasitic capacitance between two layers.

Therefore, the equivalent circuit can be simplified as Fig. 7(c), which is represented by a single capacitor. Then the intermediate lumped capacitance between the two neighbor turns when disconnected can be presented as

$$\begin{aligned} C_{\text{eq\_turn-to-turn\_dis}} &= n \times C_{\text{eq\_turn-to-turn\_wb\_dis}} \\ &= l_{\text{turn}} \times C'_{\text{ele\_turn-to-turn1}} \end{aligned} \tag{11}$$

where l_{turn} is the length of a single turn.

The equivalent circuit between two neighbor layers is presented in Fig. 8, where partial layers (red region in Fig. 8) are inserted with bobbins in between. The width of the bobbin is labeled as w_b, where the width of a layer is labeled as h. L_1 is the equivalent inductance per turn.

The equivalent capacitances per turn with and without layers are given as the following equation, where x is the ratio of turns that have bobbins between the adjacent layers and y is the ratio of turns that only have air between the adjacent layers:

$$\begin{aligned} C_{\text{eq\_turn-to-turn2\_dis}} &= C'_{\text{ele\_turn-to-turn2}} \times l_{\text{turn}} \times x \\ C_{\text{eq\_turn-to-turn2\_wb\_dis}} &= C'_{\text{ele\_turn-to-turn2\_wb}} \times l_{\text{turn}} \times y \end{aligned} \tag{12}$$

where $x = w_b/h$ and $y = 1 - w_b/h$.

Similarly, the intermediate lumped capacitance between the two layers when disconnected is obtained as the following equation when the frequency is much smaller than the characteristic frequency:

$$\begin{aligned} &C_{\text{eq\_layer-to-layer\_dis}} \\ &\quad = n \times (C_{\text{eq\_turn-to-turn2\_dis}} + C_{\text{eq\_turn-to-turn2\_wb\_dis}}) \\ &f \ll \min\left[\frac{1}{2\pi\sqrt{L_1 C_{\text{eq\_turn-to-turn2\_dis}}}}, \right. \\ &\qquad \frac{1}{2\pi\sqrt{L_1 C_{\text{ele\_turn-to-turn2\_wb\_dis}}}}, \\ &\qquad \left. \frac{1}{2\pi\sqrt{L_1 C_{\text{eq\_turn-to-turn\_dis}}}}\right]. \end{aligned} \tag{13}$$

The equivalent circuit between the inner layer and the core is presented in Fig. 9. The equivalent capacitance per turn between

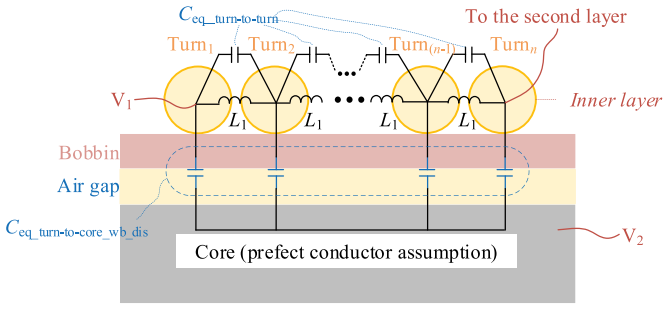


Fig. 9. Equivalent circuit of the parasitic capacitance between the inner layer and core.

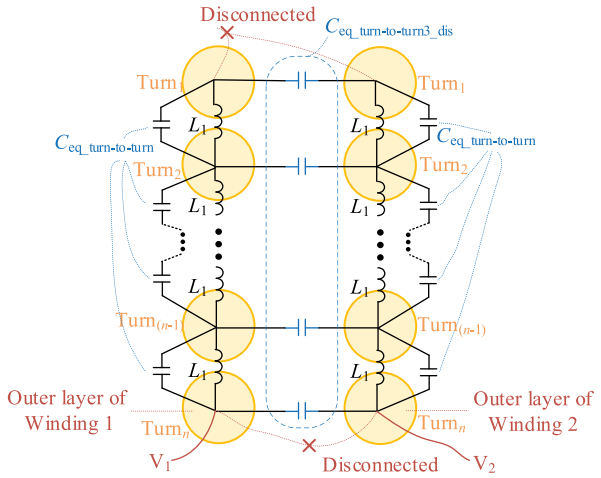


Fig. 10. Equivalent circuit of the parasitic capacitance between two windings.

the inner layer and core is presented as

$$C_{\text{eq\_turn-to-core\_wb\_dis}} = C'_{\text{ele\_turn-to-core\_wb}} \times l_{\text{turn}}. \tag{14}$$

The intermediate lumped capacitance between the inner layer and core when disconnected is obtained as the following equation when the frequency is much smaller than the characteristic frequency:

$$\begin{aligned} &C_{\text{eq\_layer-to-core\_dis}} = n \times C_{\text{eq\_turn-to-core\_wb\_dis}} \\ &f \ll \min\left[\frac{1}{2\pi\sqrt{L_1 C_{\text{eq\_turn-to-turn\_dis}}}}, \right. \\ &\qquad \left. \frac{1}{2\pi\sqrt{L_1 C_{\text{eq\_turn-to-core\_wb}}}}\right]. \end{aligned} \tag{15}$$

The equivalent circuit between the two windings is presented in Fig. 10. The equivalent capacitance per turn between the two windings is presented as

$$C_{\text{eq\_turn-to-turn3\_dis}} = C'_{\text{ele\_turn-to-turn3}} \times l_{\text{turn}}. \tag{16}$$

The intermediate capacitance between the two windings when disconnected is presented as the following equation when the

frequency is much smaller than the characteristic frequency:

$$C_{\text{eq\_wingding-to-winding\_dis}} = n \times C_{\text{eq\_turn-to-turn3\_dis}}$$
$$\text{for } f \ll \min\left[\frac{1}{2\pi\sqrt{L_1 C_{\text{eq\_turn-to-turn3\_dis}}}}, \frac{1}{2\pi\sqrt{L_1 C_{\text{eq\_turn-to-turn\_dis}}}}\right]. \quad (17)$$

The obtained intermediate capacitances will be further used in the following derivations.

B. Step 6) Deriving Lumped Capacitances Between Two Adjacent Planes When Adjacent Planes Are Connected (Excluding the Core)

In this step, the adjacent planes are connected, and thus, the voltage potential on each plane is assumed to be linearly distributed. With the intermediate lumped capacitance obtained in Step 5), the energy stored in the electric field of two connected adjacent planes can be derived, which is then used to calculate the lumped capacitance seen from the terminals of planes, based on the former derivations by using the energy-conservation law.

1) The total lumped turn-to-turn capacitance is calculated in (5) by substituting (11).
2) The total lumped winding-to-winding capacitance is given in (6) by substituting (17). This method is also adapted to the inductors with multiple windings.
3) The total lumped layer-to-layer capacitance is given in (7) by substituting (13).

C. Step 7) Deriving Lumped Capacitance Between the Inner Layer and Core Under Different Core Potentials

Three cases of the inductor with three different voltage potentials on the core are analyzed.

In this step, it is assumed that the voltage potential on the core is distributed equally. For the inductors with multilayer winding structure, the terminal at the outer layer has less capacitive couplings to the core due to larger coupling distance, and hence, the terminals at the inner layer and outer layer are characterized separately. The hot terminal and cold terminal are defined here, where the terminal closest to the inner layer is named as hot terminal, and the terminal closest to the outer layer is named as cold terminal. The voltage potential of the hot terminal is defined as V_1, while the voltage potential of the cold terminal is defined as V_2.

The lumped capacitances between the inner layer and core are discussed in three cases as follows.

1) Case 1: The core is assumed to be floating. Then, the voltage potential on the core is equal and assumed to be the average value of the potential in the inner layer. The derived capacitance is already given as (8).
2) Case 2: The core is connected to the hot terminal, which is presented as Fig. 11(a). Since the voltage potential of the hot terminal is V_1, the potential on the core is equal and clamped to V_1. The derived equation is presented as

$$C_{\text{eq\_layer-to-core2}} = 2 \times \frac{1}{3m^2} \times C_{\text{eq\_layer-to-core\_dis}} \quad (18)$$

3) Case 3: The core is connected to the cold terminal, which is presented as Fig. 11(b). Since the voltage potential of the cold terminal is V_2, the potential on the core is equal and clamped to V_2. The derived equation is given as

$$C_{\text{eq\_layer-to-core3}} = 2 \times \frac{3m^2 - 3m + 1}{3m^2} \times C_{\text{eq\_layer-to-core\_dis}}. \quad (19)$$

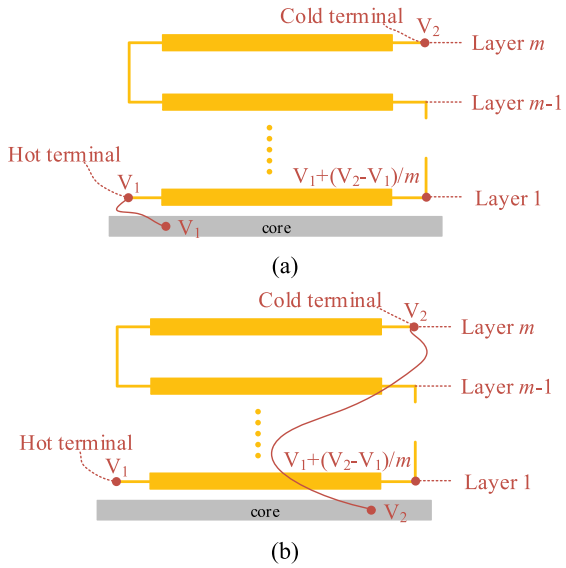


Fig. 11. Schematic of the inner layer and core with different configurations. (a) Case 2: Core is clamped to the hot terminal. (b) Core is clamped to the cold terminal.

Equations (18) and (19) can be solved by substituting (15). The detailed derivation process of (18) and (19) is attached in Appendix D.

D. Step 8) Deriving Total Lumped Capacitance Between Two Terminals Under Different Core Potential

Based on the energy-conservation law, the total lumped capacitances represent the total electrical field energy stored in the inductor, which is composed of the electric field energy stored in between the neighbor turns, neighbor layers, neighbor windings, and the inner layer to the core. Therefore, the total lumped capacitances C_{total1}, C_{total2}, and C_{total3} between the two terminals of the inductor in the three cases are calculated as the following, which is a sum of the derived lumped turn-to-turn, layer-to-layer, winding-to-winding, and layer-to-core capacitances:

In (20), shown at the bottom of the next page, for the inductors with single-layer windings, the calculated total capacitances C_{total2} and C_{total3} should be the same due to the symmetrical structure. However, for the inductors with multilayer windings, C_{total2} and C_{total3} are different due to the voltage potential difference between the inner layer and core, respectively.

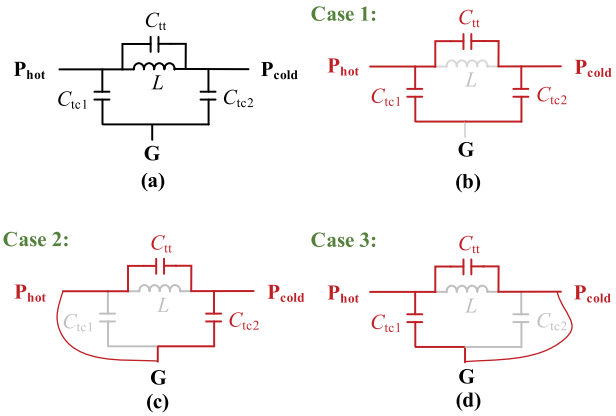


Fig. 12. Derivation of the three-terminal equivalent circuit schematic. (a) Schematic diagram. (b)–(d) Representation of three cases with different terminal connections.

E. Step 9) Deriving Total Lumped Capacitance Between Two Terminals Under Different Core Potential

Since the lumped total capacitance is dependent on three different core potentials, it is still not straightforward to understand the capacitive couplings between the two terminals and core, especially when the core is grounded. Therefore, a three-terminal equivalent circuit presented in Fig. 12(a) is introduced to account for the couplings, which is based on the derived total lumped capacitances in three different cases.

In the three-terminal equivalent circuit, the cold terminal of the inductor is represented by P_{cold}, the hot terminal is represented by P_{hot}, and the ground point of the frame/core is represented by G. L_1 is the equivalent inductance. C_{tt} represents the coupling capacitance between P_{cold} and P_{hot}. C_{tc1} represents the coupling capacitance between P_{hot} and G. C_{tc2} represents the coupling capacitance between P_{cold} and G.

The mathematical transformation can be formulated by mapping the three cases to a practical three-terminal equivalent circuit in the low-frequency range.

1) Case 1 is represented by the equivalent circuit in Fig. 12(b), where the ground point and the core are floating as well.
2) Case 2 is modeled as the equivalent circuit in Fig. 12(c), where the ground point is connected to the hot terminal, which means C_{tc1} is shorted in this case.
3) Case 3 is modeled as the equivalent circuit in Fig. 12(d), where the ground point is connected to the cold terminal, implying that C_{tc2} is shorted in this case.

Consequently, the total equivalent capacitances can be obtained as

$$\begin{cases} C_{\text{total1}} = C_{\text{tt}} + (C_{\text{tc1}} // C_{\text{tc2}}) \\ C_{\text{total2}} = C_{\text{tt}} + C_{\text{tc2}} \\ C_{\text{total3}} = C_{\text{tt}} + C_{\text{tc1}}. \end{cases} \tag{21}$$

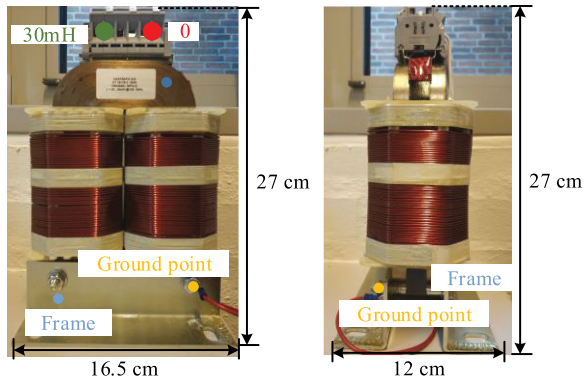


Fig. 13. Photographs of the researched MV inductor.

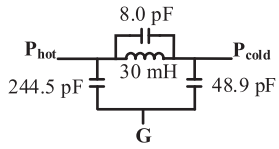


Fig. 14. Three-terminal equivalent circuit for the researched MV inductor.

For the inductors with multilayer windings, C_{tc1} and C_{tc2} are not equal, due to the different value C_{total2} and C_{total3} of inductors with a multilayer structure. Therefore, the capacitances of equivalent circuits are unbalanced in the cases of the inductor with multilayer windings. It is worth mentioning that the three-terminal equivalent circuit is obtained mathematically, where a negative capacitance may result in the calculation.

V. Model Validations

By using the explicit equations derived from the proposed physics-based modeling method, the parasitic capacitances of a 30 mH MV filter inductor are calculated theoretically based on the geometrical structure and material information of the researched inductor. The pictures of the researched 30 mH MV filter inductor are shown in Fig. 13.

A. Theoretical Calculations

Based on the derived equations (1)–(21) and physical parameters, the lumped turn-to-turn, layer-to-layer, layer-to-core, and winding-to-winding capacitance, and total lumped capacitances for three cases are calculated, which are listed in Table III. It is worth to mention that the electrical field energy stored between two windings is zero since the voltage potential on P_1P_3 and P_2P_4 are the same in this case.

By using the calculated values of the three capacitances for three cases presented in Table III, the three-terminal equivalent circuit is derived based on (21), which is given in Fig. 14. It is

Case 1: The core is floating $C_{\text{total1}} = C_{\text{eq\_turn-to-turn}} + C_{\text{eq\_layer\_to\_layer}} + C_{\text{eq\_layer\_to\_core1}} + C_{\text{eq\_winding\_to\_winding}}$
Case 2: The core is clamped to V_1 $C_{\text{total2}} = C_{\text{eq\_turn-to-turn}} + C_{\text{eq\_layer\_to\_layer}} + C_{\text{eq\_layer\_to\_core2}} + C_{\text{eq\_winding\_to\_winding}}$
Case 3: The core is clamped to V_2 $C_{\text{total3}} = C_{\text{eq\_turn-to-turn}} + C_{\text{eq\_layer\_to\_layer}} + C_{\text{eq\_layer\_to\_core3}} + C_{\text{eq\_winding\_to\_winding}}$ (20)

TABLE III
TOTAL PARASITIC EQUIVALENT CAPACITANCE FOR THE THREE DIFFERENT CASES

Case	Description	Equivalent turn-to-turn capacitance	Equivalent layer-to-layer capacitance	Equivalent layer-to-core capacitance	Equivalent winding-to-winding capacitance	Total capacitance
Case1	G is floating	0.06 pF	45.98 pF	2.72 pF	0 pF	48.76 pF
Case2	G is connected to the P_{cold}			10.86 pF		56.90 pF
Case3	G is connected to the P_{hot}			206.5 pF		252.54 pF

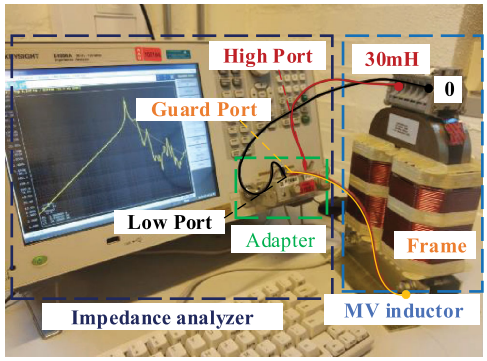


Fig. 15. Impedance measurement setup by using the Keysight E4990A and its adapter 16047.

worth to mention that the equivalent capacitance between the $P_{\rm hot}$ and G is different from the equivalent capacitance between the $P_{\rm cold}$ and G.

The valid frequency range of the designed MV inductors for using the proposed physical-based lumped-parameter model is calculated as the following equation based on the minimum characteristic frequency given in (10), (13), (15), and (17):

$$f \ll 6.8\,\text{MHz}. \tag{22}$$

B. Experimental Verifications

In order to verify the calculated parasitic capacitances of the designed inductor, the experimental results are carried out in this section. The parasitic capacitances of the three different cases are measured directly or indirectly by using a Keysight E4990A impedance analyzer and its adapter 16047. The measurement principle is based on the autobalancing bridge method [36]. Both measurement methods with and without guarding technology are utilized to validate the theoretical analysis, where the setup is shown in Fig. 15. The principles and measurement processes for these two measurement methods are well described in [36].

Fig. 16 shows the comparisons between the impedance measurement using the traditional measurement method, the guarding technology, and the theoretically obtained impedance, which is derived with the known value of designed inductance (30 mH) paralleled with the calculated parasitic capacitance. The measured parasitic capacitance is obtained with fitting by using an equivalent circuit in the impedance analyzer. Fig. 16(a) shows the comparison between the measured impedance and theoretically calculated impedance.

Since the guarding technology is a three-terminal measurement method, where each impedance of the equivalent three-terminal circuit is measured directly and individually. The measured three different capacitances are converted into the total equivalent capacitances Cases 1–3 by following (20). The calculated impedance shows good agreement with measured impedance at the resonant point before the calculated valid frequency range. Fig. 16(b) shows the comparison between the theoretically calculated impedance and converted impedance based on the measurements with the guarding method. In Fig. 16, since the damping resistances are not modeled in the theoretical calculations and converted impedance, both of them have an infinite magnitude at the first resonant frequency (FRF).

The valid frequency range should be much smaller than 6.8 MHz, which is verified in Fig. 16 as well. The unbalanced terminal-to-ground capacitances of inductors with multiple layers are also predicted by the proposed modeling method, according to Fig. 16 since the FRF in Cases 2 and 3 are not equal.

C. Comparisons and Error Analysis

The results calculated by using the proposed modeling method and the other two analytical energy-conservation based modeling methods are compared with the measurements in Table IV.

It can be found that the two typical modeling methods are only valid in Case 1, where the proposed modeling method has the least error t_s around 2% using the normal measurements and 15% using the guarding technology. As expected, [18] and [19] can only characterize a two-terminal equivalent circuit for the inductors.

In Cases 2 and 3, the calculations of using the proposed modeling method are close to the measurement results, where the maximum errors are 10% with using the normal measurements and 15% using the guarding technology. It is worth noticing that the calculations are based on purely geometrical input and material parameter estimates and thus are not fitted to any measurements. Therefore, the errors are acceptable since the absolute value is still in the pF level. Multiple reasons might be responsible for the errors.

1) The value of relative permittivity bobbin and coating material has a direct impact on results.
2) Geometrical errors might arise from the deviations of the idealized winding structure in Fig. 1 relative to the practical inductor.
3) The assumptions made for simplifying the modeling will influence the final results. For example, the voltage potential is assumed to be distributed linearly on the conductor, which might not be realistic. However, these assumptions

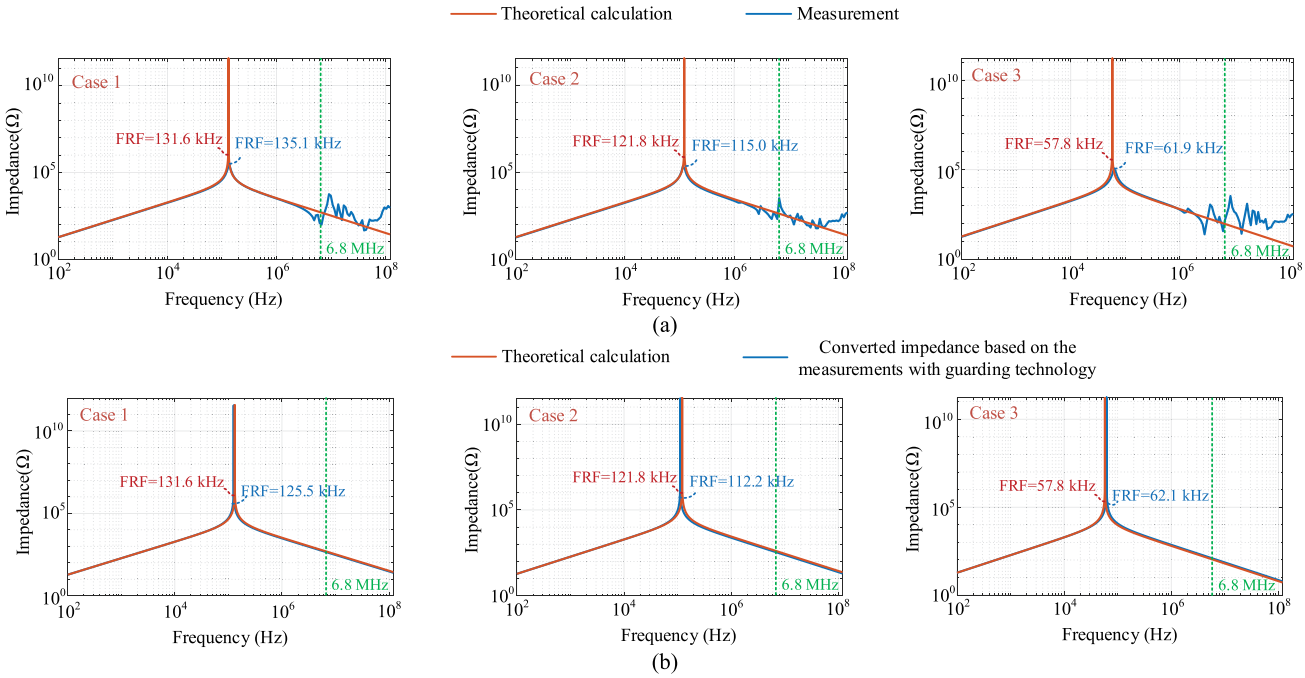
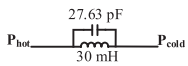
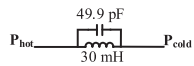
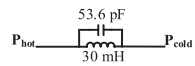
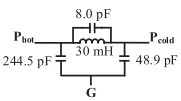
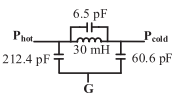
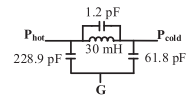


Fig. 16. Comparisons of the measured and calculated impedance of three cases. (a) Based on the theoretical analysis and measurement methods without using guarding technology. (b) Based on the theoretical analysis and calculations by measurements with the guarding technology.

TABLE IV
NUMERICAL COMPARISONS OF PARASITIC CAPACITANCES BETWEEN THE MEASUREMENTS AND CALCULATIONS

Case	Calculations (Proposed method)	Calculations (method [19])	Calculations (method [18])	Measured capacitance (Normal measurements)	Converted capacitance based on the measurements with guarding method
Case 1	48.76 pF (C_{total1})	27.63 pF	43.22 pF	49.9 pF	53.6 pF
Case 2	56.90 pF (C_{total2})	Not valid	Not valid	63.0 pF	67.1 pF
Case 3	252.54 pF (C_{total3})	Not valid	Not valid	230.1 pF	218.9 pF
Two-terminal equivalent circuit					
Three-terminal equivalent circuit		Not valid	Not valid		

are compromises between the complexity and accuracy of models.

4) The measurement methods can introduce errors to themselves. As can be seen from Table IV, the maximum error between two different measurement results is up to 5%.

VI. CONCLUSION

This article has discussed a physics-based modeling method for calculating the parasitic capacitances in inductors with considering the ground effects. Instead of using empirical equations, a computationally efficient approach for calculating the lumped capacitances between the adjacent layers, turns, windings, as well as the inner layer and core has been introduced. Furthermore, a three-terminal equivalent circuit has been developed, which enables us to characterize the capacitive couplings between two terminals of inductors and the capacitive couplings between the terminal and the core. The measurements on a commercial MV filter inductor have been shown. The results verified the correctness of the proposed modeling method, where the unbalanced capacitances between the terminals and ground of inductors are revealed.

APPENDIX

Derivation of the lumped capacitance when the adjacent planes are connected.

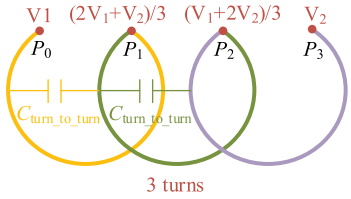


Fig. 17. Schematic for the lumped turn-to-turn capacitance of three turns (example) with linear voltage potential distribution. The lumped turn-to-turn capacitance is derived according to (a1).

A. Lumped Turn-to-Turn Capacitance

Using a winding with three turns as an example in Fig. 17, the voltage potentials at P_0, P_1, P_2, and P_3 are V_1, $(2V_1+V_2)/3$, $(V_1+2V_2)/3$, and V_2, respectively.

$$W_{\mathrm{E-field}} = \frac{1}{2}C_{\mathrm{eq\_turn-to-turn}}\left(V_2 - V_1\right)^2$$

$$\begin{aligned} W_{\mathrm{E-field}} = {} & \frac{C_{\mathrm{eq\_turn-to-turn\_dis}}}{6}\left(\left(\frac{2V_1+V_2}{3} - V_1\right)^2 \right. \\ & + \left(\frac{2V_1+V_2}{3} - V_1\right) \times \left(\frac{V_1+2V_2}{3} - \frac{2V_1+V_2}{3}\right) \\ & \left. + \left(\frac{V_1+2V_2}{3} - \frac{2V_1+V_2}{3}\right)^2\right) \\ & + \frac{C_{\mathrm{eq\_turn-to-turn\_dis}}}{6}\left(\left(\frac{V_1+2V_2}{3} - \frac{2V_1+V_2}{3}\right)^2 \right. \\ & + \left(\frac{V_1+2V_2}{3} - \frac{2V_1+V_2}{3}\right) \times \left(V_2 - \frac{V_1+2V_2}{3}\right) \\ & \left. + \left(V_2 - \frac{V_1+2V_2}{3}\right)^2\right) \\ = {} & \frac{C_{\mathrm{eq\_turn-to-turn\_dis}}(V_2 - V_1)^2}{9} \end{aligned} \tag{a1}$$

$$C_{\mathrm{eq\_turn-to-turn}} = \frac{2}{9}C_{\mathrm{eq\_turn-to-turn\_dis}}. \tag{a2}$$

For general cases considering the winding with $m \times n$ turns, the lumped capacitance contributed by turns is presented as

$$C_{\mathrm{eq\_turn-to-turn}} = \frac{nm-1}{(nm)^2}C_{\mathrm{eq\_turn-to-turn\_dis}}. \tag{a3}$$

B. Lumped Winding-to-Winding Capacitance

The lumped winding-to-winding capacitance is represented by the electrical field energy stored in between the two windings. Fig. 18 gives an example to illustrate it. It is found that the lumped capacitance is determined by the potential difference between the two windings in the efficient area.

However, the potential is fully determined by the winding layout. It is assumed that the potential difference between P_1 and P_2 is Δv_1, and the potential difference between P_3 and P_4 is Δv_2. n is the number of total turns. $(x_1 - x_2)$ is equal to $(y_1 - y_2)$ because the voltage potential is distributed evenly in the winding.

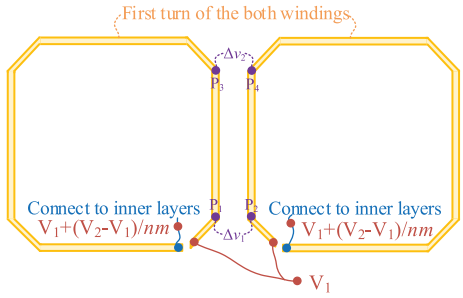


Fig. 18. Schematic for the equivalent lumped capacitance of dual windings with linear voltage potential distribution.

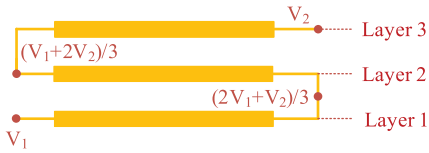


Fig. 19. Schematic for the lumped layer-to-layer capacitance of three conducted layers with linear voltage potage distribution.

The total electrical-field energy stored between the two windings is presented as (b1).

Therefore, the lumped winding-to-winding capacitance is obtained according to the following:

$$W_{\mathrm{E-field}} = \frac{1}{2}C_{\mathrm{eq\_winding\_to\_winding}}\left(V_2 - V_1\right)^2$$

$$\begin{aligned} W_{\mathrm{E-field}} = {} & \frac{C_{\mathrm{winding-to-winding}}}{6}\left(\left(\frac{\Delta v_1}{n}\right)^2 + \left(\frac{\Delta v_1}{n}\right) \right. \\ & \left. \times \left(\frac{\Delta v_2}{n}\right) + \left(\frac{\Delta v_2}{n}\right)^2\right) \times \frac{n}{m} \end{aligned} \tag{b1}$$

$$\begin{aligned} & C_{\mathrm{eq\_winding\_to\_winding}} \\ & = \frac{\left(\Delta v_1^2 + \Delta v_2^2 + \Delta v_1 \Delta v_2\right)}{3nm\left(\mathrm{V_2 - V_1}\right)^2}C_{\mathrm{eq\_winding-to-winding\_dis}}. \end{aligned} \tag{b2}$$

If both Δv_1 and Δv_2 are equal to zero, then $C_{\mathrm{eq\_winding\_to\_winding}}$ is zero.

C. Lumped Layer-to-Layer Capacitance

The variations of the core potential have impacts on the electrical-field energy stored between the two adjacent layers since the potential of the winding is assumed to be distributed evenly.

By using the same schematic shown in Fig. 19, as an example, the total electrical-field energy between the two adjacent layers is presented as

$$W_{\mathrm{E-field}} = \frac{1}{2}C_{\mathrm{eq\_layer-to-layer}}\left(V_2 - V_1\right)^2$$

$$W_{\mathrm{E-field}} = \frac{C_{\mathrm{eq\_layer-to-layer\_dis}}}{6}\left(\left(\frac{(V_1+2V_2)}{3} - V_1\right)^2\right.$$

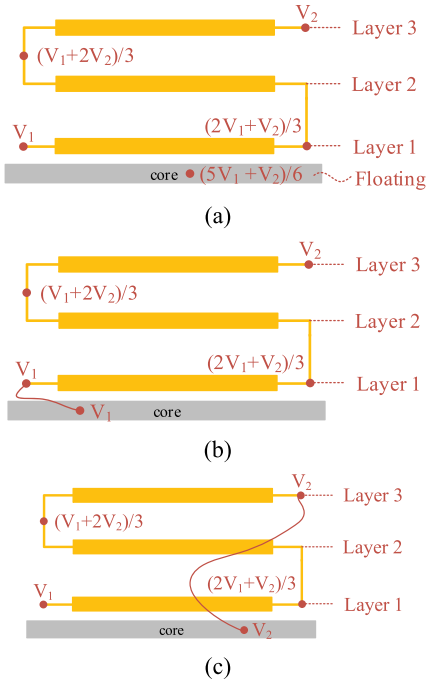


Fig. 20. Schematic for the lumped layer-to-core capacitance of three layers with linear voltage potential distribution on each layer and different voltage potential on the core. (a) Core is floating (core potential is $(5V_1+V_2)/6$). (b) Core is clamped to the hot terminal with V_1. (c) Core is clamped to the cold terminal with V_2.

$$+\left(\frac{\left(V_1+2V_2\right)}{3}-V_1\right)\times 0+0^2\Bigg)+\frac{C_{\text{eq\_layer-to-layer\_dis}}}{6}$$
$$\times\left(V_2-\frac{\left(2V_1+V_2\right)}{3}\ )^2+\left(V_2-\frac{\left(2V_1+V_2\right)}{3}\right)\times 0+0^2\right)$$
$$=\frac{4C_{\text{eq\_layer-to-layer\_dis}}V_1^2}{27}. \tag{c1}$$

The lumped layer-to-layer capacitance is derived according to the following:

$$C_{\text{eq\_layer-to-layer}}=\frac{8}{27}C_{\text{eq\_layer-to-layer\_dis}}. \tag{c2}$$

For general cases considering the winding with $m\times n$ turns, the lumped capacitance contributed by turns is presented as

$$C_{\text{eq\_layer-to-layer}}=\frac{4(m-1)}{3m^2}C_{\text{eq\_layer-to-layer\_dis}}. \tag{c3}$$

D. Lumped Layer-to-Core Capacitance

By using a winding with three layers as an example, the schematic of the winding is shown in Fig. 20. The potential at the hot terminal is assumed to be V_1, and the potential at the cold terminal is assumed to be V_2. Three different cases with a different voltage potential of the core are as follows:

Case 1: The core is floating. In this case, the core is closer to the inner winding; thus, the potential of the core is an approach to $(0+V_1/3)/2$.

Case 2: The core is connected to the start point. Therefore, the potential of the core is clamped to V_1.

Case 3: The core is connected to the endpoint. Therefore, the potential of the core is clamped to V_2.

The lumped layer-to-core capacitance of the three cases is different because of the potential difference between the inner layer and core.

Case 1:

The electrical-field energy stored between the inner layer and core for Case 1, shown in Fig. 20(a), is presented as follows:

$$W_{\text{E-field}}=\frac{1}{2}C_{\text{eq\_layer\_to\_core1}}\left(V_2-V_1\right)^2$$
$$W_{\text{E-field}}=\frac{C_{\text{layer-to-core}}}{6}\left(\left(V_1-\frac{(5V_1+V_2)}{6}\right)^2\right.$$
$$+\left(V_1-\frac{\left(5V_1+V_2\right)}{6}\right)$$
$$\left.\times\left(\frac{2V_1+V_2}{3}-\frac{\left(5V_1+V_2\right)}{6}\right)+\left(\frac{2V_1+V_2}{3}-\frac{(5V_1+V_2)}{6}\right)^2\right)$$
$$=\frac{C_{\text{layer-to-core}}(V_2-V_1)^2}{216}. \tag{d1}$$

By solving (d1), the lumped layer-to-core capacitance is presented as

$$C_{\text{eq\_layer\_to\_core1}}=\frac{1}{108}C_{\text{layer-to-core}}. \tag{d2}$$

For general cases of a winding with m layers, the lumped layer-to-core capacitance in Case 1 is presented as

$$C_{\text{eq\_layer\_to\_core1}}=\frac{1}{12m^2}C_{\text{layer-to-core}}. \tag{d3}$$

Case 2:

The total electrical-field energy stored between the inner layer and core for Case 2, shown in Fig. 20(b), is presented as (d4).

By solving the (d4), the lumped layer-to-core capacitance is presented as (d5).

For general cases of a winding with m layers, the lumped layer-to-core capacitance in Case 2 is presented as (d6)

$$W_{\text{E-field}}=\frac{1}{2}C_{\text{eq\_layer\_to\_core2}}\left(V_2-V_1\right)^2$$
$$W_{\text{E-field}}=\frac{C_{\text{layer-to-core}}}{6}\left(\left(\mathrm{V}_1-\mathrm{V}_1\right)^2+\left(V_1-V_1\right)\right.$$
$$\left.\times\left(\frac{\left(2V_1+V_2\right)}{3}-V_1\right)+\left(\frac{(2\mathrm{V}_1+\mathrm{V}_2)}{3}-V_1\right)^2\right)$$
$$=\frac{C_{\text{layer-to-core}}(V_2-V_1)^2}{54} \tag{d4}$$

$$C_{\text{eq\_layer\_to\_core2}} = \frac{1}{27} C_{\text{layer-to-core}} \tag{d5}$$

$$C_{\text{eq\_layer\_to\_core2}} = \frac{1}{3m^2} C_{\text{layer-to-core}}. \tag{d6}$$

Case 3:

The electrical-field energy stored between the inner layer and core for Case 3, shown in Fig. 20(c), is presented as

$$W_{\text{E-field}} = \frac{1}{2} C_{\text{eq\_layer\_to\_core3}} (V_2 - V_1)^2$$

$$W_{\text{E-field}} = \frac{C_{\text{layer-to-core}}}{6} \left(\left(V_1 V_2 \right)^2 + \left(V_1 - V_2 \right) \times \left(\frac{\left(2V_1 + V_2 \right)}{3} - V_2 \right) + \left(\frac{\left(2V_1 + V_2 \right)}{3} - V_2 \right)^2 \right)$$

$$= \frac{19 C_{\text{layer-to-core}} \left(V_2 - V_1 \right)^2}{54}. \tag{d7}$$

By solving the (d7), the lumped layer-to-core capacitance is presented as

$$C_{\text{eq\_layer\_to\_core3}} = \frac{19}{27} C_{\text{layer-to-core}}. \tag{d8}$$

For general cases of a winding with *m* layers, the lumped layer-to-core capacitance in Case 3 is presented a

$$C_{\text{eq\_layer\_to\_core3}} = \frac{3m^2 - 3m + 1}{3m^2} C_{\text{layer-to-core}}. \tag{d9}$$

REFERENCES

[1] J. B. Casady *et al.*, "New generation 10 kV SiC power MOSFET and diodes for industrial applications," in *Proc. PCIM Europe; Int. Exhib. Conf. Power, Intell. Motion, Renewable Energy Energy Manage.*, May 2015, pp. 96–103.

[2] D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, "99% efficient 10 kV SiC-Based 7 kV/400 V DC transformer for future data centers," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 753–767, Jun. 2019.

[3] J. Wang, R. Burgos, D. Boroyevich, and Z. Liu, "Design and testing of 1 kV H-bridge power electronics building block based on 1.7 kV SiC MOSFET module," in *Proc. Int. Power Electron. Conf.*, May 2018, pp. 3749–3756.

[4] J. Casarin, P. Ladoux, and P. Lasserre, "10 kV SiC MOSFETs versus 6.5 kV Si-IGBTs for medium frequency transformer application in railway traction," in *Proc. Int. Conf. Elect. Syst. Aircraft, Railway, Ship Propul. Road Veh.*, Aachen, Germany, 2015, pp. 1–6.

[5] B. Hu *et al.*, "A survey on recent advances of medium voltage silicon carbide power devices," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2018, pp. 2420–2427.

[6] N. Christensen *et al.*, "Common-mode current mitigation for medium voltage half-bridge SiC modules," in *Proc. 19th Eur. Conf. Power Electron. Appl.*, Sep. 2017, pp. 1–8.

[7] T. Huber, A. Kleimajer, and R. Kennel, "Ultra-low inductive power module design with integrated common-mode noise shielding," in *Proc. 19th Eur. Conf. Power Electron. Appl.,* Sep. 2017, pp. 1–9.

[8] D. N. Dalal *et al.*, "Impact of power module parasitic capacitances on medium voltage SiC MOSFETs switching transients," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 298–310, Mar. 2020.

[9] C. DiMarino *et al.*, "Design and experimental validation of a wire-bondless 10 kV SiC MOSFET power module," *IEEE J. Emer. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 381–394, Mar. 2020.

[10] A. Anurag, S. Acharya, and S. Bhattacharya, "Gate drivers for high-frequency application of silicon-carbide MOSFETs: design considerations for faster growth of LV and MV applications," *IEEE Power Electron. Mag.*, vol. 6, no. 3, pp. 18–31, Sep. 2019.

[11] X. Zhang *et al.*, "A gate drive with power over fiber-based isolated power supply and comprehensive protection functions for 15-kV SiC MOSFET," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 946–955, Sep. 2016.

[12] H. Zhao *et al.*, "Behavioral modeling of ground current in filter inductors of medium-voltage SiC-MOSFET-based converters," in *Proc. IEEE Appl. Power Electron. Conf.*, Mar. 2020, pp. 1972–1978.

[13] S. Acharya, A. Anurag, Y. Prabowo, and S. Bhattacharya, "Practical design considerations for MV LCL filter under high d*v*/d*t* conditions considering the effects of parasitic elements," in *Proc. 9th IEEE Int. Symp. Power Electron. Distrib. Gener. Syst.*, Jun. 2018, pp. 1–7.

[14] Z. Ouyang and M. A. E. Andersen, "Overview of planar magnetic technology-fundamental properties," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4888–4900, Sep. 2014.

[15] A. Anurag, S. Acharya, S. Bhattacharya, and T. R. Weatherford, "Thermal performance and reliability analysis of a medium voltage three-phase inverter considering the influence of high dv/dt on parasitic filter elements," *IEEE J. Emerg. Sel. Topics Power Electron*, vol. 8, no. 1, pp. 486–494, Mar. 2020.

[16] ANSYS, Inc., "ANSYS Q3D Extractor." [Online]. Available: http://www.ansys.com/products/electronics/ansys-q3d-extractor. Accessed on: Apr. 19, 2018.

[17] A. B. Jørgensen, S. Bęczkowski, C. Uhrenfeldt, N. H. Petersen, S. Jørgensen, and S. Munk-Nielsen, "A fast-switching integrated full-bridge power module based on GaN eHEMT devices," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2494–2504, Mar. 2019.

[18] Z. Shen, H. Wang, Y. Shen, Z. Qin, and F. Blaabjerg, "An improved stray capacitance model for inductors," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 11153–11170, Nov. 2019.

[19] E. C. Snelling, *SoftFerrites: Properties and Applications*, London, U.K.: Butterworth, 1988.

[20] P. Thummala, H. Schneider, Z. Zhang, and M. A. E. Andersen, "Investigation of transformer winding architectures for high voltage (2.5 kV) capacitor charging and discharging applications," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5786–5796, Aug. 2016.

[21] M. Zdanowski, K. Kostov, J. Rabkowski, R. Barlik, and H.-P. Nee, "Design and Evaluation of Reduced Self-Capacitance Inductor in DC/DC Converters with Fast-Switching SiC Transistors," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2492–2499, May 2014.

[22] J. Biela and J. W. Kolar, "Using transformer parasitics for resonant converters—A review of the calculation of the stray capacitance of transformers," *IEEE Trans. Ind. Appl.*, vol. 44, no. 1, pp. 223–233, Jan./Feb. 2008.

[23] A. Massarini and M. K. Kazimierczuk, "Self-capacitance of inductors," *IEEE Trans. Power Electron.*, vol. 12, no. 4, pp. 671–676, Jul. 1997.

[24] A. Ayachit and M. K. Kazimierczuk, "Self-capacitance of single-layer inductors with separation between conductor turns," *IEEE Trans. Electromagn. Compat.*, vol. 59, no. 5, pp. 1642–1645, Oct. 2017.

[25] G. Grandi, M. K. Kazimierczuk, A. Massarini, and U. Reggiani, "Stray capacitances of single-layer solenoid air-core inductors," *IEEE Trans. Ind. Appl.*, vol. 35, no. 5, pp. 1162–1168, Sep./Oct. 1999.

[26] S. Zhu, X. Yuan, and P. Mellor, "Modelling of high-frequency effects of laminated iron-core power inductors and reduction of parasitic capacitance,"In *Proc. 43rd Annu. Conf. IEEE Ind. Electron. Soc.*, Beijing, China, 2017, pp. 1299–1306.

[27] L. F. de Freitas Gutierres and G. Cardoso, "Analytical technique for evaluating stray capacitances in multiconductor systems: single-layer air-core inductors," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 6147–6158, Jul. 2018.

[28] N. B. Chagas and T. B. Marchesan, "Analytical Calculation of Static Capacitance for High-Frequency Inductors and Transformers," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1672–1682, Feb. 2019.

[29] *IEEE Standard for General Requirements for Dry-Type Distribution and Power Transformers*, IEEE Standard C57.12.01-2015, 2015.

[30] T. Guillod, F. Krismer, and J. W. Kolar, "Electrical shielding of MV/MF transformers subjected to high d*v*/d*t* PWM voltages," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 2502–2510.

[31] LWW Group, "Techincal data for winding wire," Jul. 2016. [Online]. Available: http://www.lww.se/wp-content/uploads/2017/06/LWW-brochure-2016.pdf

[32] Michael-Kunststofftechnik, "Bobbins for cores: Type for c-core," Nov. 2019. [Online]. Available: https://www.michael-kunststofftechnik.com/spulenkoerper-fuer-kerne-produkte.php?fthid=198

[33] LANXESS, "DURETHAN BKV 30 H-polyamide 6," May 2005. [Online]. Available: https://techcenter.lanxess.com/scp/americas/en/docguard/PIB_Durethan_BKV30H.pdf?docId=76997
[34] The engineering toolbox, "Relative permittivity—The dielectric constant," Nov. 2019. [Online]. Available: https://www.engineeringtoolbox.com/relative-permittivity-d_1660.html
[35] Wikipedia, "Vacuum permittivity," Sep. 2019. [Online]. Available: https://en.wikipedia.org/wiki/Vacuum_permittivity
[36] Keysight Technologies, *Impedance Measurement Handbook*. [Online]. Available: https://literature.cdn.keysight.com/litweb/pdf/5950-3000.pdf

Hongbo Zhao (Student Member, IEEE) received the B.S. degree in electrical engineering and its automation from Southwest Jiaotong University, Chengdu, China, in 2015. He is currently working toward the Ph.D. degree with Aalborg University, Aalborg, Denmark.

His research interests include medium-voltage converters and their filters utilized by wide-bandgap power devices.

Dipen Narendra Dalal (Student Member, IEEE) received the M.Sc. degree in energy engineering with a specialization in power electronics and drivers in 2016 from Aalborg University, Aalborg, Denmark, where he is currently working toward the Ph.D. degree with the Department of Energy Technology.

His current research interests include wide-bandgap power semiconductor devices and medium-voltage high-power converters.

Asger Bjørn Jørgensen received the M.Sc. and Ph.D. degrees in energy engineering from Aalborg University, Aalborg, Denmark, in 2016 and 2019, respectively.

He is currently working as a Postdoctoral Researcher with the Department of Energy Technology, Aalborg University. His research interests include power module packaging, wide-bandgap power semiconductors, and multiphysics finite element analysis within power electronic applications.

Jannick Kjær Jørgensen received the M.Sc. degree in nanotechnology with a specialization in nanomaterials and nanophysics from Aalborg University, Aalborg, Denmark, in 2018.

He is currently working as a Research Assistant with the Department of Energy Technology, Aalborg University. His research interests include packaging and modeling of wide-bandgap power semiconductor devices and medium-voltage power modules.

Xiongfei Wang (Senior Member, IEEE) received the B.S. degree from Yanshan University, Qinhuangdao, China, in 2006, and the M.S. degree from the Harbin Institute of Technology, Harbin, China, in 2008, both in electrical engineering, and the Ph.D. degree in energy technology from Aalborg University, Aalborg, Denmark, in 2013.

Since 2009, he has been with the Department of Energy Technology, Aalborg University, where he became an Assistant Professor in 2014, an Associate Professor in 2016, a Professor and Research Program Leader for electronic power grid (eGrid) in 2018, and the Director of Aalborg University-Huawei Energy Innovation Center in 2020. His current research interests include modeling and control of grid-interactive power converters, stability and power quality of converter-based power systems, and active and passive filters.

Dr. Wang was selected into Aalborg University Strategic Talent Management Program in 2016. He is a recipient of six IEEE Prize Paper Awards, the 2016 Outstanding Reviewer Award of the IEEE TRANSACTIONS ON POWER ELECTRONICS, the 2018 IEEE PELS Richard M. Bass Outstanding Young Power Electronics Engineer Award, the 2019 IEEE PELS Sustainable Energy Systems Technical Achievement Award, and the 2019 Highly Cited Researcher by Clarivate Analytics (former Thomson Reuters). He serves as a Member-at-Large for Administrative Committee of IEEE Power Electronics Society in 2020–2022, and as an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS, the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, and the *IEEE Journal of Emerging and Selected Topics in Power Electronics*.

Szymon Bęczkowski received the M.Sc. degree in electrical engineering from the Warsaw University of Technology, Warsaw, Poland, in 2007, and the Ph.D. degree from Aalborg University, Aalborg, Denmark, in 2012.

He is currently working as an Associate Professor with the Department of Energy Technology, Aalborg University. His research interests include optimization of power electronic converters, power module packaging, and SiC technology.

Stig Munk-Nielsen (Member, IEEE) received the M.Sc. and Ph.D. degrees from Aalborg University, Aalborg, Denmark, in 1991 and 1997, respectively.

He is currently a Professor with the Department of Energy Technology, Aalborg University. His research interests include LV and MV Si, SiC, and GaN converters, packaging of power electronic devices, electrical monitoring apparatus for IGBTs, failure modes, and device test systems. In the last ten years, he has been involved or has managed ten research projects. He has authored or coauthored 221 international power electronic papers.

Christian Uhrenfeldt (Member, IEEE) received the M.Sc. degree in physics from Aalborg University, Aalborg, Denmark, in 2004, and the Ph.D. degree in the field of semiconductor material science from Aarhus University, Aarhus, Denmark, in 2008.

He is currently working as an Associate Professor on power electronics packaging and materials with the Department of Energy Technology, Aalborg University. His research interests include packaging of power modules, physics-based modeling of power electronic components, and semiconductor diagnostics in power electronics.