Phase-Shift Modulated Interleaved *LLC* Converter With Ultrawide Output Voltage Range

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***Abstract*—Conventional frequency modulated *LLC* topology is unsuitable for ultrawide voltage range applications and suffers from poor voltage regulation performance at light load conditions. To cope with those issues, this article proposes a novel two-phase dual *LLC* resonant converter. The primary side of the proposed converter is two paralleled half-bridges *LLC*, and the transformers' secondary sides are in reverse series with shared full bridge rectifier. Both resonant tanks are driven by two fixed-frequency square waves, whose frequencies are always tuned at the optimal resonant frequency. A phase shift is introduced between those two square waves to regulate the output voltage. The proposed topology demonstrates good voltage regulation performance, which is weakly dependent on the load condition. Zero-voltage switching and zero-current switching are well realized on the power MOSFETs and diodes in a wide range. A 1-kW rated laboratory prototype is designed to convert 390 V input to 10–420 V output. The prototype demonstrates a 98.1% peak efficiency and good voltage regulation capability. The experimental results agree well with the theoretical analysis.**

***Index Terms*—*LLC*, phase-shift modulation, resonant converter, ultrawide output range.**

I. Introduction

In SOME specific applications such as deeply depleted electric vehicle battery charging and programmable power supplies, an ultrawide output voltage range with galvanic isolation is required [1]–[3]. Thus, the design of the isolated dc/dc converter needs to be adapted to and optimized for an ultrawide output voltage range.

As a prevalent isolated dc/dc converter, the *LLC* resonant converters are widely employed due to the advantages of simple structure, zero-voltage switching (ZVS) for MOSFETs and zero-current switching (ZCS) for diodes in a wide load range, high efficiency, and high power density [4]–[7]. The typical voltage gain characteristics of conventional *LLC* converter with frequency modulation is shown in Fig. 1. However, as shown, the switching frequency (f_s) must swing in a wide range to fit this wide voltage gain range. When f_s is too low, the ZVS feature may get lost. When f_s is beyond the resonant frequency (f_r), it suffers from poor voltage regulation due to the impact of junction capacitance (C_j) of secondary-side rectifying diodes. Moreover, the magnetic component size is constrained by the lower bound f_s. Consequently, this brings significant challenges to optimally design *LLC* converter with wide output voltage range and the efficiency degrades fast when f_s deviates away from f_r.

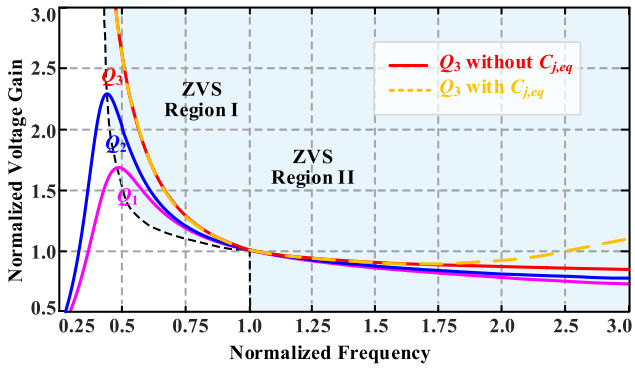

Fig. 1. DC gain curves of the conventional frequency modulated *LLC* converter.

Many techniques have been proposed to overcome the issues of traditional frequency modulated *LLC* converter in wide output range applications. Those methods can be mainly divided into four categories:

1) changing the resonant parameters;
2) modifying the structure of secondary-side rectifier;
3) adopting reconfigurable primary-side structure;
4) modifying the control and modulation strategies.

The first category is based on changing the resonant parameters. The voltage gain curve of *LLC* converter is highly related to the resonant parameters including L_r, C_r, and L_m. Thus, an extended voltage regulation range can be obtained by changing the resonant parameters. In [8]–[11], the resonant parameters are changed to improve the system performance in different load conditions. In [8] and [9], a switch-controlled capacitor based *LLC* topology is proposed. However, the introduction of extra passive components leads to additional power loss and degraded power density. Moreover, the transient issues during process of adding/removing the passive components are difficult

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to tackle. In [10] and [11], an auxiliary *LC* resonant circuit is introduced to increase the voltage gain of conventional *LLC* converter. However, it increases the core loss and resonant tank input current. This incurs high conduction and switching loss and high current stresses on the primary-side switches.

The secondary category is based on modifying the secondary-side structure. In [12] and [13], the rectifier structures reconfigure among full bridge (FB) rectifier, voltage doubler, and voltage-quadrupler rectifier. Hence, the output voltage range is extended. However, extra switches and conduction loss are introduced. Moreover, during the mode switching, the output voltage changes abruptly. This causes severe current spikes and might incur device failure. In [14] and [15], a secondary-side modulated *LLC* converter is proposed. The output voltage is regulated by the duty cycle of secondary-side MOSFETs. It does not have mode switching and the output voltage range can be continuously regulated. However, the normalized voltage gain range is limited. Besides, it has high turn-OFF current and asymmetric inductor current.

The third category is based on adopting reconfigurable primary-side structures. In [16]–[18], a FB and half bridge (HB) hybrid structure is proposed. In [16], the primary current can be reduced by changing the equivalent turn-ratio and magnetizing inductance. However, only one transformer is enabled when the input voltage is less than the threshold V_{th}. The transformers are flawed with low utilization. Moreover, it need two secondary rectifiers and the state of bidirectional switch cannot be gradually changed in one mode. In [17], the output voltage is regulated by the controlling the percentage of operating time of the FB and HB during a switching circle. Those kinds of converters require two additional active switches, which operate with hard switching and suffer from high turn-OFF currents. In [18], the *LLC* resonant tank has been split into two branches. By changing the modulation strategies, the converter has low gain mode and medium gain mode, which is helpful for wide voltage gain range. However, the hybrid structure of FB and HB on the primary-side [16]–[18] is suitable for wide input voltage range applications only.

The last category is based on modifying the control and modulation strategies. In [19] and [20], two-stage *LLC* structure is proposed with front-stage ac/dc converter with power factor correction (PFC). The wide output voltage range is realized by controlling dc-link voltage and the f_s variation of *LLC* converter is remarkably narrowed down. However, the traditional boost PFC converter is no longer suitable here. Changing the PFC topology increases the complexity of circuit and control. In [21] and [22], burst mode control strategies are proposed to improve the light load regulation capacity and efficiency of the *LLC* converter. However, controller design is very complicate and a high-frequency oscillation exists during the OFF state and EMI issues are introduced. In [23] and [24], interleaved *LLC* structure are proposed to reduce the current stress and extend the output range. In [24], an interleaved *LLC* resonant converter with hybrid rectifier structure is proposed. However, it significantly increase the components count, which increase the cost of system volume. Moreover, due to the addition of two didoes, the voltage gain is 0.5 instead of 0 when the phase shift φ is 0. Therefore, the output voltage range is limited and cannot reach 0.

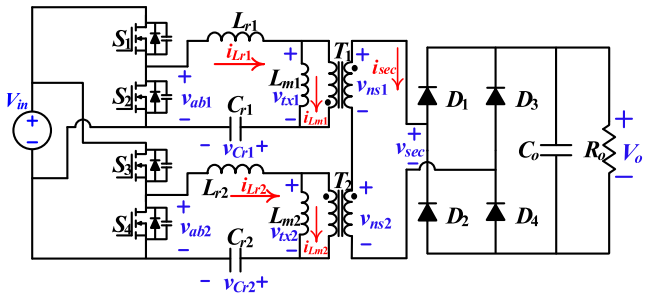

Fig. 2. Schematic of the proposed phase-shift modulated interleaved *LLC* converter.

In this article, an interleaved *LLC* resonant converter with phase-shift modulation is proposed. The concept was partially presented in [25]. This article is an extension of the conference paper. The primary-side of proposed topology consists of two parallel connected HBs-*LLC* resonant tanks. Two transformers have their secondary-side terminals reverse-seriesly connected. An FB diode rectifier is shared by two resonant units. Compared with the conventional *LLC* topology, the proposed topology does not increase the count of switches. It always operate at the resonant frequency, which bring convenience to the optimal design of magnetic components. The output voltage is regulated by the phase-shift between two HBs. The benefits of the proposed converter include: ultrawide output voltage range; fixed frequency control to simplify magnetic component design; low-switch devices count; wide ZVS range of all MOSFETs; high power supply utilization; low turn-OFF current.

This article is organized as follows: Section II introduced the operation principles. The detailed circuit modeling and theoretical analysis are presented in Section III. Section IV demonstrates the experimental results. Finally, the article concludes in Section V.

II. Operation Principles

The schematic of the proposed converter is illustrated in Fig. 2. Two interleaved HBs are featured with identical resonant tanks ($L_{r1} = L_{r2} = L_r, C_{r1} = C_{r2} = C_r, L_{m1} = L_{m2} = L_m, n_1 = n_2 = n$). The two HB-*LLC* resonant tanks are parallel in-series out and the secondary-side is a traditional FB rectifier, which is shared by two reverse-seriesly connected secondary sides of transformer T_1 and T_2.

In the proposed converter, each HB functions as a square wave generator with fixed f_r. Each pair of power MOSFETs (S_1 and S_2, S_3 and S_4) are complementarily turned ON and OFF with a deadband t_d. The range of phase shift between two HB-*LLC* structures is constrained to [0,π]. When $\varphi = \pi$, it means the phase shift between two HB-*LLC* primary-side square-waves is π. Meanwhile, the secondary sides are clamped to $\pm 1/2nV_o$. Hence, it is similar to an FB *LLC* converter that operates at resonant frequency, the normalized voltage gain G is 1. When $\varphi < \pi$, the phase shift between two resonant tank leads to discontinuous conduction mode of secondary side rectifier. Thus, the power delivered to the load decreases and the normalized voltage gain also drops. At the extreme case with $\varphi = 0$, the current of secondary side rectifier is zero and the output voltage is

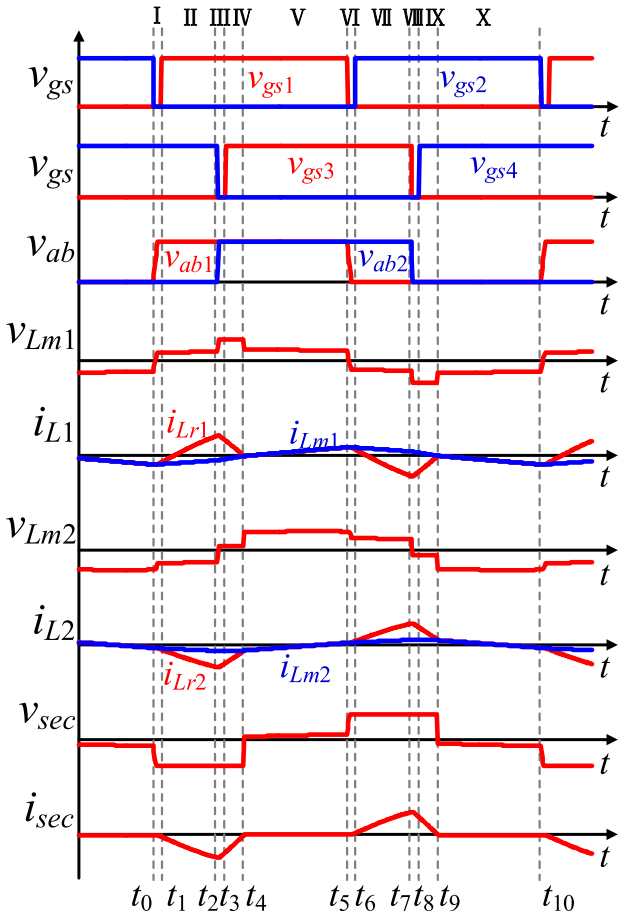

Fig. 3. Critical steady-state waveforms.

zero. The critical steady state waveforms with $\varphi < \pi$ is shown in Fig. 3. As shown in Fig. 3, the steady-state circuit operation can be divided into ten operation modes. Fig. 4 shows the equivalent circuits of the first five modes over a half switching cycle and the next five modes are symmetrical.

Mode I : $[t_0, t_1)$[see Fig. 4(a)], before t_0, $S_{2,4}$ are ON, $S_{1,3}$ are OFF and the secondary side is open circuit. L_{m1} resonants with L_{r1} and C_{r1}, L_{m2} resonants with L_{r2} and C_{r2}. At t_0, S_2 is turned OFF and other switches state are unchanged. At this moment, the inductor current $i_{L_{r1}}$ is negative, which charges the C_{oss} of S_2 and discharges C_{oss} of S_1. This negative current can create the ZVS conditions for S_1 turn ON.

Mode II : $[t_1, t_2)$[see Fig. 4(b)], the C_{oss} of S_1 is discharged to zero because of the negative current of $i_{L_{r1}}$ before t_1. At t_1, S_1 is turned ON with ZVS. In this mode, diode D_2 and D_3 starts to conduct and the secondary-side voltage v_{sec} is clamped at $-V_o$, and $i_{L_{r1}}$ increases while $i_{L_{r2}}$ decreases. The secondary-side current i_{sec} is decrease from zero to $i_{\text{sec}}(t_2)$. According to KVL and KCL, we can get the following:

$$V_{\text{in}} = L_m \frac{di_{L_{m1}}(t)}{dt} + v_{C_{r1}}(t) + L_r \frac{di_{L_{r1}}(t)}{dt} \tag{1}$$

$$0 = L_m \frac{di_{L_{m2}}(t)}{dt} + v_{C_{r2}}(t) + L_r \frac{di_{L_{r2}}(t)}{dt} \tag{2}$$

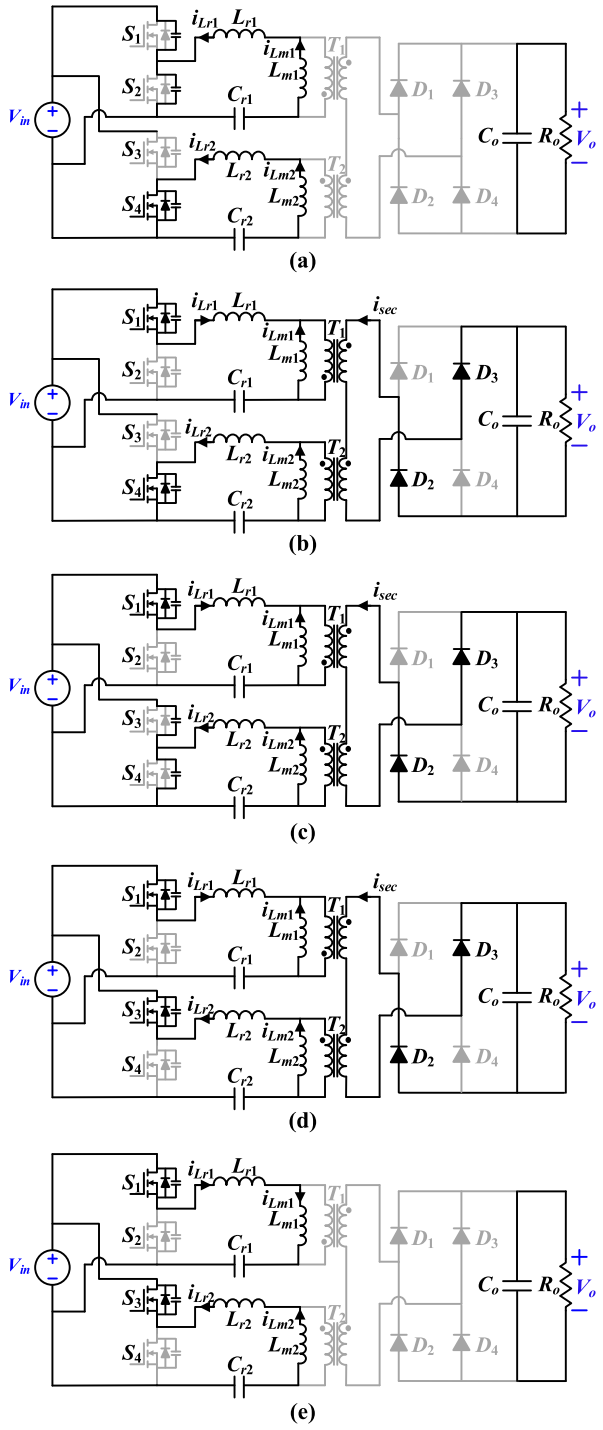

Fig. 4. Equivalent circuits over half switching period: (a) Mode I, $t_0 \le t < t_1$; (b) Mode II, $t_1 \le t < t_2$; (c) Mode III, $t_2 \le t < t_3$; (d) Mode IV, $t_3 \le t < t_4$; (e) Mode V, $t_4 \le t < t_5$.

$$- L_m \frac{di_{L_{m1}}(t)}{dt} + L_m \frac{di_{L_{m2}}(t)}{dt} = -nV_o. \tag{3}$$

Mode III : $[t_2, t_3)$[see Fig. 4(c)] This mode is the deadband time of $S_{3,4}$, at t_2, S_4 turned OFF and the inductor current $i_{L_{r2}}$ is negative, which provides the negative current to charges the C_{oss} of S_4 and discharges C_{oss} of S_3. Thus, S_3 is turned ON with ZVS.

Mode IV : $[t_3, t_4)$[see Fig. 4(d)], At t_3, S_3 is turned ON with ZVS. In this mode, the input voltages of both resonant tanks are $V_{\rm in}$ while the transformer is reverse-seriesly connected. Thus, $i_{L_{r1}}$ decreases and $i_{L_{r2}}$ increases. Meanwhile, D_2 and D_3 are still ON and the secondary-side voltage $v_{\rm sec}$ is clamped at $-V_o$. $i_{\rm sec}$ increases from $i_{\rm sec}(t_3)$ to zero

$$V_{\rm in} = L_m \frac{di_{L_{m1}}(t)}{dt} + v_{C_{r1}}(t) + L_r \frac{di_{L_{r1}}(t)}{dt} \tag{4}$$

$$V_{\rm in} = L_m \frac{di_{L_{m2}}(t)}{dt} + v_{C_{r2}}(t) + L_r \frac{di_{L_{r2}}(t)}{dt} \tag{5}$$

$$-L_m \frac{di_{L_{m1}}(t)}{dt} + L_m \frac{di_{L_{m2}}(t)}{dt} = -nV_o. \tag{6}$$

Mode V : $[t_4, t_5)$[see Fig. 4(e)], $i_{L_{r1}}$ is equal to $i_{L_{m1}}$; $i_{L_{r2}}$ is equal to $i_{L_{m2}}$. Thus, $i_{\rm sec}$ reaches zero at t_4 and $D_{2,3}$ are turned OFF with zero current. In this mode, all diodes are OFF and the secondary side is open circuited. L_{m1} participates into the resonance with L_{r1} and C_{r1}; L_{m2} participates into the resonance with L_{r2} and C_{r2}. Mode V ends when S_1 is turned OFF

$$V_{\rm in} = L_m \frac{di_{L_{m1}}(t)}{dt} + v_{C_{r1}}(t) + L_r \frac{di_{L_{r1}}(t)}{dt} \tag{7}$$

$$V_{\rm in} = L_m \frac{di_{L_{m2}}(t)}{dt} + v_{C_{r2}}(t) + L_r \frac{di_{L_{r2}}(t)}{dt} \tag{8}$$

$$i_{L_{r1}}(t) = i_{L_{m1}}(t) \qquad i_{L_{r2}}(t) = i_{L_{m2}}(t). \tag{9}$$

III. Circuit Analysis

A. Voltage Gain

Usually, the first harmonic approximation (FHA) method is used to analyze the *LLC* resonant converter with frequency modulation. Nevertheless, the proposed converter always operates at f_r and the output voltage is regulated by φ. v_{L_m} of each resonant tank are not clamped at $\pm 1/2nV_o$ and the inductor current is not a sine wave. Thus, the FHA is not suitable here. In order to simplify the analysis, we ignore the impact of t_d on voltage gain G. The normalized voltage gain is defined as

$$G = \frac{nV_o}{V_{\rm in}}. \tag{10}$$

The inductor ratio L_n is defined as

$$L_n = \frac{L_m}{L_r}. \tag{11}$$

The normalized time variable θ is defined as

$$\theta = \omega_0 t \tag{12}$$

where ω_0 is the angular resonant frequency

$$\omega_0 = \frac{1}{\sqrt{L_r C_r}}. \tag{13}$$

A second angular resonant frequency appears when the secondary-side rectifiers are OFF. It is denoted as ω_1

$$\omega_1 = \frac{1}{\sqrt{(L_r + L_m) C_r}} \tag{14}$$

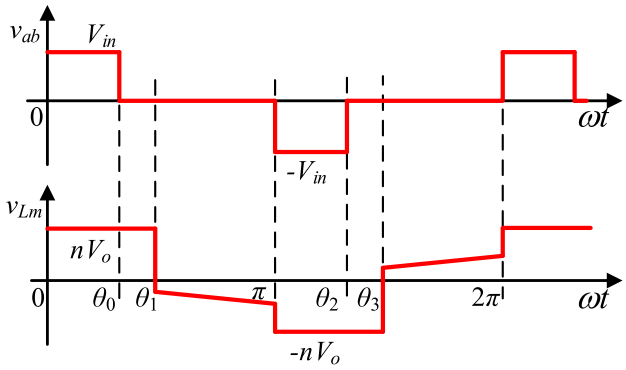

Fig. 5. Critical waveforms of $v_{ab}(t)$ and $v_{L_m}(t)$.

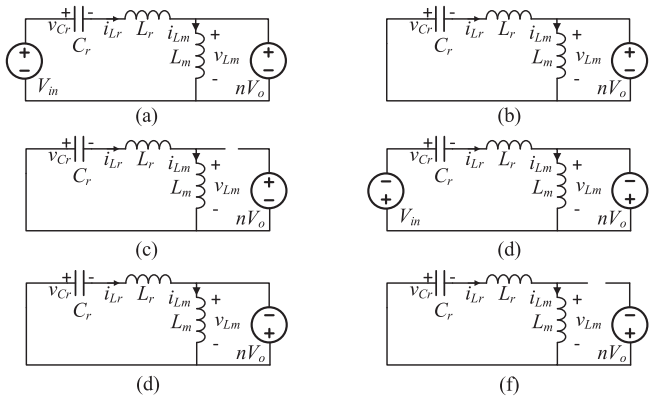

Fig. 6. Simplified equivalent circuits of equivalent resonant tank. (a) Mode II($0 \le \omega_0 t < \theta_0$). (b) Mode IV($\theta_0 \le \omega_0 t < \theta_1$). (c) Mode V($\theta_1 \le \omega_0 t < \pi$). (d) Mode VII ($\pi \le \omega_0 t < \theta_2$). (e) Mode IX ($\theta_2 \le \omega_0 t < \theta_3$). (f) Mode X ($\theta_3 \le \omega_0 t < 2\pi$).

$v_{ab}(t)$, $i_{L_m}(t)$, $i_{L_r}(t)$, and $v_{C_r}(t)$ are defined as

$$v_{ab}(t) = v_{ab1}(t) - v_{ab2}(t) \tag{15}$$

$$i_{L_m}(t) = i_{L_{m1}}(t) - i_{L_{m2}}(t) \tag{16}$$

$$i_{L_r}(t) = i_{L_{r1}}(t) - i_{L_{r2}}(t) \tag{17}$$

$$v_{C_r}(t) = v_{C_{r1}}(t) - v_{C_{r2}}(t). \tag{18}$$

Combing (1–9), we can get the following equation in each Mode:

$$v_{ab}(t) = L_m \frac{di_{L_m}(t)}{dt} + v_{C_r}(t) + L_r \frac{di_{L_r}(t)}{dt}. \tag{19}$$

In Mode II, $S_{1,4}$ are ON and $S_{2,3}$ are OFF and $D_{2,3}$ are conduct, $v_{ab}(t)$ is $V_{\rm in}$ and $v_{L_m}(t)$ is nV_o. In Modes IV and V, S_1 and S_3 are ON. Hence, $V_{\rm in}$ is zero. However, in Mode V, the secondary-side current is zero. This means $v_{L_m}(t)$ is no longer clamped at nV_o and L_m participates into the resonance. φ equals θ_0 in Fig. 5.

As shown in Fig. 5, in a full switching cycle, there are six operation modes. The corresponding equivalent circuits are plotted in Fig. 6. Indeed, we can treat the two interleaved phase shift HBs *LLC* as one phase shift FB *LLC* for analysis. Only numerical solutions can be derived from the voltage and current relationships in the time domain [26].

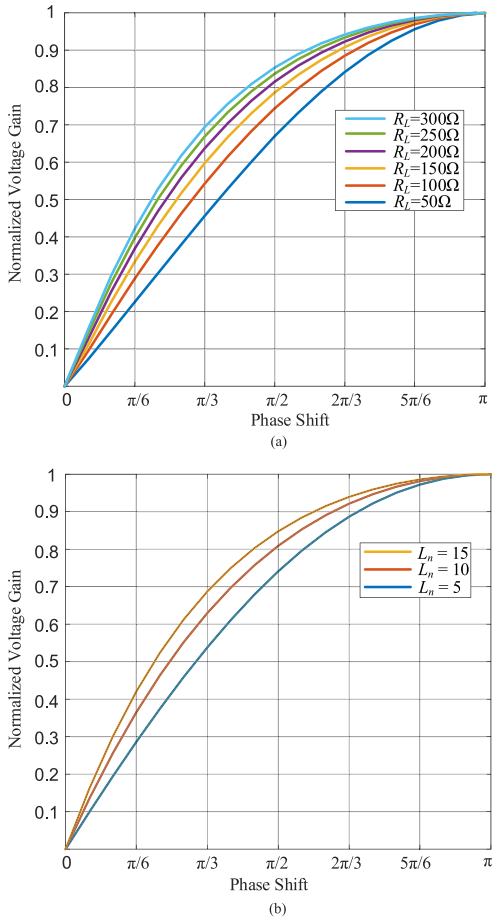

Fig. 7. Voltage gain curves versus φ with different: (a) R_L; (b) L_n.

Since Modes VI–X are symmetric to Modes I–V, we can get the following equations:

$$i_{L_r}(\pi) + I_{L_r0} = 0 \tag{20}$$

$$v_{C_r}(\pi) + V_{C_r0} = 0 \tag{21}$$

$$i_{L_r}(\theta_1) - i_{L_m}(\theta_1) = 0 \tag{22}$$

where I_{L_r0} and V_{C_r0} are the initial values of i_{L_r} and v_{C_r} at t_1, respectively.

During the first half period, power is delivered to the load only in Modes II and IV. According to the law of energy conservation, the output voltage should satisfy following:

$$\int_{t_1}^{t_4} (i_{L_r}(t) - i_{L_m}(t))\, dt = \frac{V_o}{n f_s R_L}. \tag{23}$$

Combing (20)–(23), the normalized voltage gain can be solved numerically by MATLAB for a given φ with R_L and L_n. The results are visualized in Fig. 7. As shown in Fig. 7, the normalized voltage gain varies from 0 to 1. When $\varphi = \pi$, the proposed converter is similar to a conventional phase-shift modulated *LLC* converter. Hence, the voltage gain G is 1. When $\varphi = 0$, the voltage on two secondary sides are always canceled. Therefore, zero power is delivered to the load and G is 0. Therefore, we can get the continuous output voltage gain in the range of [0,1] in all load conditions by changing φ.

Fig. 7(a) and (b) demonstrates the effect of R_L and L_n on G, respectively. In order to minimize the circulating current and conduction loss, L_m should be maximized, which indicates that L_n needs to be maximized. With the increase of R_L and L_n, the voltage gain G increases with the same φ and it is very sensitive to φ in the case of small φ. In order to achieve a wider output voltage within a certain phase shift range, L_n should be constrained. Hence, we choose $L_n = 12$ in this article to achieve wide output range and low circulating current and conduction loss.

B. ZVS Performance

In the previous section, two resonant tanks are addressed in a coupled manner to solve the voltage gain function versus φ with different R_L and L_n. However, in the analysis of MOSFET ZVS, the current through that specific MOSFET should be considered separately. This means we should figure out the current for each resonant tank, separately.

The two resonant tanks need to be decoupled during the analysis. $v'_{ab}(t)$, $i'_{L_m}(t)$, $i'_{L_r}(t)$, and $v'_{C_r}(t)$ are defined as

$$v'_{ab}(t) = v_{ab1}(t) + v_{ab2}(t) \tag{24}$$

$$i'_{L_m}(t) = i_{L_{m1}}(t) + i_{L_{m2}}(t) \tag{25}$$

$$i'_{L_r}(t) = i_{L_{r1}}(t) + i_{L_{r2}}(t) \tag{26}$$

$$v'_{C_r}(t) = v_{C_{r1}}(t) + v_{C_{r2}}(t). \tag{27}$$

Combining (1-9), we can get the following equation in each mode:

$$\begin{aligned} v'_{ab}(t) &= L_m \frac{di'_{L_m}(t)}{dt} + v'_{C_r}(t) + L_r \frac{di'_{L_r}(t)}{dt} \\ &= v'_{C_r}(t) + (L_m + L_r)\frac{di'_{L_r}(t)}{dt} \end{aligned} \tag{28}$$

where $i'_{L_m}(t) = i'_{L_r}(t)$.

According to (28), we can find that L_m is always participates into resonance. Define $v'_{CN}(t)$ and $i'_{LN}(t)$ as following:

$$v'_{CN} = \frac{v'_{C_r}(t)}{V_{\text{in}}}, \qquad i'_{LN} = \frac{i'_{L_r}(t) Z_0}{V_{\text{in}}} \tag{29}$$

where $Z_0 = \sqrt{L_r/C_r}$.

Fig. 8 shows the waveform of $v'_{ab}(t)$. As shown, v'_{ab} is V_{in} during the interval of $0 \le \omega t < \theta_0$ and $\pi \le \omega t < \theta_0$. Hence, the trajectory in this stage is an ellipse centered at (1,0). v'_{ab} is $2V_{\text{in}}$ during the interval of $\theta_0 \le \omega t < \pi$. It means that the trajectory in this stage is an ellipse centered at (2,0). In the last stage, v'_{ab} is 0. This means that the center of ellipse is (0,0). Therefore, the trajectory of v'_{CN} and i'_{LN} is shown in Fig. 9.

In this article, L_n is design to be large, which means L_m is much larger than L_r, and the angular resonant frequency $\omega_1 \gg \omega_0$. Moreover, L_m resonants with L_r and C_r all the time. Hence, v'_{C_r} is approximately equal to V_{in}. We can approximately assume $v'_{CN} = 1$ to simplify the analysis without losing much accuracy. Thus, (28) can be approximated as

$$v'_{ab}(t) \approx V_{\text{in}} + \frac{L_m + L_r}{L_m} v'_{L_m}(t) \approx V_{\text{in}} + v'_{L_m}(t). \tag{30}$$

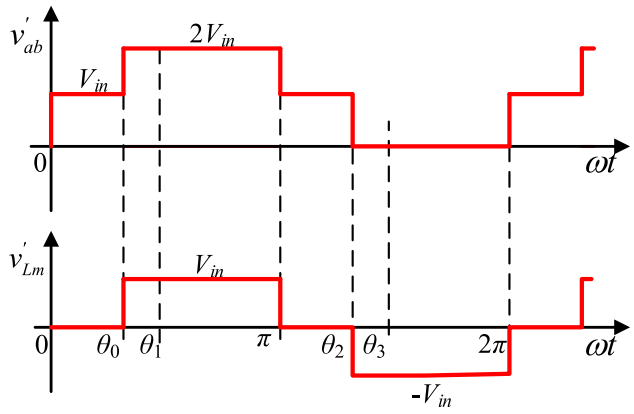

Fig. 8. Typical waveforms of $v'_{ab}(t)$ and $v'_{L_m}(t)$.

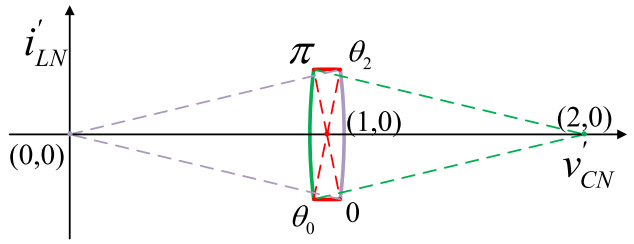

Fig. 9. Trajectory of v'_{CN} and i'_{LN}.

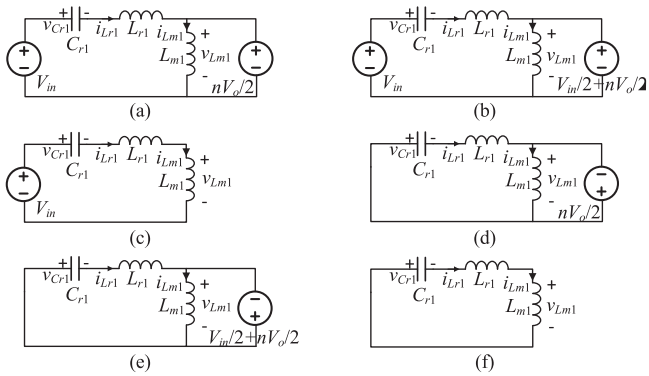

Fig. 10. Simplified equivalent circuits of resonant tank 1. (a) Mode II($0 \le \omega_0 t < \theta_0$). (b) Mode IV ($\theta_0 \le \omega_0 t < \theta_1$). (c) Mode V ($\theta_1 \le \omega_0 t < \pi$). (d) Mode VII ($\pi \le \omega_0 t < \theta_2$). (e) Mode IX ($\theta_2 \le \omega_0 t < \theta_3$). (f) Mode X ($\theta_3 \le \omega_0 t < 2\pi$).

According to $v_{L_m}(t)$ and $v'_{L_m}(t)$, we can consider each resonant tank separately by decoupling two transformer. The simplified equivalent circuits of resonant tanks 1 and 2 are shown in Figs. 10 and 11, respectively. The trajectory of each resonant tank is shown in Fig. 12. In Mode II, the trajectory of resonant tank 1 is a circle centered at $(1 - 1/2\ G, 0)$ while the resonant tank 2 is centered at $(1/2\ G, 0)$. The trajectory of resonant tank 1 is a circle centered at $(1/2 - 1/2\ G, 0)$, and the trajectory of resonant tank 2 is a circle centered at $(1/2 + 1/2\ G, 0)$ in Mode IV. In Mode V, L_m resonants with L_r and C_r and the input voltage of both resonant is V_{in}. Hence, the trajectory of both resonant tanks is an ellipse centered at (1, 0).

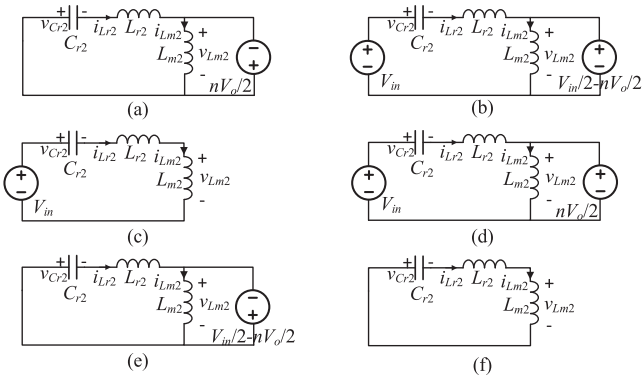

Fig. 11. Simplified equivalent circuits of resonant tank 2. (a) Mode II ($0 \le \omega_0 t < \theta_0$). (b) Mode IV ($\theta_0 \le \omega_0 t < \theta_1$). (c) Mode V ($\theta_1 \le \omega_0 t < \pi$). (d) Mode VII ($\pi \le \omega_0 t < \theta_2$). (e) Mode IX ($\theta_2 \le \omega_0 t < \theta_3$). (f) Mode X ($\theta_3 \le \omega_0 t < 2\pi$).

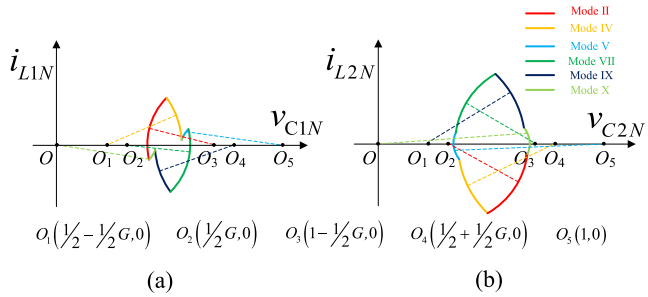

Fig. 12. Trajectory of resonant tanks. (a) Resonant tank 1. (b) Resonant tank 2.

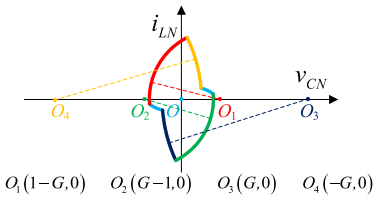

Fig. 13. Trajectory of conventional phase-shift modulated *LLC* converter.

Since Modes VI–X are symmetric to Modes I–V, the trajectory of other modes is similar to that of Modes I–V.

The switching actions of $S_{1,2}$ happen at time "0" and time "π." The switching actions of $S_{3,4}$ happen at time θ_0 and θ_2. S_1 is turned ON at time "0" and S_2 is turned ON at θ_0. The trajectory of conventional phase-shift modulated *LLC* converter is shown in Fig. 13. As illustrated in Fig. 12, $S_{1,2}$ are more vulnerable to lose their ZVS and their currents are symmetrical. Hence, we just need to consider the ZVS condition of S_1. The turn ON current of switching S_1 $i_{Lr1}(t_1)$ can be solved via numerical analysis. The ZVS condition can be expressed as follows:

$$\frac{1}{2}L_k {i_{Lr1}}^2(t_1) \ge \frac{1}{2}C_{\text{oss.eq}}V_{\text{in}}^2 \tag{31}$$

$$|i_{Lr1}(t_1)| \ge \sqrt{\frac{C_{\text{oss.eq}}}{L_k}}V_{\text{in}}. \tag{32}$$

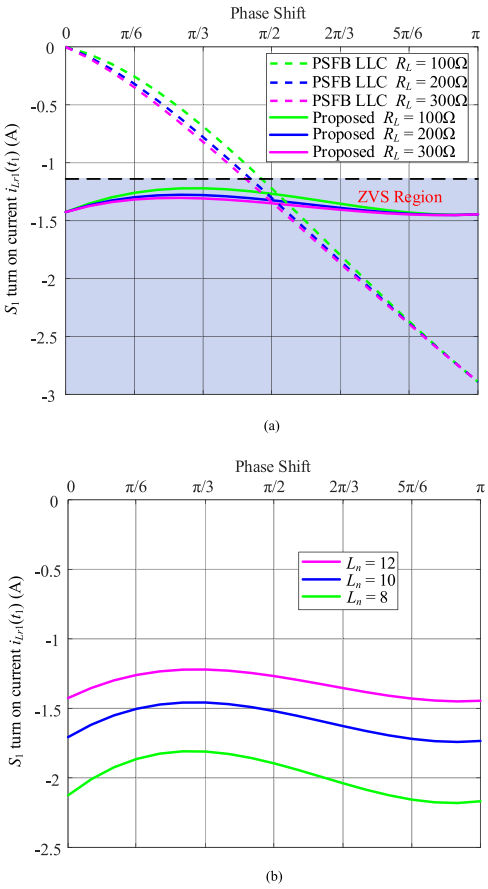

Fig. 14. Profiles of $i_{Lr1}(t_1)$ versus phase shift with different: (a) R_L; (b) L_n.

Fig. 14(a) shows the profiles of $i_{Lr1}(t_1)$ in the proposed converter and traditional PSFB *LLC* converter. As shown, the traditional PSFB *LLC* converter may loss ZVS at lower phase shift condition, while the proposed converter exhibits a wide ZVS condition for any phase shift. Therefore, compared with the traditional PSFB *LLC* converter, the proposed converter is featured with an extended ZVS range. Fig. 14(b) demonstrates the profiles of $i_{Lr1}(t_1)$ versus phase shift with different L_n. As indicated, the turn ON current decreases with the increase of L_n, in this article, we choose $L_n = 12$, to ensure a good tradeoff between wide ZVS range and low circulating current.

C. Loss Analysis

Since all MOSFETs can achieve ZVS turning-ON and all diodes can achieve ZCS turning-OFF, the main losses include MOSFET turn-OFF loss, conduction loss, and the magnetic core loss.

1) Conduction Loss: On the primary side, the currents of MOSFETs S_1 and S_2 are half-wave resonant tank 1 current and S_2 and S_3 are half-wave resonant tank 2. The average current of each secondary-side diode is half the output current. Therefore, the conduction loss can be calculated as

$$P_{\text{con}} = R_{\text{on}}(I_{1\text{rms}}^2 + I_{2\text{rms}}^2) + 2V_D I_o \tag{33}$$

TABLE I
SIMULATED PERFORMANCE VERIFICATION

V_o (V)	250	335	420
$I_{r1,rms}$ (A)	5.5	4.09	3.04
$I_{r2,rms}$ (A)	6.55	5	3.04
$I_{s,rms}$ (A)	5.38	3.98	2.65
Turning-off current of $S_{1,2}$ (A)	1.21	1.33	1.62
Turning-off current of $S_{3,4}$ (A)	10.9	8.53	1.62
ΔB_1 (T)	0.07	0.08	0.09
ΔB_2 (T)	0.13	0.12	0.09

where R_{on} is the ON resistance of primary-side MOSFETs, V_D is the forward voltage drop for the secondary-side diodes, $I_{1\text{rms}}$ and $I_{2\text{rms}}$ are the rms current of resonant tank 1 and 2, respectively, and I_o is the output current.

The coil loss of magnetic component is a part of conduction loss. It can be calculated as

$$P_{\text{coil}} = \rho_w \frac{l_w}{A_w} I_{\text{rms}}^2 \tag{34}$$

where ρ_w, l_w, A_w are the parameters of the conductors and I_{rms} is the rms current. It should be noted that Litz wire and interleaved winding help us to mitigate the skin effect and proximity effect.

2) MOSFET Turn-OFF Loss: The proposed converter can achieve ZVS turn ON and diodes can achieve ZCS turn OFF. Thus, the turn-ON loss of MOSFET and turn-OFF loss of diode is negligible, the switching loss mainly attributes to the MOSFET turn-OFF loss. When MOSFET is turned OFF, the overlap between v_{ds} and i_{ds} contributes to the turning OFF loss. Since the MOSFET is turn ON with ZVS, the energy stored on the output capacitor (C_{oss}) after the turn ON transition is recycled during the next turn ON transition. Thus, the switching loss is expressed as follows:

$$P_{\text{off}} = \left(\frac{1}{2} V_{\text{off}} I_{\text{off}} T_{\text{off}} - \frac{1}{2} C_{\text{oss}} V_{\text{off}}^2\right) f_s \tag{35}$$

where V_{off} is the reverse blocking voltage and I_{off} is the MOSFET current at the turn OFF. T_{off} is the turn-OFF time and can be estimated from the datasheet, f_s is the switching frequency.

3) Magnetic Core Loss: For magnetic component, the core loss is the other loss of magnetic loss in addition to coil loss. Steinmetz's equation is used to estimate the core loss

$$P_{\text{core}} = K_c f_s^{\alpha} \Delta B^{\beta} \tag{36}$$

where K_c, α, and β are provided from the datasheet and ΔB is the variation of the magnetic flux, which can be calculated based on the Faraday low of electromagnetic induction.

The simulation data with different V_o at full load condition is summarized in Table I, where $I_{r1,\text{rms}}$ and $I_{r2,\text{rms}}$ are the rms value of resonant tank 1 and 2, respectively, $I_{s,\text{rms}}$ is the rms value of i_{sec}, and ΔB is the flux variation.

According to Table I, different power losses are analyzed and the data are visualized in Fig. 15. As shown, the turning-OFF current of $S_{3,4}$ increases with the decrease of output voltage. This causes the mismatch of ΔB in two transformers. Moreover, the rms current of each resonant tank increases with the decrease

TABLE II
COMPARISON WITH *LLC*-BASED CONVERTER TOPOLOGIES FOR WIDE OUTPUT RANGE

Topologies	FB-*LLC* converter [7]	FB-*LLC* with secondary-side modulated [14]	Interleaved HB-*LLC* with voltage-doubler rectifiers [23]	Interleaved FB-*LLC* with hybrid rectifier [24]	This work
Modulation	PFM	PWM	PFM	PFM+PSM	PSM
Number of switches	4	5	4	8	4
Number of diodes	4	3	4	6	4
Number of transformers	1	1	2(center-tapped)	2	2
Number of filter capacitors	1	2	4	1	1
Input voltage	400V	390V	400V	400V	390V
Output voltage	250-420V	250-420V	50-420V	150-500V	10-420V
Power level	3.3kW	1kW	1.5kW	3.5kW	1kW
Peak efficiency	98.2%	96.7%	95.65%	98%	98.1%

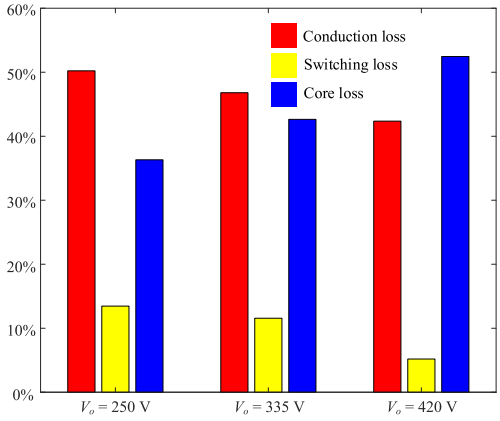

Fig. 15. Power loss breakdown with different output voltage.

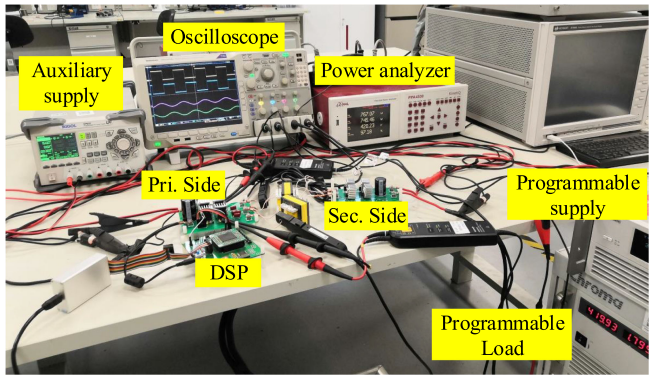

Fig. 16. Photograph of the experimental setup.

of output voltage. Thus, as shown in Fig. 15, the percentage of switching loss and conduction loss increases as the phase shift decreases.

D. Performance Comparison

As reviewed in Section I, many papers have been proposed to improve the performance of *LLC* converter in wide-output range applications. The comparison with the state-of-the-art *LLC*-based topologies with wide output range is summarized in Table II. Wang and Li [14] utilized a semiactive rectifier to extend the voltage gain range via duty cycle control. However, the output gain is constrained between 1 and 2.

In [23] and [24], interleaved HB-*LLC* converter with voltage-doubler rectifier and FB-*LLC* converter with hybrid rectifier are proposed. Their control strategies are PFM and PFM+PSM, respectively. In order to obtain a wide output voltage range in [23], a wide switching frequency range is required. Moreover, four output filter capacitors and four diodes are required on the secondary side. In [24], the converter operates in PSM mode in high-output voltage scenarios, and operates in PSM mode in low-output voltage scenarios. However, it increases the control complexity. The output voltage range is still limited. The converter is featured with high components count, which increase the cost and system volume. The last column in Table II demonstrates the performance of this article. As shown, the proposed converter has a widest output voltage range (10–420 V), singular phase shift control, and low components count.

IV. EXPERIMENTAL RESULTS

A 1 kW/100 kHz prototype with 390 V input and 10–420 V output is designed. Fig. 16 shows the photo of the experimental setup. Since f_s is fixed at f_r, the output voltage is regulated by φ. The turns ratio n is designed as 13:14 to achieve 420-V output voltage when $\varphi = \pi$, the output voltage is 420 V. Table III summarizes the circuit design parameters.

The steady-state experimental waveforms of 420 V/1000 W output are shown in Fig. 17. It is seen that φ between v_{gs1} and v_{gs3} is π. Fig. 17(a) captures the waveforms of v_{ab1}, v_{ab2} and

TABLE III
DESIGN PARAMETERS OF THE PROTOTYPE

Components	Values
V_{in} (Input voltage)	390V
V_o (Output voltage)	10-420V
$L_{r1,2}$ (Resonant inductor)	28.1μH
$C_{r1,2}$ (Resonant capacitor)	90nF
$L_{m1,2}$ (Magnetizing inductor)	350μH
C_o (Output capacitor)	100μF
$n_{1,2}$ (Turns ratio)	13 : 14
f_s (Switching frequency)	100kHz
S_{1-4} (MOSFTEs)	SCT3120AL
D_{1-4} (Diodes)	C3D06065I

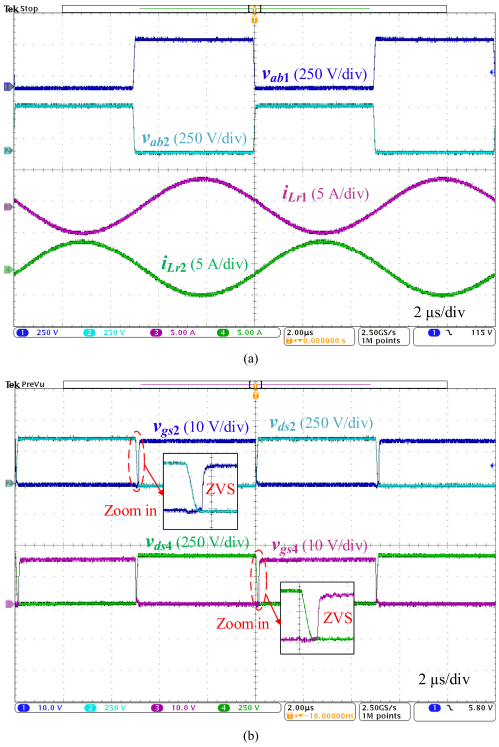

Fig. 17. Experimental steady-state waveforms with $V_o = 420\,\mathrm{V}$, $P_o = 1000\,\mathrm{W}$: (a) v_{ab1}, v_{ab2}, i_{Lr1}, and i_{Lr2}; (b) v_{gs2}, $v_{\mathrm{ds}2}$, v_{gs4}, and $v_{\mathrm{ds}4}$.

i_{Lr1}, i_{Lr2}. The secondary side of two transformer is connected in reverse series, and v_{ab1} and v_{ab2} are complementary symmetrical. Thus, i_{Lr1} and i_{Lr2} are symmetrical and the output power is shared by the two HB-*LLC* converters. Furthermore, each HB-*LLC* converter operates at f_r and the control signal are symmetrical. Hence, the soft-switching performance of each HB-*LLC* converter is identical to that of traditional HB-*LLC* converter. Fig. 17(b) indicates that the soft-switching of the primary-side switch is achieved.

Figs. 18 and 19 show the steady-state waveforms with 250 V/500 W and 100 V/100 W output, respectively. Figs. 18(a) and 19(a) capture the waveforms of v_{ab1}, v_{ab2} and i_{Lr1}, i_{Lr2}. The secondary sides of two transformer are connected in reverse series, and the phase shift between v_{ab1} and v_{ab2} is φ. Hence, i_{Lr1} and i_{Lr2} are asymmetrical. There is a stage where no current flows through the diode and L_m resonants with L_r and C_r. From Figs. 18(a) and 19(a), we can find that with the increase of φ, the

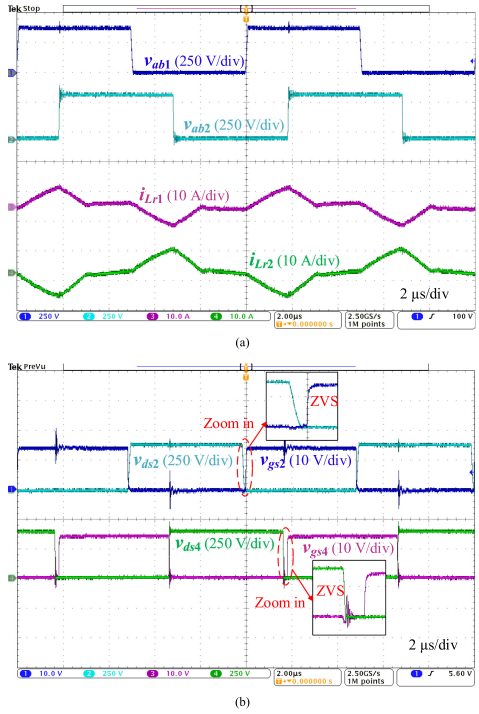

Fig. 18. Steady-state waveforms with $V_o = 250\,\mathrm{V}$, $P_o = 500\,\mathrm{W}$: (a) v_{ab1}, v_{ab2}, i_{Lr1}, and i_{Lr2}; (b) v_{gs2}, $v_{\mathrm{ds}2}$, v_{gs4}, and $v_{\mathrm{ds}4}$.

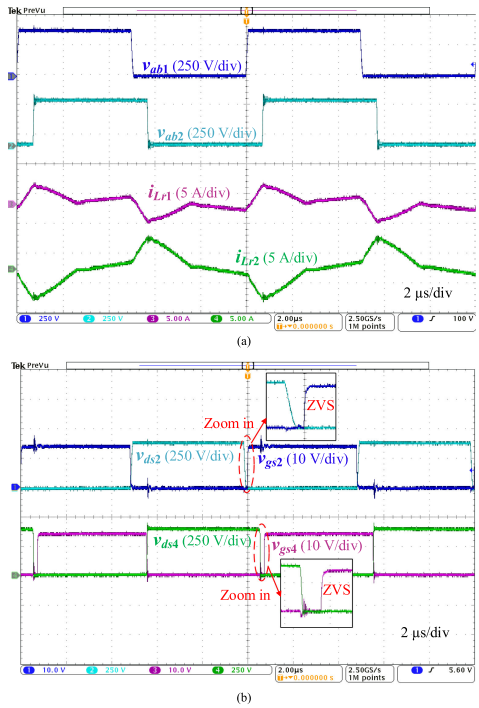

Fig. 19. Experimental steady-state waveforms with $V_o = 100\,\mathrm{V}$, $P_o = 100\,\mathrm{W}$: (a) v_{ab1}, v_{ab2}, i_{Lr1}, and i_{Lr2}; (b) v_{gs2}, $v_{\mathrm{ds}2}$, v_{gs4}, and $v_{\mathrm{ds}4}$.

output voltage increases and the voltage and current waveforms follow the theoretical analysis. Figs. 18(b) and 19(b) show the soft-switching of the primary-side switch. It is seen that the phase shift is small in low-output voltage condition, the ZVS can also be achieved in all primary-side switches of two resonant

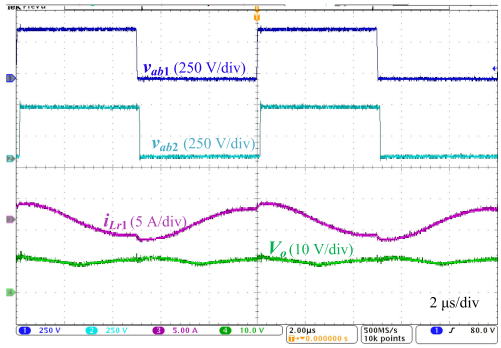

Fig. 20. Experimental steady-state waveforms with $V_o = 10$ V, $P_o = 20$ W.

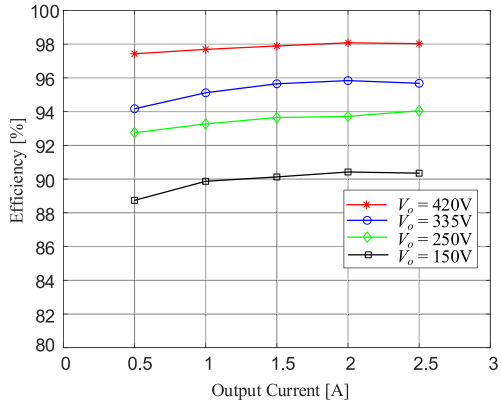

Fig. 21. Curves of efficiency versus output current with different V_o.

tanks. Fig. 20 shows the steady-state waveforms with 10 V/20 W output. The output voltage can be close to zero when tune φ to close to zero.

The efficiency versus the output power is measured and plotted in Fig. 21. As shown, the prototype demonstrates good efficiency performance over the wide output voltage range. The peak efficiency reaches 98.1% at full load. The efficiency drops with the decrease of the output voltage. This is mainly due to the fact that the circulating current increases with the decrease of phase shift. Thus, the circulating current induced conduction loss also increases.

V. Conclusion

In this article, an interleaved HB phase shift *LLC* resonant converter was proposed for ultrawide output voltage range applications. The operation principle and detailed theoretical analysis are presented. Two interleaved *LLC* units can be analyzed as one FB phase shift *LLC* converter by coupling two resonant tanks. Therefore, the voltage gain can be solved numerically. The ZVS range is analyzed qualitatively. In comparison with conventional phase shift *LLC* topology, it exhibits wider ZVS range. The proposed topology has wide output voltage rang with fixed-frequency operation, wide ZVS range, low switching devices count, and high efficiency. The fixed-frequency operation facilitates an easy optimization of the magnetic component design. A 1-kW rated prototype is designed to verify its effectiveness and feasibility. The designed converter demonstrates an output voltage range much wider than the state of the art. The peak efficiency is measured as 98.1%. A wide ZVS range is also achieved experimentally.

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