Letters

PCB-Embedded GaN-on-Si Half-Bridge and Driver ICs With On-Package Gate and DC-Link Capacitors

Stefan Moench, *Member, IEEE*, Richard Reiner, Patrick Waltereit, Fouad Benkhelifa, Jan Hückelheim, Dirk Meder, Martin Zink, Thomas Kaden, Stefan Noll, Sebastian Mansfeld, Nicola Mingirulli, Rüdiger Quay, *Senior Member, IEEE*, and Ingmar Kallfass, *Member, IEEE*

***Abstract*—A low-inductive half-bridge and gate driver package with on-package gate and dc-link capacitors is realized by printed circuit board (PCB) embedding of two GaN-on-Si ICs. While monolithic half-bridge and driver integration reduces on-chip parasitics, it does not solve the interconnection challenge to external capacitors. This letter solves this issue through advantageous combination of PCB embedding and monolithic circuit integration. This letter uses GaN-on-Si power circuits with integrated gate drivers, freewheeling diodes, and temperature and current sensors. GaN ICs are fabricated with thick copper on both sides, which makes them applicable to commercial PCB-embedding technologies. Thermal aspects are discussed and electromagnetic simulations used to compare the PCB-embedded package to a bond wire based package. A PCB-embedded dc–dc converter is operated up to 350 V and 450 W with up to 98.7% efficiency. 380 V hard-switching transitions show below 8% over- and undershoot despite over 120 V/ns slew rates. Parallel platelike placement of silicon flip-chip capacitors above the gate driver final stage transistors and separated only by a thin PCB layer increased the gate-loop parasitic inductance by only 40 pH.**

***Index Terms*—Bridge circuits, driver circuits, gallium nitride, multichip modules, power integrated circuits, printed circuits, semiconductor device packaging.**

I. Introduction

MONOLITHIC integration of circuits and sensors [1]–[5] in the lateral GaN-on-Si technology increases the functionality and integration density at low additional chip area and cost [6]. Monolithic power stages with a single or two half-bridge transistors and integrated gate drivers have already been commercialized [7], [8]. However, there are still critical external interconnections required for the operation of monolithic power ICs in converters: The gate driver requires interconnection to external gate supply capacitors. The half-bridge power path requires interconnection to external dc-link capacitors. In both cases, the parasitic inductance of this external interconnections will ultimately limit the switching performance [9]. To address this challenge, this letter uses printed circuit board (PCB)-embedding technology to package two GaN ICs in a half-bridge package with on-package bypass capacitors. This combination of monolithic circuit integration, package-level integration, and on-package capacitors simultaneously enables high functionality and low parasitic inductance.

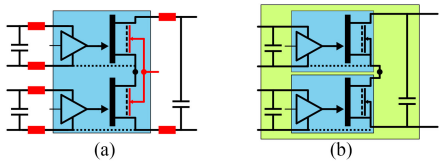

Fig. 1. (a) Monolithic half-bridge/driver has interconnect parasitics. (b) PCB embedding of two ICs as half-bridge with on-package gate/dc-link capacitors.

Fig. 1(a) illustrates how a monolithic GaN half-bridge with integrated gate drivers [4], [7], [10] does not solve the interconnect problem to external capacitors. Furthermore, the monolithic GaN-on-Si half-bridge on a common silicon substrate requires an alternative substrate termination due to the common backside of the high-side and low-side devices, which results in static and dynamic substrate biasing effects [11], [12]. Additional technological steps, such as GaN-on-SOI [13], are another way to avoid the substrate biasing effects, but still do not solve the external interconnect challenge. Fig. 1(b) shows how PCB embedding of two discrete GaN power ICs (power transistor, gate driver, and integrated sensors) as a half-bridge with on-package capacitors solves two problems at the same time: First, the packaging allows low-inductive interconnection to gate-loop and power-loop capacitors. Second, the discrete half-bridge based on two GaN-on-Si power ICs allows separate substrate-to-source

Manuscript received May 11, 2020; revised June 6, 2020; accepted June 21, 2020. Date of publication June 28, 2020; date of current version September 4, 2020. This work was supported by the German Federal Ministry of Education and Research (BMBF) under Grant GaNIAL (FKZ: 16EMO215K). *(Corresponding author: Stefan Moench.)*

Stefan Moench, Richard Reiner, Patrick Waltereit, Fouad Benkhelifa, Dirk Meder, Martin Zink, and Rüdiger Quay are with the Fraunhofer IAF, Fraunhofer Institute for Applied Solid State Physics, 79108 Freiburg, Germany (e-mail: stefan.moench@iaf.fraunhofer.de; richard.reiner@iaf.fraunhofer.de; patrick.waltereit@iaf.fraunhofer.de; fouad.benkhelifa@iaf.fraunhofer.de; dirk.meder@iaf.fraunhofer.de; martin.zink@iaf.fraunhofer.de; ruediger.quay@iaf.fraunhofer.de).

Jan Hückelheim and Ingmar Kallfass are with the Institute of Robust Power Semiconductor Systems, University of Stuttgart, 70569 Stuttgart, Germany (e-mail: jan.hueckelheim@ilh.uni-stuttgart.de; ingmar.kallfass@ilh.uni-stuttgart.de).

Thomas Kaden, Stefan Noll, Sebastian Mansfeld, and Nicola Mingirulli are with the Robert Bosch GmbH, 70465 Stuttgart, Germany (e-mail: thomas.kaden@de.bosch.com; stefan.noll2@de.bosch.com; sebastian.mansfeld@de.bosch.com; nicola.mingirulli@de.bosch.com).

Color versions of one or more of the figures in this article are available online at https://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2020.3005621

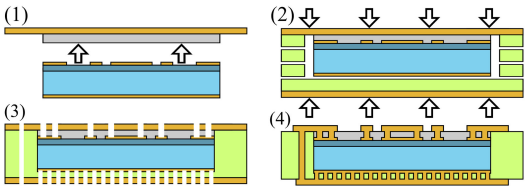

Fig. 2. PCB-embedding process flow [15].

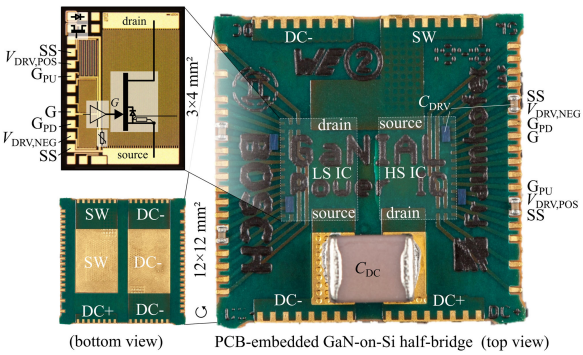

Fig. 3. PCB-embedded GaN half-bridge with on-package gate/dc-link capacitors.

termination, which avoids static and dynamic substrate biasing effects.

II. PCB Embedding for Half-Bridge Integration

The $3 \times 4\,\text{mm}^2$ ICs (published in [14]) are based on a 600- V GaN-on-Si technology [5] and integrate a 85-mΩ power transistor with an intrinsic freewheeling diode, a push–pull gate driver, an auxiliary transistor and diode for further functionality, a temperature sensor, and a current sensor. Fig. 3 shows an IC photograph and the schematic. The topside and backside metals of the GaN IC were fabricated with galvanic copper, which makes them suitable for commercial PCB-embedding processes. The topside copper is 5 μm thick. The wafer is thinned down to 135 μm as a tradeoff between thermal resistance and mechanical stability.

Fig. 2 shows the process flow for embedding of two ICs in a two-layer PCB with 70 μm copper.

1) The IC topside is glued with 35-μm-thick nonconductive adhesive (NCA) to the PCB topside copper layer.
2) Multilayer pressing (with cavities for the ICs in three of four prepreg layers).
3) First, mechanical drilling of through hole vias between outer PCB layers outside the IC area. Then, laser opening of the PCB copper and NCA for the microvias, stopping in the copper pads on both sides of the ICs.
4) First, copper filling of the through hole vias and microvias. Then, structuring of the PCB copper layout. Finally, applying the solder mask and silk screen.

Fig. 3 shows a top view of the PCB package with two embedded GaN ICs and on-package decoupling capacitors for the gate loops and the power loop. In the bottom view of the package, the thermal pads and power-stage connections are visible. The package dimensions are $12 \times 12\,\text{mm}^2$ with a thickness of 420 μm. The pad layout is compatible to a quad-flat-no-leads (QFN) package with 80 pins and 0.5-mm pitch. An embedded chip-QFN package approach was also proposed in [16]. The

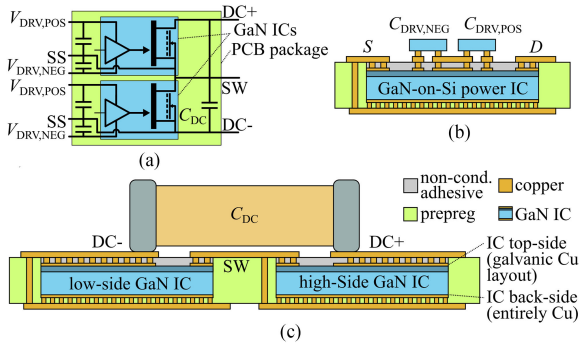

Fig. 4. PCB-embedded half-bridge with on-package gate/dc-link capacitors. (a) Schematic of integrated circuit. (b) On-package gate-supply capacitors for low-inductive gate loop. (c) On-package dc-link high-voltage capacitors for low-inductive power loop.

pads for the power stage and driver (on the high side, rotated pin-out compared to low-side) are labeled in Fig. 3, and further pins access further integrated circuits, such as temperature and current sensors and auxiliary devices.

This letter uses the "ET Microvia V1" embedding technology from Würth Elektronik CBT with the process flow from [15], which is also adapted in [17]. While the dielectric strength of the NCA layer itself is initially sufficient as high-voltage isolation [18], further possible failures of PCB-embedded packages from resin densification [18], humidity, or delamination [19] should be further studied. In addition to the gluing of the ICs in the package, the mechanical stability of the thin package is improved by the high number of microvias on both IC sides and the vias outside the IC area inside the PCB package. Nevertheless, mechanical reliability tests should be performed. In [16], good mechanical stability of even thinner embedded ICs in a comparable process is reported.

III. On-Package Gate and DC-Link Capacitors

Fig. 4(a) shows a schematic of two GaN ICs in a PCB-embedded package with gate and power decoupling capacitors. The schematic shows that all critical switched-current loops are closed within the package, which minimizes parasitic interconnect inductance. Fig. 4(b) illustrates how the on-package gate-supply capacitors are placed directly above the pads of the GaN IC's integrated gate driver, minimizing gate-loop inductance. Fig. 4(c) shows how an on-package dc-link capacitor is placed close to the half-bridge ICs. As on-package gate-loop decoupling capacitors, silicon chip capacitors (Si-Caps., 10 nF, 11 V, Murata UBSC.935152492510, 0201M) are used and mounted in a flip-chip assembly directly above the embedded ICs. Additional multilayer capacitors for the gate supply are placed at the edges of the package (10 nF, 10 V, X7R, 0201). As on-package dc-link decoupling capacitor, a multilayer ceramic capacitor is used (33 nF, 630 V NP0, 1210). In [3], on-package power-loop capacitors are also used for a GaN-based PCB-embedded multilevel converter.

IV. Parasitic Inductance

The parasitic inductances of the PCB-embedded module and a wire-bonded module [14] were simulated (Momentum EM simulation, S-parameters, 100 MHz), and the results are shown

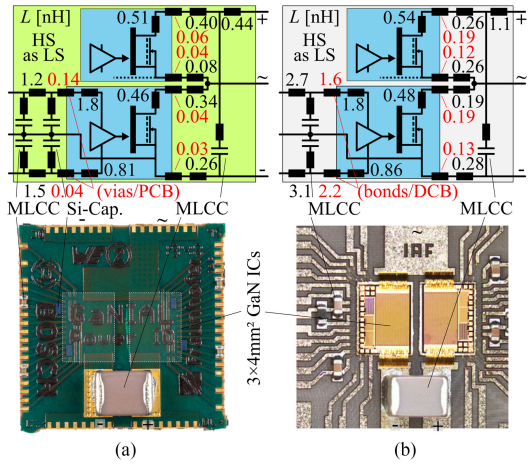

Fig. 5. Parasitic inductance of (a) PCB-embedded half-bridge with ceramic and Si on-package capacitors and (b) wire-bonded DCB module [14].

TABLE I
PARASITIC POWER LOOP AND GATE LOOP INDUCTANCE

	Wire-bonding to MLCC	PCB-embedding to MLCC	PCB-embedding to Si-Cap.
Power-loop	2.64 nH (23.9%)	2.22 nH (7.7%)	-
Gate-loop PU	3.40 nH (47.1%)	3.14 nH (4.5%)	1.94 nH (7.2%)
Gate-loop PD	3.06 nH (71.9%)	2.35 nH (1.7%)	0.85 nH (4.7%)

in Fig. 5. The ICs per se are large parts of the power loop and the integrated driver layout and the power transistors have on-chip inductance. Thus, a full flattened IC layout (transistors in ON-state) is cosimulated as nested technology. Table I lists the total loop inductances and shows the assembly-specific partial inductances thereof in percent (DCB: bond wires, PCB embedding: microvias, and PCB metal above the drain and source pads). The ICs themselves contribute 44% of 2.22 nH power-loop inductance in the PCB-embedded package (39% of 2.64 nH on the DCB). While all power-loop bond wires sum up to 0.63 nH (DCB assembly), the micro-via interconnect in the PCB-embedded package adds only 0.17 nH. The on-chip driver with wiring to the power transistor contributes 1.8 nH (pull up) and 0.86 nH (pull down) to the gate loop. The interconnections to the nearest capacitor increase the gate-loop inductance further by 89% (pull up) and 256% (pull down), whereas the PCB embedding adds only 8% and 5%.

The slightly different placement of the pull-up and pull-down Si-Caps. affects the gate-loop inductance differently: The placement of the pull-up capacitor outside the IC area adds 0.14 nH, whereas the placement of the pull-down capacitor above the IC adds only 40 pH. Furthermore, the traces of the PCB package above the IC increases the electromagnetic coupling, reducing the inductance of the pull-down transistor by 6%.

The packages of the used capacitors add further series inductance (ESL), which is indicated without values in Fig. 5. From datasheets, the ESL is around 100 pH (Si-Cap.), 120 pH (0201 MLCC capacitors, PCB package), 300 pH (0402 MLCC capacitors, DCB package), and 1 nH (MLCC dc link).

Segmentwise inductances were extracted by dividing the closed loops in successive parts. Mutually coupled inductances are substrated from the remaining loop segments from each segment's self-inductance. This method causes the sum of all segment inductances to match the total loop inductance. All parasitic inductances are simulated, and the PCB-embedded power-loop inductance is additionally measured (LCR meter, 2 MHz) as 2.35 nH (2.22 nH sim.) for verification.

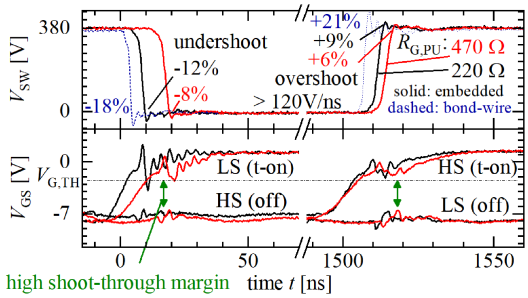

Fig. 6. Hard-switching transitions without inductor at 380 V input voltage.

V. EMBEDDED HALF-BRIDGE CONVERTER OPERATION

The PCB-embedded package with on-package capacitors is soldered onto a ceramic substrate. The hybrid assembly approach combining PCB embedding, a ceramic, and on-package passive components is also realized in [20] with external Si-based gate drivers and discrete GaN transistors. This letter embeds a GaN power IC, which provides a gate driver and other functionalities. The embedded subassembly was soldered to a dc board [see Fig. 7(b)]. A dual-input predriver circuit from [21] was used. To adjust the switching speed, the predriver gate resistor which drives the pull-up transistor $R_{\mathrm{G,PU}}$ (see [21]) is varied. This section uses only MLCCs as on-package gate capacitors. Fig. 6 shows measured hard-switching transitions at 380 V input. No inductor is connected to the half-bridge, which allows characterization of hard-switching transitions for both the high-side and low-side transistors. For $R_{\mathrm{G,PU}} = 470\,\Omega$, clean switching with -8% and +6% undershoot and overshoot is measured, despite high maximum slew rates of +122 V/ns and -150 V/ns. The slew rate increased to +142 V/ns and -174 V/ns for $R_{\mathrm{G,PU}} = 220\,\Omega$, and measured overshoot and undershoot of +9% and -12%. Fig. 6 also shows a higher overshoot above 18% for the bond-wire module from [14] (the faster switching is from a slightly different driver). Despite high slew rates, the measured gate voltages in Fig. 6 show negligible parasitic coupling into the OFF-state transistors, which avoids shoot-through conditions with a high margin. The measurements in Fig. 6 are at room temperature, and due to the high gate–source voltage margin, a stable switching operation is expected also at elevated temperatures. Even though the Schottky gates used in this letter are not as susceptible to overvoltage or threshold-voltage shift as p-GaN gates, no severe gate–source overvoltage is observed in Fig. 6. Fig. 7(a) shows the measured dc–dc converter efficiency up to 450 W and 350 V (50% duty cycle, 65 kHz, 50-ns deadtime, hard switching). At 300 V, 0 A, the switching frequency was varied to 42 and 100 kHz, both increasing the power loss. Loss estimation at 300 V, 2.5 A amounts to 30% inductor core and winding losses, above 15% from dynamically increased ON-resistance, below 10% switching loss, including C_{OSS}-related loss, and unaccounted losses (leakage currents, the setup, and ESR of the dc capacitors).

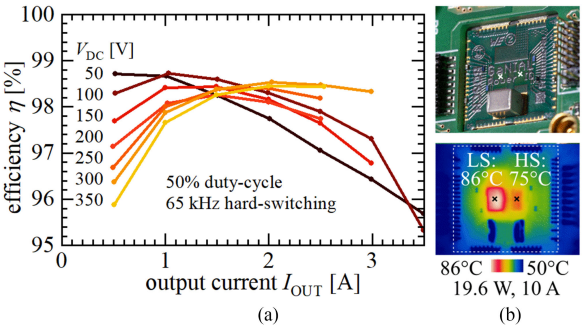

Fig. 7. (a) DC–DC converter efficiency. (b) Module and thermal image.

VI. Thermal Considerations

An array of 332 copper-filled microvias (100 μm diameter) per IC connects the two large thermal pads (see Fig. 3) through the 65 μm thick prepreg to the two IC backsides (22% fill factor). The calculated [22] thermal resistance of each IC from the channel to the backside of the IC is 0.08 K/W, and increases by 0.14 K/W from the PCB-embedded package (micro-via array and thermal pads). The PCB package was soldered to a 0.3 mm thick AlN ceramic substrate and attached by thermal paste to a baseplate (controlled elevated temperature of 50 °C). A dc current of 10 A was forced through both transistors in series in ON-state to cause 19.6- W heating power [intentionally higher than the highest power loss during dc–dc converter operation in Fig. 7(a)]. A thermal image in Fig. 7(b) shows an average case temperature increase of 30.5 K [measurement positions in Fig. 7(b)], which is a thermal resistance of 1.56 K/W. Even though the absolute temperature increase is still low, the measured thermal resistance (which also includes the attachment to the baseplate) is significantly higher than the calculated contribution of the IC and PCB package. The thermal measurement is interpreted as in [22] to mean that the PCB-packaging technology itself is not the limiting factor when using a dense array of copper-filled thermal vias.

VII. Conclusion

The GaN-on-Si technology enables monolithic integrated power circuits, such as gate drivers and half-bridges, but does not solve the interconnection to external capacitors, which are part of the critical gate and power loops. This letter solves this challenge by combining monolithic integration with advanced packaging: The combination of GaN power ICs, PCB embedding, and on-package decoupling capacitors is a viable solution to unleash the full switching capabilities of wide bandgap semiconductors up to the power converter level.

Acknowledgment

The authors would like to thank L. Haase and J. Wolf for providing advice and expertise and Würth Elektronik CBT for insight and support. The authors would also like to thank Murata for Si-Cap. samples, and the staff at Fraunhofer IAF who was involved in the epitaxy, fabrication, and characterization of the devices.

References

[1] Y. Yamashita, S. Stoffels, N. Posthuma, S. Decoutere, and K. Kobayashi, "Monolithically integrated E-mode GaN-on-SOI gate driver with power GaN-HEMT for MHz-switching," in *Proc. IEEE 6th Workshop Wide Bandgap Power Devices Appl.*, 2018, pp. 231–236.

[2] Y. Zhang, M. Rodriguez, and D. Maksimovic, "Very high frequency PWM buck converters using monolithic GaN half-bridge power stages with integrated gate drivers," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7926–7942, Nov. 2016.

[3] B. Weiss, R. Reiner, P. Waltereit, R. Quay, and O. Ambacher, "Operation of PCB-embedded, high-voltage multilevel-converter GaN-IC," *Proc. IEEE 5th Workshop Wide Bandgap Power Devices Appl.*, 2017, pp. 398–403.

[4] X. Li *et al.*, "Demonstration of GaN integrated half-bridge with on-chip drivers on 200 mm engineered substrates," *IEEE Electron Device Lett.*, vol. 40, no. 9, pp. 1499–1502, Sep. 2019.

[5] R. Reiner *et al.*, "Monolithically integrated power circuits in high-voltage GaN-on-Si heterojunction technology," *IET Power Electron.*, vol. 11, no. 4, pp. 681–688, 2018.

[6] J. Roberts, J. Styles, and D. Chen, "Integrated gate drivers for e-mode very high power GaN transistors," in *Proc. IEEE Int. Workshop Integr. Power Packag.*," 2015, pp. 16–19.

[7] N. Fichtenbaum, M. Giandalia, S. Sharma, and J. Zhang, "Half-bridge GaN power ICs: Performance and application," *IEEE Power Electron. Mag.*, vol. 4, no. 3, pp. 33–40, Sep. 2017.

[8] A. Lidow, "Gallium nitride integration: Breaking down technical barriers quickly [expert view]," *IEEE Power Electron. Mag.*, vol. 7, no. 1, pp. 56–63, Mar. 2020.

[9] R. Bayerer, "Parasitic inductance hindering utilization of power devices," in *Proc. 9th Int. Conf. Integr. Power Electron. Syst.*, 2016, pp. 1–8.

[10] Y. Uemoto *et al.*, "GaN monolithic inverter IC using normally-off gate injection transistors with planar isolation on Si substrate," in *Proc. IEEE Int. Electron Devices Meeting*, 2009, pp. 1–4.

[11] B. Weiss *et al.*, "Substrate biasing effects in a high-voltage, monolithically-integrated half-bridge GaN-Chip," in *IEEE 5th Workshop Wide Bandgap Power Devices Appl.*, 2017, pp. 265–272.

[12] V. Unni, H. Kawai, and E. Narayanan, "Increased static R ON in GaN-on-silicon power transistors under high-side operation with floating substrate conditions," *Electron. Lett.*, vol. 51, no. 1, pp. 108–110, 2015.

[13] X. Li *et al.*, "Suppression of the backgating effect of enhancement-mode p-GaN HEMTs on 200 mm GaN-on-SOI for monolithic integration," *IEEE Electron Device Lett.*, vol. 39, no. 7, pp. 999–1002, Jul. 2018.

[14] S. Moench *et al.*, "A 600 V GaN-on-Si power IC with integrated gate driver, freewheeling diode, temperature and current sensors and auxiliary devices," in *Proc. 11th Int. Conf. Integr. Power Electron. Syst.*, 2020, pp. 1–6.

[15] Würth Elektronik, "Embedding Technology: Design Guide Version 2.0," Feb. 2017.

[16] D. Manessis, L. Boettcher, A. Ostmann, R. Aschenbrenner, and H. Reichl, "Innovative approaches for realisation of embedded chip packages—Technological challenges and achievements," in *Proc. 59th Electron. Compon. Technol. Conf.*, 2009, pp. 475–481.

[17] E. Dechant, N. Seliger, and R. Kennel, "Performance of a GaN Half Bridge Switching Cell with Substrate Integrated Chips," in *Proc. PCIM Europe; Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*," 2019, pp. 1–7.

[18] E. Dechant, N. Seliger, and R. Kennel, "A study of dielectric breakdown of a half-bridge switching cell with substrate integrated 650 V GaN dies," in *Proc. IEEE Int. Workshop Integr. Power Packag.*, 2019, pp. 18–23.

[19] S. Dwarakanath, P. M. Raj, V. Smet, V. Sundaram, M. D. Losego, and R. Tummala, "High-temperature and moisture-ageing reliability of high-density power packages for electric vehicles," in *Proc. IEEE 68th Electron. Compon. Technol. Conf.*, 2018, pp. 179–184.

[20] A. B. Jørgensen, S. Beczkowski, C. Uhrenfeldt, N. H. Petersen, S. Jørgensen, and S. Munk-Nielsen, "A fast-switching integrated full-bridge power module based on GaN eHEMT devices," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2494–2504, Mar. 2019.

[21] S. Moench *et al.*, "Monolithic integrated quasi-normally-off gate driver and 600 V GaN-on-Si HEMT," in *Proc. IEEE 3rd Workshop Wide Bandgap Power Devices Appl.*," 2015, pp. 92–97.

[22] R. Reiner *et al.*, "PCB-Embedding for GaN-on-Si power devices and ICs," in *Proc. 10th Int. Conf. Integr. Power Electron. Syst.*," 2018, pp. 1–6.