Letters

Nonlinear $C_{oss} - V_{DS}$ Profile Based ZVS Range Calculation for Dual Active Bridge Converters

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***Abstract*—Generally, power electronic converters are designed to obtain the highest efficiency at rated power while they are most often operated under partial loading conditions. For dual active bridge converters, the zero-voltage-switching (ZVS) conditions can be impaired under light load situations. While load depending ZVS operation has been introduced by prior-art approaches, the nonlinear characteristic of the output capacitance in a power device is often not considered and its effect on operating boundaries of ZVS is neglected. In this letter, based on practical switching transients, an improved method of calculating the ZVS range is introduced. By taking into account the nonlinearity of output capacitance, the method is developed from a detailed analysis of real switching transients. A 2.5-kW prototype is built, and a comprehensive comparison with prior-art approaches is conducted to validate the accuracy of the proposed method.**

***Index Terms*—Dual active bridge converter, zero-voltage switching.**

I. Introduction

ONE advantage of the dual-active bridge (DAB) converter [1] is the inherent capability of naturally achieving zero-voltage-switching (ZVS) for all switches without any auxiliary circuits, and this advantage has facilitated a wide application of DAB converters, such as in distributed power systems [2], energy storage systems [3], and electric vehicles [4]. However, due to the lower leakage inductance current in light-load conditions, the charge stored in the transistor output capacitor may not be totally released during the dead time, and this might result in ZVS failure owing to high voltage across the transistor at the turn-ON instant. This failure would further increase the switching losses, impair the electromagnetic compatibilityperformance [5] and even damage the power devices [6].

There are two commonly used methods to identify the limitations on the control variables for achieving ZVS, i.e., current-based method [7], [8] and energy-based method [9]. Therein, the current-based method is developed from the body diode conduction when the power device is switched ON and thus ZVS conditions can be attained by controlling a positive or negative leakage inductance current at the switching instants. However, the positive/negative current direction is the result of the ZVS achievement, which is not sufficient to guarantee a soft switching. In respect to the energy-based method, the ZVS is achieved under the condition that the energy stored in the output capacitance C_{oss} is totally released before the transistor is switched ON. This method is better by requiring a minimum leakage inductance current at the switching instants. However, the nonlinearity of the parasitic output capacitance is usually not taken into account, in spite of the fact that the output capacitance of a power device varies a lot during the turn-ON/turn-OFF procedure. Besides, the calculation procedure is complex regarding the square mathematical operation of the stored energy (e.g., $1/2Li^2$). Moreover, due to that more converter components are involved in the calculation, a high modeling accuracy of the involved components (e.g., the transformer) is required for an accurate ZVS range calculation and this accurate modeling would further increase the complexity. Consequently, owing to the missing consideration of the nonlinearity and the complex calculation procedure, the obtained ZVS range using the method would contain some critical operating points that could lead to ZVS failure.

A charge-based ZVS calculation method is proposed in [10], where the nonlinear change of output capacitance is involved. This method can achieve a more accurate ZVS operating range, and thus this letter also calculates the ZVS range based on the charge balance. But compared to the method in [10], the main difference and improvements of the proposed method in this letter are listed in the following.

First, the calculation of the available charges in [10] is not appropriate. In [10], the integration of the bridge current starts from the zero-crossing time instants to the switching moment, and the results are compared with the required discharge of the output capacitance. However, the time range between the two zero-crossing instants [10] might not be the discharging time interval of the output capacitance. In practical switching transients (cf. Section II), the actual integration limits should start from the instant when the drain-source voltage begin to reduce, and end at the instant when the drain-source voltage

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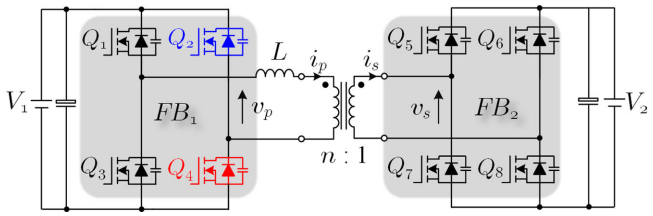

Fig. 1. Circuit topology of a DAB converter with full bridges FB_1 and FB_2.

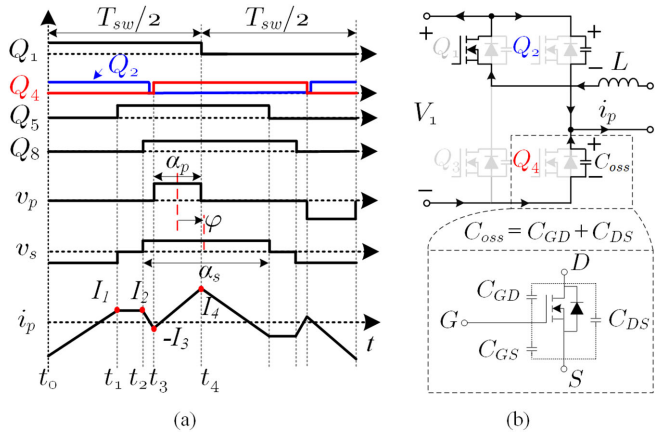

Fig. 2. Operation of the DAB converter. (a) Typical operation mode characterized by α_p, α_s, and φ. (b) General MOSFET model and resultant circuit state of the full bridge FB_1 during the turn-ON of Q_4.

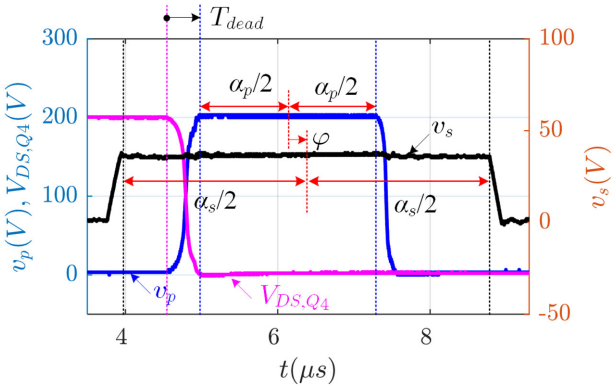

Fig. 3. Detailed description of the three control variables α_p, α_s, and φ in practical control.

becomes zero. The whole discharging interval is within this starting point and ending point, during which the discharge of the output capacitance synchronizes with the charge movement in the bridge current. Hence, this discharging interval is the proper integration interval for calculating the conveyed charges by the bridge current. Actually, this discharging interval is equal to the dead time, and it is not involved in the charge calculation in [10]. More details can be found in Section IV.

Second, the half dc-bus voltage change consideration in [10] is not appropriate because the drain-source voltage of a power device will switch between zero and the whole dc-bus voltage during transients. The turn-ON of one power device corresponds to the turn-OFF of the other one at the same time. Therefore, the charge and discharge of the power devices in the same bridge leg are analyzed together (Section III) in this letter.

In this letter, a nonlinear C_{oss} profile based ZVS range calculation method is presented according to practical switching transients in a DAB converter. Notably, this method can be applied to the full load range, but due to that the DAB is easier to lose ZVS in light load, this letter will focus on light-load operation. The measured switching transients are first shown in Section II. Then, ZVS analysis concerning the nonlinear change of the output capacitance is conducted in Section III. Next, a comparative analysis with other ZVS calculation methods is presented and verified by experimental results in Section IV, including a comparison with the charge-based method proposed in [10]. In Section V, the conclusion is summarized.

II. Practical Switching Transients

A DAB converter topology is shown in Fig. 1. It mainly consists of two full bridges (i.e., FB_1 and FB_2) generating a two-level or three-level ac voltage (i.e., v_p and v_s) across the transformer-inductor combination. A generalized light-load modulation method [11] is applied and relevant working waveforms are as shown in Fig. 2(a). Therein, three control variables are used to regulate the converter, i.e., duty cycles (α_p, α_s) of v_p, v_s and the phase shift angle (φ) between the fundamental components of these two voltages. It is common that a dead time T_{dead} is inserted between the two power devices in the same leg (e.g., Q_2 and Q_4) to avoid short circuit. As a result, this might cause φ to drift in practical control, and hence the dead time effect on the control variables should be considered and properly compensated [12], [13]. In this letter, by using the dead time compensation methods in [12], the practical control variables are depicted in details, as shown in Fig. 3.

As highlighted in Fig. 2(a), the power device Q_4 is turned ON at $t = t_3$, and meanwhile, Q_2 is turned OFF and Q_1 is kept ON. Consequently, the transient turning ON procedure of Q_4 can be described by the FB_1 transition circuit in Fig. 2(b). In a MOSFET device, parasitic capacitances are coupled among the drain, source and gate terminals, denoted by C_{GD}, C_{GS}, and C_{DS} in Fig. 2(b). On this basis, a nonlinear characteristic defined by $C_{oss} = C_{GD} + C_{DS}$ is often used to analyze the dynamic switching procedure (cf. Section III).

TABLE I
System Parameters of a DAB Prototype

Parameter	Variable	Value
Input DC voltage	V_1	200 V
Output DC voltage	V_2	35 V
Turns ratio of the transformer	$n:1$	3.5 : 1
Switching frequency	f_{sw}	60 kHz
Leakage inductance	L	45 μH

Using $V_1 = 200$ V from a dc power source, the measured transient drain-source voltages and gate-source voltages of Q_4 and leakage inductance currents are shown in Fig. 4. The key experimental parameters of the DAB setup are listed in Table I. In Fig. 4, there are eight groups of $V_{DS,Q4}$ and $V_{GS,Q4}$ corresponding to the phase shift φ varying from 3° to 10°. The

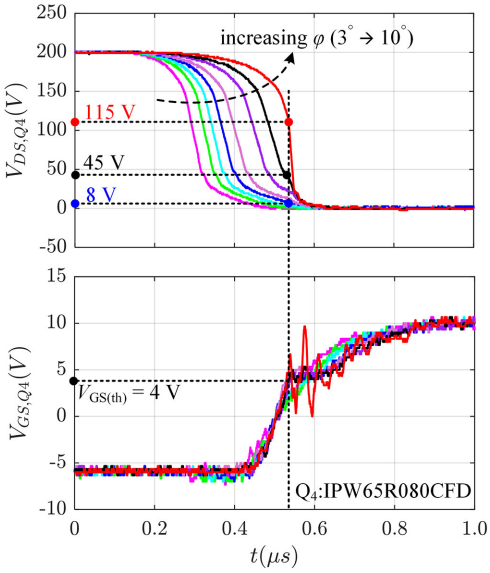

Fig. 4. Measured transient drain-source voltages and gate-source voltages of Q_4 at turning ON. Control parameters: $\alpha_p = 60°$, $\alpha_s = 110°$, and $\varphi = 3°$, $4°, 5°...$ $10°$ in the eight cases, respectively.

used power device Q_4 is Infineon IPW65R080CFD, and the threshold voltage $V_{GS(th)} = 4$ V can be read from the datasheet or manually measured. During the interval $t \in [0.2\ \mu s, 0.6\ \mu s]$, $V_{DS,Q4}$ decreases from V_1 to 0 due to the discharge of output capacitance $C_{oss,Q4}$. In the meantime, $V_{GS,Q4}$ gradually increases and when it reaches $V_{GS(th)}$, the transistor is turned ON. Hence, if the drain-source voltage has been reduced to zero or near-zero at this instant, ZVS can be achieved. Otherwise, it transfers to hard switching if $V_{DS,Q4}$ is still relatively high, and $V_{GS,Q4}$ starts to oscillate. In conclusion, in order to realize ZVS of Q_4, the output capacitance $C_{oss,Q4}$ should be sufficiently discharged.

III. Implementation of Nonlinear C_{oss}–V_{DS} Profile in ZVS Analysis

As concluded from the practical switching transients in the last section, the charges stored in the output capacitance should be fully released before turning ON in order to achieve ZVS. Hence, in order to obtain an accurate ZVS range, first the stored charges should be properly calculated with varying V_{DS} and nonlinear C_{oss}. Regarding this, the C_{oss} trajectory hardly varies with the temperature for Si super-junction [14], wide bandgap SiC [15] and GaN [16] devices, and thus the nonlinear $C_{oss} - V_{DS}$ profile can be adopted to calculate the stored charges.

As shown in Fig. 2(b), the transient voltages $V_{DS,Q2}$ and $V_{DS,Q4}$ can be described by

$$\begin{cases} C_{oss,Q2}\dfrac{dV_{DS,Q2}}{dt} = -i_{D,Q2} \\ C_{oss,Q4}\dfrac{dV_{DS,Q4}}{dt} = i_{D,Q4} \end{cases} \tag{1}$$

where $i_{D,Q2}$ and $i_{D,Q4}$ are the drain currents of Q_2 and Q_4, respectively. Combining (1) with the following relationship

$$\begin{cases} i_{D,Q4} + i_{D,Q2} = i_p \\ V_{DS,Q4} + V_{DS,Q2} = V_1 \end{cases} \tag{2}$$

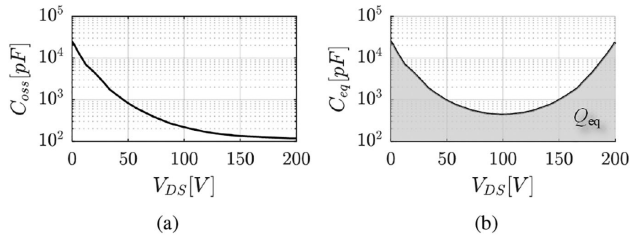

Fig. 5. Nonlinear profiles. (a) C_{oss}. (b) C_{eq} along with V_{DS} for Infineon IPW65R080CFD.

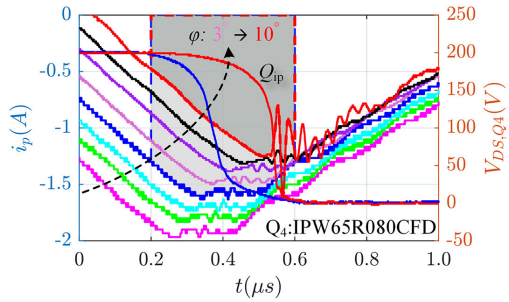

Fig. 6. Measured leakage inductance currents i_p with $\varphi = 3° \sim 10°$ and source-drain voltages $V_{DS,Q4}$ with $\varphi = 6°, 10°$ at the turn-ON of Q_4. The lighter and darker patched areas are the conveyed charges Q_{ip} by i_p in the cases of $\varphi = 6°$ and $\varphi = 10°$, respectively.

leads to

$$i_p = [C_{oss,Q2} + C_{oss,Q4}]\frac{dV_{DS,Q4}}{dt}. \tag{3}$$

For simplification, an equivalent capacitance C_{eq} defined as

$$C_{eq} = C_{oss}(V_1 - V_{DS,Q4}) + C_{oss}(V_{DS,Q4}) \tag{4}$$

is introduced to replace the term $C_{oss,Q2} + C_{oss,Q4}$ in (3). The values of $C_{oss}(V_1 - V_{DS,Q4})$ and $C_{oss}(V_{DS,Q4})$ in (4) can be extracted from the nonlinear $C_{oss} - V_{DS}$ profile shown in Fig. 5(a), which is usually given in the datasheet. Therefore, the C_{eq} trajectory can be obtained as shown in Fig. 5(b).

The equivalent charge Q_{eq} stored in C_{eq} with an OFF-state drain-source voltage V_1 can be calculated by

$$Q_{eq} = \int_0^{V_1} C_{eq} dV_{DS}. \tag{5}$$

The patched area in Fig. 5(b) denotes the charge quantity with $V_1 = 200$ V.

On the other hand, another condition for ZVS is that the stored charges Q_{eq} can be fully released into the leakage inductance current i_p, which means the conveyed charges in i_p should be larger than Q_{eq}. The total charges Q_{ip} in i_p at the turning ON of Q_4 could be represented by the patched areas in Fig. 6. Therein, the lighter patched area denotes Q_{ip} in the case of $\varphi = 6°$ and the darker is Q_{ip} in the case of $\varphi = 10°$. It can be seen that the value of Q_{ip} decreases as φ is increased from 3° to 10°. For the convenience of analysis, $t = 0.6\ \mu s$ is deemed the time origin and $t = 0.2\ \mu s$ the transient ending. Therefore, the transient charge Q conveyed by i_p during change of V_{DS} can be calculated by using a numerical integration technique. Corresponding to different φ, the trajectories of Q are shown by different marked

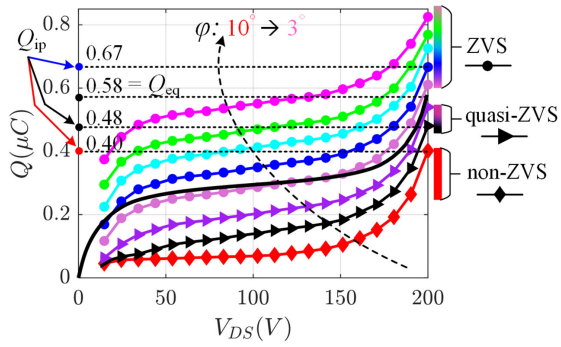

Fig. 7. Numerical integration (i.e., marked lines) of the measured currents i_p and the transient charge of C_{eq} (i.e., solid line) as the drain-source voltage of Q_4 reversely changes from 0 to 200 V.

lines in Fig. 7. Note that Q is equal to the total charge Q_{ip} when V_{DS} reaches 200 V. As a comparison, the transient charge stored in the equivalent output capacitance C_{eq} is also shown in Fig. 7, denoted by the solid line with a final value of Q_{eq} [cf. Fig. 5(b)].

In the case of $\varphi = 10°$, the available charge $Q_{ip} = 0.4\ \mu C$ in the current is lower than the stored charge $Q_{eq} = 0.58\ \mu C$ in the equivalent capacitance, indicating an insufficient discharge of C_{eq}. Hence, $V_{DS,Q4}$ sharply drops from 115 to 0 V in less than 0.1 μs (cf. Fig. 4) and severe oscillations are induced in the leakage inductance current. This non-ZVS case should be avoided since it might increase the switching losses and even potentially break the power device [6] due to high dv/dt. In cases of $\varphi = 3°...7°$, the charge Q_{ip} is larger than Q_{eq}, e.g., $Q_{ip} = 0.67\ \mu C$ with $\varphi = 6°$. Therefore, the equivalent capacitance C_{eq} can be totally discharged before Q_4 is turned ON. In terms of the middle cases where $\varphi = 8°, 9°$, the transferred charge Q_{ip} (equals 0.48 μC with $\varphi = 9°$) by the current is a bit lower than Q_{eq}, also implying an insufficient discharge of C_{eq}. One difference from the 10° case is that the drain-source voltage of Q_4 has reduced to a sufficient low level at turning ON, e.g., 45 V for $\varphi = 9°$ and even lower for $\varphi = 8°$ (cf. Fig. 4). Thus, no obvious oscillations are stimulated and they are named as quasi-ZVS in Fig. 7. Due to that the switching losses are increased in quasi-ZVS cases (i.e., $\varphi = 8°, 9°$) and the power devices could be impaired in non-ZVS cases (i.e., $\varphi = 10°$), the ZVS is regarded failed in the quasi-ZVS and non-ZVS cases.

IV. ZVS Range Comparison With Experimental Validation

There are mainly three approaches to derive the ZVS range in literature, named as App1, App2, and App3 in the following, and the proposed ZVS range calculation method is represented by Pro.

App1: The most often used method [7] to calculate the ZVS conditions is by

$$I_3 = \frac{nV_2}{4\pi L f_{sw}}\left[(k-1)\alpha_p - 2\varphi\right] \geq 0 \rightarrow \alpha_p \geq \frac{2}{k-1}\varphi \quad (6)$$

where $k = V_1/(nV_2)$ is the input/output dc voltage ratio and f_{sw} is the switching frequency.

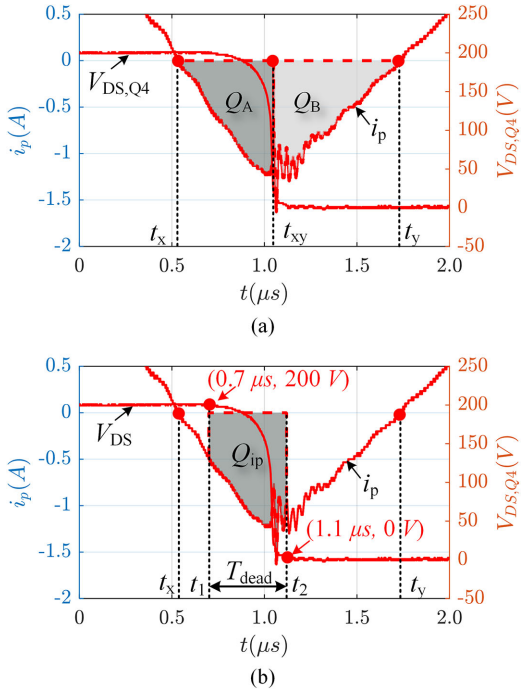

Fig. 8. (a) In the calculation method of App3, the defined two charges Q_A and Q_B in [10] with the case of $\varphi = 10°$, corresponding to the integration ranges of $[t_x,\ t_{xy}]$ and $[t_{xy},\ t_y]$, respectively. (b) In the proposed method Pro., the defined Q_{ip} and relevant integration range $[t_1,\ t_2]$, which is also the dead time interval.

App2: Another conventional method [9], [17] to calculate the ZVS conditions is focusing on the energy exchange, leading to

$$\alpha_p \geq \frac{2}{k-1}\varphi + \frac{4\pi L f_{sw}}{(k-1)nV_2}\sqrt{\frac{|\ 4nCV_1V_2 - 2CV_1^2\ |}{L}} \quad (7)$$

where $C = 1/V_1 \int_0^{V_1} C_{oss} dV_{DS}$. In this energy-based method, other than the missing consideration of the nonlinearity of the output capacitance, the calculation is complex and it is difficult to achieve the same accuracy as the proposed method. This is because more converter components are involved in the derivation [17], and the calculation will become even more complex if the nonlinear C_{oss} is considered.

App3: A third method in [10] is comparing the stored charges Q_{coss} in $C_{oss,Q4}$ (i.e., $Q_{coss} = \int_0^{V_1} C_{oss} dV_{DS}$) with the two defined charges Q_A and Q_B as shown in Fig. 8(a), resulting in

$$\begin{cases} Q_A = -\int_{t_x}^{t_{xy}} i_p dt \geq Q_{coss} \\ Q_B = -\int_{t_{xy}}^{t_y} i_p dt \geq Q_{coss} \end{cases} \Longrightarrow$$

$$\alpha_p \geq \max.\left\{ \begin{matrix} \frac{2}{k-1}\varphi + \frac{4\pi f_{sw}}{k-1}\sqrt{\frac{LQ_{eq}}{nV_2}}, \\ \frac{2}{k-1}\varphi + \frac{4\pi f_{sw}}{k-1}\sqrt{\frac{(k-1)LQ_{eq}}{nV_2}} \end{matrix} \right\}. \quad (8)$$

Although the nonlinearity of the output capacitance is included in this method, the integration limits are not properly considered. As comparison, the integration limits of App3 and the proposed method are depicted in Fig. 8(b), represented by t_x, t_y, and t_1, t_2, respectively. It can be seen from Fig. 8(b)

that the discharging procedure of the output capacitance of Q_4 is completed within $[t_1,\ t_2]$, which means that this procedure has not began at $t = t_x$ and has finished at $t = t_y$. Therefore, the involved ranges of $[t_x,\ t_1]$ and $[t_2,\ t_y]$ in the calculation [cf. (8)] of the conveyed charges of i_p in App3 is not appropriate. As a result, although the calculated Q_A and Q_B

$$\begin{cases} Q_A = 0.36\ \mu C > Q_{coss} = 0.29\ \mu C \\ Q_B = 0.44\ \mu C > Q_{coss} = 0.29\ \mu C \end{cases} \tag{9}$$

satisfy the ZVS conditions (8) in App3, the soft switching actually fails in the operating case of $\varphi = 10°$, as shown in Fig. 8(a).

Pro.: Based on the ZVS analysis in Section III, the proposed method of deriving ZVS condition is to compare the stored charges in the equivalent capacitance C_{eq} with the conveyed charges in current i_p during transients, i.e.,

$$Q_{ip} = -\int_0^{T_{\text{dead}}} i_p dt \geq Q_{eq} = \int_0^{V_1} C_{eq} dV_{DS} \tag{10}$$

The time $0 \rightarrow T_{\text{dead}}$ in (10) [cf. Fig. 8(b)] can be mapped to $0.6\ \mu s \rightarrow 0.2\ \mu s$ in Fig. 6. For comparing with App3, the calculated Q_{ip} and Q_{eq} are

$$Q_{ip} = 0.4\ \mu C < Q_{eq} = 0.58\ \mu C \tag{11}$$

and it does not satisfy the ZVS condition (10) of the proposed method, which is consistent with the failed ZVS case in Fig. 8(b).

As discussed in Section III (cf. Fig. 7), the boundary ZVS case is at $\varphi = 7°$. Seen from the practical i_p waveform in the case of $\varphi = 7°$ in Fig. 6, an approximate method to estimate Q_{ip} is by dividing the transient procedure into two intervals

$$i_p = \begin{cases} -I_3,\ t \in \left[0, \dfrac{T_{\text{dead}}}{2}\right) \\ -I_3 + \dfrac{nV_2}{L}\left(t - \dfrac{T_{\text{dead}}}{2}\right), t \in \left[\dfrac{T_{\text{dead}}}{2}, T_{\text{dead}}\right] \end{cases} \tag{12}$$

where $0 \rightarrow T_{\text{dead}}/2$ corresponds to $0.6\ \mu s \rightarrow 0.4\ \mu s$ in Fig. 6, and $T_{\text{dead}}/2 \rightarrow T_{\text{dead}}$ is $0.4\ \mu s \rightarrow 0.2\ \mu s$. In other words, the value of i_p is approximated as constant $-I_3$ in the first half of the dead time and a linear change in the second half. Hence, the ZVS limitation can be further derived by combining (10) and (12), resulting in

$$\alpha_p \geq \frac{2}{k-1}\varphi + \frac{4\pi L f_{sw}}{(k-1)nV_2}\left[\frac{Q_{eq}}{T_{\text{dead}}} + \frac{nV_2}{8L}T_{\text{dead}}\right]. \tag{13}$$

Note that the converter might operate in other working scenarios [e.g., Q_2 turns OFF before Q_8 turns ON in Fig. 2(a)] with a different combination of the three control variables, and in that case, the calculation of the peak value of i_p will be changed accordingly, but the principle of the proposed ZVS range derivation remains the same.

Using the same parameters as in Fig. 4, the calculated ZVS ranges ($\alpha_p - \varphi$ plane) of Q_4 can be obtained with different approaches, as shown in Fig. 9. For practical validation, 24 experimental cases with different system configurations Config.1∼3 are also depicted in the figure. The key parameters of the three configurations can be found in Table II. In Config.1, the value of φ is regulated from 3° to 10°, which is the same as Fig. 4, and the boundary is at $\varphi_b = 7°$ (cf. Fig. 7). Note that in order to distinguish the measured experimental ZVS boundary from the calculated results with different methods, φ_b is introduced in Table II to denote the practical ZVS boundary. Similarly, by varying φ between 6° ∼ 13° and 9° ∼ 16°, the measured ZVS boundaries are found at $\varphi_b = 10°$ and $\varphi_b = 12°$ for Configs. 2 and 3, respectively. As a comparison, the calculated ZVS boundaries using prior-art approaches App1∼App3 and the proposed method Pro. are shown in the last four columns of Table II. It can seen that the calculated boundary φ with the proposed method is more close to the measured φ_b than the other three approaches.

In order to further verify the accuracy of proposed method with different input/output dc voltages, Config.4∼6 are implemented. In Config.4, the practical transient waveforms of $V_{DS,Q4}$ and i_p are shown in top inset and middle inset of Fig. 10. Similar to Fig. 7, the numerical integration results are shown in the bottom inset of Fig. 10, from which the measured boundary $\varphi_b = 5°$ can be obtained. Applying the same procedure to Configs. 5 and 6, the measured and calculated ZVS boundaries are as listed in Table II. By comparing the measured boundary φ_b with the calculated values using different methods, the same conclusion can be achieved that the proposed method can predict a more accurate ZVS boundary than the other three methods.

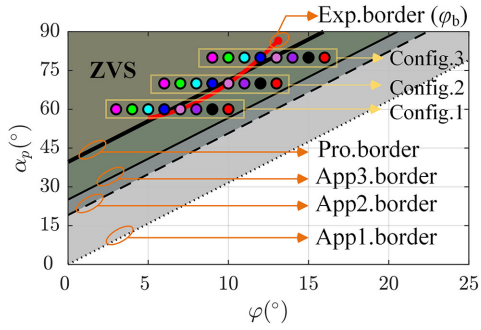

Fig. 9. Calculated ZVS boundaries of Q_4 using prior-art approaches $App1$, $App2$, $App3$, and the proposed method $Pro.$, and experimental cases (denoted by marked points) with different system parameter configurations (cf. Table II) and the obtained experimental ZVS boundaries (i.e., Exp. border).

TABLE II
MEASURED AND CALCULATED ZVS BOUNDARIES FOR DIFFERENT SYSTEM PARAMETER CONFIGURATIONS

Configs.	V_1	V_2	α_p	α_s	$\boldsymbol{\varphi_b}$	App1	App2	App3	Pro.
Config.1	200 V	35 V	60°	110°	**7°**	19°	13°	11°	6.4°
Config.2	200 V	35 V	70°	140°	**10°**	22.2°	16.1°	14.2°	9.6°
Config.3	200 V	35 V	80°	160°	**12°**	25.3°	19.3°	17.4°	12.8°
Config.4	200 V	45 V	110°	160°	**5°**	14.8°	7.3°	6°	5°
Config.5	230 V	25 V	40°	150°	**16°**	32.6°	23.2°	17.6°	15.4°
Config.6	170 V	25 V	40°	150°	**5°**	18.9°	16.4°	8.6°	5.6°

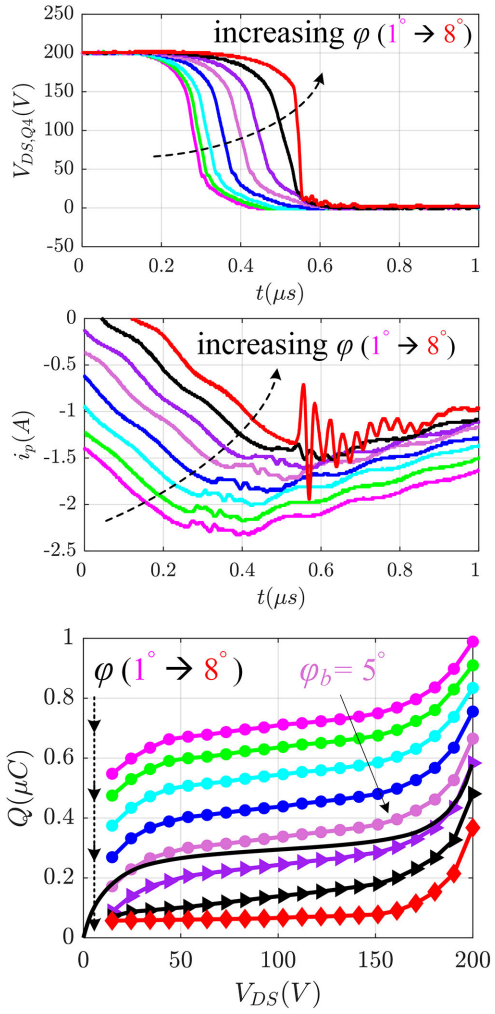

Fig. 10. Measured transients of $V_{DS,Q4}$, i_p and numerical integration of measured i_p for Config.4 in the top inset, middle inset and bottom inset, respectively.

V. Conclusion

Based on the practical switching transient, an accurate ZVS range calculation method is presented by considering the nonlinearity nature of output capacitance in a power device. The method considers both charge and discharge of the power devices in the same bridge leg. On this basis, the concepts of equivalent capacitance and equivalent charge are derived to analyze the ZVS transition and calculate the ZVS range. Compared to prior-art ZVS range calculation approaches where the nonlinear output capacitance is not considered, the proposed method has a higher accuracy. Although more calculations are needed, this is worthy to use as it is vital in practice to accurately forecast the ZVS boundary. Multiple experiments with different system parameters are implemented and the results are in agreement with the theoretical prediction.

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