New Semiquadratic High Step-Up DC/DC Converter for Renewable Energy Applications

Sara Hasanpour, Yam P. Siwakoti, *Senior Member, IEEE*, Ali Mostaan, and Frede Blaabjerg, *Fellow, IEEE*

***Abstract*—In this article, a new semiquadratic high step-up coupled-inductor dc/dc converter (SQHSUCI) with continuous input current and low voltage stress on semiconductor components is presented. The proposed structure employs a coupled-inductor (CI) and two power switches with simultaneous operation to achieve an extremely high voltage conversion ratio in a semiquadratic form. The voltage stress across the main power switch is clamped by two regenerative clamp capacitors. Here, the switching losses of both MOSFETs have been reduced by applying quasi-resonance operation of the circuit created by the leakage inductance of the CI along with the balancing and clamp capacitors. Therefore, by considering the high gain conversion ratio along with low voltage stress on components, the magnetic and semiconductors losses of the SQHSUCI are reduced significantly. Also, the energy stored in the leakage inductance of CI is recycled to the output capacitor. These features make the proposed SQHSUCI more suitable for industrial applications. The operation principle, steady state, and also comparisons with other related converters in continuous conduction mode (CCM) are discussed in detail. Finally, experimental results of a prototype with 20 V input and 200 W–200 V output at 50 kHz switching frequency, verify the theoretical advantages of the proposed strategy.**

***Index Terms*—Buck–boost converter, coupled-inductor, renewable energy sources.**

I. Introduction

NOWADAYS, renewable energy sources (RES) such as photovoltaic and fuel cells have been rapidly developed. Because of the low dc voltage levels of these sources (<50 V), high step-up dc/dc switch-mode converters are often used as the interface circuit to reach an appropriate output voltage (300–400 V) for many applications. Using current-fed structures of step-up converters with low input current ripple plays an important role in proper operation of the RES for maximum extraction [1]. The other desired performance indicators of these converters are high conversion ratio, low voltage and current stresses, common ground, high efficiency, and low cost. Moreover, the demand of nonisolated converters with simple structure along with higher efficiency and lower cost of implementation is ever increasing [2], [3]. It is noteworthy that for high-power applications (>1 kW), modular converters with higher volume and cost are often used.

The conventional boost converter with simple structure and continuous input current can be adopted to provide a step-up voltage gain in renewable sources. However, in practice, this converter cannot provide a proper high voltage gain, even in the extreme duty cycles. In fact, because of high stress across switching devices, this converter has to endure high switching and diode reverse recovery losses, so that the voltage conversion ratio and the power handling capacity are severely restricted. As a result, it is necessary to improve such conventional converters to achieve high voltage gain along with high efficiency with a reasonable duty ratio. In the last years, by means of some voltage boosting circuits such as voltage multipliers (VM), switched-capacitors, switched-inductors, voltage lift (VL), and also multistage techniques, many modified step-up topologies have been suggested. However, achieving a wide voltage conversion ratio in these converters often requires the use of a large number of components. In addition, high spikes on components in these converters lead to decreased efficiency, which limits their applications [2], [3].

Today, utilizing magnetic devices including coupled inductor (CI) and transformer along with other voltage-boosting circuits, especially VMs, is a favorite candidate for high step-up converters. In fact, in these converters, the performance of voltage boosting circuits is greatly improved by adjusting the turn's ratio of CI, which helps to achieve a wider range of voltage gain at suitable duty cycles. However, such converters often suffer from voltage spike across the main switch that causes from the stored energy in leakage inductor of CI, which can be resolved with the help of clamp capacitors [3], [4]. Under some conditions, the leakage inductor can also provide soft-switching conditions as used in [5].

So far, many step-up topologies based on CI boost converter (CIBC) with extended output voltage have been proposed. In [4], [6]–[15], new types of step-up converters using CI along with VM and regenerative passive clamp capacitor have been suggested. In these converters, soft-switching conditions are achieved with the help of the leakage inductance of the CL. However, utilizing CI in series with the input source leads to

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Sara Hasanpour is with the Department of Electrical Engineering, Ramsar Branch, Islamic Azad University, Ramsar 4691966434, Iran (e-mail: s.hasanpour@iauramsar.ac.ir).

Yam P. Siwakoti is with the Faculty of Engineering and Information Technology, University of Technology Sydney, Sydney 2007, Australia (e-mail: yam.siwakoti@uts.edu.au).

Ali Mostaan is with the Department of Electrical Engineering, Iranian Central Oil Field Company, Tehran 3354451048, Iran (e-mail: ali_8457@yahoo.com).

Frede Blaabjerg is with the Department of Energy Technology, Aalborg University, 9220 Aalborg, Denmark (e-mail: fbl@et.aau.dk).

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high input ripple due to the effect of the reflected current on the primary side of CI, which limits their applications in RES. In order to reduce the input current ripple, current-fed converters such as boost or SEPIC converters can be integrated with CIBC [5], [16]–[21]. In these structures using VMs, the voltage gain is higher than the conventional converters and also switching and reverse recovery losses are alleviated with the help of the leakage inductor.

Another solution to the further extension of voltage conversion range along with maintaining the input current with low ripple is the quadratic/cascaded boost and also hybrid boost structures [11], [22]–[28]. In these solutions, the voltage gain ratio is often improved as a quadratic or semiquadratic function. However, high voltage stress and high current stress are often the main disadvantages of these converters. In recent years, to improve the performance, these converters are combined with CI, clamp capacitors, and VM circuits. The use of a large number of components along with input current with high ripple are the main demerits of the hybrid high-gain converter with semiquadratic voltage gain as proposed in [11]. Moreover, a new coupled-inductor cascaded boost converter with lossless passive snubber has been suggested in [22]. However, the mentioned converter has demerits including the use of large number of components and also high switching and diode reverse recovery losses. Moreover, two types of hybrid quadratic boost structures are presented in [23] and [24], which can provide an ultra-high voltage gain with the use of a large number of passive components along with suffering high voltage stress on the main power switch. In [25] and [26], two new single-switch quadratic boost high step-up converters have been proposed. In these converters, despite high voltage stress on the main power switch, the voltage gain rate has not increased significantly. In high voltage gain hybrid cascaded connect converters proposed in [27] and [28], due to the use of MOSFET in the middle stage of the circuit, high voltage and current stresses are applied to it.

Based on the above aspects, the objective of this paper is to present a new modified step-up converter (SQHSUCI) with ultra-high voltage gain like semi-quadratic function, continues input current with low ripple along with enough high-efficiency for application in the RES. The proposed converter is based on a hybrid cascade connection of a boost and a buck–boost converter as stacked coupled-inductor. The dual-switch structure with simultaneous operation of the proposed converter along with the use of a regenerative passive clamp capacitor leads to a significant reduction in the voltage stress on the main power switch. To further improve the converter efficiency, quasi-resonance operation between the leakage inductor of the CI and middle capacitors of the converter is applied.

The remainder of this article is organized as follows. The proposed converter operation is described in Section II. After steady-state and efficiency analysis in Section III, DCM performance analysis is given in Section IV. Comparison with other related converters is discussed in Section V. Design considerations are given in Section VI. Experimental results are shown in Section VII. Finally, Section VIII concludes the article.

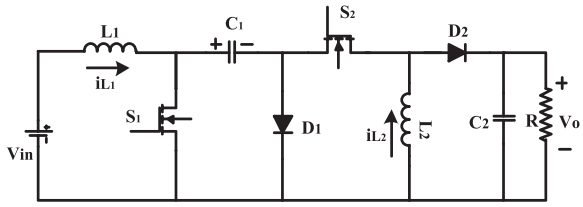

Fig. 1. Cascade connection between boost and buck–boost converters [29].

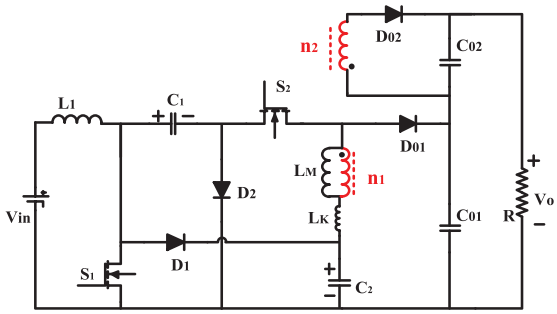

Fig. 2. Schematic of the proposed SQHSUCI.

II. Description of the Proposed SQHSUCI Operation

A cascade connection between boost and buck–boost converters is shown in Fig. 1 [29]. This converter with low voltage stress on the main power MOSFET and continuous input current can provide a step-up/down conversion ratio as follows:

$$M_{\mathrm{CCM(ideal)}} = \frac{D}{(1-D)^2}. \tag{1}$$

Here, D is the duty cycle of switches. Although the voltage gain of this converter is a quadratic function, it does not have a high voltage conversion ratio. For example, under large duty cycle $D = 0.65$, the ideal voltage gain of this converter is $M = 5.3$. However, due to the low voltage level of the RES, a step-up converter with an ultra-voltage gain is often necessary. As mentioned, the use of CI is a simple, effective, and proper technique to achieve a wide voltage conversion ratio without increasing the duty-cycle of the converter.

Fig. 2 shows the equivalent circuit of the proposed SQHSUCI, which is a modified structure of the converter in Fig. 1. In the proposed converter to further increase the voltage gain ratio, the secondary side of CI is stacked at the output. The proposed SQHSUCI consists of two power switches (S_1 and S_2) with simultaneous operation, an input inductor (L_1), a CI, four diodes (D_1, D_2, D_{01}, and D_{02}), and four capacitors (C_1, C_2, C_{01}, and C_{02}). In this converter, a regenerative passive clamp capacitor C_2 is used to reduce the voltage stress of the main power switch and increase the voltage gain ratio. In addition, because of the presence of quasi-resonant operation (QRO) among the leakage inductance of the CI, C_1, and C_2, the current shape of the MOSFETs S_1 and S_2 along with the output diode D_{02} has a sinusoidal form. This reduces the switches' turn-OFF losses and eliminates the reverse recovery loss in this diode.

To simplify the steady-state analysis of the SQHSUCI, some assumptions are made as follows.

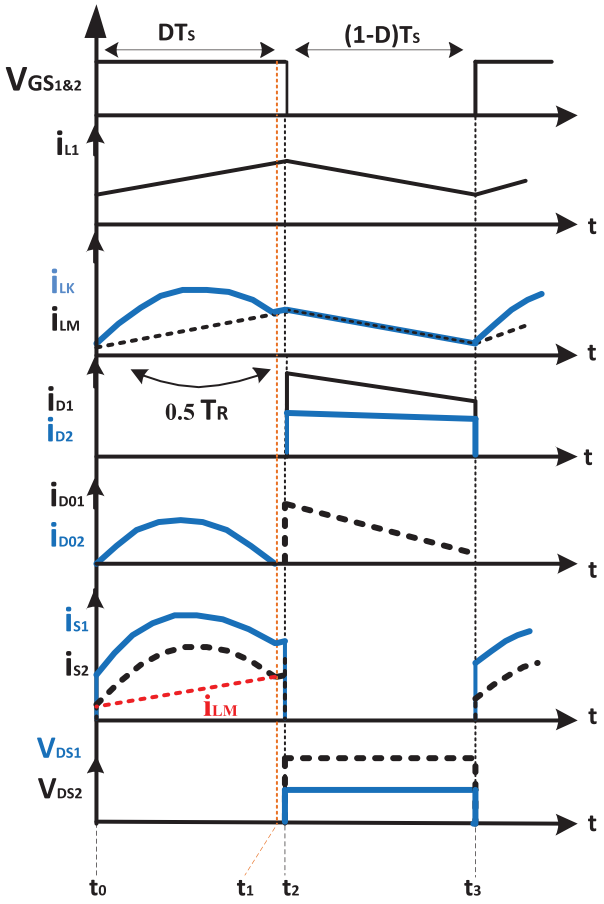

Fig. 3. Key steady-state waveforms of the proposed SQHSUCI during the different time phases.

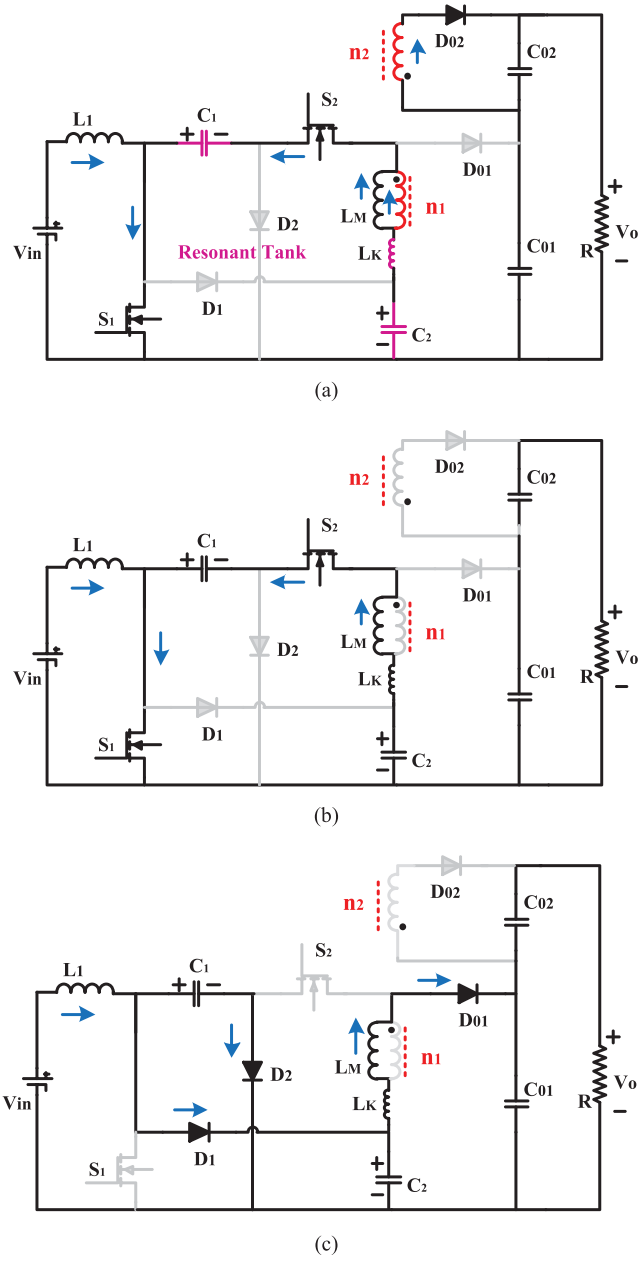

Fig. 4. Current flow path of the proposed SQHSUCI during one switching period under CCM operation: (a) Mode *I* $[t_0 - t_1]$, (b) Mode *II* $[t_1 - t_2]$, and (c) Mode *III* $[t_2 - t_3]$.

1) All converter semiconductor components are considered ideal.
2) All capacitors are large enough, so their voltages are assumed to be nearly constant during one switching cycle, so their voltage ripples are neglected.
3) The CI is modeled with a magnetizing inductor (L_m) and a merged leakage inductor (L_k) at the primary side with a coupling-coefficient $k = L_m/(L_m + L_k)$ and turns ratio $n = n_2/n_1$.
4) The input inductor and magnetizing inductor are considered large enough, so their current ripples are neglected.

Theoretical key waveforms of the components voltages and currents of the proposed converter under continuous conduction mode (CCM) for one switching cycle are depicted in Fig. 3. Moreover, the proposed SQHSUCI has three operating modes in each switching cycle as is shown in Fig. 4(a)–(c).

Mode I $[t_0 < t < t_1]$**:** At $t = t_0$, the power switches S_1 and S_2 begin to conduct simultaneously, and diode D_{02} is in turn-ON state. At the same time, diodes D_1, D_2, and D_{01} are reverse-biased by V_{C1}, V_{C2}, and $V_{C1} - V_{C01}$, respectively. The current-flow path of the SQHSUCI in this mode is shown in Fig. 4(a). The input inductor L_1 receives energy from the input voltage source V_{in} through S_1, then its current increases linearly. In this mode, the converter operates in QRO with the help of the leakage inductance on the primary side of the CI (L_K) and the balancing (C_1) and clamp (C_2) capacitors. With the help of this resonant tank, the currents of the power switches S_1 and S_2 and also diode D_{02} increase in the sinusoidal form. This results in a significant reduction in the turn-OFF state losses of the power switches as well as alleviate reverse recovery loss of the diode D_{02}. Since the voltages of capacitors C_1 and C_2 $(V_{C1} + V_{C2})$ are applied to the magnetizing inductor, its current increases linearly. On the other hand, the output capacitor C_{02} received energy from the leakage inductor and also balancing (C_1) and clamp (C_2) capacitors through CI and D_{02}. In addition, the output capacitor C_{01} supplies the output load in series. The resonant frequency

can be found using the following equations:

$$V_{L1} = V_{\text{in}} \tag{2}$$

$$V_{LM} = k(V_{C1} + V_{C2}) \tag{3}$$

$$i_{S2} = i_{Lk} \tag{4}$$

$$i_{S1} = i_{Lk} + i_{L1} \tag{5}$$

$$f_R = \frac{1}{T_R} = \frac{1}{2\pi\sqrt{L_k \frac{C_1 C_2}{C_1 + C_2}}}. \tag{6}$$

Here, k and f_R are the coupling-coefficient of the leakage inductance and resonant frequency, respectively. To ensure the resonant operation in the SQHSUCI, the resonant frequency should be higher than the switching frequency $(f_R > fs)$ of the converter.

Mode II [$t_1 < t < t_2$]: This transition time interval starts at the instant $t = t_1$ when QRO is finished and the current of the output diode D_{02} naturally reaches zero without reverse recovery loss, as shown in Fig. 4(b). In this mode, the current passing through switch S_1, leakage inductor (i_{Lk}), and magnetizing inductor (i_{LM}) are identical. The currents of the magnetizing and input inductors are increased, which is the same as Mode I. Moreover, the output load is supplied by the output capacitors C_{01}, C_{02}. The following equations can be written in this mode:

$$V_{L1} = V_{\text{in}} \tag{7}$$

$$V_{LM} = k(V_{C1} + V_{C2}) \tag{8}$$

$$i_{S2} = i_{LM} \tag{9}$$

$$i_{S1} = i_{LM} + i_{L1}. \tag{10}$$

Mode III [$t_2 < t < t_3$]: At the time $t = t_2$, switches S_1 and S_2 are turned OFF and diodes D_1, D_2, and D_{01} are forward-biased, simultaneously. During this time interval, as it is shown in Fig. 4(c), the energy of the input inductor is transferred to capacitors C_1 and C_2, so their current decreases linearly. Moreover, the voltage stress across the main power switch S_1 is clamped by the capacitors C_1 and C_2 in parallel. The output capacitor C_{01} is charged by the energy previously stored in the magnetizing inductor. Consequently, the currents of the magnetizing and the leakage inductors decrease linearly. It is noteworthy that, due to the low level of the magnetizing inductor current at the end of this mode, the output diode D_{01} will be switched OFF at minimum reverse recovery loss. The following equations are expressed in this mode:

$$V_{L1} = V_{\text{in}} - V_{C1} = V_{\text{in}} - V_{C2} \tag{11}$$

$$V_{LM} = k\left(V_{C1} - V_{C01}\right) \tag{12}$$

$$I_{D01} = I_{LK}. \tag{13}$$

The resonant operation in the proposed converter can occur in two ways including below resonance (BR) $(T_R/2 < DT_{\text{S}})$ and above resonance (AR) $(T_{\text{R}}/2 > DT_{\text{S}})$, the minimum values of the switching and diode reverse recovery losses occur in the critical mode operation $(T_R/2 \approx DT_S)$ of the converter, which will be investigated in the next subsection. In critical mode and nonresonant performances, the converter has two operating modes including, Modes I and III.

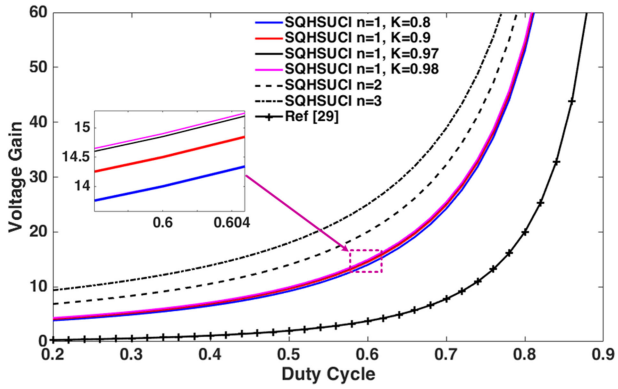

Fig. 5. Voltage gain of the proposed SQHSUCI versus duty cycle, various turns ratios of CI, and several coupling-coefficients compared to the converter in [29] (cascaded boost and buck–boost).

III. Steady-State Analysis of the SQHSUCI

A. Voltage Conversion Ratio in CCM

The time transition of Mode II in CCM operation is significantly short, which can be neglected. To simplify the steady-state analysis, all four assumptions made in Section II are considered. By applying the inductor volt–second balance principle for the input inductor (L_1), the voltage of the middle capacitors C_1 and C_2 is achieved as

$$V_{C1} = V_{C2} = \frac{V_{\text{in}}}{1 - D} \tag{14}$$

where D is the duty cycle of the power switches S_1 and S_2. On the other hand, from the volt–second balance for the magnetizing inductors (L_M), the output semistage voltage gains in CCM are expressed as follows:

$$V_{C01} = \frac{(1 + D)\, V_{\text{in}}}{(1 - D)^2} \tag{15}$$

$$V_{C02} = nk\left(V_{C1} + V_{C2}\right) = \frac{2nkV_{\text{in}}}{(1 - D)}. \tag{16}$$

Therefore, the static voltage conversion ratio of the proposed converter is achieved by adding (15) and (16) as follows:

$$M_{\text{CCM(ideal)}} = \frac{1 + D + 2nk\,(1 - D)}{(1 - D)^2}. \tag{17}$$

Fig. 5 shows the voltage gain ratio of the proposed converter versus duty cycle, several turns ratios of CI, and coupling-coefficients (k) compared to the converter in [29] (in Fig. 1). As it is shown in this figure, by applying the proposed technique, the voltage gain ratio of the SQHSUCI has increased significantly compared to the converter in [29] (Fig. 1). For example, in the proposed converter, if the value of $D = 0.65$ and $n = 1$ are selected, the ideal voltage gain is $M = 18.77$, that is, three and a half times than the converter in [29] (with $M = 5.3$ in $D = 0.65$). Moreover, it is clear that the small coupling coefficients ($k = 0.9$ and $k = 0.8$) of the leakage inductor can decrease the voltage gain ratio. However, for low power rates of CI, this coefficient is a higher value, which has no significant effect on the conversion ratio, and then it can be set at one ($k \approx 1$) in (17). Consequently, the ideal voltage conversion ratio of the proposed SQHSUCI is

expressed as

$$M_{\mathrm{CCM(ideal)}} = \frac{1 + D + 2n\,(1 - D)}{(1 - D)^2}. \tag{18}$$

Furthermore, as shown in Fig. 5, the voltage conversion ratio of the SQHSUCI is increased exponentially versus the duty cycle as semiquadratic form and proportionally versus the turns' ratio of CI. Consequently, the proposed converter is able to provide an ultrahigh-voltage conversion ratio.

B. Voltage Stresses on Semiconductors in CCM

Voltage stress is one of the important indicators of the converters to choose the proper components. In the proposed SQHSUCI, the maximum voltage stress on the main power switch S_1 is clamped by capacitors C_2 and C_1, simultaneously. Based on the previous calculations, the voltage stresses across switches S_1 and S_2 and diodes D_1, D_{01}, and D_{02} are obtained as follows:

$$V_{DS1} = \frac{V_{\mathrm{in}}}{1 - D} = \frac{(1 - D)\,V_o}{1 + D + 2n\,(1 - D)} \tag{19}$$

$$V_{DS2} = V_{CO1} = \frac{(1 + D)\,V_o}{1 + D + 2n\,(1 - D)} \tag{20}$$

$$V_{D01} = \frac{2V_{\mathrm{in}}}{(1 - D)^2} = \frac{2V_o}{1 + D + 2n\,(1 - D)} \tag{21}$$

$$V_{D02} = \frac{2nV_{\mathrm{in}}}{(1 - D)^2} = \frac{2nV_o}{1 + D + 2n\,(1 - D)}. \tag{22}$$

It is clear from (19)–(22) that the voltage stresses across semiconductors are inversely dependent on the turn's ratio of CI (n). Therefore, in a larger turn's ratio, the voltage stresses are reduced significantly.

C. Current Stresses of Semiconductors in CCM

Considering a lossless performance along with neglecting the current ripple of magnetic components in CCM operation, the average values of the input and magnetizing inductors currents are calculated as

$$I_{\mathrm{in}_{(\mathrm{AVG})}} = MI_o \tag{23}$$

$$I_{\mathrm{LM(AVG)}} = \frac{I_o}{1 - D} \tag{24}$$

where $M_{\mathrm{ideal}}^{\mathrm{CCM}}$ and I_o are the static voltage gain and the output load current, respectively. According to (24), the average current passing through the magnetizing inductor is not dependent on the turn's ratio of CI (n). This will result in a significant reduction in the CI core size. Moreover, the current stresses passing through the diodes are given by applying the ampere–second law on the capacitors C_{01} and C_{02} as

$$I_{D01\mathrm{MAX}} = \frac{I_O}{1 - D} \tag{25}$$

$$I_{D02\mathrm{MAX}} = \frac{\pi I_O}{2\mathrm{D}} \tag{26}$$

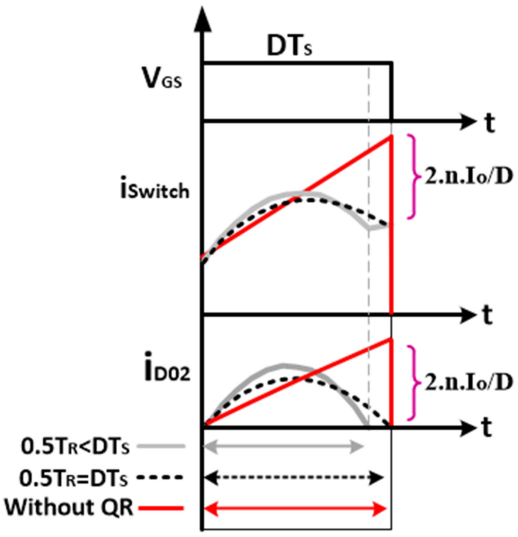

Fig. 6. Shape of current through the switch and the output diode D_{o2} in QRO mode.

$$I_{D1(\mathrm{MAX})} = \frac{(1 + nD)\,I_O}{(1 - D)^2} \tag{27}$$

$$I_{D2(\mathrm{MAX})} = \frac{(D + 2n - 3nD)\,I_O}{(1 - D)^2}. \tag{28}$$

Fig. 6 illustrates the current shape of the converter power switch along with output diode D_{02} under three states of resonance including without QRO, BR, and critical mode $(T_R/2 \approx DT_S)$. It is clear that due to the QRO effect, the current shape of output diode D_{02} has a sinusoidal form. As shown in this figure, the critical operation of the SQHSUCI eliminates the reverse recovery loss of the output diode along with reducing the switches turn-OFF loss by $2nI_o/D$. Consequently, the efficiency can be significantly improved. Considering critical mode operation and using (4), (5), (23), and (24), the maximum and root mean square (rms) values of switches current are calculated as

$$i_{S1}\,(\mathrm{t}) = MI_O + \frac{I_O}{1 - D} + \frac{\pi nI_O}{2\mathrm{D}}\sin\,(\omega_r t) \tag{29}$$

$$I_{S1(\mathrm{MAX})} = \frac{I_O}{1 - D} + \frac{\pi nI_O}{2\mathrm{D}} + MI_O \tag{30}$$

$$I_{S1(\mathrm{RMS})} =$$

$$I_O\sqrt{D.\left(\frac{2\,(1 + n - nD)}{(1 - D)^2}\right)^2 + \frac{(n\pi)^2}{8D} + \frac{4n\,(1 + n - nD)}{(1 - D)^2}} \tag{31}$$

$$i_{S2}\,(\mathrm{t}) = \frac{I_O}{1 - D} + \frac{\pi nI_O}{2\mathrm{D}}\sin\,(\omega_r t) \tag{32}$$

$$I_{S2(\mathrm{MAX})} = \frac{I_O}{1 - D} + \frac{\pi nI_O}{2\mathrm{D}} \tag{33}$$

$$I_{S2(\mathrm{RMS})} = I_O\sqrt{\frac{D}{(1 - D)^2} + \frac{2n}{1 - D} + \frac{(n\pi)^2}{8D}}. \tag{34}$$

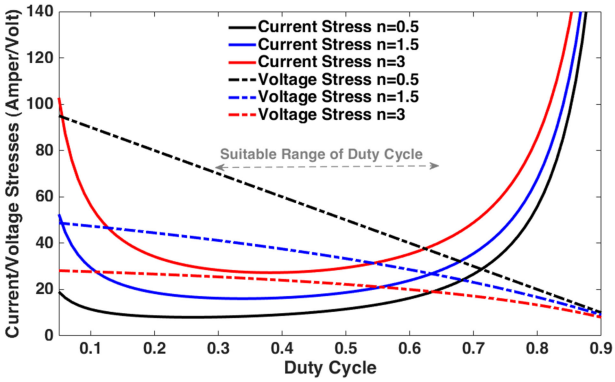

Fig. 7. Main power switch voltage and current stress comparison of the proposed SQHSUCI for $V_o = 200$ V and $P_o = 200$ W.

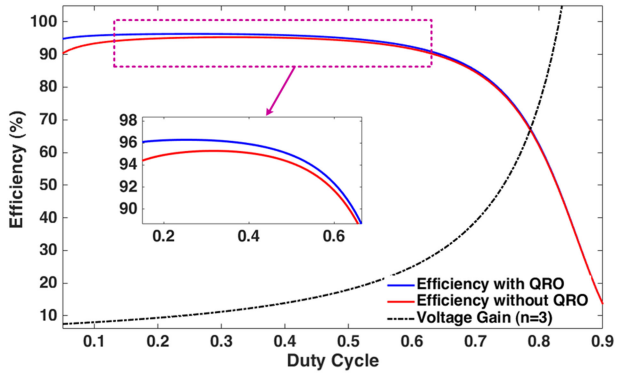

Fig. 8. Effect of QRO performance of the proposed SQHSUCI on efficiency improvement.

Also, the voltage and current stresses comparison of the main power switch of the proposed SQHSUCI under $V_o = 200$ V and $P_o = 200$ W is shown in Fig. 7. According to this figure, when the turn's ratio of the CI is increased, the voltage stress of the main power switch is decreased, while the current stress level is increased. Moreover, the suitable range of duty cycle to achieve the lower values of voltage and current stresses of the main switch is between $0.3 < D < 0.7$.

D. Analysis of Theoretical Efficiency

In practice, the presence of parasitic resistors in converter components including MOSFETs, magnetic devices, capacitors, and diodes are the main causes of power loss.

The power losses of MOSFETs are mainly divided into three main parts: turn-ON, turn-OFF, and conduction losses. The MOSFETs conduction losses of the proposed SQHSUCI are calculated as

$$P^{\text{Loss}}_{SW(\text{Cond.})} = R_{ds1(\text{ON})}.I^2_{s1(\text{RMS})} + R_{ds2(\text{ON})}.I^2_{s2(\text{RMS})}. \tag{35}$$

Here, $R_{ds(\text{on})}$ is the static drain-to-source ON-resistance. The turn-OFF and turn-ON state losses of the power MOSFETs S_1 and S_2, which are related to their drain to source voltage stresses, are estimated as

$$P^{\text{Loss}}_{SW(\text{NO})} = \frac{1}{2T_S}\left[I_{ds1(\text{on})}V_{ds1}t_{\text{on}1} + I_{ds2(\text{on})}V_{ds2}t_{\text{on}2}\right] \tag{36}$$

$$P^{\text{Loss}}_{SW(\text{off})} = \frac{1}{2T_S}\left[I_{ds1(\text{off})}V_{ds1}t_{\text{off}1} + I_{ds2(\text{off})}V_{ds2}t_{\text{off}2}\right] \tag{37}$$

where t_{off} and t_{on} are, respectively, the time of turn-OFF and turn-ON transition of the MOSFETs. In addition, $I_{ds1(\text{on or off})}$ and $I_{ds2(\text{on or off})}$ are the values of the MOSFETs current at the turn-ON or turn-OFF instants, respectively. As shown in Fig. 6, due to the QRO performance of the proposed converter, the current at the turn-OFF instants of the power MOSFETs is significantly reduced.

Considering the parasitic resistors of the converter magnetic components (L_1 and CI), the copper losses can be expressed as

$$P^{\text{Loss}}_{\text{Mag.(Copper)}} = r_{L1}I^2_{L1(\text{RMS})} + r_{LM}I^2_{LM(\text{RMS})}. \tag{38}$$

In addition, the power dissipation of body diode in the ON-state is related to the maximum forward drop voltage (V_F) and it is expressed as

$$P^{\text{Loss}}_{\text{Diode}} = V_F I_{D(\text{AVG})}. \tag{39}$$

It is noteworthy that the voltage drop of diodes increases at higher currents level. The equivalent series resistance (r_{esr}) causes losses in the capacitors that is expressed as follows:

$$P^{\text{Loss}}_{\text{Cap.}} = r_{\text{esr}}I^2_{C(\text{RMS})}. \tag{40}$$

Consequently, the theoretical efficiency of the SQHSUCI is found as

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}}. \tag{41}$$

The effect the QRO performance of the proposed SQHSUCI on efficiency improvement is demonstrated in Fig. 8. The values of converter parameters are assumed as follows: $V_{\text{in}} = 20$ V, $R = 700\ \Omega$, $r_{L1} = r_{LM} = 50$ mΩ, $f_s = 60$ kHz, $t_{d(\text{off})} = 50$ ns, $t_{d(\text{on})} = 20$ ns, $r_{ds1,2(ON)} = 18$ mΩ, $r_{D1} = r_{D01} = r_{D02} = 7$ mΩ, $r_{\text{esr}C1} = 25$ mΩ, $r_{\text{esr}C01} = r_{\text{esr}C02} = 250$ mΩ, $V_{F1} = V_{FO1} = V_{FO2} = 0.5$ V, and $n = 3$. It is clear that the resonant performance in the SQHSUCI can play an effective role in improving the converter efficiency. Moreover, the calculated efficiency and ideal voltage gain curves versus the duty cycle and different turn's ratio ($n = 3/1.5/0.5$) of CI are illustrated in Fig. 9. As it is shown, by increasing the duty cycles and turns ratio of CI, the converter efficiency is decreased. Moreover, due to the high voltage and current levels in high duty cycles, a sudden drop happens in converter efficiency, which limits the maximum power-handling capacity. This sudden drop in efficiency occurs in all high step-up converters, especially in the classical flyback converter. Reducing power losses along with increasing the voltage gain ratio in the proposed converter has led to high power-handling capacity.

IV. DCM Performance Analysis

A. Boundary Between CCM and DCM

Under some conditions, such as very light output load, switching frequency drop, and also small input inductor, the proposed

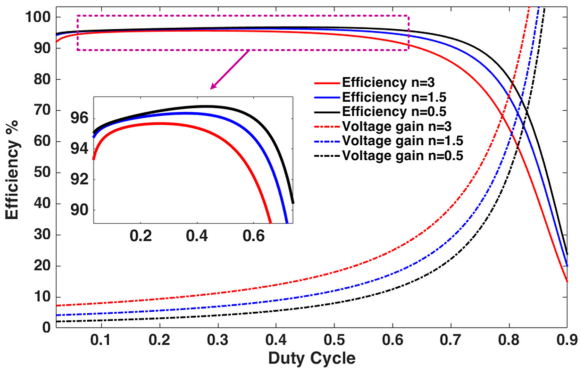

Fig. 9. Efficiency and ideal voltage gain versus the duty cycle and different turn's ratio of CI.

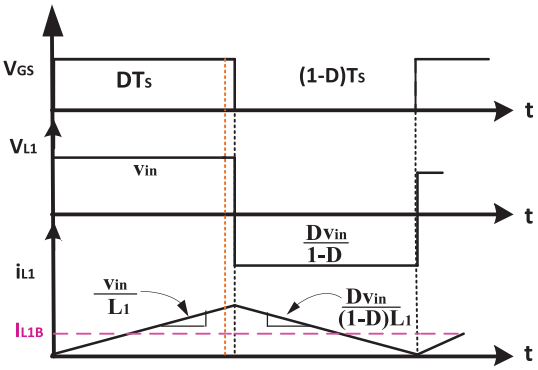

Fig. 10. Inductor voltage and current waveforms at the boundary of CCM/DCM mode.

converter inevitably operates in discontinuous conduction mode (DCM). In this condition, the current of the input inductor L_1 falls to zero before the next switching cycle and crosses from the boundary condition between CCM and DCM. The voltage and current of L_1 in boundary operation are illustrated in Fig. 10. The average value of the input current can be calculated as

$$I_{L1B} = \frac{V_{L1} D T_S}{2L_1}. \tag{42}$$

Here, subscript *B* represents the boundary condition. Substituting (11) and (18) into (42) leads to

$$I_{L1B} = \frac{V_o D(1-D)^2}{2L_1 f_s \left(1 + D + 2n\left(1-D\right)\right)}. \tag{43}$$

The boundary-value of the output load current can be derived from (43) as follows:

$$I_{OB} = \frac{V_o D(1-D)^4}{2L_1 f_s (1 + D + 2n\left(1-D\right))^2}. \tag{44}$$

Here, the normalized value of the output current in boundary condition is defined as follows:

$$\frac{I_{OB}}{\frac{V_o}{2L_1 f_s}} = \frac{D(1-D)^4}{\left(1 + D + 2n\left(1-D\right)\right)^2}. \tag{45}$$

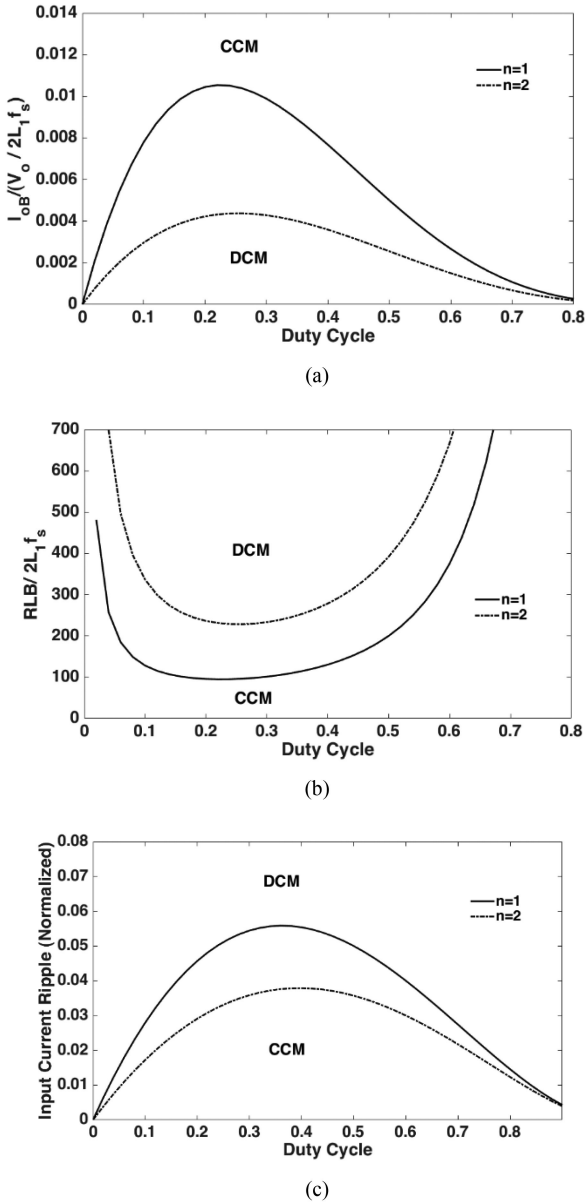

Fig. 11. Normalized (a) output load current, (b) output load resistance, and (c) input current ripple versus *D* and *n*.

Furthermore, the normalized value of the boundary load resistance (R_{LB}) can also be given as

$$\frac{R_{LB}}{2L_1 f_s} = \frac{\left(1 + D + 2n\left(1-D\right)\right)^2}{D(1-D)^4}. \tag{46}$$

Fig. 11(a) and (b) depicts the normalized values of the output current and load resistance versus D and n at the boundary condition. According to this figure, the maximum values of output load currents in the boundary of CCM/DCM are

$$I_{oB\mathrm{Max}} = \begin{cases} 0.01052 \frac{V_o}{2f_s L_{1\min}} & (D = 0.22,\ n = 1) \\ 0.00438 \frac{V_o}{2f_s L_{1\min}} & (\ D = 0.26,\ n = 2). \end{cases} \tag{47}$$

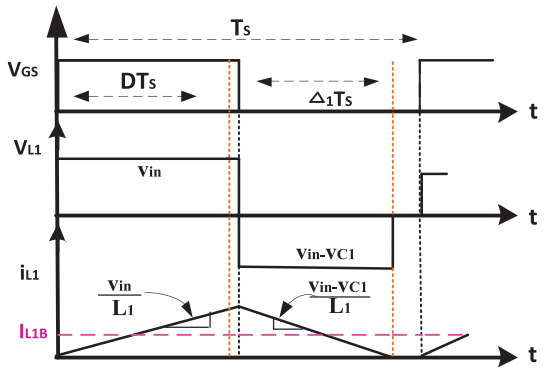

Fig. 12. Inductor voltage and current waveforms in DCM mode.

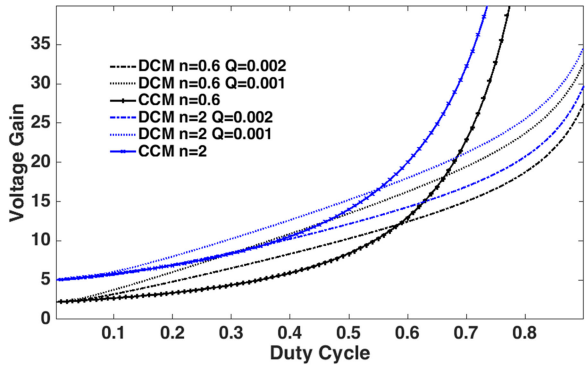

Fig. 13. Voltage gain comparison between DCM and CCM performance under various Q and *n*.

Thus, the minimum value of the input inductor required for guaranteeing CCM performance can be derived from

$$L_1 > L_{1\min} = \begin{cases} 0.00526\frac{R_L}{f_s} \ (D = 0.22,\ n = 1) \\ 0.00219\frac{R_L}{f_s} \ (D = 0.26,\ n = 2). \end{cases} \tag{48}$$

Also, the normalized input current ripple can be given as

$$\frac{\Delta i_{\text{in}}}{\frac{V_o}{L_1 f_s}} = \frac{D(1-D)^2}{1 + D + 2n\,(1-D)}. \tag{49}$$

The normalized value of the input current ripple curve is illustrated in Fig. 11(c). According to this plot, the input current ripple reduced with decreasing the turn's ratio of the CI.

B. DCM Operation

Key waveforms of the voltage and current of L_1 during DCM performance of the proposed converter are depicted in Fig. 12. Using the volt–second balance for the input inductor, time duration Mode III ($_1$) can be achieved as

$$DV_{\text{in}} + \Delta_1\,(V_{\text{in}} - V_{C1}) = 0 \tag{50}$$

$$\Delta_1 = \frac{DV_{\text{in}}}{V_{C1} - V_{\text{in}}}. \tag{51}$$

Also, the voltage of capacitor C_1 can be derived by applying the volt–second balance to the magnetizing inductor (L_m) as follows:

$$V_{C1} = \frac{1-\text{D}}{1+\text{D}} V_{01}. \tag{52}$$

Substituting (52) into (51) and rearranging result in

$$\Delta_1 = \frac{D\,(1+D)}{(1-D)\,M_{01} - 1 - D} \tag{53}$$

$$M_{01} = \frac{V_{01}}{V_{\text{in}}}. \tag{54}$$

Considering operating Mode I and using (52), the output semistage voltage gain in DCM is expressed as

$$M_{02} = \frac{V_{C02}}{V_{\text{in}}} = 2n\left(\frac{1-D}{1+D}\right) M_{01}. \tag{55}$$

The static voltage gain ratio of the proposed converter in DCM (M_{DCM}) is given by adding (54) and (55) as follows:

$$M_{\text{DCM}} = M_{01} + M_{02} = M_{01}\left(1 + 2n\left(\frac{1-D}{1+D}\right)\right). \tag{56}$$

The output semistage voltage gain as a function of total voltage gain in DCM can be given using (26) as follows:

$$M_{01} = \frac{M_{\text{DCM}}}{1 + 2n\left(\frac{1-\text{D}}{1+\text{D}}\right)}. \tag{57}$$

Regarding Fig. 12 and (2), the average value on the input current (equal to input inductor current) is written as

$$I_{\text{in}} = \frac{V_{\text{in}} D T_S}{2L_1}\,(D + \Delta_1)\,. \tag{58}$$

Substituting (51) into (58) and then rearranging, the voltage gain of the converter in DCM (M_{DCM}) as a function of D, n, and Q is obtained as (59), shown at the bottom of this page

$$Q = \frac{f_S L_1}{R}. \tag{60}$$

Fig. 13 shows the voltage gain comparison between DCM and CCM performance versus duty cycle and different values of Q and n. It is clear that the voltage gain ratio in DCM operation is highly dependent on the converter parameters (Q). For this reason, DCM performance is usually not recommended.

V. Comparison With the Other Related Converter Topologies

To justify the advantages of the proposed converter, some comparisons are provided in this section. Table I compares some

$$M_{DCM} = \frac{((1 + D + 2n - 2nD)\,Q) + \sqrt{((1 + D + 2n - 2nD)\,Q)^2 + 4Q\,(1-D)\,\frac{D^2}{2}\,(1-D)}}{2\,Q\,(1-D)} \tag{59}$$

TABLE I
COMPARISON BETWEEN THE PROPOSED SQHSUCI AND VARIOUS RELATED CONVERTERS

Converter Topology	No. of Components					Voltage Gain	L.I.C.R	Voltage Stress on Switches	Voltage Stress on Output Diodes	Efficiency 100watt,
	S	D	C	CI+L	T					
[5]	1	4	5	1+1	12	$\frac{(n+1)D+1}{1-D}+2n$	Yes	$\frac{V_o}{1+D+n(2-D)}$	$\frac{(1+n)V_o}{1+D+n(2-D)}$	95.5%
[6]	1	4	4	1+0	10	$\frac{2+(2-D)n}{1-D}$	No	$\frac{V_o}{2+(2-D)n}$	$\frac{(1+n)V_o}{2+(2-D)n}$	92.1%
[7]	1	4	4	1+0	10	$\frac{2+(1+D)n}{1-D}$	No	$\frac{V_o}{2+(1+D)n}$	$\frac{(1+n)V_o}{2+(1+D)n}$	95.8%
[8]	1	4	4	1+0	10	$\frac{2+(1+D)n}{1-D}$	No	$\frac{V_o}{2+(1+D)n}$	$\frac{(1+n)V_o}{2+(1+D)n}$	96.5%
[10]	1	6	6	1+0	14	$\frac{3+2n+nD}{1-D}$	No	$\frac{V_o}{3+2n+nD}$	$\frac{(1+n)V_o}{3+2n+nD}$	91.5%
[13]	1	4	4	1+0	10	$\frac{2+n}{1-D}$	No	$\frac{V_o}{2+n}$	$\frac{V_o}{2+n}, \frac{(1+n)V_o}{2+n}$	96.2%
[17]	1	4	5	1+1	12	$\frac{1+n(1+D)}{1-D}$	Yes	$\frac{V_o}{1+n(1+D)}$	$\frac{nV_o}{1+n(1+D)}$	96.7%
[18]	1	4	5	1+1	12	$\frac{1+n(1+D)}{1-D}$	Yes	$\frac{V_o}{1+n(1+D)}$	$\frac{V_o}{1+n(1+D)}, \frac{nV_o}{1+n(1+D)}$	97.0%
[20]	1	4	5	1+1	12	$\frac{2+n+D}{1-D}$	Yes	$\frac{V_o}{2+n+D}$	$\frac{(1+n)V_o}{2+n+D}$	95.2%
[22]	1	6	4	1+2	14	$\frac{1+nD}{(1-D)^2}$	Yes	$\frac{V_o}{1+nD}$	$\frac{(1+n)V_o}{(1+nD)}, \frac{(1+n(n+1+D))V_o}{n(1+n)(1+nD)}$	92.9%
[23]	2	6	6	1+1	16	$\frac{1+2n}{(1-D)^2}$	Yes	$\frac{V_o}{1+2n}, \frac{V_o}{1+2n}$	$\frac{nV_o}{1+2n}, \frac{nV_o}{1+2n}$	90.1%
[25]	1	5	4	1+1	12	$\frac{1+n}{(1-D)^2}$	Yes	$\frac{V_o}{1+n}$	$\frac{V_o}{1+n}, \frac{nV_o}{1+n}, \frac{nV_o}{1+n}$	91.8%
[27]	1	6	5	1+1	14	$\frac{2+n+nD}{(1-D)^2}$	Yes	$\frac{V_o}{2+n+nD}$	$\frac{(1+n)V_o}{2+n+nD}$	90.7%
[28]	1	5	4	1+1	12	$\frac{2+n}{(1-D)^2}$	Yes	$\frac{V_o}{2+n}$	$\frac{(1+n)V_o}{2+n}$	94.5%
Proposed converter	2	4	4	1+1	12	$\frac{1+D+2n(1-D)}{(1-D)^2}$	Yes	$\frac{V_o(1-D)}{1+D+2n(1-D)}, \frac{V_o(1+D)}{1+D+2n(1-D)}$	$\frac{2V_o}{1+D+2n(1-D)}, \frac{2nV_o}{1+D+2n(1-D)}$	96.1%

S=Switch, D=Diode, C=Capacitor, T=Total Device Count, L.I.C.R= Low Input Current Ripple

typical performance indicators, including component counts, static voltage gain, input current ripple, the voltage stress, and theoretical efficiency of the proposed SQHSUCI in comparison with related previously reported work.

Comparison results of voltage conversion ratio for various duty cycles and same turns ratio ($n = 2$) of the proposed topology and the other converters presented in Table I are depicted in Fig. 14. As it is shown in this figure, only the proposed SQHSUCI and converters in [10], [23], [27], and [28] have a higher voltage conversion ratio than the others for all ranges of duty cycles. However, achieving a wide voltage conversion ratio in the converters in [10], [23], and [27] requires the use of a large number of components. Also, high input current ripple is the other demerit of the converters in [10] and [27], which limits their applications in the RES.

Moreover, Fig. 15 indicates the normalized voltage stress across the main power switch that has a dominant power loss versus the duty cycle and same turns ratio ($n = 2$) of the converters introduced in the comparison shown in Table I. It can be seen that the voltage stress in the SQHSUCI along with converter in [10] are at the lowest level in comparison to the other converters. This allows to select MOSFET with lower *Rds(on)*. Also, despite the high voltage gain, the converter in [28] suffers from high voltage and current stresses on its single power switch and input diodes, respectively. According to Table I, under the same working point (20 V/200 V, $f_s = 50$ kHz, $P_{\text{out}} = 100$ W, and $n = 0.6$) and parasitic components (resistance and voltage drop), the proposed converter can demonstrate enough high efficiency against others. In fact, because of the QRO performance in the proposed converter, the switches turn-OFF and the output diode reverse recovery losses are alleviated.

In addition, higher voltage gain in the SQHSUCI as semiquadratic form leads to significantly reduced turns ratio and duty cycle. Consequently, the performance indicators of the proposed topology including voltage stresses, overall efficiency, power density, costs, and volume in magnetic component against the other related step-up topologies are improved in the same conditions.

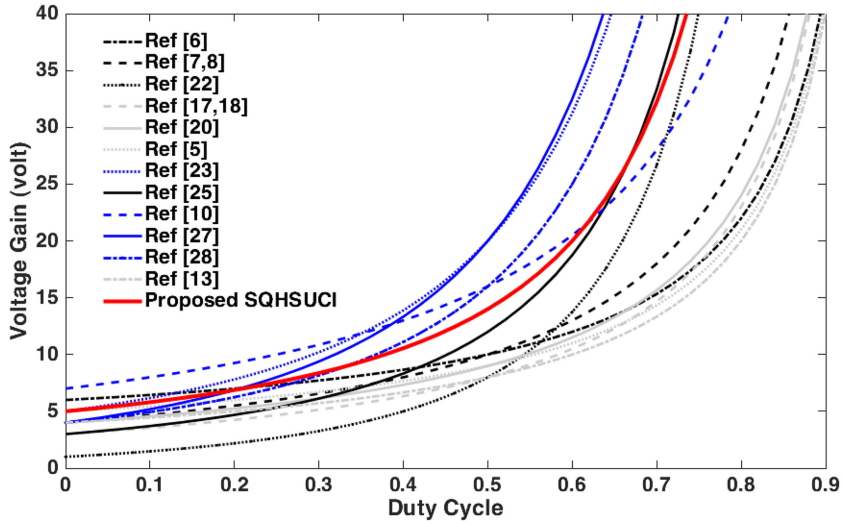

Fig. 14. Voltage gain comparison of the proposed SQHSUCI and various high step-up power converter structures introduced in Table I ($n = 2$).

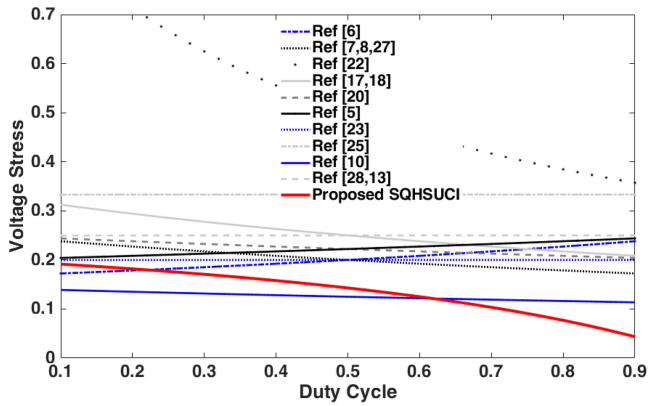

Fig. 15. Normalized voltage stress across main power switch of the high step-up converters introduced in Table I ($n = 2$).

VI. Design Considerations of the SQHSUCI for QRO Performance

The turn's ratio of the CI (n) is calculated using the static voltage gain (18) as follows:

$$n = \frac{M(1-D)^2 - 1 - D}{2(1-D)}. \tag{61}$$

Since the performance indicators, especially voltage and current stresses of the semiconductors of the SQHSUCI, are a function of D and n, then it is necessary to select these values appropriately. According to Fig. 7, the best choice for the duty cycle ranges to have the minimum current and voltage stress across the main power MOSFET is $0.3 < D < 0.7$.

Fortunately, because of the ultrahigh-voltage gain ratio in the proposed converter, it does not require the use of CI with a very large number of turn's ratio. According to Fig. 9, increasing the number of turn's ratio of the CI leads to a decrease in the efficiency of the converter.

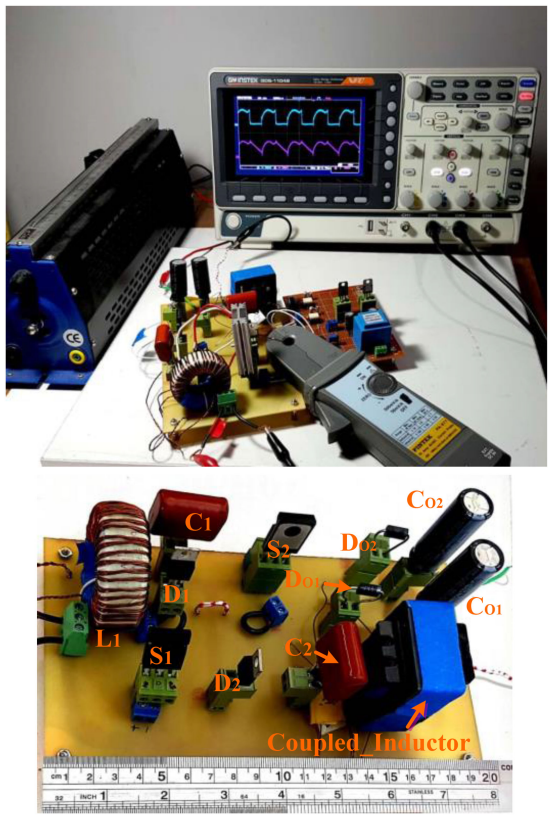

Fig. 16. Photographs of the proposed SQHSUCI prototype.

In order to guarantee the proper performance of the RES and extend their lifetime, it is better to extract continuously current from these sources with low ripple. By considering the maximum 20% allowable current ripple, the minimum value of the input inductor of the proposed SQHSUCI is obtained as follows:

$$L_1 = \frac{V_{\text{in}} D}{\Delta I_{L1} f_s} > \frac{V_{\text{in}} D}{20\% I_{L1} f_s} > \frac{RD}{20\% M^2 f_s} \tag{62}$$

where R and M are the output load and static voltage gain, respectively. Because the magnetizing inductor (L_M) of the CI is located in the middle stage of the circuit, there is no need to design it with a low current ripple. As a result, the value of the leakage inductor is also reduced significantly. Using (14) and (24), the minimum value of L_M can be written as

$$L_M = \frac{V_{LM} D}{\Delta I_{LM} f_s} > \frac{2V_{C1} D}{75\% i_{LM} f_s} > \frac{2RD}{75\% M f_s}. \quad (63)$$

Using the RMS values of the secondary side voltage and current of the CI, the Volt-Ampere (VA) rating of the CI can be obtained as

$$VA_{CI} = \frac{n\pi P_O}{1 + D + 2n(1-D)} \cdot \sqrt{\frac{(1-D)}{2}}. \quad (64)$$

Usually, parameter A_P (product of window winding area $\times$ cross-sectional area) is used for the proper selection of the magnetic core [30], where is defined as

$$A_P = \left[\frac{K_i . L . \hat{I}^2 . \sqrt{1+\gamma}}{B_{\max} . K_t . \sqrt{K_u \Delta T}} \right]^{\frac{8}{7}} 10^8 \quad (65)$$

where K_u is the window utilization factor, K_t is a constant value 48 200, γ is the ratio of iron loss to copper loss, $B_{\max}$ is the maximum flux density ($B_{\max} = 0.4$ for ferrite Mn–Zn), L is the inductance value, $\hat{I}$ is the peak current, K_i is the current waveform factor, and ΔT is the allowable temperature rise.

The output capacitors C_{01} and C_{02} are designed based on the allowable voltage ripple (usually 1% of V_{out}) and the output power as

$$C_{01} = \frac{P_{\text{out}}}{V_{\text{out}} \Delta V_{C01} f_s} > \frac{P_{\text{out}}}{V_{\text{out}} . 1\% . V_{C01} . f_s} \quad (65)$$

$$C_{02} = \frac{P_{\text{out}}}{V_{\text{out}} \Delta V_{C02} f_s} > \frac{P_{\text{out}}}{V_{\text{out}} . 1\% . V_{C02} . f_s}. \quad (66)$$

It should be noted that the electrolytic capacitors with higher rate of capacitance usually have less r_{esr}, so it is more desirable. The intermediate capacitors of the proposed converter C_1 and C_2 are based on their maximum current along with considering the critical mode operation $(TR/2 = DT_S)$ as

$$C_1 = C_2 = \frac{2I_0}{\Delta V_{C1}(1-D) f_s} > \frac{2DI_0}{(10 - 15\%) V_{C1}(1-D) f_s} \quad (67)$$

$$C_1 = C_2 = \left(\frac{D}{f_s \pi} \right)^2 \frac{2}{L_K}. \quad (68)$$

Moreover, the VA rating of the capacitors C_1 and C_2 are obtained as (69) and (70), shown at the bottom of this page.

TABLE II
SPECIFICATIONS OF THE IMPLEMENTED PROTOTYPE

Parameter	Values
Output Power(P_{out})	200 W
Input Voltage(V_{in})	20 V
Output Voltage(V_{out})	200 V
Switching Frequency(f_s)	50 kHz
Capacitors C_{01} , C_{02}	220 uF/250 V with r_{esr} = 0.15 Ω
Capacitors C_1, C_2	6.6 uF/4.7 uF 250 V with r_{esr} = 25 mΩ
Power Switches S_1,S_2	IRFB4227PbF with $R_{ds(ON)}$ = 19.7 mΩ, $t_{d(on)}$ = 33 ns, $t_{d(off)}$ = 21 ns
Input Inductor L_1	0.38 mH with r_{L1} = 60 mΩ
CI	EE42/21/15 n = 0.6
Magnetizing Inductor L_M	0.6 mH
Coupling Coefficient k	0.985
Diode D_{01} and D_{02}	MUR440/415 With Maximum V_F = 1.05/0.71 in 3 A
Diode D_1 and D_2	MBR10100 with maximum V_F=0.65 in 10 A

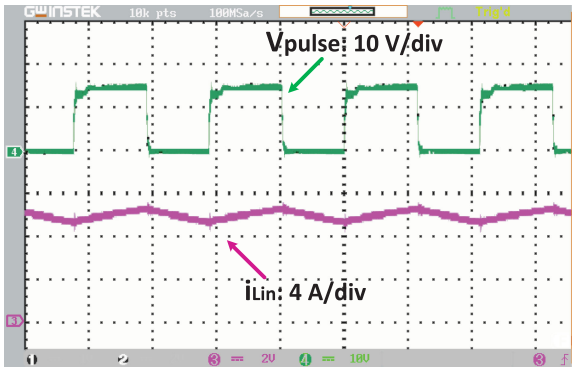

Fig. 17. Measured waveforms of the gate voltage and input inductor current i_{L1}.

VII. EXPERIMENTAL RESULTS

To further validate the theoretical analysis of the proposed SQHSUCI, a 200-W prototype is provided, as shown in Fig. 16. The values of different components of the implemented prototype are given in Table II. According to design consideration analysis, to achieve 200-V output voltage, $D = 0.55$ and $n = 0.6$ are considered. According to the CL current peak $(\hat{I} = 3\ A)$ and assuming $\gamma = 1, B_{\max} = 0.4$ (for ferrite Mn–Zn), $\Delta T = 15$, $K_i = 0.9$, and $K_u = 0.3$, the value of A_P to choose a proper core is about 2 cm^4. For this purpose, a ferrite core EE 42/21/15 is chosen for the CI in the prototype circuit. The experimental waveforms of the SQHSUCI prototype are depicted in Figs. 17–25.

The input inductor current waveform in the time domain is shown in Fig. 17, which is continuous with $i_{\text{Lin}} = 0.8$ A ripple

$$VA_{C1} = \frac{(1-D) P_o}{1 + D + 2n(1-D)} \sqrt{\frac{D}{(1-D)^2} + \frac{(n\pi)^2}{8D} + \frac{n}{1-D} + (1-D)\left(\frac{D + 2n - 3nD)}{(1-D)^2} \right)^2} \quad (69)$$

$$VA_{C2} = \frac{(1-D) P_o}{1 + D + 2n(1-D)} \sqrt{\frac{D}{(1-D)^2} + \frac{(n\pi)^2}{8D} + \frac{n}{1-D} + (1-D)\left(\frac{D(1+n)}{(1-D)^2} \right)^2} \quad (70)$$

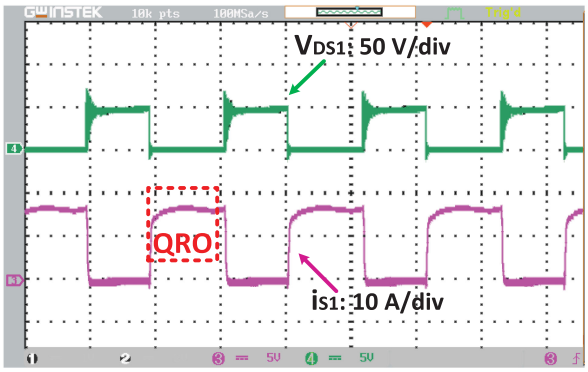

Fig. 18. Measured waveforms of the voltage and current of switch S_1.

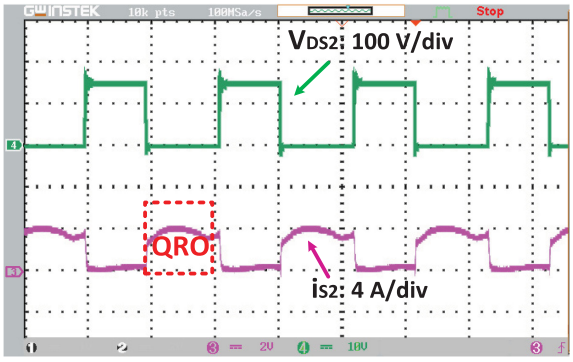

Fig. 19. Measured waveforms of the voltage and current of switch S_2.

Fig. 20. Measured waveforms of the voltage and current of diode D_1.

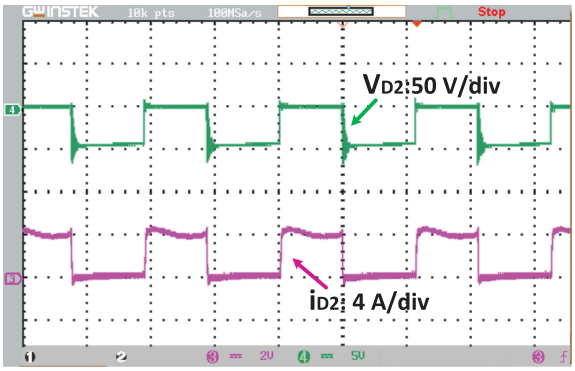

Fig. 21. Measured waveforms of the voltage and current of diode D_2.

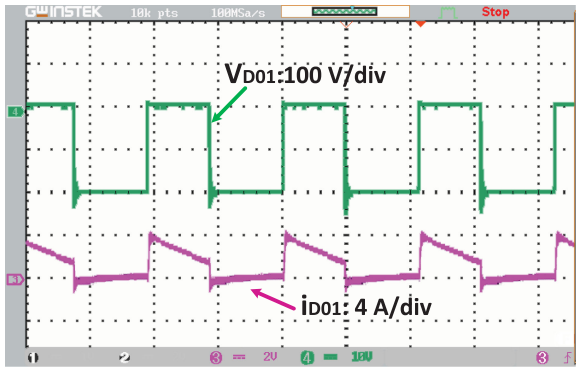

Fig. 22. Measured waveforms of the voltage and current of diode D_{o1}.

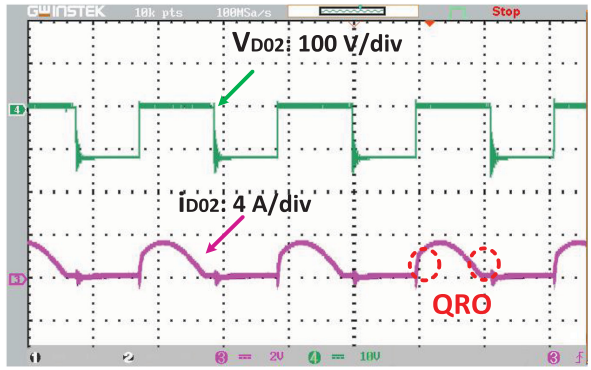

Fig. 23. Measured waveforms of the voltage and current of diode D_{o2}.

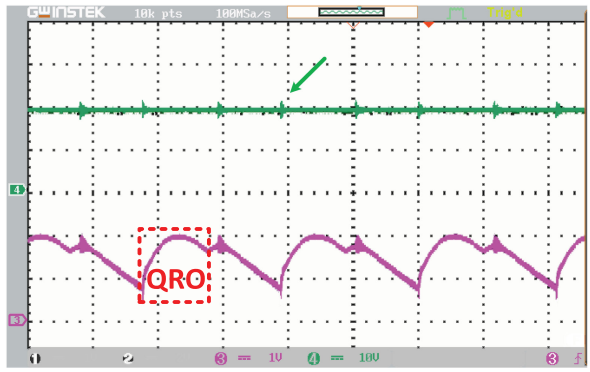

Fig. 24. Measured waveforms of the output voltage and leakage inductor current of the CI under output power 200 W and input voltage 20 V.

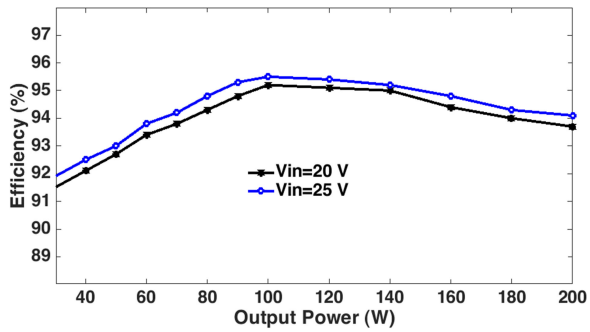

Fig. 25. Measured efficiency versus the output power.

(0.16% $I_{\rm in}$). The measured voltage and current stresses on the MOSFETs (S_1 and S_2) along with QRO area are depicted in Figs. 18 and 19. As it is shown, the voltage stresses across S_1 and S_2 are 45 and 149 V, respectively. Also, due to the QRO performance of the circuit, the turn-OFF current of the MOSFETs is reduced. Moreover, Figs. 20–23 show the experimental results of voltage and current stress of the converter diodes, which closely agrees with the theoretical analysis. According to these figures, the reverse recovery losses of the output diode D_{01} are significantly reduced. The waveforms of the output voltage and current of the leakage inductance of CI are also displayed in Fig. 24.

In addition, Fig. 25 shows the practical efficiency of the laboratory prototype at several output powers from 30 to 200 W under different input voltages $V_{\rm in} = 20$ V and $V_{\rm in} = 25$ V and the same output voltage $V_{\rm out} = 200$ V. The maximum efficiency of the SQHSUCI in 100 W and $V_{\rm in} = 25$ V is about 95.5%. By increasing the input voltage, the efficiency is improved. It can be seen that the proposed converter has an acceptable efficiency under various output voltages.

VIII. Conclusion

In this article, a new coupled-inductor high step-up converter with continuous input current has been proposed. The proposed topology can provide a high step-up voltage gain, and low input current ripple under low voltage spikes across the power components. Moreover, the design of a resonant tank in the converter has reduced switching and reverse recovery losses. In addition to the key role of the leakage inductor in the resonance performance, its stored energy is also transferred to the output capacitor. The operation principle, the steady-state analysis, and the merits of the proposed converter against the other related converters are discussed in detail. Experimental results of a laboratory prototype at 200 W with 20 V input voltage and 200 V output voltage proved the feasibility of the proposed converter. According to all the aforementioned features, the proposed converter is a competitive option in renewable energy applications.

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Sara Hasanpour was born in Iran, in 1979. She received the B.S. degree in electronic engineering from Azad Islamic University, Lahijan Branch, Iran, in 2002, the M.S. degree from the Isfahan University of Technology, Isfahan, Iran, in 2005, and the Ph.D. degree in power electronics engineering from the University of Guilan, Rasht, Iran, in 2019.

She is currently an Assistant Professor with Azad Islamic University, Ramsar Branch, Ramsar, Iran. Her major research interests include design and implementation of step-up/step-down switch-mode dc/dc converters with high-power density, renewable energy technologies, control and modeling of switched-mode dc/dc converters, and electronic ballasts.

Dr. Hasanpour received the Best Ph.D. Thesis Award in power electronics engineering in Iran, awarded by the Power Electronics Society of Iran, 2020.

Yam P. Siwakoti (Senior Member, IEEE) received the B.Tech. degree in electrical engineering from the National Institute of Technology, Hamirpur, India, in 2005, the M.E. degree in electrical power engineering from the Norwegian University of Science and Technology, Trondheim, Norway, and Kathmandu University, Dhulikhel, Nepal, in 2010, and the Ph.D. degree in electronic engineering from Macquarie University, Sydney, Australia, in 2014.

He was a Postdoctoral Fellow with the Department of Energy Technology, Aalborg University, Denmark, from 2014 to 2016. He was a Visiting Scientist with the Fraunhofer Institute for Solar Energy Systems, Freiburg, Germany, from 2017 to 2018. He is currently a Senior Lecturer with the Faculty of Engineering and Information Technology, University of Technology Sydney, Australia.

Dr. Siwakoti is a recipient of the prestigious Green Talent Award from the Federal Ministry of Education and Research, Germany, in 2016. He serves as an Associate Editor of three major journals of IEEE (IEEE TRANSACTIONS ON POWER ELECTRONICS, IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, and IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS), and the *IET Power Electronics*. He is also a peer-review College Member of Engineering and Physical Science Research Council (EPSRC), UK.

Ali Mostaan was born in Iran, in 1979. He received the B.S. degree in electrical engineering from the Iran University of Science and Technology, Tehran, Iran, in 2003, and the M.S. degree in electrical power engineering from the University of Guilan, Rasht, Iran, in 2013.

His research interests include power electronic converters topologies, modeling, and control.

Mr. Mostaan is a frequent reviewer of the IEEE TRANSACTION OF INDUSTRIAL ELECTRONICS, the IEEE TRANSACTION ON POWER ELECTRONICS, the IEEE INDUSTRIAL ELECTRONICS MAGAZINE, and the *IET Power Electronics*.

Frede Blaabjerg (Fellow, IEEE) received the Ph.D. degree in electrical engineering from the Aalborg University, Denmark, in 1995.

He was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. He was an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998, with the Aalborg University. From 2017, he became a Villum Investigator. He is honoris causa at University Politehnica Timisoara (UPT), Romania, and Tallinn Technical University (TTU) in Estonia. He is the author or co-author of more than 600 journal papers in the fields of power electronics and its applications. He is the co-author of four monographs and editor of ten books in power electronics and its applications. His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics, and adjustable speed drives.

Dr. Blaabjerg has received 32 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014, the Villum Kann Rasmussen Research Award 2014, and the Global Energy Prize in 2019. He was the Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS, from 2006 to 2012. He has been a Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007, and for the IEEE Industry Applications Society from 2010 to 2011 as well as from 2017 to 2018. In 2019–2020, he serves as the President of IEEE Power Electronics Society. He is the Vice-President of the Danish Academy of Technical Sciences too. He was nominated in 2014–2018 by Thomson Reuters among the 250 most cited researchers in engineering all over the world.