Measuring and Separating Conducted Three-Wire Emissions From a Fault-Tolerant, NPC Propulsion Inverter With a Split-Battery Using Hardware Separators Based on HF Transformers

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***Abstract*—Conducted emissions on the traction battery's power cables in EVs must be limited to avoid unwanted electromagnetic interference (EMI). When designing an EMI filter, it is advantageous to have information of the common mode (CM) and differential mode (DM) noise levels. This article deals with the measurement and separation of the dc side's three-wire DM/CM noise of a fault-tolerant three-level neutral-point-clamped (NPC) inverter with a split-battery system. Two hardware separators, based on small-circuit highfrequency transformers, were developed to identify the dc side's CM, line-DM, and phase-DM noise levels. Their characterized CM and DM rejection ratios for the frequency range from 150 kHz to 110 MHz are at least −33 and −21 dB, respectively. The separated noise of the NPC inverter was measured, using an inductive load, when operating the inverter with three-level and two-level modulation, resembling normal operation and a possible operation under fault, respectively. A simple three-wire CM model of the used testbed and the DM power module oscillation were derived to validate the separated noise's resonance peaks/valleys. It has been seen that the CM noise is dominant, especially below 10 MHz, except for the power module oscillations. Furthermore, when using the two-level modulation, in the case of a clamping diode fault, the noise levels are increased by about 3 dB.**

***Index Terms*—Common mode (CM), differential mode (DM), electromagnetic compatibility, electromagnetic emissions (EME), electromagnetic interference (EMI), neutral-point-clamped (NPC) inverter, noise measurement.**

Manuscript received November 8, 2019; revised February 18, 2020 and May 3, 2020; accepted May 29, 2020. Date of publication June 7, 2020; date of current version September 4, 2020. This work was supported by the Swedish Energy Agency and the German Federal Ministry of Education and Research (BMBF, support code 16EMO0176). This paper was presented in part at the IEEE Transportation Electrification Conference and Expo, Detroit, MI, USA, June 2019. Recommended for publication by Associate Editor J. Biela. *(Corresponding author: Anton Kersten.)*

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Digital Object Identifier 10.1109/TPEL.2020.3000586

I. Introduction

IN MODERN electric vehicles, the proper functioning of all electronic devices must be ensured to guarantee an adequate and safe operation of the entire vehicle. The propulsion inverter, as the most powerful component, bears a high risk of electromagnetic interference (EMI) with other onboard or surrounding devices. Therefore, potential sources of electromagnetic emissions (EME) should be identified and mitigated during an early stage of the inverter's and the system's design process to reduce radiated and conducted emissions before applying shielding and filters. Standards, for example, CISPR 25 [2], MIL-STD-461 [3], or SAE J1113/41 [4], classify electric drivetrains by the noise levels on dc-power cables. However, the mentioned standards do not distinguish between common mode (CM) and differential mode (DM) quantities, whereas these are beneficial for the application of effective noise mitigation techniques, as, for example, EMI filters.

Due to increased voltage and current slew rates, wide-bandgap semiconductor converters can achieve high switching frequencies ($f_{\mathrm{sw}} >> 20\,\mathrm{kHz}$) while maintaining a high propulsion inverter efficiency ($\eta > 98\%$) [5]. The drawback is increased EME [6]–[11]. This makes the design of EMI filters, particularly for high nominal dc-link voltages of 800 V, for EVs very challenging [12]. In comparison to two-level inverters, multilevel inverters reduce conducted emissions due to a reduced output voltage swing [13]–[16], while maintaining a lower current THD [17]. Therefore, multilevel inverters are gaining in interest within the field of vehicle propulsion applications [18]–[20]. One of them is the three-level neutral-point-clamped (NPC) inverter [21]. Its neutral point potential is usually formed by a capacitive voltage divider and an unbalance of the dc-link voltages by the low-order harmonics, including the dominant third harmonic [22], should be mitigated [23], [24], especially at a low speed. For example, a high torque demand at low-speed operation (e.g., climbing a curb) can quickly drain one capacitor. The fault-tolerant, three-level NPC inverter, described in [25], utilizes a dual battery pack with two series-connected battery modules. Through an additional connection of the capacitors' to

the battery modules' midpoint, the capacitor voltages are not just tied to the battery modules' voltages, the topology also allows for a fault-tolerant operation of the power train in the case of single semiconductor faults, referred to as a "limp home" mode [25].

However, the additional neutral point connection forms a unique three-wire dc source, whereas the test procedures and limitations, stated in CISPR 25 [2], are usually applied to single dc sources (two-wire), requiring only two line impedance stabilization networks (LISNs) for the measurement of conducted emissions [26], [27]. Furthermore, the classical two-wire CM and DM consideration, as described in [9], cannot be applied to localize CM/DM resonances. Several solutions for hardware separators, utilizing passive or active circuitry like operational amplifiers, can be found in [9], [28]–[33]. Anyhow, these are either used for common two-level inverters [9], [28], [29] or for ac appliances (ac side) [30]–[33], typically regulated by CISPR 14-1 [34]. Thus, the question arise: How to measure and separate the noise levels of the three-wire dc side of the fault-tolerant NPC inverter in accordance to CISPR 25?

Therefore, this article shows how to measure the conducted emissions of the fault-tolerant NPC inverter according to CISPR 25 [2], using three LISNs, and the noise separation of the three-wire CM/DM is explained. Additionally, two compact hardware CM/DM separators, based on small-circuit HF transformers, for the CM, line-DM, and phase-DM noise levels were developed and characterized. A test setup with an artificial machine load and an NPC prototype inverter are used for measurements. The characteristic resonances of the test setup are modeled and the inverter is operated with three-level and two-level modulation, resembling normal operation and operation under an open-circuit fault of a clamping-diode, respectively.

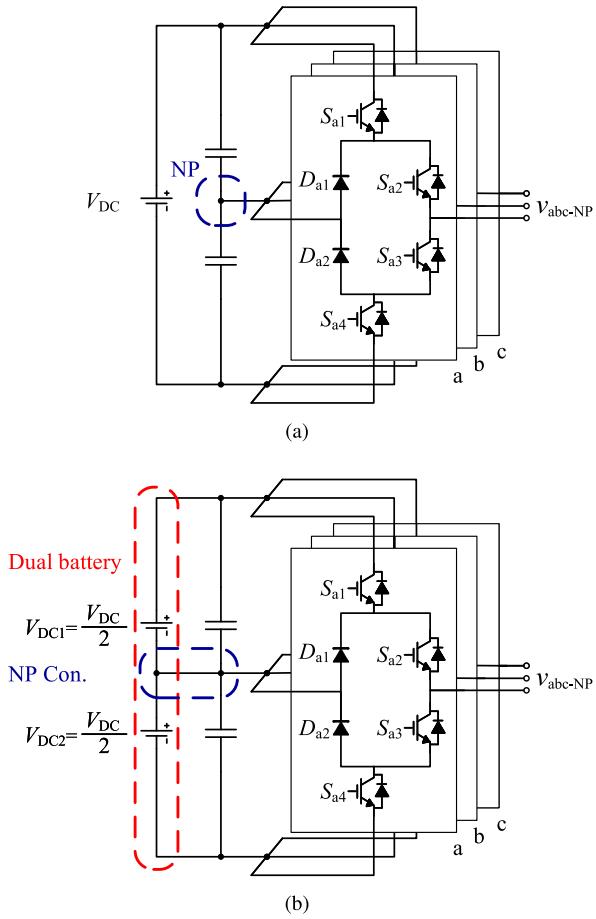

Fig. 1. Common three-level NPC inverter (a) without and (b) with additional NP connection including a split-battery [25].

II. NPC Inverter With Neutral Point Connection

Commonly, the three-level NPC inverter is supplied by a single dc source, as can be seen in Fig. 1(a) [21]. Each capacitor has a nominal voltage rating equal to half of the full dc-link voltage. The switches are usually operated in pairs, so that each phase has three valid switching states, which results in an instantaneous phase output voltage as

$$v_{\mathrm{abc-NP}}(S) = \frac{V_{\mathrm{DC}}}{2} S \quad \text{with} \quad S = \{1, 0, -1\}\,. \tag{1}$$

Thus, transforming all valid 27 switching combinations into the $\alpha\beta$-plane, the space vector diagram, as depicted in Fig. 2(a), is obtained. Space vector modulation (SVM) is a common approach to synthesize the reference output voltage by the time average of the three nearest vectors over one switching period [35]. As can be seen, the zero vector and each small vector have three or two valid switching states, respectively. Only the medium and large vectors do not have any redundancy. Using the zero switching state $S = 0$ in any phase (small or medium vectors) leads to a current flowing into the neutral point of the dc-link capacitors that closes through the positive and the negative dc-link rail [22]. Thus, the neutral point current contains a substantial third-harmonic component, which can lead to an oscillation of the capacitor voltages, so that a switch can be exposed to a higher voltage than under nominal conditions. A proper selection of the small vectors must be ensured to keep the dc-link capacitors balanced. Several modulation techniques can be found in the literature [24], [35], and [23] to mitigate these oscillations. However, the adaption of the modulation technique typically comes with the cost of increased switching losses [23], [24], although it is also possible to balance the capacitor voltages over several switching cycles without adding additional switching events. Fig. 2(b) and (c) depicts, for instance, the voltage synthesis in Region II, equally sharing the medium vector time intervals, as implemented in Plexim's software tool PLECS [36]. Consequently, in the case of an inverter fault, as an open- or a short-circuit switch fault, the valid space vectors would be compromised and the capacitor voltages would diverge without being balanced any longer. Thus, the neutral point would shift either to the positive or negative potential and the inverter's controllability would be lost [25].

A neutral point connection to a dual battery system, sometimes also referred to as a split-battery system [37], as shown in Fig. 1(b), ties the capacitor voltages to the battery potentials. Thus, another low impedance path through the battery packs is provided for the third harmonic component. Thereby, the low-frequency voltage swing of the neutral point is eliminated and in the case of a single-inverter switch fault, as described in [25], the drive train can still be operated with limited power,

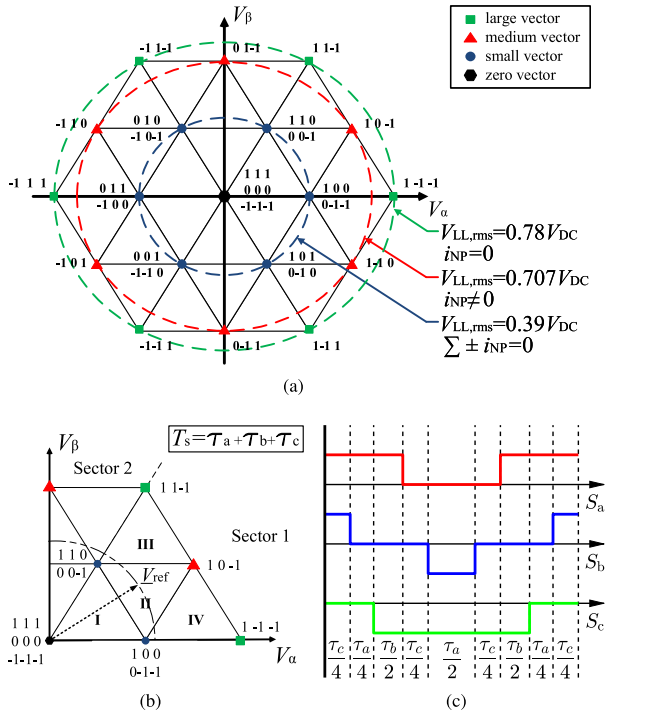

Fig. 2. (a) Three-level SVM diagram in the $\alpha\beta$-plane and (b) voltage synthesis in Region II with (c) equal usage of redundant small vectors to reduce the neutral point current.

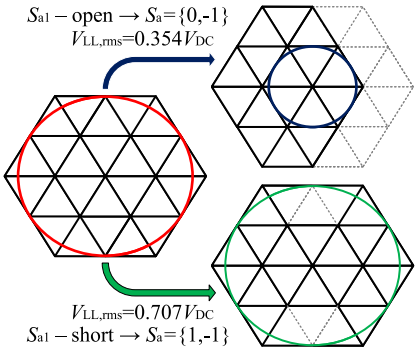

Fig. 3. Fault-tolerant operation of NPC inverter: adaption of valid space vectors in case of an open- or short-circuit fault of semiconductor switch S_{a1}.

referred to as a limp home mode. For example, Fig. 3 depicts the remaining valid space vectors in the case of an open- or a short-circuit fault of a semiconductor valve S_{a1}. It can be seen that the maximum output voltage is not affected in the case of a short-circuit fault and only phase a must be operated in two-level modulation according to

$$v_{a-NP}(S) = \frac{V_{DC}}{2} S \quad \text{with} \quad S = \{1, -1\}. \tag{2}$$

In the case of an open-circuit fault, the maximum output voltage is halved and all phases must be operated in a single source operation according to

$$v_{abc-NP}(S) = \frac{V_{DC}}{2} S \quad \text{with} \quad S = \{0, -1\}. \tag{3}$$

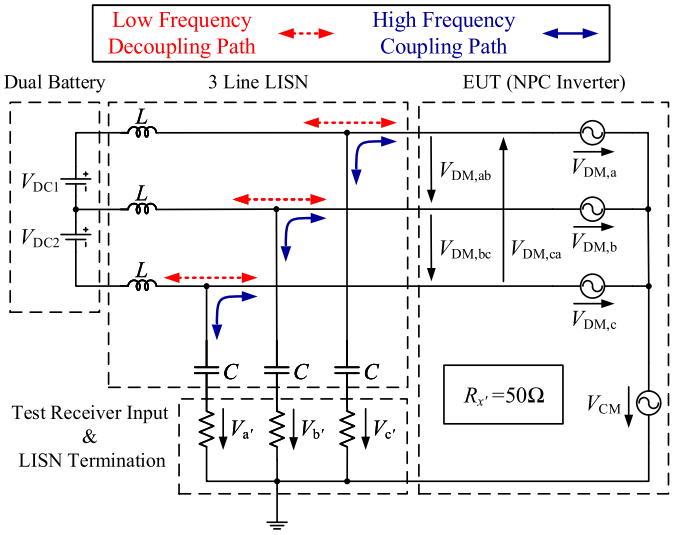

Fig. 4. Schematic of the noise measurement for the NPC inverter, including three LISNs. The LC-filter couples the high frequency noise of the EUT into the measurement receiver.

A detailed analysis about the fault tolerance of the NPC inverter with a neutral point connection can be found in [25].

III. Three-Wire Noise and CM and DM Separators

Since the three-level NPC inverter, as shown in Fig. 1(b), is supplied by a dual battery with a connected neutral point, the dc side cannot be considered as a classical two-wire inverter system. Thus, it must be dealt with a three-wire or three-phase CM/DM system, depicted in Fig. 4 as the equipment under test (EUT). The definition and separation of three-phase DM/CM quantities are already known from classical three-phase ac systems, as, for example, described in [30]–[32] and [33]. The corresponding standard CISPR 14-1 [34] regulates the conducted EMI within the frequency range from 150 kHz to 30 MHz. Hence, for the noise measurement according to CISPR 25 [2], three LISNs, often referred to as a special type of artificial mains network (AMN), must be inserted between the split battery and the dc-link capacitors' terminals of the NPC inverter to have a defined network impedance. These are required to couple the high-frequency noise into the measurement equipment, whereas the low-frequency components are still conducted via the dc-link rails. When measuring the noise levels, each output of the LISNs must be terminated by 50 Ω, either by the spectrum analyzer's input or by external terminations, to provide a symmetric measurement condition. As seen from the measurement scheme, shown in Fig. 4, the CM noise of the three-wire system is defined as the mean of the three LISN measurement outputs as

$$V_{CM} = \frac{V_{a'} + V_{b'} + V_{c'}}{3} \tag{4}$$

whereas each of the three-phase DM noise spectra can be determined by the corresponding LISN measurement output and the CM noise as

$$V_{DM,x} = V_{x'} - V_{CM} \quad \text{with} \quad x = \{a, b, c\}. \tag{5}$$

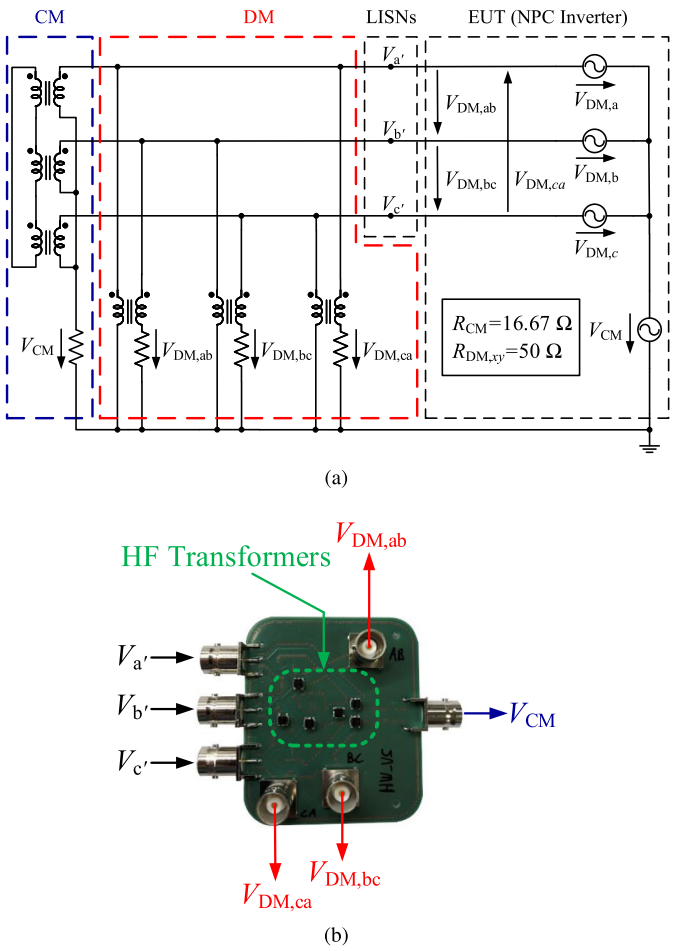

Fig. 5. *CM and line-DM separation* using HF transformers. (a) Schematic separation of the high-frequency noise coupled into the LISN. (b) PCB of the corresponding separator.

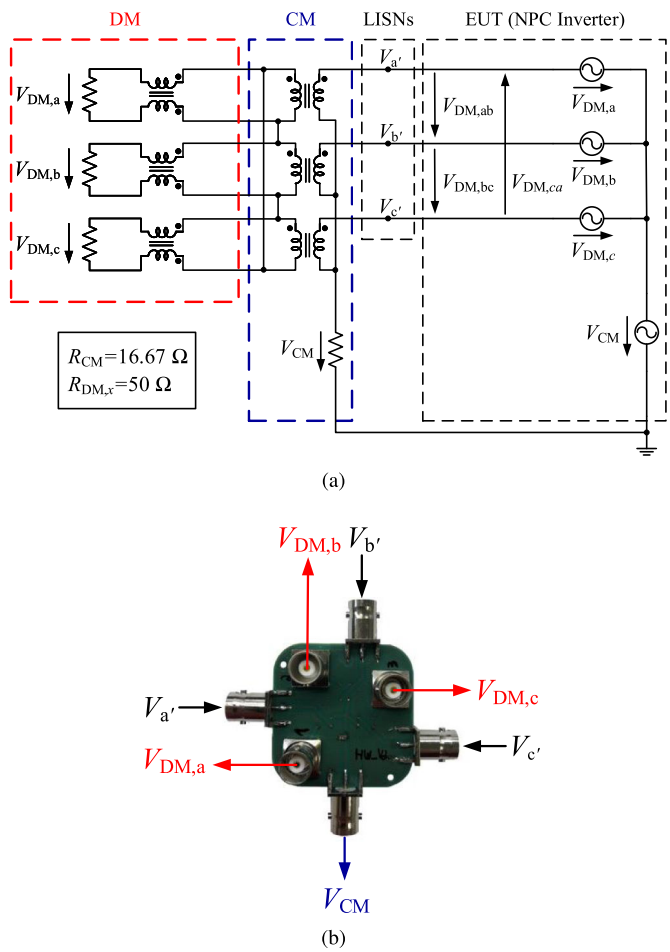

Fig. 6. *CM and phase-DM separation* using HF transformers. (a) Schematic separation of the high-frequency noise coupled into the LISN. (b) PCB of the corresponding separator.

Consequently, the line-DM noise spectra can be obtained by the subtraction of two-phase measurement outputs as

$$V_{\mathrm{DM},xy} = V_{x'} - V_{y'} \quad \text{with} \quad xy = \{\mathrm{ab}, \mathrm{bc}, \mathrm{ca}\}\,. \tag{6}$$

Equations (4)–(6) are referred to as noise separation. Typically, swept-tuned spectrum analyzers acquire only the magnitude information over a broad frequency range, so that these cannot distinguish/separate between DM and CM quantities. On the other hand, real-time spectrum analyzers, such as a fast Fourier transform analyzer, can acquire both magnitude and phase information, but the frequency range is limited to low-frequency signals up to 150 kHz. Therefore, the noise separation is quite challenging, since the phase angle of the noise components must be taken into account over a broad frequency up to several megahertz (CISPR 25: 150 kHz $\leq f \leq$ 108 MHz). In order to overcome the limited frequency range, an additional hardware separator, which is inserted between the three LISNs' outputs and the spectrum analyzer, could be used.

A. Noise Separation Based on HF Transformers

Within the scope of this article, two compact hardware separators based on small-circuit HF transformers were developed for the dc side of the NPC inverter, including its additional neutral point connection. Both separator topologies are based on [30] and [31], which were originally intended to be used for power electronic systems connected to the three-phase mains (ac-side). Similar analyses regarding the design and characterization of hardware separators using small-circuit transformers can be found in [32] and [33]. Figs. 5 and 6 show the equivalent circuit diagrams and the PCB designs of the separators.

Both separators utilize the same CM separation technique, whereas the DM measurement differs. The first separator, shown in Fig. 5, measures the line-DM quantities. Here, the DM separation is placed directly at the terminals of the LISNs with an adjacent connection of the CM mode separation part. The second separator, shown in Fig. 6, measures the phase-DM quantities. Here, the CM separation is placed directly at the terminals of the LISNs with an adjacent connection of the CM mode separation part. It should be noted that, when using either of the separators, the output terminations (50 Ω) of the LISNs should not be affected. Thus, all DM outputs must be terminated by 50 Ω and the CM output must be terminated by 50/3 Ω, as described in [31] and [30]. Since the CM output of the separators has an internal 25 Ω resistor mounted on the PCB, the required termination resistances are achieved by using external 50 Ω terminators or

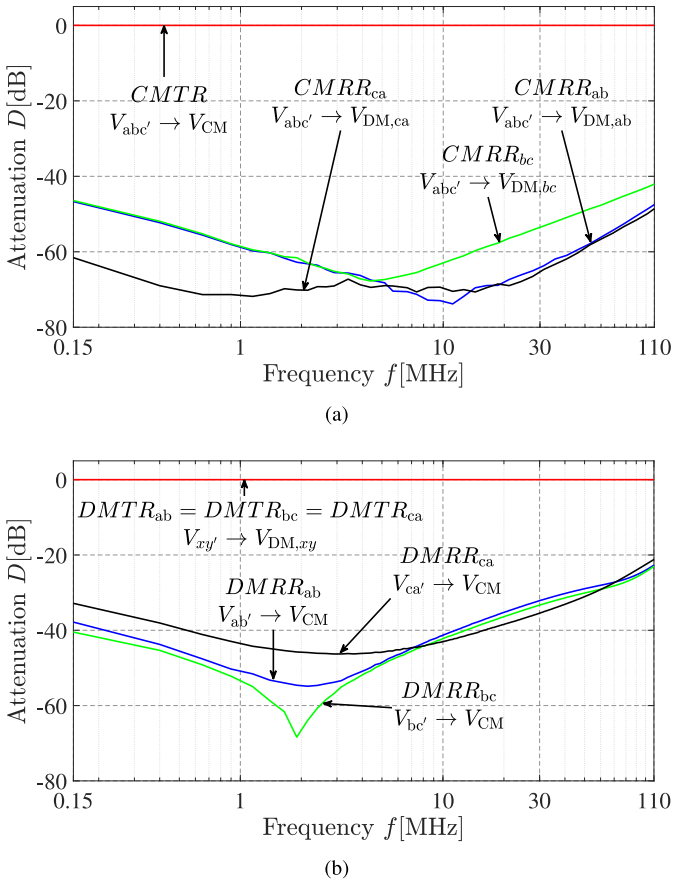

Fig. 7. (a) CM and (b) DM characteristic of the *CM/line-DM separator*.

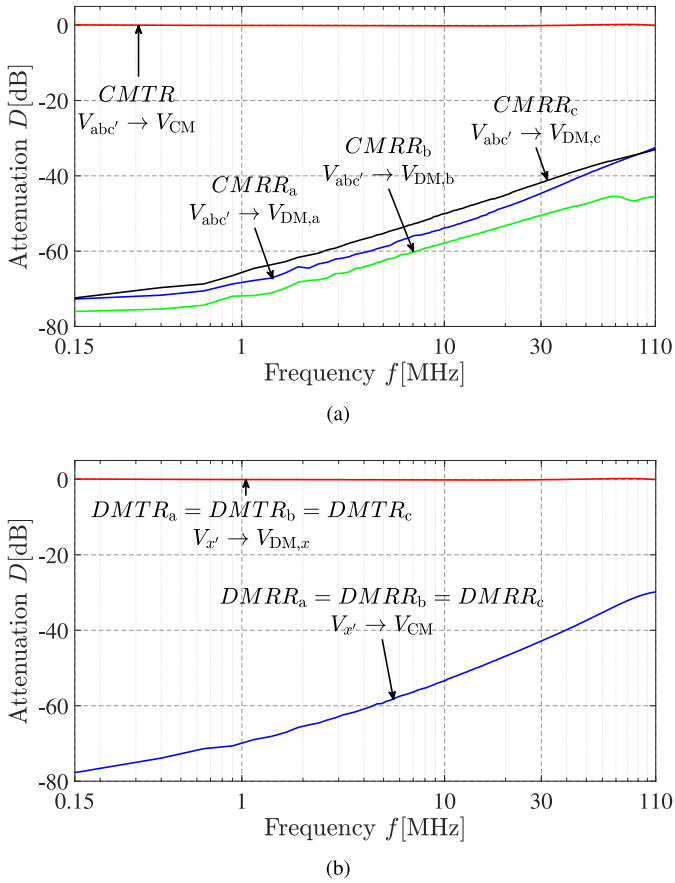

Fig. 8. (a) CM and (b) DM characteristic of the *CM/phase-DM separator*.

the input impedance of the spectrum analyzer. For the PCB realization, the TC1-42x+ [38] small-circuit HF-transformers from Minicircuits were selected, achieving a very compact and cost-effective separator design in comparison to [30]–[33]. The chosen HF transformers have an operational frequency range from 250 kHz up to 400 MHz with a typical insertion loss of 0.3 dB. In Fig. 6, the HF transformers are not visible, since these are placed on the backside of the PCB. In the following pages, separator one and two are referred to as CM/line-DM and CM/phase-DM separator, respectively. The consideration of line or phase DM noise should be chosen in accordance with possible mitigation techniques. For example, if the traction system is on a floating potential, it might be more suitable to consider line-DM noise levels and, thus, to apply X instead of Y-capacitors [39].

B. Characterization of the CM/Line-DM Separator

The performance of the three-phase CM/line-DM noise separator can be characterized by the following quantities.

1) CM transmission ratio (CMTR), which can be calculated as follows:

$$\mathrm{CMTR}(f) = 20\,\mathrm{dB} \cdot \log\left(\left|\frac{V_{\mathrm{CM,out}}}{V_{\mathrm{CM,in}}}\right|\right) \Bigg| \begin{matrix} V_{\mathrm{DM,a}} = 0 \\ V_{\mathrm{DM,b}} = 0 \\ V_{\mathrm{DM,c}} = 0 \end{matrix} \tag{7}$$

2) Line-DM transmission ratios (DMTR_{xy}), which can be calculated as follows:

$$\mathrm{DMTR}_{xy}(f) = 20\,\mathrm{dB} \cdot \log\left(\left|\frac{V_{\mathrm{DM},xy,\mathrm{out}}}{V_{\mathrm{DM},xy,\mathrm{in}}}\right|\right) \Bigg| \begin{matrix} V_{\mathrm{DM},y} = -V_{\mathrm{DM},x} \\ V_{\mathrm{DM},z} = V_{\mathrm{CM}} = 0 \end{matrix} \tag{8}$$

with $xyz = \{\mathrm{abc,bca,cab}\}$

3) CM rejection ratios (CMRR_{xy}), which can be calculated as follows:

$$\mathrm{CMRR}_{xy}(f) = 20\,\mathrm{dB} \cdot \log\left(\left|\frac{V_{\mathrm{DM},xy,\mathrm{out}}}{V_{\mathrm{CM,in}}}\right|\right) \Bigg| \begin{matrix} V_{\mathrm{DM,a}} = 0 \\ V_{\mathrm{DM,b}} = 0 \\ V_{\mathrm{DM,c}} = 0 \end{matrix} \tag{9}$$

with $xy = \{\mathrm{ab,bc,ca}\}$

4) Line-DM rejection ratios (DMRR_{xy}), which can be calculated as follows:

$$\mathrm{DMRR}_{xy}(f) = 20\,\mathrm{dB} \cdot \log\left(\left|\frac{V_{\mathrm{CM,out}}}{V_{\mathrm{DM},xy,\mathrm{in}}}\right|\right) \Bigg| \begin{matrix} V_{\mathrm{DM},y} = -V_{\mathrm{DM},x} \\ V_{\mathrm{DM},z} = V_{\mathrm{CM}} = 0 \end{matrix} \tag{10}$$

with $xyz = \{\mathrm{abc,bca,cab}\}$

The measured CM and line-DM characteristics of the separator are shown in Fig. 7(a) and (b), respectively. The CMTR and the DMRR are about 0 dB for the considered frequency range, so that the CM and DM noises are transmitted undiminished to the

corresponding outputs. The CMRRs of the three DM outputs are at least -42 dB, which corresponds to an attenuation of 0.79% relative to the input signal. The DMRR characteristics show an attenuation lower than -32 dB for up to 30 MHz and -21 dB for up to 110 MHz, which corresponds to an attenuation relative to the input signal of 2.5% and 8.91%, respectively. It can be seen that both CMRRs and DMRRs show a slight asymmetric behavior. This, however, is not crucial due to the high attenuation factors.

C. Characterization of the CM/Phase-DM Separator

The performance of the three-phase CM/phase-DM noise separator can be characterized by the following quantities.

1) CM Transmission Ratio (CMTR), which can be calculated as follows:

$$\mathrm{CMTR}(f) = 20\,\mathrm{dB}\cdot\log\left(\left|\frac{V_{\mathrm{CM,out}}}{V_{\mathrm{CM,in}}}\right|\right)\Bigg|_{\substack{V_{\mathrm{DM,a}}=0\\V_{\mathrm{DM,b}}=0\\V_{\mathrm{DM,c}}=0}} \tag{11}$$

2) Phase-DM Transmission Ratios (DMTR_x), which can be calculated as follows:

$$\mathrm{DMTR}_x(f) = 20\,\mathrm{dB}\cdot\log\left(\left|\frac{V_{\mathrm{DM},x,\mathrm{out}}}{V_{\mathrm{DM},x,\mathrm{in}}}\right|\right)\Bigg|_{\substack{V_{\mathrm{DM,y}}=-V_{\mathrm{DM,x}}\\V_{\mathrm{DM,z}}=-V_{\mathrm{DM,x}}\\V_{\mathrm{CM}}=0}} \tag{12}$$

$$\text{with } xyz = \{\mathrm{abc,bca,cab}\}$$

3) CM Rejection Ratios (CMRR_x), which can be calculated as follows:

$$\mathrm{CMRR}_x(f) = 20\,\mathrm{dB}\cdot\log\left(\left|\frac{V_{\mathrm{DM},x,\mathrm{out}}}{V_{\mathrm{CM,in}}}\right|\right)\Bigg|_{\substack{V_{\mathrm{DM,a}}=0\\V_{\mathrm{DM,b}}=0\\V_{\mathrm{DM,c}}=0}} \tag{13}$$

$$\text{with } x = \{\mathrm{a,b,c}\}$$

4) Phase-DM Rejection Ratios (DMRR_x), which can be calculated as follows:

$$\mathrm{DMRR}_x(f) = 20\,\mathrm{dB}\cdot\log\left(\left|\frac{V_{\mathrm{CM,out}}}{V_{\mathrm{DM},x,\mathrm{in}}}\right|\right)\Bigg|_{\substack{V_{\mathrm{DM},y}=-V_{\mathrm{DM},x}\\V_{\mathrm{DM},z}=-V_{\mathrm{DM},x}\\V_{\mathrm{CM}}=0}} \tag{14}$$

$$\text{with } xyz = \{\mathrm{abc,bca,cab}\}$$

The measured CM and phase-DM characteristics of the separator are shown in Fig. 8(a) and (b), respectively. Again, the CMTR and the DMRR are about 0 dB for the considered frequency range, so that the CM and DM noises are transmitted undiminished to the corresponding outputs. The CMRRs of the three DM outputs are at least -33 dB, whereas the attenuation at low frequencies is up to about -78 dB. The DMRR characteristics show an attenuation of at least -33 dB, which corresponds to an attenuation of 1.6% relative to the input signal. It can be seen that the DMRRs are symmetrical, whereas the DMRRs show a slightly asymmetric behavior, however, less pronounced than for the CM/line-DM separator.

D. Comparison With Available Hardware Separators

In comparison to the available hardware separators in [30]–[33], the transformer size is significantly reduced. Due to the integrated small-circuit design, the presented separators can be easily manufactured, achieving a compact design. In relation to [30]–[32], the transmission ratios are more constant along the whole frequency range, and the rejection ratios for both DM and CM are improved by at least 10 dB. Furthermore, the separator presented in [32] was only intended for frequencies up to 30 MHz.

IV. NPC Inverter Testbed for Validation

The previously described hardware separators were used to quantify the DM and CM noise levels of an NPC inverter with a connected neutral point, so that their performance could be validated. The prototype of the IGBT-based NPC inverter can be seen in Fig. 9. It utilizes the SKM300MLI066TAT three-level half-bridge modules from Semikron, with a nominal blocking capability of 600 V and a current rating of 300 A [40]. A nominal dc-link voltage of $V_{\mathrm{DC}} = 400$ V was chosen, so that each dc-link capacitor was supplied by about 200 V. In a real application, a dc-link voltage of 800 V would be an appropriate choice for the chosen IGBT blocking voltage capability. A custom-made three-phase *RL*-load, utilizing an air-core coil, was used as an artificial machine load (AML), as shown in Fig. 10. The AML is suggested to mimic an induction machine at standstill. Due the absence of a back EMF, the derivative of the current ripple (di/dt) is theoretically the highest [12], [41]. In an actual application, when using an electric machine, the measurement results could be different. Each phase of the AML had a nominal inductance of 220 μH and a resistance of about 50 mΩ, resulting in a power factor $\cos\phi$ close to zero. The current rating was about 125 A rms when using forced air cooling. The complete laboratory test bench can be seen in Fig. 11, built according to the standard CISPR series 16 [42]. The surface of the test bench was covered by a copper sheet (ground plate). Spacers were used to have a defined distance of 5 cm between the test equipment and the ground plate.

A. Noise Characteristic of Test Setup

To actually validate the performance of the separators, the dominant CM and DM resonance frequencies of the testbed should be known. Therefore, the CM characteristic of the LISN and the AML are modeled and the approximate resonance frequency of the DM power module oscillation is calculated in the following section. For a complete CM/DM model, the dc-link capacitors, including the busbars and their parasitics, would need to be considered as well. However, these do not significantly affect the dominant noise levels [43] and, therefore, these are not part of the article's scope.

1) CM Modeling of AML: Fig. 12(a) depicts an ideal LISN fed by an ac swept current i_{AC}. Considering the transmission ratio of the input and the output current, as shown in Fig. 12(b), a high attenuation of almost -80 dB at a frequency of about

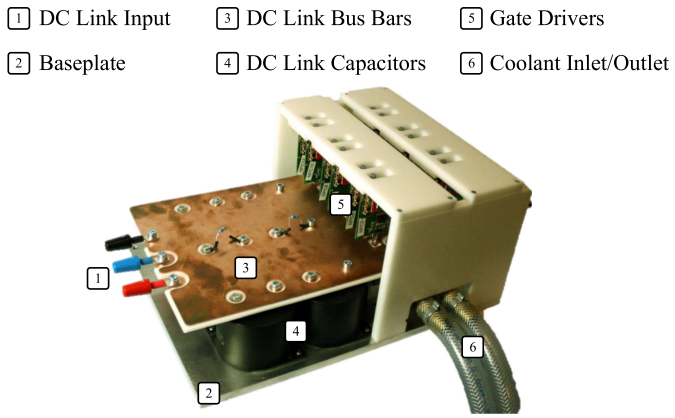

Fig. 9. Three-level NPC inverter prototype utilizing IGBT three-level half-bridge modules.

Fig. 10. Three-phase *RL*-load, air-core coil with forced air cooling.

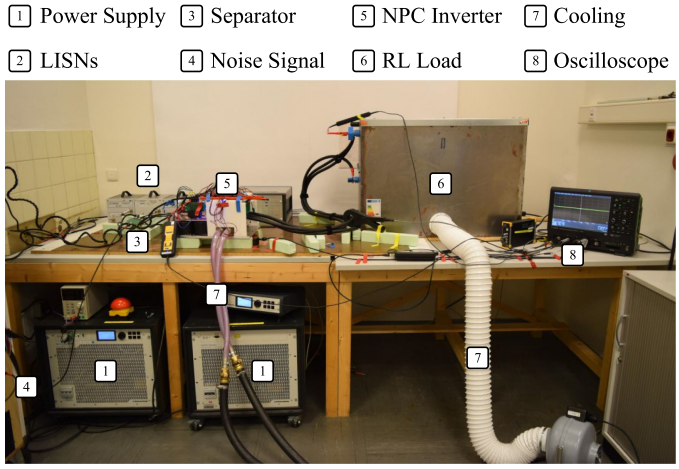

Fig. 11. EMI measurement testbench for three-level NPC inverter.

225 kHz is observed. As emphasized in Fig. 12(a), this characteristic attenuation is actually caused by the low-frequency decoupling inductor and the 100 nF capacitor, forming a notch filter. The resonance frequency can be easily calculated as

$$f_{\text{res,LISN}} = \frac{1}{2\pi\sqrt{LC}} = 225\,\text{kHz}\,. \tag{15}$$

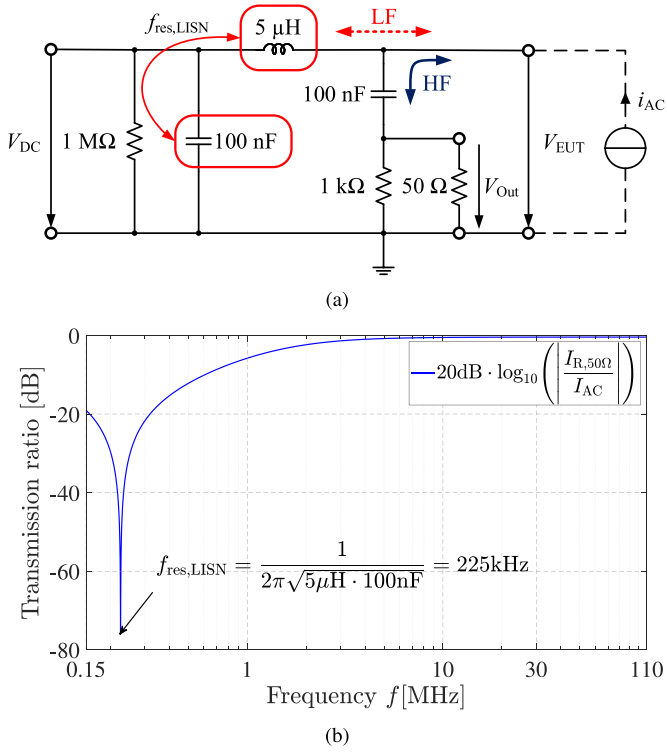

Fig. 12. (a) Equivalent circuit of an ideal LISN. (b) Transmission ratio with high attenuation at a resonance frequency of 225 kHz.

The impedance of the AML has been previously modeled and parameterized in [11] and [12] . The modeled impedance network can be seen in Fig. 13(a). The DM path contains the impedance of the cable connections and the actual *RL*-load. The CM path resembles the parasitic current over the bearings of an electric motor to ground. For this purpose, four series-connected capacitors of 9.4 nF, giving a total capacitance of 2.35 nF, were implemented. Taking all three phases of the AML and the LISNs into account, a simple CM model [43], as depicted in Fig. 13(b), can be obtained. The disturbance source, the inverter, is now modeled as a simple voltage source V_{AC}. The total CM impedance can be calculated as

$$\begin{aligned}\bar{Z}_{\text{CM,AML+Con}} &= \frac{\bar{Z}_{\text{con,DC}}}{3} + \frac{\bar{Z}_{\text{con,AC}}}{3} + \frac{R_{\text{con,ph}}}{3} \\ &+ j\omega\frac{L_{\text{con,ph}} + L_{\text{ph,gnd}}}{3} + \frac{4}{j\omega 3 C_{\text{ph,gnd}}} + \bar{Z}_{\text{con,gnd}}\end{aligned} \tag{16}$$

which results in

$$\bar{Z}_{\text{CM,AML+Con}} = j\omega 2.06\mu\text{H} + 2\text{m}\Omega - j\frac{1}{\omega 7.05\text{nF}}\,. \tag{17}$$

A high attenuation at about 1.3 MHz can be observed in the transmission ratio $\frac{V_{\text{EUT}}+V_{\text{AC}}}{V_{\text{AC}}}$, as shown in red in Fig. 13(c). This resonance is caused by the AML and the resonance frequency can be accordingly calculated as

$$f_{\text{res,AML}} = \frac{1}{2\pi\sqrt{7.05\text{nF}\cdot 2.06\mu\text{H}}} = 1.33\text{MHz}\,. \tag{18}$$

The overall transmission ratio of the disturbance voltage V_{AC} and the output voltage of the LISNs V_{Out} can be seen in

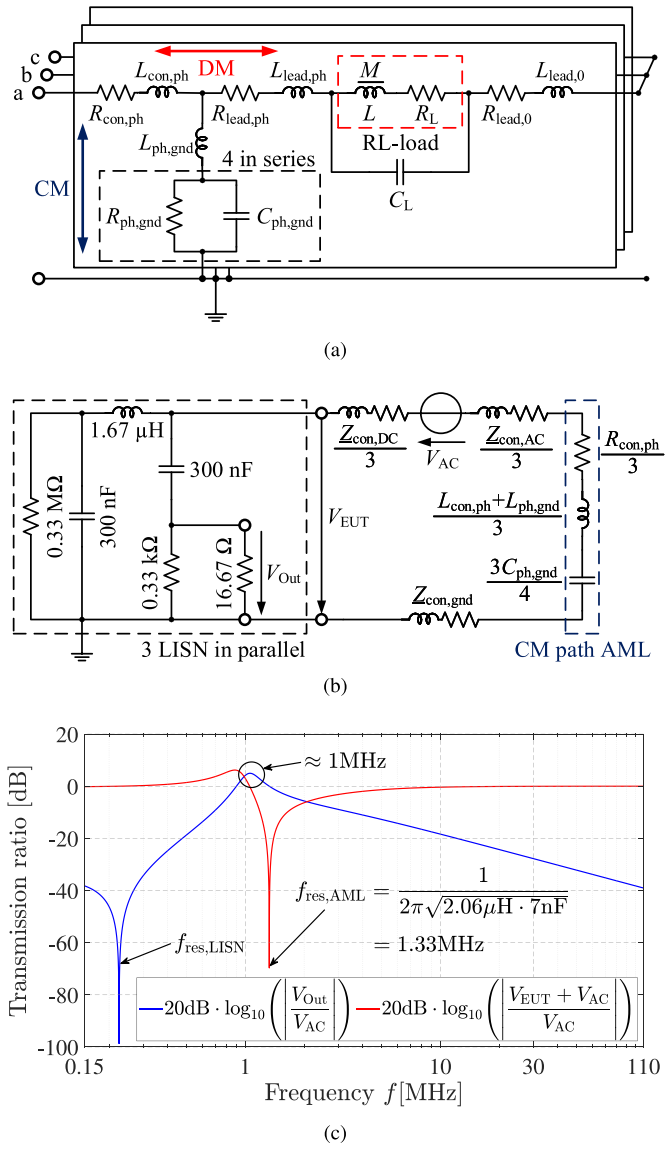

Fig. 13. (a) Equivalent circuit model of the AML. (b) CM model of the LISN and AML. (c) Corresponding disturbance transmission ratio.

Fig. 13(b), depicted in blue. On the one hand, the LISN causes an attenuation of the disturbance around the resonance frequency $f_{\mathrm{res,LISN}}$. On the other hand, the AML forms a low impedance path at the resonance frequency $f_{\mathrm{res,AML}}$, driving a disturbance into the LISN. Therefore, the combination of AML and LISN causes that the disturbance is actually worsened at about 1 MHz. The two mentioned CM resonances are mainly caused by the test setup. Therefore, these should be easily identified, using the separators, as CM noise. It should be noted that the shown CM model covers just the low-frequency characteristics to explain the two mentioned resonance points.

2) Power Module Oscillations: A characteristic DM resonance of the inverter is typically caused by the semiconductor power modules. Fig. 14(a) depicts the equivalent circuit of one NPC inverter half-leg, including its parasitics with C_{oss} as the output capacitance of each IGBT and L_σ as the stray inductance of the module packaging. The stray inductance of the used power

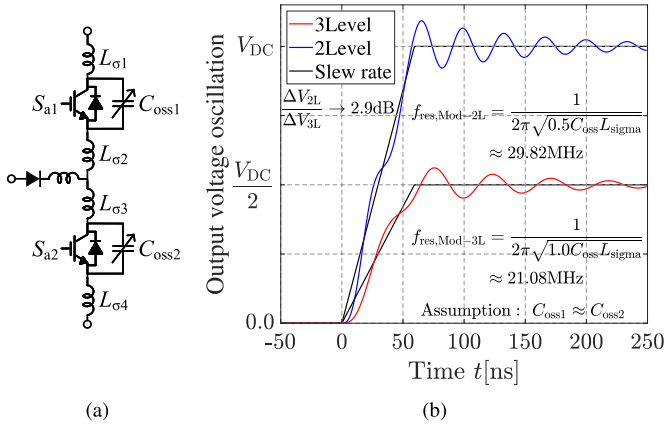

Fig. 14. (a) Modeled parasitics of an NPC inverter half-leg. (b) Resulting power module oscillations using two-level and three-level output voltage modulation.

modules was determined, using 3-D FEM simulations, to be

$$L_{\sigma,\mathrm{half-leg}} = L_{\sigma1} + L_{\sigma2} + L_{\sigma3} + L_{\sigma4} = 25\mathrm{nH} \tag{19}$$

and the IGBTs' output capacitance C_{oss} was estimated to be about 2.28 nF. Each time a switching action is performed, the resonance of the *LC*-circuit is triggered. However, it should be observed that the resonance frequency is different for two-level and three-level modulation. If two-level modulation is used, the output is switched between the positive and the negative dc-link rail (full dc-link voltage is switched), so that the combined capacitance corresponds to $0.5 \cdot C_{\mathrm{oss}}$. If three-level modulation is used, the output is either switched between the neutral and the positive or the neutral and the negative potential (half of the dc-link voltage is switched), so that the resonance capacitance corresponds to $1 \cdot C_{\mathrm{oss}}$ (during the zero state, S_{a2} is already switched and, thus, C_{oss2} is shorted). Assuming that $C_{\mathrm{oss1}} = C_{\mathrm{oss2}}$, the module resonance frequency when using two-level and three-level modulation corresponds to

$$f_{\mathrm{res,Mod-2L}} = \frac{1}{2\pi\sqrt{0.5 \cdot C_{\mathrm{oss}} L_\sigma}} = 29.81\mathrm{MHz} \tag{20}$$

and

$$f_{\mathrm{res,Mod-3L}} = \frac{1}{2\pi\sqrt{1 \cdot C_{\mathrm{oss}} L_\sigma}} = 21.08\mathrm{MHz} \tag{21}$$

respectively. Fig. 14(b) shows the modeled power module oscillations. Since the same inverter and gate driver circuitry are used, the voltage slew rate or the voltage swing of the two-level operation is twice of that of the three-level modulation. As can be seen in the graph, the voltage oscillation's magnitude of the three-level in comparison to the two-level modulation is reduced by about 2.9 dB. However, it should be noted that the output capacitance has a nonlinear characteristic [44]. Therefore, the calculated resonance frequencies in (20) and (21) can slightly differ in reality. Nevertheless, the provided equations and illustrations provide a reasonable characterization of the power module oscillation when using two- and three-level output voltage modulations.

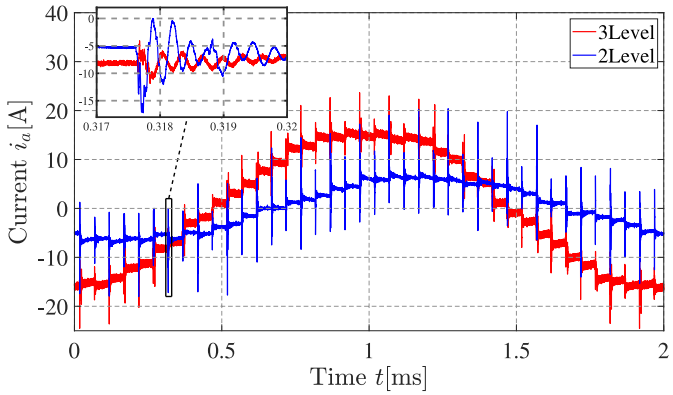

Fig. 15. Single-phase load currents for three-level and two-level operation.

B. Inverter Output Voltage Modulation

During the investigation, the inverter was operated either with three-level SVM, as described in [36] and Section II, or with classical two-level SVM (avoidance of small and medium vectors shown in Fig. 2 [25]), changing the instantaneous output voltage in (1) to

$$v_{\mathrm{abc-NP}}(S) = \frac{V_{\mathrm{DC}}}{2} S \quad \text{with} \quad S = \{1, -1\}. \tag{22}$$

The two-level modulation should resemble an operation under an inverter fault condition, as, for example, an open-circuit fault of a diode in the clamping path [25]. A switching frequency of 10 kHz was chosen. An open-loop control approach, using a fixed modulation index, was selected. The blanking time and the voltage drop across the semiconductor switches were not taken into account. It should be noted that the switching frequency of a multilevel inverter is referred to as the average frequency at which a phase leg is operated and should not be misinterpreted as the average switching frequency of individual semiconductor switches [45]. The fundamental frequency f_1 was set to 500 Hz and the modulation indices were chosen to be 3.75% and 7.5% for the two-level and the three-level modulation, respectively. It should be noted, the maximum possible modulation index was about 23% due to absence of a back EMF. Furthermore, due to the absence of the back EMF, the derivative of the current ripple is unaffected by the modulation index. Thus, the noise levels are unaffected as well by the modulation index. Fig. 15 shows the load current in phase a when using two-level and three-level operations. It can be observed that a displacement current is triggered at each switching event. As shown in Fig. 15, the three-level modulation reduces the peak of the displacement current by about 50%. It should be noted that no EMI filter is applied.

V. Quantification and Separation of Conducted Electromagnetic Emissions

When operating the inverter, the outputs of the three LISNs were connected to the noise-separator and the measured noise signal was fed from the testbed to the spectrum analyzer. Fig. 16 shows the spectra obtained at the outputs of the three LISNs measured with a peak detector. A Gaussian filter was selected. The spectrum analyzer's Resolution Bandwidth (RBW) was set

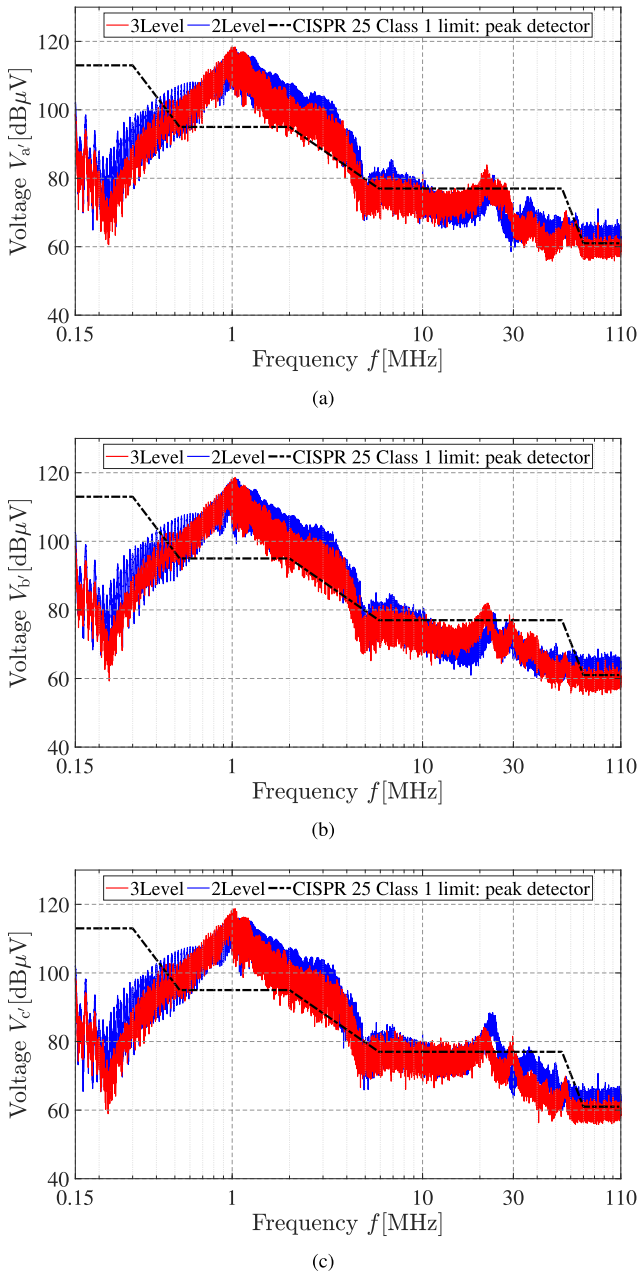

Fig. 16. Three and two-level noise spectra at (a) positive, (b) neutral, and (c) negative dc-link rail.

to 3 kHz. Since the CISPR 25 recommends a video bandwidth (VBW) of at least three times the RBW [2], the spectrum analyzer automatically adjusted the VBW to 30 kHz, which resulted in a sweep time of about 16.5 s. As described in Section III, three typical resonances were observed. One resonance valley occurs around 225 kHz, while a second dominant resonance peak is present at about 1 MHz. A smaller resonance peak is also located around 25 MHz. These three resonance points can be associated with the previously described LISN, AML, and power module oscillations, respectively. As can be seen from the three LISNs' outputs, the module resonance is not symmetrical. The highest noise level is observed at the negative dc-link rail ($V_{c'}$). Furthermore, it can be seen that the three-level in comparison to the two-level modulation does not only reduce the noise level

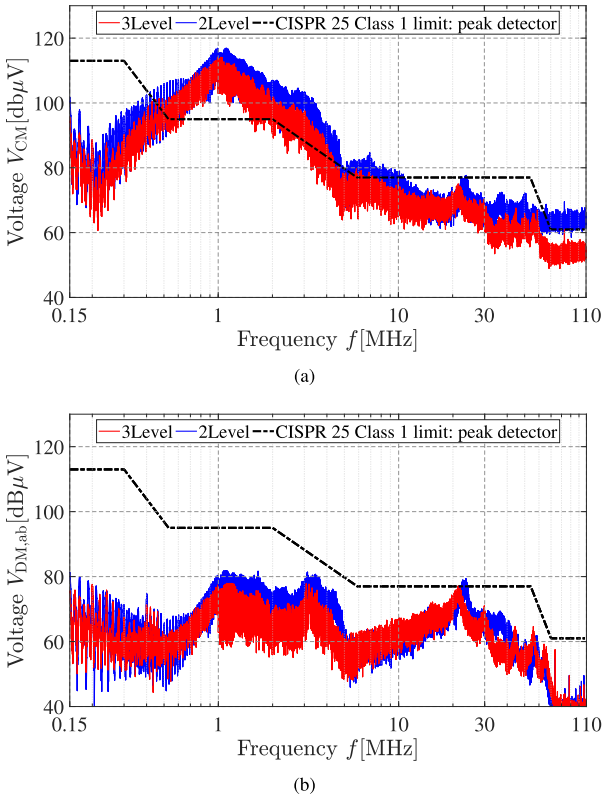

Fig. 17. Measured (a) *CM* and (b) *line-DM* ($V_{\mathrm{DM,ab}}$) noise, when operating with two-level and three-level modulation.

by 3 to 6 dB, it affects also the module resonance frequency as similarly described in (20) and (21).

A. Separated Noise

To validate the performance of the separators, the measured noise was separated into CM, line-DM, and phase-DM quantities.

1) CM and Line-DM Noise: Fig. 17(a) and (b) shows the separated CM and one line-DM ($V_{\mathrm{DM,ab}}$) spectrum, respectively, measured with the CM/line-DM separator. Since the three line-DM spectra show similar noise levels, just $V_{\mathrm{DM,ab}}$ is shown here. Similar to the two-level inverter investigation in [9], the CM is also predominant for the three-level NPC inverter with a connected neutral point. It can be seen that the noise levels using two-level operation are slightly increased by 3 up to 6 dB for both CM and DM. Furthermore, as modeled in Section III, it is observed that the LISN and AML resonances are driven by the CM, whereas the module resonance is driven by the DM. Regarding the power module resonance, the two-level in comparison to the three-level modulation shifts the resonance frequency from about 25 to 21 MHz and the noise level is reduced by about 3 dB.

2) CM and Phase-DM Noise: The obtained results of the CM/phase-DM separator can be seen in Fig. 18. Regarding the CM, a similar noise spectrum as for the CM/line-DM separator was obtained, as can be seen in Fig. 18(a). Fig. 18(b) and (c) shows the phase-DM spectra $V_{\mathrm{DM,a}}$ and $V_{\mathrm{DM,b}}$, respectively. The third phase-DM spectrum $V_{\mathrm{DM,c}}$ is not displayed, since it does not qualitatively differ from $V_{\mathrm{DM,a}}$. $V_{\mathrm{DM,a}}$ shows a similar

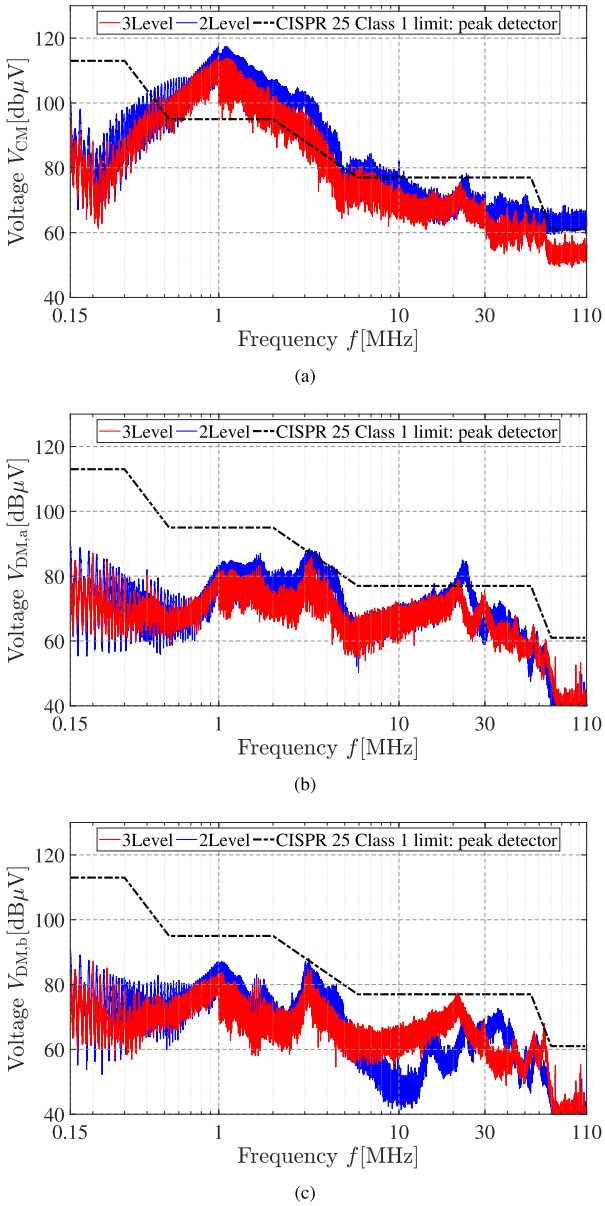

Fig. 18. Measured (a) *CM* and (b) *phase-DM* at positive ($V_{\mathrm{DM,a}}$) and (c) neutral dc-link rail ($V_{\mathrm{DM,b}}$), when operating with two-level and three-level modulation.

spectrum as $V_{\mathrm{DM,ab}}$, while the phase quantities seem slightly increased compared to the line quantities. When in two-level operation, $V_{\mathrm{DM,b}}$ shows a significant noise reduction in the range above 4 MHz, since the zero switching state of each phase leg is not used and the power module oscillation is not triggered. The spectrum at lower frequencies is not effected.

B. Parasitic CM Current Over Ground Plate

Typically, the high-voltage traction system in a car is isolated. Though, the unwanted parasitic currents, capacitively or inductively coupled, in the motor bearings [46] or the vehicle's chassis are other criteria to assess the EME of the traction inverter and, thus, can be used to verify the measured CM noise reduction. For this purpose, a current sensor was mounted on a flat copper bar between the inverter's heatsink and the ground sheet, as can

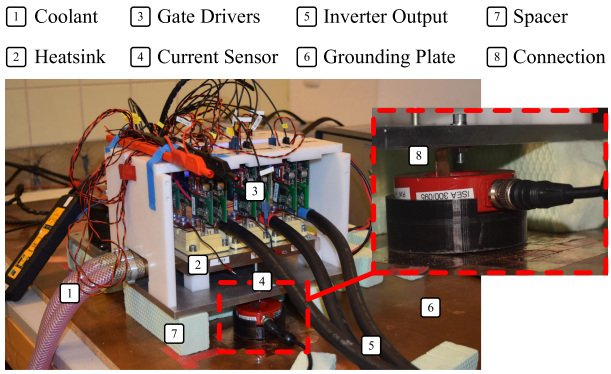

Fig. 19. Current sensor mounting to measure the parasitic current through the ground plate.

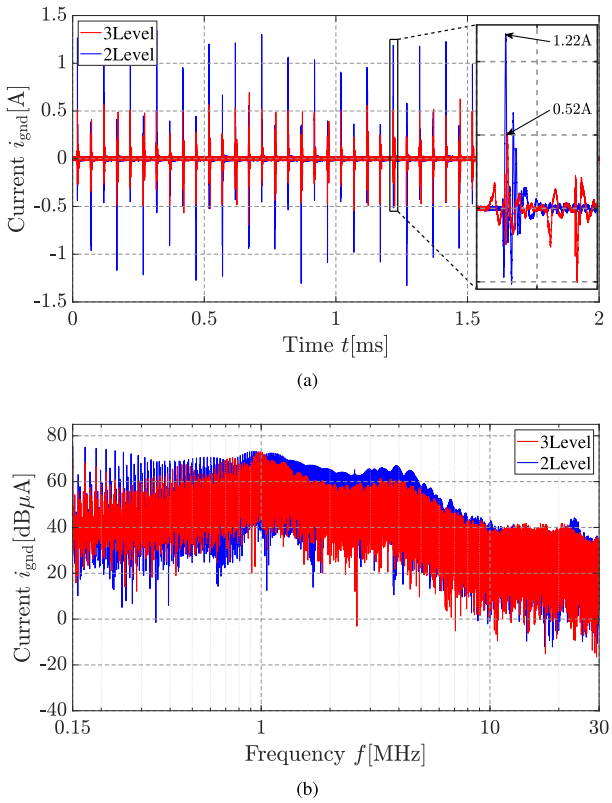

Fig. 20. Measured parasitic current through the ground plate (a) in time and (b) in frequency domain.

be seen in Fig. 19. The power modules are electrically insulated from the heatsink by the internal ceramic substrate and the star point of the *RL*-load is floating. The measured waveforms of the parasitic currents through the ground plate can be seen in Fig. 20(a) and (b). At each switching event, a displacement current is triggered, generating broadband emissions. It can be seen that the three-level modulation reduces the peak of the current spikes by about 50%, which is consistent with the previously measured noise reduction of about 6 dB. In the logarithmic plot shown in Fig. 20, the characteristic of the AML at 1 MHz can be recognized, and it can be seen that the emissions at the sidebands are reduced by about 3–6 dB. This in turn confirms the acquired CM results of the separators.

VI. Conclusion

Due to the additional neutral point connection, the three-level NPC inverter's dc side forms a three-wire CM/DM system. This article has presented an approach to separate the three-wire noise of a three-level NPC inverter with a connected neutral point, using two different hardware separators based on small-circuit HF transformers. Two very compact separator prototypes have been built and their CM/DM frequency characteristics have been measured, showing reasonable noise transmission and rejection ratios. An EMI testbed with three LISNs has been used to measure the conducted noise of the NPC inverter. A simple three-wire CM model has been introduced to explain the characteristic CM resonances of the test setup and a short derivation of the DM power module oscillations using two- and three-level output voltage modulation has been given. For the investigation, the inverter has been operated with three-level and two-level modulation, resembling normal operation and operation under fault condition, respectively. The noise has been separated into CM, line, and phase-DM quantities. The CM noise is predominant. The two typical resonance points of the testbed, caused by the LISN and the AML, could be clearly identified by both separators. Furthermore, the resonance frequency of the power module oscillations, including their dependence on the modulation technique, have been modeled and significantly measured by both the phase-DM and the line-DM separator. Additionally, it has been shown that the two-level in comparison to the three-level operation increases the noise levels by 3–6 dB and the measured parasitic current through the ground plate confirms the CM noise increase of about 50%.

Thus, it can be concluded that the compact hardware separators could be easily used to identify critical CM and DM noise levels so that an EMI filter can be accordingly designed.

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