Low Common-Mode Noise *LLC* Resonant Converter With Static-Point-Connected Transformer

Keon-Woo Kim, *Student Member, IEEE*, Yeonho Jeong, *Member, IEEE*, Jae-Sang Kim, *Student Member, IEEE*, and Gun-Woo Moon, *Member, IEEE*

***Abstract*—A new structure of the transformer and its winding layout are proposed to reduce the common-mode (CM) noise generated from the planar transformer (PT). In the proposed converter, two half-bridge *LLC* resonant converters are connected in parallel on the primary side, and the secondary side of them is connected in series. The proposed converter can be utilized for the medium-to-high power applications due to the full-bridge structure of the primary side. For each transformer, one of the terminals is connected to the static point, which has zero *dv*/*dt* characteristic. Thus, the primary-side layer can have the same *dv*/*dt* characteristics with the secondary-side layer. By adjacently locating the primary and secondary layers, which have the same *dv*/*dt* characteristic, the CM current and noise generated from PT can be significantly reduced. Therefore, the proposed converter can achieve a high power density by reducing the size of the electromagnetic interference filter.**

***Index Terms*—Common mode (CM) noise, planar transformer (PT), LLC resonant converter.**

I. Introduction

A FULL-BRIDGE (FB) structure is widely used for the medium-to-high power applications, such as electric vehicle battery chargers and server powers [1]–[4]. These applications require a high power density due to the growing interest of low-profile power supplies. Typically, they utilize a high switching frequency to reduce the size of magnetics and the soft-switching converters with the zero voltage switching (ZVS) and zero current switching (ZCS) should be adopted to reduce the switching loss. Among the soft-switching converters, an *LLC* resonant converter is a great candidate due to the benefit of a wide ZVS range of the primary switches and ZCS characteristic of the rectifier diodes [5]–[9]. In addition, the planar transformer (PT) becomes a great option for the resonant inductor and transformer to achieve the low height and volume [10], [11]. In order to use the PT, a printed circuit board (PCB) is necessary for the winding of the transformer. Each layer of the PCB contains the primary or secondary turns of the transformer, and the adjacent primary and secondary layers lead to a large parasitic capacitance. Also, the voltage potential of the layers rapidly changes according to the switching frequency, which means the large *dv*/*dt*, and each layer has a different *dv*/*dt*. Thus, the large amount of the common-mode (CM) current flowing through the parasitic capacitors results in a high level of the CM noise and deteriorates the electromagnetic interference (EMI) performance of the converter [12]. Although the EMI filter should be adopted to satisfy the EMI standard, the EMI filter occupies a large area due to the bulky inductor [13]. In addition, a high level of the CM noise leads to the large size of the EMI filter and significantly decreases the power density of converters.

In order to reduce the CM noise of the converters, many works have been studied [13]–[31]. These methods can be categorized into three groups. The first method adds additional windings or layers to the transformer [13]–[21]. In [14], an antiphase winding is added for good CM noise attenuation. Also, previous works in [13] and [15]–[18] use the shielding layer to suppress the CM noise. However, extra windings should be added, and it results that the winding area in the transformer is increased. These methods increase the conduction loss in the additional windings due to the eddy current. Although Fei *et al.* [19] increase the efficiency by utilizing half of the shielding layer as the primary turn, it still requires the shielding layer for every space between the primary and secondary windings. The work in [20] can decrease the CM noise by modifying the PT layout. However, this method requires an additional winding area due to the intermittent ground layout between the windings. Second, the CM noise reduction techniques can be achieved by applying additional passive components [21]–[25]. Those techniques require additional components, such as the capacitor, inductor, transformer, and coupled-balanced choke. They improve the EMI performance by constructing balanced CM noise models. However, it is difficult to make balanced CM noise models because they are sensitive to the tolerance of components. The third category reduces the CM noise by overlapping the primary and secondary layers having a similar *dv*/*dt* characteristic [26]–[29]. These works can be implemented by a simple method, such as arranging the layers in proper sequence or changing the location of the diode and transformer. However, their techniques are implemented based on the flyback, forward, and half-bridge *LLC* resonant converter. Thus, their solutions are difficult to be implemented for the medium-to-high

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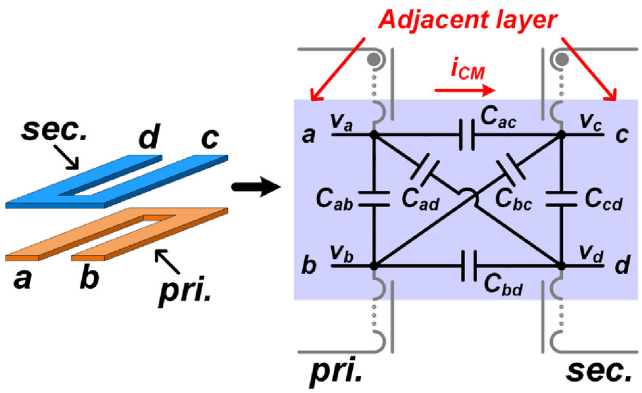

Fig. 1. Parasitic capacitor model in the transformer.

power application because of the large conduction loss on the primary side.

This article proposes a new structure and winding layout having a small CM noise based on the FB structure for the medium-to-high power application. The proposed converter contains two parallel-connected half-bridge circuits on the primary side and the transformers of each half-bridge circuits are connected in series on the secondary side. For each transformer, one of the terminals can be connected to the static point, which is ground or input voltage $V_{\rm in}$. Due to the static-point-connected transformer structure, there are primary and secondary layers having the same *dv*/*dt* characteristics. Thus, the CM current flowing through the parasitic capacitors in the PT can be decreased by overlapping the primary and secondary layers with the same *dv*/*dt* characteristics. As a result, the proposed converter can have a low CM noise and achieve a high power density with the small size of the EMI filter.

II. CM Noise Characteristic in Converters

A. Review for CM Noise in the PT

The CM noise is generated due to the CM current $i_{\rm CM}$ flowing through the parasitic capacitors between the primary and secondary layers in the PT. Fig. 1 shows the parasitic capacitor model between adjacent two layers in the PT. $i_{\rm CM}$ in the PT can be expressed as follows [29]:

$$i_{\rm CM} = C_{ac}\left(\frac{dv_a}{dt}-\frac{dv_c}{dt}\right)+C_{ad}\left(\frac{dv_a}{dt}-\frac{dv_d}{dt}\right) + C_{bc}\left(\frac{dv_b}{dt}-\frac{dv_c}{dt}\right)+C_{ad}\left(\frac{dv_b}{dt}-\frac{dv_d}{dt}\right) \quad (1)$$

where C_{ac}, C_{ad}, C_{bc}, and C_{bd} are the parasitic capacitors between the adjacent primary and secondary layers in the transformer, and v_a, v_b, v_c, and v_d are the voltage versus ground at the point *a*, *b*, *c*, and *d*, respectively, as shown in Fig. 1.

When the voltage waveforms of the adjacent layers are the same, the slope of v_a and v_b is the same with that of v_c and v_d, respectively, i.e., $dv_a/dt = dv_c/dt$ and $dv_b/dt = dv_d/dt$. Moreover, if the overlapping layers have the same number of turns and symmetric PCB layout, the parasitic capacitances can be assumed as the same value, i.e., $C_{ad} = C_{bc}$. From (1), $i_{\rm CM}$ can be zero with two previous assumptions. Therefore, if the adjacent primary and secondary layers have the same voltage waveform, number of turns, and symmetric PCB layout, there is no CM current through parasitic capacitors. Moreover, parasitic capacitors between the primary or secondary layers do not need to be considered because the CM current do not flow through those capacitors.

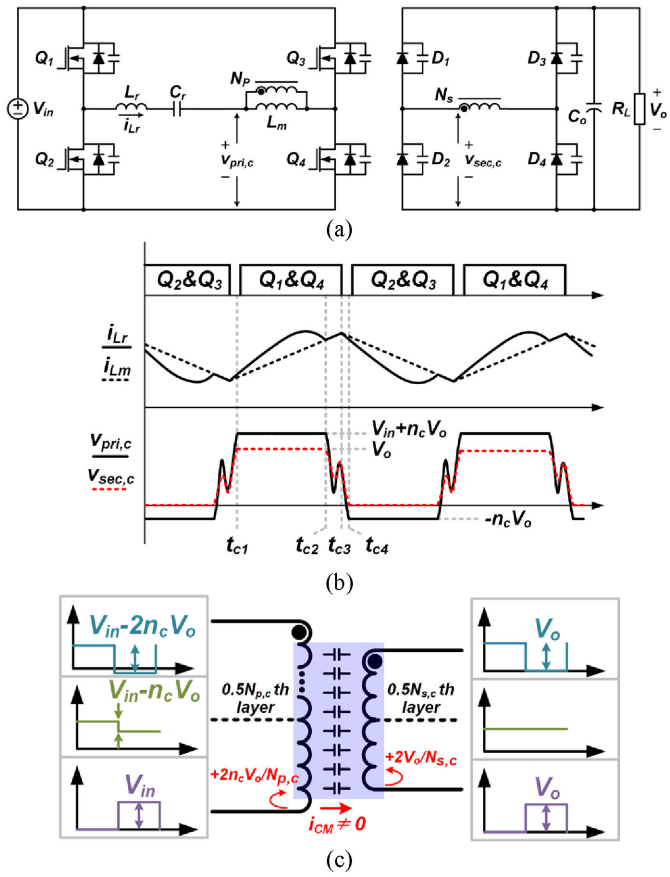

Fig. 2. FB *LLC* resonant converter. (a) Circuit diagram. (b) Operational waveforms. (c) Voltage waveforms of layers.

B. CM Noise Characteristic in the Conventional Converter

Fig. 2(a) shows the FB *LLC* resonant converter. The primary turn of the transformer is $N_{p,c}$, secondary turn of the transformer is $N_{s,c}$, and turns ratio n_c is $N_{p,c}/N_{s,c}$. The operational waveforms of the FB *LLC* resonant converter are shown in Fig. 2(b). The voltage potentials versus ground at the dot terminal on the primary and secondary sides of the transformer $v_{{\rm pri},c}$ and $v_{{\rm sec},c}$ are presented. $v_{{\rm pri},c}$ fluctuates between $V_{\rm in}+n_cV_o$ and $-n_cV_o$, and $v_{{\rm sec},c}$ changes between zero and V_o. In order to analyze the voltage potential at each layer, the voltage waveforms of layers in the FB *LLC* resonant converter are shown in Fig. 2(c). On the primary side, the voltage potential of the nondot terminal in the transformer changes from zero to $V_{\rm in}$. The voltage-potential-variation on the primary side is changed by $2n_cV_o/N_{p,c}$ per turn. The voltage potentials of every layer on the primary side except for a nondot terminal are expressed with the sum of $V_{\rm in}$ and V_o term. Thus, there is no static point on the primary side layer,

as shown in Fig. 2(c), because V_o is changed depending on the operation conditions, and the combination of $V_{\rm in}$ and V_o terms cannot be a constant value. The voltage potential of the nondot terminal on the secondary side in the transformer changes from zero to V_o. The voltage potential of every layer on the secondary side is expressed with V_o term. Thus, the center point of the transformer, $0.5N_{s,c}$th layer, becomes the static point, as shown in Fig. 2(c). There are no same voltage waveforms between the primary and secondary layers under the entire operation conditions because V_o is changed from 270 to 420 V. Therefore, the CM current flows through parasitic capacitors between the primary and secondary layers, and it increases the CM noise.

C. CM Noise Characteristic in the Proposed Converter

Fig. 3(a) shows the circuit diagram of the proposed converter. On the primary side, two half-bridge *LLC* resonant converters are connected in parallel. Two transformers have the same turns both on the primary and secondary sides. The primary turns of T_1 and T_2 are N_p, the secondary turns of T_1 and T_2 are N_s, and turns ratio n is N_p/N_s. On the primary side, the nondot terminal of T_1 is connected to the ground and the dot terminal of T_2 is connected to $V_{\rm in}$. On the secondary side, the nondot terminal of T_1 and dot terminal of T_2 are connected, as shown in Fig. 3(a). Thus, one of the terminals of the transformers is connected to the static point and those connections make static-point-connected transformers. Fig. 3(b) presents the operational waveforms of the proposed converter. The voltage across the secondary side of the transformer is $0.5V_o$ in the proposed converter, which is the half of $v_{{\rm pri},c}$ because the secondary sides of the transformers are connected in series. Thus, the peak current of the magnetizing currents in the proposed converter is almost half compared with that in the conventional converter.

In order to apply the analysis in Section II-A, the voltage waveforms of the layers in the proposed converter should be analyzed. In Fig. 3(c), the voltage waveforms of the layers in T_1 and T_2 are described. On the primary side, the nondot terminal of T_1 and dot terminal of T_2 are static points, and it means that the voltage potentials of both static points are not changed. The voltage-potential-variation of the primary side in T_1 and T_2 is changed by nV_o/N_p per turn. On the secondary side, the nondot terminal of T_1 and dot terminal of T_2 is the static point because they are the center point of the transformers. The voltage-potential-variation of the secondary side in T_1 and T_2 is changed by V_o/N_s per turn.

For T_1, *dv/dt* of the nondot terminals on the primary and secondary side is zero. In addition, the voltage-potential-variation per turn is the same for the primary and secondary side because nV_o/N_p is equal to V_o/N_s. Thus, the primary and secondary layer can have the same voltage waveform if the primary and secondary side layers are overlapped one by one, starting from the first layer, as shown in Fig. 4. In the end, the voltage potential versus ground at the N_sth layer on the primary side of T_1 $v_{pri1[Ns]}$ and the voltage potential versus ground at the N_sth layer on the primary side of T_2 $v_{pri2[Ns]}$ have the same voltage shape, as shown in Fig. 3(b). For T_2, *dv/dt* of the dot terminals on the primary and secondary side is zero. In addition, the voltage-potential-variation per turn is the same for the primary and secondary side because of $nV_o/N_p = V_o/N_s$. Thus, similar to the T_1, the primary and secondary layers can have the same voltage waveform if the primary and secondary side layers are overlapped one by one starting from the last layer, as shown in Fig. 4. Finally, the voltage potential versus ground at the $(N_p - N_s)$th layer on the primary side of T_1 $v_{pri1[Np-Ns]}$ and the voltage potential versus ground at the first layer on the

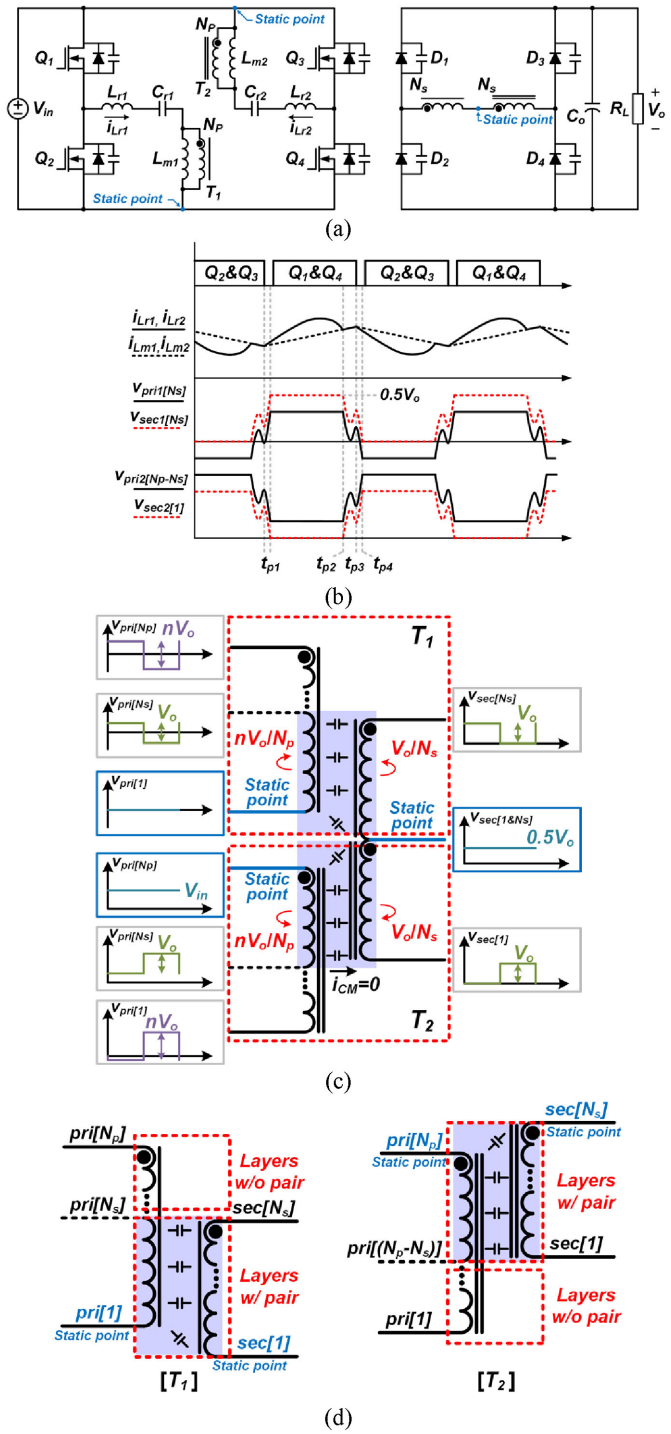

Fig. 3. Proposed converter. (a) Circuit diagram. (b) Operational waveforms. (c) Voltage waveforms of layers. (d) Pair of layers in the transformer.

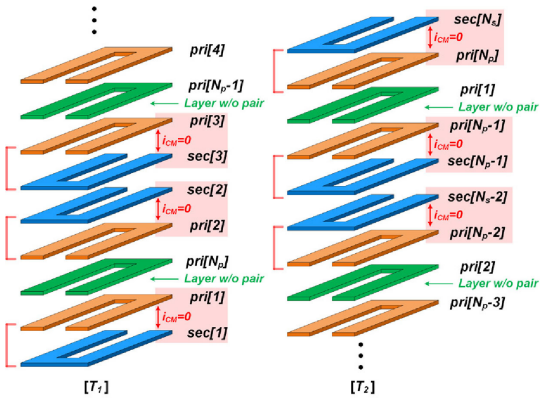

Fig. 4. Winding layout of the transformer in the proposed converter.

TABLE I
LAYOUT OF PROTOTYPE CONVERTERS

Layers	Conv.	Prop. T_1	Prop. T_2
20th	sec[1]	sec[8]	sec[1]
19th	pri[1]	pri[8]	pri[5]
18th	sec[2]	pri[9]	pri[4]
17th	pri[2]	pri[7]	pri[6]
16th	pri[3]	sec[7]	sec[2]
15th	sec[3]	sec[6]	sec[3]
14th	pri[4]	pri[6]	pri[7]
13th	pri[5]	pri[10]	pri[3]
12th	sec[4]	pri[5]	pri[8]
11th	pri[6]	sec[5]	sec[4]
10th	pri[7]	sec[4]	sec[5]
9th	sec[5]	pri[4]	pri[9]
8th	pri[8]	pri[11]	pri[2]
7th	pri[9]	pri[3]	pri[10]
6th	sec[6]	sec[3]	sec[6]
5th	pri[10]	sec[2]	sec[7]
4th	pri[11]	pri[2]	pri[11]
3rd	sec[7]	pri[12]	pri[1]
2nd	pri[12]	pri[1]	pri[12]
1st	sec[8]	sec[1]	sec[8]

primary side of T_2 $v_{pri2[1]}$ have the same voltage shape, as shown in Fig. 3(b). When N_p is the same with N_s, every primary and secondary layer can be paired. When N_p is different from N_s, layers without a pair should be considered. This article will explain the case when N_p is larger than N_s. As shown in Fig. 3(d), from the (N_s+1)th to N_pth layers of the primary side in T_1 and from the first to (N_p-N_s-1)th layers are the primary layers without the pair. The winding layout of T_1 and T_2 for the proposed converter is described in Fig. 4. As aforementioned, $i_{\rm CM}$ between the adjacent primary and secondary layers is zero because those two layers have no *dv*/*dt* difference. As shown in Fig. 4, layers without the pair can be placed between two primary layers, which have their pair because there is no CM current between two different primary layers.

The whole layout of the prototype converters is given in Table I. The transformer of the conventional converter is composed of the interleaved winding structure and it results in a large CM current between the primary and secondary layers. Although the transformer of the proposed converter has the same interleaved winding structure, there is no CM current between the primary and secondary layers because the adjacent layers have the same *dv*/*dt* characteristic.

D. Transformer Design

The voltage gain of the *LLC* resonant converter can be calculated based on the fundamental harmonic approximation (FHA) [30]. Based on the FHA, the voltage gains of the conventional converter $M_{\rm conv}$ and the proposed converter $M_{\rm prop}$ can be calculated as follows:

$$M_{\rm conv}=\frac{V_{o,{\rm conv}}^{F}}{V_{{\rm in},{\rm conv}}^{F}}=\frac{\frac{4n_cV_o}{2\pi}\sin(2\pi f_st)}{\frac{4V_{\rm in}}{\pi}\sin(2\pi f_st)}=\frac{n_cV_o}{V_{\rm in}} \quad (2)$$

$$M_{\rm prop}=\frac{V_{o,{\rm prop}}^{F}}{V_{{\rm in},{\rm prop}}^{F}}=\frac{\frac{4nV_o}{2\pi}\sin(2\pi f_st)}{\frac{4V_{\rm in}}{\pi}\sin(2\pi f_st)}=\frac{nV_o}{V_{\rm in}} \quad (3)$$

where f_s is the switching frequency, $V_{o,{\rm conv}}^{F}$ and $V_{{\rm in},{\rm conv}}^{F}$ are the fundamental components of the V_o and $V_{\rm in}$ for the conventional converter, respectively, and $V_{o,{\rm prop}}^{F}$ and $V_{{\rm in},{\rm prop}}^{F}$ are the fundamental components of the V_o and $V_{\rm in}$ for the proposed converter, respectively.

According to (2) and (3), $M_{\rm conv}$ and $M_{\rm prop}$ are the same when two converters have the same turns ratio. Thus, with assumptions that they use the same turns ratio and resonant tank, their operating switching frequency range and the minimum switching frequency $f_{s,\min}$ can also be the same. The effective cross-sectional area for the transformer of the proposed converter A_e and that of the conventional converter $A_{e,c}$ can be calculated as follows:

$$A_e=\frac{L_mI_{Lm,\max}}{N_pB_{\max}}=\frac{V_{\rm trans}}{4N_pB_{\max}f_{s,\min}} \quad (4)$$

$$A_{e,c}=\frac{L_{m,c}I_{Lm,\max,c}}{N_{p,c}B_{\max}}=\frac{V_{{\rm trans},c}}{4N_{p,c}B_{\max}f_{s,\min}} \quad (5)$$

where L_m is the magnetizing inductance of the proposed converter, $L_{m,c}$ is the magnetizing inductance of the conventional converter, $I_{Lm,\max}$ is the peak of the magnetizing inductor current for the proposed converter, $I_{Lm,\max,c}$ is the peak of the magnetizing inductor current for the conventional converter, $V_{\rm trans}$ is the voltage across the transformer in the primary side for the proposed converter, $V_{{\rm trans},c}$ is the voltage across the transformer in the primary side for the conventional converter, and $B_{\max}$ is the maximum flux density.

In (4) and (5), $V_{\rm trans}$ is $0.5nV_o$ and $V_{{\rm trans},c}$ is nV_o. Thus, if $N_p=N_{p,c}$ and $L_m=L_{m,c}$, the proposed converter can use the half size of the core for T_1 and T_2, which means that A_e is $0.5A_{e,c}$. T_1 and T_2 can be merged by utilizing the side legs as the transformers of the proposed converter and the transformer of the conventional converter can be made up by utilizing the center leg, as shown in Fig. 5. Therefore, the total core size of two converters is the same.

III. EXPERIMENTAL RESULTS

The prototype converters are implemented with a 1.5-kW *LLC* resonant converter and the design specification is input

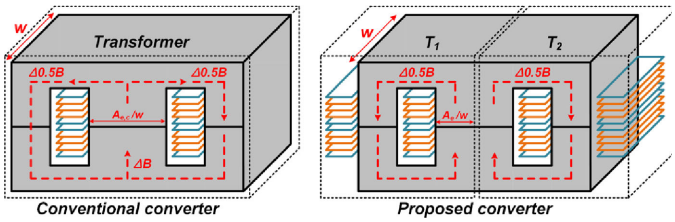

Fig. 5. Transformer of the conventional and proposed converter.

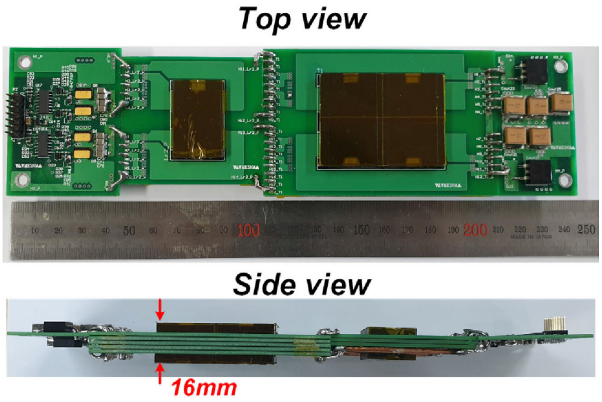

Fig. 6. Prototype of the proposed converter.

TABLE II
COMPONENT LIST OF THE PROTOTYPE CONVERTERS

	Conventional converter	Proposed converter
Primary switches (Q_1, Q_2, Q_3, and Q_4)	GS66508T ($V_{ds,max}$ = 650 V and $I_{DS,avg}$ = 30 A)	
Transformers (L_m, L_{m1}, and L_{m2})	ELP 38/8/25 * 2 (material: N49, 40 μH and turn-ratios= 12:8)	
Resonant inductors (L_r, L_{r1}, and L_{r2})	ELP 32/6/20 (material: N49 and 11.2 μH)	
Resonant capacitors (C_r, C_{r1}, and C_{r2})	GRM32D7U3A222JW31L * 4 (8.8 nF)	
Rectifier diodes (D_1, D_2, D_3, and D_4)	SCS210AJ (V_R=650 V and I_F=10 A)	

voltage = 400 V, output voltage = 270–420 V, and resonant frequency = 500 kHz. The prototype of the proposed converter is shown in Fig. 6 and the detailed component list is presented in Table II.

A. Comparison of Voltage Waveforms and Efficiency

Figs. 7 and 8 show the key experimental waveforms of the conventional FB *LLC* and proposed converters. In Fig. 7, the experimental waveforms of the conventional converter for the resonant inductor current i_{Lr}, the voltage waveform on the primary side $v_{\mathrm{pri,conv}}$, and the voltage waveform of the secondary side $v_{\mathrm{sec,conv}}$ are presented. Fig. 7(a) shows the waveforms at $V_o = 270$ V and Fig. 7(b) presents the waveforms at $V_o = 420$ V, which is the worst case in terms of the CM noise attenuation due to the largest *dv/dt* characteristic across the parasitic capacitors of the transformer. It notes that the voltage-potential variations of two adjacent layers are different. Thus, there is a significant CM current between the primary and secondary sides, and it results

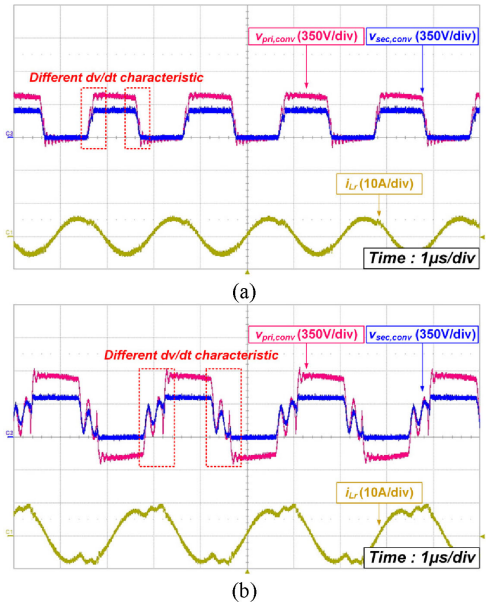

Fig. 7. Experimental waveforms of the conventional converter. (a) At $V_o = 270$ V. (b) At $V_o = 420$ V.

in the large CM noise. Fig. 8 shows the experimental waveforms of the proposed converter for the resonant inductor current i_{Lr1} and i_{Lr2}, the voltage waveform of T_1 at the N_sth layer of the primary side $V_{\mathrm{pri},T1}$, the voltage waveform of T_1 at the N_sth layer of the secondary side $V_{\mathrm{sec},T1}$, the voltage waveform of T_2 at the $(N_p - N_s)$th layer of the primary side $V_{\mathrm{pri},T2}$, and the voltage waveform of T_2 at the first layer of the secondary side $V_{\mathrm{sec},T2}$ are expressed. Fig. 8(a) and (b) shows the waveforms at $V_o = 270$ V for T_1 and T_2, and the key waveforms at $V_o = 420$ V for T_1 and T_2 are presented in Fig. 8(c) and (d). The voltage waveforms of the primary and secondary sides for T_1 and T_2 are the same. Thus, there is no CM current between two adjacent primary and secondary layers due to the same *dv/dt* characteristics. Although there are small voltage ripples on the primary side of the proposed converter due to the tolerance of the component value, they hardly worsen the CM noise. As a result, the proposed converter has a lower CM noise compared with the conventional converter.

Fig. 9 shows the measured efficiency of the prototype converters. The efficiency of the proposed converter is higher than that of the conventional converter under the entire output voltage conditions. The peak of the magnetizing current is proportional to the voltage across the transformer. The peak of the magnetizing current in the conventional converter is much larger than that in the proposed converter because the voltage across the transformer is two times larger in the conventional converter. Consequently, the large peak current results in the large turn-OFF loss of primary switches. Also, it leads to a large rms current flowing through the primary side, which brings the large conduction loss of the primary switches and circuit. The difference in the efficiency becomes more significant according to the increase of the output voltage because the influence of the conduction and turn-OFF losses grows.

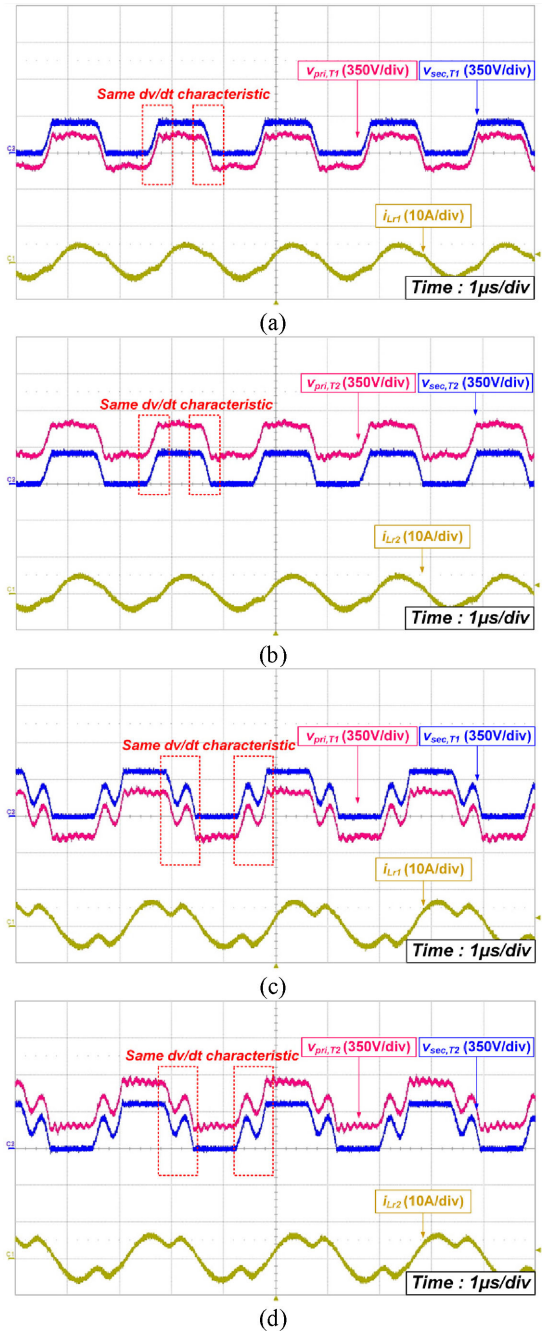

Fig. 8. Experimental waveforms of the proposed converter. (a) T_1 side at $V_o = 270$ V. (b) T_2 side at $V_o = 270$ V. (c) T_1 side at $V_o = 420$ V. (d) T_2 side at $V_o = 420$ V.

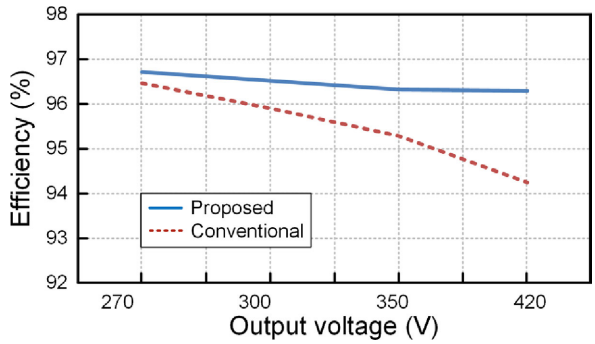

Fig. 9. Measured efficiency of prototype converters.

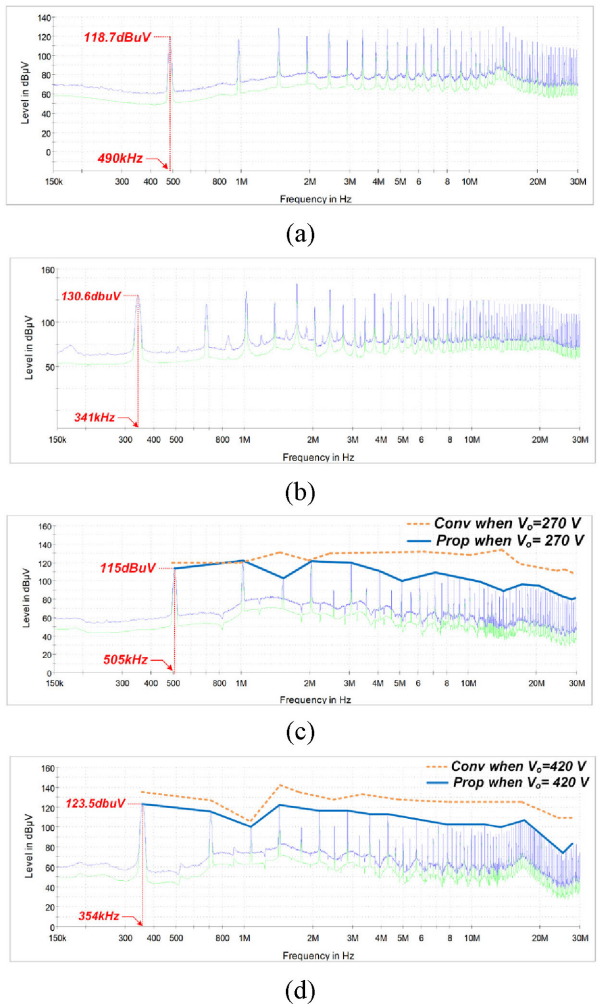

Fig. 10. Measured CM noise of prototype converters. (a) Conventional converter at $V_o = 270$ V (b) and at $V_o = 420$ V. (c) Proposed converter at $V_o = 270$ V (d) and at $V_o = 420$ V.

B. Comparison of CM Noise

In this article, there is an assumption that the CM noises generated from the parasitic capacitors of the primary switches are the same for the conventional FB *LLC* resonant and proposed converter. The CM noises generated from the parasitic capacitors of the primary switches are proportional to the capacitance and *dv*/*dt* difference between the parasitic capacitors. Capacitances are the same due to the same PCB layout and *dv*/*dt* differences are the same because the voltage waveforms across the parasitic capacitors of those components are the same. Thus, most of the CM noise differences come from the differences in the transformer structure and winding layout.

Fig. 10 shows the measured CM noise of the conventional FB *LLC* resonant and proposed converter without the EMI filter. At $V_o = 270$ V, the first peak is located around 500 kHz, which is the operating switching frequency in Fig. 10(a) and (c). In Fig. 10(b) and (d), the first peak is located around 350 kHz,

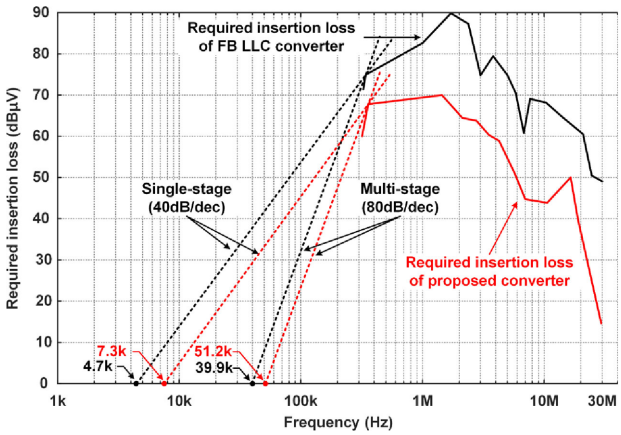

Fig. 11. Required insertion loss for the proposed converter and FB *LLC* resonant converter.

which is the operating switching frequency at $V_o = 420$ V. Most of the peak values appear at multiples of the switching frequency. The CM noise of the proposed converter has smaller peak values under almost the entire frequency range compared with the conventional converter. It means that the CM noise generated from the parasitic capacitors of the transformer is decreased because the voltage across the transformer fluctuates depending on the switching frequency.

C. Expected EMI Filter Design

To satisfy the EMI standard, the EMI filter should be employed and it is designed based on EN55022B standard in this article. According to Shih *et al.* [31], the required CM noise attenuation (insertion loss) $V_{\text{req·CM}}$ can be obtained as follows:

$$(V_{\text{req\_CM}})_{\text{dB}} = (V_{\text{meas,CM}})_{\text{dB}} - (V_{\text{Limit}})_{\text{dB}} + 3\ \text{dB} \quad (6)$$

where $V_{\text{meas,CM}}$ is the measured CM noise amplitude, V_{Limit} is the quasi-peak CM noise limit, and 3 dB is for the safety margin.

Fig. 11 shows the required insertion loss for the conventional FB *LLC* resonant and proposed converter at $V_o = 420$ V because this condition has the largest differences of the *dv*/*dt* characteristic at each layer of the transformer. Two types of the CM filter, which are single-stage *LC* and multistage *LCLC* CM filters, are widely used, and both filters will be discussed [32]. In the case of the single-stage *LC* CM filter, the relation between $V_{\text{req·CM}}$ and corner frequency $f_{R,\text{CM}}$ can be obtained as follows:

$$(V_{\text{req\_CM}})_{\text{dB}} = 40 \log\left(\frac{f_{\text{meas}}}{f_{R,\text{CM}}}\right) \quad (7)$$

where f_{meas} is the frequency at $V_{\text{meas,CM}}$.

Using (7), $f_{R,\text{CM}}$ of the proposed converter and that of the conventional FB *LLC* resonant converter is 7.3 and 4.7 kHz, respectively. Moreover, $f_{R,\text{CM}}$ is determined by the CM choke L_{CM} and *Y* capacitor C_Y as follows:

$$f_{R,\text{CM}} \approx \frac{1}{2\pi}\frac{1}{\sqrt{2L_{\text{CM}}C_Y}}. \quad (8)$$

According to (8), the size of L_{CM} can be reduced with high $f_{R,\text{CM}}$ and the size of L_{CM} is the most dominant factor of EMI filters. Thus, the EMI filter size can be reduced by 36% for the single-stage *LC* CM filter, as shown in Fig. 11. In the case of the multistage *LCLC* CM filter, the relation between $V_{\text{req·CM}}$ and $f_{R,\text{CM}}$ can be obtained as follows:

$$(V_{\text{req\_CM}})_{\text{dB}} = 80 \log\left(\frac{f_{\text{meas}}}{f_{R,\text{CM}}}\right). \quad (9)$$

Using (9), $f_{R,\text{CM}}$ of the proposed converter and $f_{R,\text{CM}}$ of the conventional FB *LLC* resonant converter are 39.9 and 51.2 kHz, respectively. Therefore, the EMI filter size is reduced by 22% for the multistage *LCLC* CM filter, as shown in Fig. 11.

IV. Conclusion

This article proposes a new structure and winding layout of the transformer to reduce the CM noise generated from the PT. The proposed converter can decrease the CM current between the primary and secondary layers in the transformer because the voltage waveforms of the adjacent two layers have the same *dv*/*dt* characteristic. It can be achieved by connecting the terminal of the transformers to the static point, which results in the static-point-connected transformer and aligning the layers to the appropriate position. Consequently, the proposed converter can improve the power density of the converter by reducing the size of the EMI filter.

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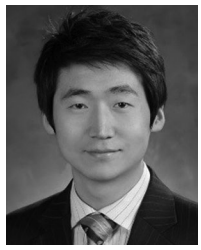

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