Letters

Gate-Drive Power Supply With Decayed Negative Voltage to Solve Crosstalk Problem of GaN Synchronous Buck Converter

Yu Chen, *Member, IEEE*, Ruwen Wang, Xinmin Liu, and Yong Kang

***Abstract*—Gallium-Nitride (GaN) transistor suits for high switching frequency condition to build high power density converters. However, it suffers from crosstalk problem especially in bridge-structure applications, that is, the fast voltage changing of the switching node causes a positive or negative voltage spike on the gate-source voltage of GaN transistor, which results in false turn-ON and gate breakdown of the transistor, respectively. Rather than specially designing the gate driver, this letter proposes an idea of using a gate-drive power supply (GDPS) with decayed negative output to solve the crosstalk problem. With the proposed GDPS, a negative driving voltage is provided when the positive voltage spike appears to avoid false turn-ON, and then the negative driving voltage naturally decays to zero before the negative voltage spike appears to avoid gate breakdown. Such a GDPS is realized by a simple forward-flyback topology, and the commercial gate-drive ICs can be cooperated with it conveniently. Experimental results show the effectiveness of the proposed method.**

***Index Terms*—Crosstalk, forward-flyback, Gallium-Nitride (GaN) transistor, gate-drive power supply (GDPS), synchronous buck converter.**

I. Introduction

NOWADAYS, power electronic converters are moving toward high power density. In order to improve power density of converters, the switching frequency should be increased to reduce the volume of passive components. Wide-bandgap devices, such as Gallium-Nitride (GaN) transistor, suit for this scenario. Compared with Si devices such as Si MOSFET, GaN transistor has much lower gate charge Q_g, zero gate-drain recovery charge Q_{rr}, and lower ON-state resistance $R_{\mathrm{ds(on)}}$, so it can switch faster with less switching and conduction losses [1], [2].

However, GaN transistor has higher switching speed, lower threshold voltage, and lower minimum allowable gate-source voltage, and thus it is severely affected by the crosstalk problem especially in bridge-structure applications. When a GaN transistor switches, a rapid voltage change of the switching node is caused, and an unwanted positive voltage spike or negative voltage spike appears on the gate-source voltage of its complementary switch [3], [4]. The positive voltage spike may exceed the threshold voltage V_{th}, causing false turn-ON. Therefore, a bipolar gate-drive power supply (GDPS) is usually needed to provide a negative driving voltage, reducing the potential of the positive voltage spike to avoid false turn-ON. However, when the negative voltage spike appears, the superposition of the negative voltage spike and the negative voltage may exceed the minimum allowable gate-source voltage of GaN transistor, resulting in gate breakdown [5].

To solve the contradiction above, many driving circuits have been presented. A complete driving circuit includes a gate driver and a GDPS, and the researchers usually focus on the gate driver design, considering the GDPS as a standard device. One kind of method is to reduce the switching speed of the switch which causes crosstalk. Increasing the turn-ON/turn-OFF gate-resistance and paralleling an external gate-source capacitor can decrease the switching speed; however, it increases the switching loss. Another kind of method is to enhance the noise-immune ability of the switch suffering from crosstalk. Paralleling an external gate-source capacitor can decrease the amplitude of voltage spikes while it brings in additional switching losses [4], [5]. Adding auxiliary circuit or changing gate-resistance can offer a low impedance path and thus can decrease both of the positive and negative voltage spikes [6]–[10]. Multilevel gate driver can also be utilized to increase the safe driving voltage margin [11]–[13]. For example, Zhang *et al.* [11] and Zhang *et al.* [12] used a full bridge structure to introduce multilevel driving voltage, and He *et al.* [13] used a voltage divider to split the voltage of the GDPS into a positive voltage and a negative voltage, and then used an extra switch to discharge the negative voltage capacitor. However, the methods above need to specially design the gate driver, and it is more likely to introduce stray parameters between the driven switch and the GDPS because the gate drivers are more complicated.

Noticing that the output voltage of the gate driver can also be controlled by its GDPS, we therefore propose to solve the crosstalk problem by designing the GDPS. Different from the existing power supplies with regulated and constant

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Yu Chen, Ruwen Wang, Xinmin Liu, and Yong Kang are with the State Key Laboratory of Advanced Electromagnetic Engineering and Technology, Hubei 430074, China, and also with the School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Hubei 430074, China (e-mail: ayu03@163.com; rwwang@hust.edu.cn; lxmhust@hust.edu.cn; ykang@hust.edu.cn).

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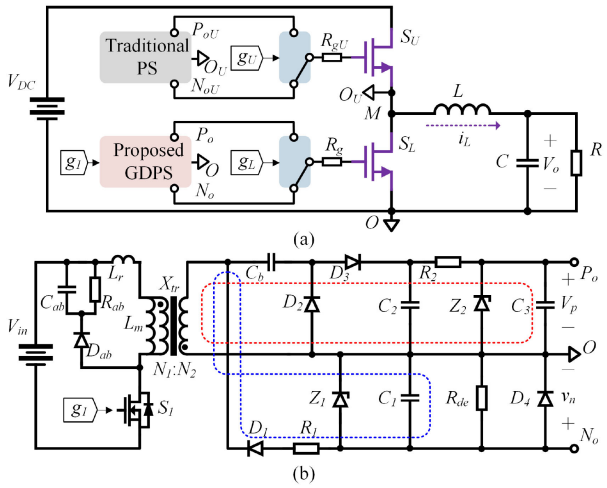

Fig. 1. Topologies of (a) synchronous buck converter and (b) proposed GDPS.

multioutputs [1], [14]–[17], a negative voltage is generated by the proposed GDPS when the positive voltage spike appears to avoid false turn-ON, and then the negative voltage naturally decays to zero before the negative voltage spike appears to avoid gate breakdown. The contributions of this letter are as follows.

1) Rather than designing the gate driver [6]–[13], the proposed method solves the crosstalk problem through designing the GDPS. The commercial gate-drive ICs can be utilized, and hence the complexity and stray parameters resulted from the gate driver can be avoided.
2) Rather than obtaining the multilevel voltage by extra active switches [11]–[13], the proposed GDPS provides a decayed negative voltage. By cooperating with the commercial gate-drive ICs, the multilevel driving voltage can be obtained and it is always under the right potential when the positive and negative crosstalk occur.
3) Compared with the existing multioutput forward or flyback converters [1], [14]–[17], the proposed GDPS is simpler since it fully uses the nature of forward-flyback and voltage doubler structures, and thus, only one active switch and one winding are required.

The rest of this letter is organized as follows. In Section II, the proposed GDPS is introduced and a synchronous buck converter with the proposed GDPS is analyzed. In Section III, the experimental prototype is built to verify the validity. Finally, the conclusion is given in Section IV.

II. Proposed GDPS

A. Topology Description

Fig. 1(a) shows a synchronous buck converter. S_U is the control switch; S_L is the synchronous switch; L is the inductor; and C is the output capacitor. The drivers of S_U and S_L are supplied by a traditional PS (power supply) and the proposed GDPS, respectively. Fig. 1(b) shows the topology of the proposed GDPS. It contains one transformer $X_{\rm tr}$ (with turn ratio $N = N_1{:}N_2$, where N_1 and N_2 are the winding turns of the primary side and secondary side, respectively), and one switch S_1 on the primary side. With capacitor C_b, diodes D_2 and D_3, a voltage doubler circuit is structured and two independent loops, i.e., the positive loop (the red path) and the negative loop (the blue path), are formed to generate the positive constant voltage V_p and the decayed negative voltage v_n, respectively. The gating signal g_1 of S_1 is cooperated with g_U (the gating signal of S_U). C_2, C_3, and C_b are relatively large (μF magnitude) to keep V_p constant. C_1 is relatively small (several nF) to ensure the fast-generating and rapid-decay of v_n. Resistor R_2 and Zener diode Z_2 are used to fine-tune V_p, and resistor R_1 and Zener diode Z_1 are used to fine-tune v_n. In addition, C_{ab}, R_{ab}, and D_{ab} form a snubber to absorb the energy stored in leakage inductor L_r. D_4 is used to clamp v_n, and $R_{\rm de}$ is used to accelerate the decay.

B. Operation Modes

Fig. 2 shows the operation modes. The fine-tuning circuit (R_2 and Z_2) are merged as the load of V_p and the snubber is ignored for simplification. Fig. 3 shows the key waveforms. Besides, only the continuous current mode (CCM) of the synchronous buck converter is considered in this letter and the direction of the inductor current, i_L, stays the same. Before Mode I, S_U is OFF and S_L is ON; i_L flows through S_L. The voltage of C_1 is stabled at V_{n0}.

Mode I [t_0, t_1]: At t_0, the gate signal $g_L = 0$ and point G connects to point N. The turning-OFF loop (including gate-source capacitor C_{gsL}, gating resistor R_g, parasitic inductor L_g, the gate-drive IC, and C_1, see the green line) is formed. Since C_1 is small, it is discharged quickly and v_n decays to zero from negative value rapidly. However, since S_1 is still in ON-state ($g_1 = 1$), C_1 gets energy supplement from the PS $V_{\rm in}$ through the negative loop (see the blue line) and v_n can be recovered to V_{n1} at t_1. At the same time, the loop including the secondary winding, D_2 and C_b is formed (see the red line), and C_b is charged for later boost purpose.

For the synchronous buck converter, although S_L is in OFF-state, i_L can still flow through S_L in the reverse direction.

Mode II [t_1, t_2]: At t_1, the gate signal $g_1 = 0$ so S_1 is turned OFF. The energy stored in the magnetic inductance L_m of transformer $X_{\rm tr}$ transfers to C_2 through the positive loop (see the red line). Since C_b is in series in the loop, V_p is boosted to a high level to adapt the requirement of turning-ON. At the same time, since no energy can be sent to C_1 through the negative loop, the negative output v_n decays naturally from V_{n1} to zero.

In addition, at t_1, the gate signal $g_U = 1$ and S_U is turned ON. v_M (the voltage potential of node M) steps from zero rapidly with high dv/dt, causing charging current of the gate-drain capacitor C_{gdL} and the drain-source capacitor C_{dsL} of S_L. Part of the charging current flows through the turning-OFF loop (see the green line), resulting in a positive voltage spike $v_{\rm sp+}$ on R_g and L_g. However, since v_n is now the negative V_{n1}, the gate-source voltage $v_{gsL} = V_{n1} + v_{\rm sp+}$ is always below $V_{\rm th}$. After t_1, v_n decays to zero. Since no more positive voltage spike will appear, such a zero gate-source voltage is safe.

For the synchronous buck converter, S_U is always ON after t_1 so i_L flows through it in this mode. Since S_L is always OFF in

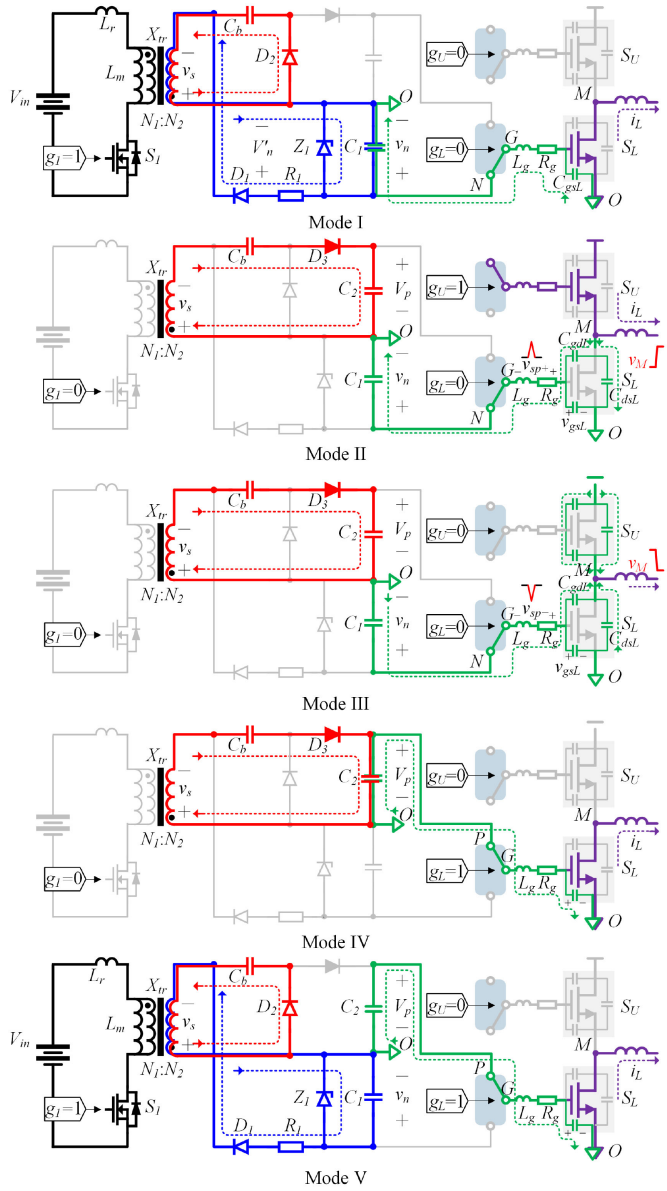

Fig. 2. Equivalent circuits of operation modes.

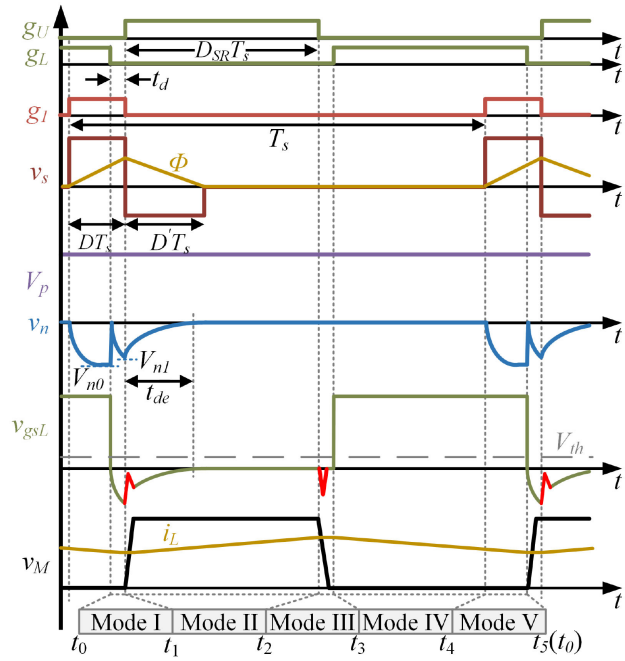

Fig. 3. Key waveforms of the proposed GDPS and the synchronous buck converter.

this mode, the delay of g_1 and the turn-OFF performance of S_1 will not affect the operation of the synchronous buck converter.

Mode III [t_2, t_3]: At t_2, the gate signal $g_U = 0$ and S_U of the synchronous buck converter is turned OFF. i_L charges the parasitic capacitors of S_U and discharges C_{dsL} and C_{gdL} of S_L. The discharging current flowing through C_{gdL} and the turning-OFF loop causes a negative voltage spike $v_{\mathrm{sp}-}$ on R_g and L_g (see the green line). Since v_n has decayed to zero before t_2, $v_{gsL} = 0 + v_{\mathrm{sp}-}$ (where $v_{\mathrm{sp}-}$ is negative value) can be far away from the minimum allowable gate-source voltage, protecting the transistor from gate breakdown.

Mode IV [t_3, t_4]: At t_3, C_{dsL} is fully discharged to zero, and the gate signal $g_L = 1$ can be applied (the point G turns to point P). The turning-ON loop (including gate-source capacitor C_{gsL}, gating resistor R_g, parasitic inductor L_g, the gate-drive IC, and C_2, see the green line) is formed and gets energy from C_2. Therefore, S_L is turned ON and i_L flows through it to achieve synchronous rectification. Since v_M is almost unchanged, no voltage spike appears on the gate-source voltage of S_U.

Besides, the energy stored in L_m might be run out during mode II, mode III, or mode IV. After that, the positive loop (see the red line) is cut off and no energy is sent to C_2. However, stable V_p can still be guaranteed since the capacitance of C_2 is large.

Mode V [t_4, t_5]: At t_4, the gate signal $g_1 = 1$ and S_1 is turned ON. C_1 is charged again through the negative loop (see the blue line). Since C_1 is relatively small, it is charged rapidly and then v_n is stable at V_{n0}, preparing the initial voltage for the next cycle. At the same time, C_b is charged through the secondary side of X_{tr} and D_2 (see the red line).

Since S_L is always on in this mode, the delay of g_1 and the turn-ON performance of S_1 will not affect the operation of the synchronous buck converter.

C. Parameter Design

During mode I and mode V, S_1 is in ON-state. Since the ON-resistance of S_1 is small, it is ignored during analysis. The increment of Φ can be expressed as

$$\Delta\Phi_+ = (V_{Cb} + V_D)DT_s/N_2 \tag{1}$$

where D is the duty cycle of g_1; T_s is the period of proposed GDPS; V_D is the forward voltage of diode D_2; and V_{Cb} is the voltage of C_b. V_{Cb} is constant since C_b is relatively large and can be expressed as

$$V_{Cb} = V_{\mathrm{in}}L_m/[N(L_m + L_r)] - V_D. \tag{2}$$

During modes II, III, and IV, S_1 is in OFF-state and the decrement of Φ can be expressed as

$$\Delta\mathbf{\Phi}_- = (V_p - V_{Cb} + V_D)D'T_s/N_2 \tag{3}$$

where $D^{'}$ is the duty cycle that energy transfers to the positive loop. Since $\Delta\mathbf{\Phi}_+ = \mathbf{\Delta\Phi}_-$, $D^{'}$ can be derived as

$$D' = D(V_D + V_{Cb})/(V_D + V_p - V_{Cb}). \tag{4}$$

To achieve the working condition in Fig. 3, i.e., $\mathbf{\Phi}$ decreases to zero before t_4, $D^{'} < 1-D$ needs to be met.

P_p, the dissipative power of V_p, can be expressed as V_pI_p, where I_p is the average dissipative current and should be equal to the average current flowing into C_2. Therefore

$$P_p = V_pI_p = V_pI_{s\max}D'/2 \tag{5}$$

where $I_{s\max}$ is the maximum current of the secondary side, and $I_{s\max} = NI_{p\max} = N\left[V_{\text{in}}DT_s\,/\,(L_m + L_r)\right]$. With (2), (4), and (5), V_p can be derived as

$$V_p = \frac{2P_p(L_m + L_r)(L_mV_{\text{in}} - 2L_mNV_D - 2L_rNV_D)}{2P_pNL_m^2 + 2NP_pL_r^2 + 4NP_pL_mL_r - ND^2V_{\text{in}}^2T_sL_m}. \tag{6}$$

Thus, to generate the desired V_p, the corresponding duty cycle D can be derived from (6) as

$$D = \sqrt{\frac{2P_p(L_m + L_r)[N(L_m + L_r)(2V_D + V_p) - L_mV_{\text{in}}]}{L_mNT_sV_{\text{in}}^2V_p}}. \tag{7}$$

Meanwhile V_n', the voltage of negative loop before fine-tuning (see the blue line in mode I of Fig. 2), can be expressed as $-V_{Cb}$. In addition, to get the desired V_{n1} through fine-tuning by R_1 and Z_1, $V_n' \geq V_{n1}$ should be met.

Besides, the decay time t_{de} can be calculated as

$$t_{\text{de}} = 3R_{n\text{eq}}(C_1 + C_{gsL}) \tag{8}$$

where $R_{n\text{eq}}$ is the equivalent resistor of the negative loop and t_{de} can be shorten through paralleling an energy releasing resistance R_{de} with C_1, which is equivalent to decreasing $R_{n\text{eq}}$.

Furthermore, D_{SR}, the duty cycle of the synchronous buck converter, should satisfy $t_{\text{de}}/T_s < D_{\text{SR}} < 1 - D$. Otherwise, v_n would still be negative when S_U is turned OFF, as the counterexamples shown in Fig. 4. In such cases, the negative voltage spike resulted from the turn-OFF process would be superposed on the negative v_n, increasing the risk of gate breakdown.

III. Experimental Verification

A. Parameters and Design Considerations

To verify the effectiveness of the proposed GDPS, a prototype is built, as shown in Fig. 5(a) and (b). The key parameters of the proposed GDPS and the synchronous buck converter are listed in Table I, and the control signals g_U, g_L, g_1 are all generated by DSP TMS320F28377S. The switching frequency is 500 kHz. The minimal switching transient of GaN transistor is about 5.4 ns, which results in serious crosstalk problem to the synchronous switch S_L. Therefore, the proposed GDPS is used to supply the gate driver of S_L in the prototype.

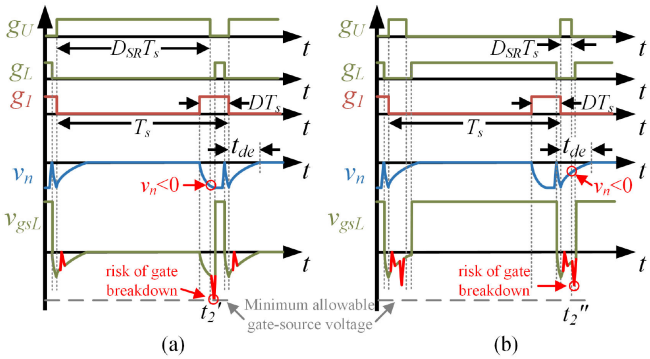

Fig. 4. Key waveforms (a) when the restriction $D_{\text{SR}} < 1-D$ is not satisfied and (b) when the restriction $t_{\text{de}}/T_s < D_{\text{SR}}$ is not satisfied.

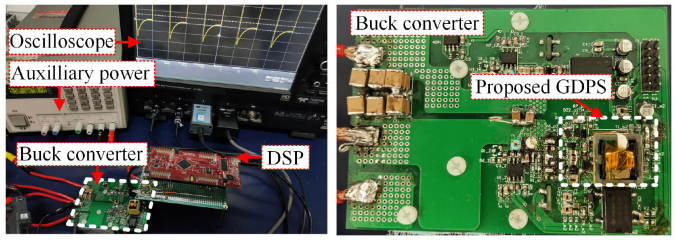

Fig. 5. Photographs of (a) prototype and (b) details of the synchronous buck converter.

TABLE I
Parameters of the Proposed GDPS and the Synchronous Buck Converter

Parameter	Value	Parameter	Value
S_U and S_L	GS66508T	Driver IC	Si8271
S_1	SQ2348ES	V_{DC}	300V
V_0	130V	T_s/f_s	2μs/500kHz
D_{SR}	0.45	R_{gon}	12Ω
R_{goff}	2Ω	L	176μH
t_{d}	60ns	V_{in}	5V
L_m	20μH	L_r	3μH
N	1	V_D	0.32V
D	0.16	C_1	2.2nF
C_2	30μF	C_3	30μF

Since the switching speed of GaN transistor is fast, the switching speed of S_1 should be comparable so that it can cooperate better with the GaN transistor. Fortunately, the operation voltage of the GDPS is low, and thus low-voltage Si MOSFET can meet the requirement above. SQ2348ES, a low-voltage Si MOSFET, is chosen as S_1 in our design. The rise time and fall time given in the datasheet are 8 and 6 ns, respectively, which approach to the switching performance of the GaN transistor. In addition, since the gate charge and ON-resistance of S_1 are about 8 nC and 0.032 Ω, respectively, and the operating current of the proposed GDPS is very small, the calculated switching loss is as low as 20 mW.

According to the analysis in modes II and V, the switching performance of S_1 will not affect the operation of the synchronous buck converter. However, C_1 should adapt to the deadtime since it is recharged during the deadtime period. With the parameters of the experimental prototype, $C_1 = 2.2$ nF is chosen so that

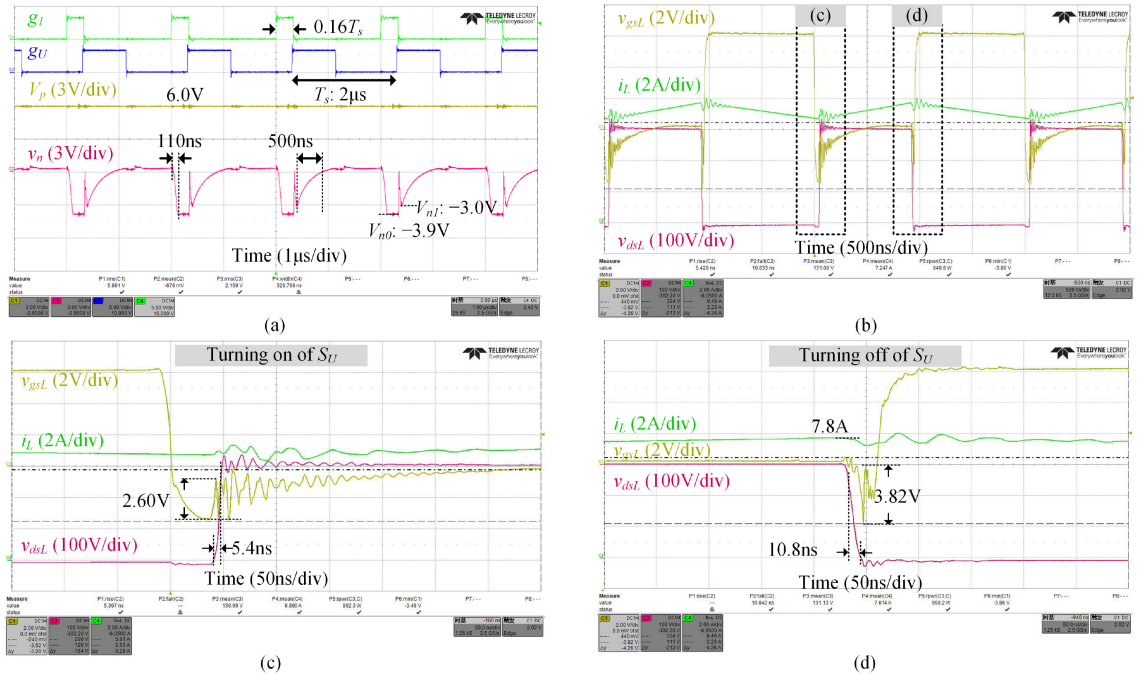

Fig. 6. Waveforms of (a) control signals and the proposed GDPS and (b) synchronous buck converter; the detailed waveforms of (c) turning ON of S_U and (d) turning OFF of S_U.

v_n can reach the desired value V_{n1}. D is set as 0.16 to get the desired $V_p = 6.2$ V; V_n' can be calculated as -4.03 V, so that Z_1 can fine-tune the negative voltage v_n; $t_{\rm de}$ is chosen as 500 ns; so, $R_{\rm de} = 200\ \Omega$ is paralleled with C_1. P_p can be estimated to be 60 mW. Besides, the restriction for $D_{\rm SR}$ can be calculated as $0.25 < D_{\rm SR} < 0.84$. It implies that the synchronous buck converter can adapt to the wide range change of the input or output voltage in most of the CCM applications.

B. Experimental Results

The waveforms of the proposed GDPS are shown in Fig. 6(a). It can be seen that g_1 is ahead of g_U. When g_1 is high, v_n increases to -3.9 V in 110 ns, and rapidly decays to zero due to the turning-OFF of S_L. However, v_n can recover fast since the GDPS still works under forward mode, so $V_{n0} = -3.0$ V can be obtained when S_U is turned ON. It is seen that v_n decays to zero before S_U is turned OFF with $t_{\rm de} = 500$ ns. At the same time, V_p keeps constant at 6.0 V. Above phenomena are consistent with our design.

Fig. 6(b) shows the waveforms of the synchronous buck converter (working under 300 V, 7.25 A), with details in Fig. 6(c) and (d). Fig. 6(c) shows the turning-ON process of S_U. When S_U is turned ON, v_M rises from 0 to 300 V in 5.4 ns ($dv/dt = 55.6$ V/ns), and a positive voltage spike with the amplitude of 2.60 V appears. However, the negative voltage $V_{n1} = -3.0$ V has been prepared, so v_{gsL} is lower than -0.40 V. Since the parasitic inductance exists in the turning-ON loop, a high-frequency oscillation on v_{gsL} can be observed, however, v_{gsL} can always be lower than 0 V. Fig. 6(d) shows the turning-OFF process of S_U. When S_U is turned OFF, $i_L = 7.8$ A charges and discharges the parasitic capacitances of S_U and S_L, respectively, making v_M vary from 300 to 0 V within 10.8 ns ($dv/dt = 27.8$ V/ns). A negative voltage spike with the amplitude of 3.82 V appears. Since v_n has already decayed to zero, v_{gsL} is within the maximum negative voltage limitation with sufficient margin. The above phenomena match well with the analysis, and the GaN transistor has been well protected.

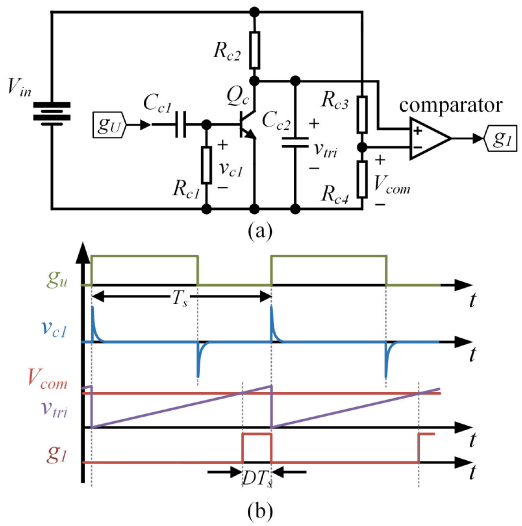

Fig. 7. Simple circuit to generate g_1 according to g_U. (a) Circuit diagram. (b) Key waveforms.

C. Discussion

In order to provide the right potential of v_n for the gate driver when the positive voltage spike or the negative voltage spike appears, the frequency of g_1 should be exactly the same as the frequency of the synchronous buck converter. When the working frequency of the synchronous buck converter changes, the

parameters of the proposed GDPS should be fine-tuned according to part *C*, Section II, and g_1 should also be generated properly. Nevertheless, the generation of g_1 is easy. In our experiment, g_1 is generated conveniently by an ePWM unit in the same DSP that is used to generate g_U and g_L. If g_U and g_L are generated by the analog methods, the simple circuit shown in Fig. 7(a) can be used to generate g_1 according to g_U, and the key waveforms are shown in Fig. 7(b). When g_U is inputted, the high-pass filter (C_{c1} and R_{c1}) outputs a positive pulse v_{c1} which is aligned with the rising edge of g_U. v_{c1} triggers the transistor Q_c to discharge C_{c2} rapidly. After discharging, $V_{\rm in}$ charges C_{c2} again through R_{c2}, and $v_{\rm tri}$, the voltage across C_{c2}, increases almost linearly until the next positive pulse v_{c1} appears. A constant voltage $V_{\rm com}$ is formed by the voltage divider (R_{c3} and R_{c4}), and therefore, g_1 can be generated through comparing $v_{\rm tri}$ with $V_{\rm com}$ by the comparator, and the duty cycle *D* can be fine-tuned by $V_{\rm com}$.

IV. Conclusion

To solve the crosstalk problem in GaN synchronous buck converter, this letter proposes a method based on a GDPS with forward-flyback topology. The proposed GDPS can provide a constant positive 6.0-V voltage and a decayed negative output voltage. A -3.0-V negative driving voltage is provided when the positive voltage spike resulted from crosstalk appears, and the gate-source voltage is lower than 0 V to avoid false turn-ON. This -3.0-V voltage then decays to 0 V before the negative voltage spike appears to avoid gate breakdown. The loss of the GDPS in our experiments is about 24 mW. The proposed GDPS is low-cost and simple-structured, and can be cooperated with the commercial gate-drive ICs conveniently.

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