Extended Range Bridgeless PFC Converter With High-Voltage DC Bus and Small Inductor

Hamed Valipour, *Graduate Student Member, IEEE*, Mohammad Mahdavi, Martin Ordonez, *Member, IEEE*, Peter F. Ksiazek, *Member, IEEE*, and Rahul Madhav Khandekar, *Member, IEEE*

***Abstract*—Utility power lines voltage levels vary in different geographical locations, ranging from 208 to 480 $V_{\rm rms}$. Power factor correction (PFC) converters are typically designed for a particular input voltage and do not accept a wide range of line voltages. This results in multiple product designs and revisions and increased production costs to accommodate the various ac voltage levels used around the world. A PFC converter capable of coping with a wide input voltage range, from 90 $V_{\rm rms}$ up to 530 $V_{\rm rms}$, would significantly decrease costs and streamline development. In this article, an extended input voltage range PFC converter is proposed, which provides a high and almost flat efficiency curve throughout the entire operating voltage range with an 800 $V_{\rm DC}$ bus voltage. The proposed converter has a flexible bridgeless structure with simple control, low-current ripples, low common mode noise, and startup inrush current handling capabilities. Theoretical analysis and waveforms are discussed and experimental results for a 2-kW prototype are given, thereby validating the expected behavior. The operation of the proposed extended input voltage range PFC converter is also compared to the traditional totem-pole PFC showing more than 1% efficiency improvements at full load and a higher power factor in the proposed design.**

***Index Terms*—AC/DC converter, boost, bridgeless, extended range input voltage, power factor correction (PFC), wide input voltage range.**

I. Introduction

POWER factor correction (PFC) circuits are widely used due to the restrictions enforced by the standards, for instance IEC61000-3-2 [1]. In grid-connected applications, such as telecommunication systems, electric vehicle (EV) chargers, and energy storage systems, the requirements of these standards must be met [2]–[5]. The utility power lines typically are 208, 230, 240, 277, or 480 $V_{\rm rms}$ in different geographic locations depending on the power system configuration [6]. For example, in some areas, there are only delta connections available for the use of grid-connected converters without access to neutral. In some other areas, star connections are also available even sometimes with split phase connections. The required input voltage range to support all of these line voltages is 208 $V_{\rm rms}-10\%$ to 480 $V_{\rm rms}+10\%$. The required converter should be able to operate from 187 to 530 $V_{\rm rms}$ with full power range and from 90 to 187 $V_{\rm rms}$ with a derated power range. The derated power range is required in split phase connections. Therefore, the required range of operation is from 90 $V_{\rm rms}$ to 530 $V_{\rm rms}$. Traditionally, due to the wide range of voltage levels, different designs are used. This results in multiple stock keeping units of products for different applications [7].

With this wide input voltage range (90–530 $V_{\rm rms}$), each ac/dc converter may need to operate with a 530 $V_{\rm rms}$ input feed requiring a PFC boost converter to deliver an 800 $V_{\rm DC}$ link. This high-voltage bus decreases the efficiency in the boost converter in lower line voltages. Therefore, the PFC converter cannot maintain a high efficiency through a wide input range. There are limited solutions in the literature to maintain a high efficiency in a very wide input voltage range while simultaneously providing unity power factor at the input [7]–[9].

A wide input voltage range PFC converter based on a flying capacitor converter is proposed in [8] with 200 $V_{\rm rms}$ and 415 $V_{\rm rms}$ as input voltages. This converter topology exerts a low voltage stress on the semiconductors and requires only a small inductor. However, the measured efficiency is low, the number of the components is high, and the control algorithm is complicated with balancing issues for the output capacitors. A high-voltage power converter with a configurable input is proposed in [7] to support a wide range of input voltages from 180 to 528 $V_{\rm rms}$. This converter changes its configuration in different input voltages using additional switches at the input. The voltage stress of the semiconductors in this converter is low, and the inductor size is small. However, the number of the components is high and requires two isolated dc/dc converter after the PFC stage. This converter also suffers from inrush current issues at startup and common-mode interferences in its current form, but can be modified to solve these issues. An adaptive PFC converter is proposed in [9] with $80-520$ $V_{\rm rms}$ input voltage range, which changes its structure in different input voltages with a range switch. This converter has a simple and effective structure as well as a small inductor in its design. Nonetheless, this structure does not regulate the output voltage in the whole input voltage range, which transfers the regulation burden to the dc/dc stage. Also, this structure does not provide a common-mode connection

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Hamed Valipour, Mohammad Mahdavi, and Martin Ordonez are with the Electrical and Computer Engineering Department, The University of British Columbia, Vancouver, BC V6T 1Z4, Canada (e-mail: hvalipour@ece.ubc.ca; mahdavi@ece.ubc.ca; mordonez@ieee.org).

Peter F. Ksiazek and Rahul Madhav Khandekar are with the Alpha Technologies, Ltd., Burnaby, BC V6T 1Z4, Canada (e-mail: Peter.Ksiazek@alpha.ca; Rahul.Khandekar@alpha.ca).

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between the input and output ports in some of its operational modes in which it needs some modifications. In addition to the previous characteristics, the converters in [7]–[9] all have additional losses because of the full-bridge diode rectifier as their input stage.

There are also other types of converters in the literature, which exhibit some useful features in a wide input voltage range applications, but have not been tested in the required range ($90-530\ V_{\rm rms}$) [10]–[27]. SEPIC, CUK, and buck–boost converters can be used for the wide-input range application [10]–[14]. These types of converters can have a lower bus voltage compared to the boost-typed converters. On the other hand, the voltage and current stress on the semiconductor switching elements is higher resulting in increased conduction losses; therefore, these types of structures are not suitable for higher power applications. Buck and boost converters are other candidates that utilize a lower bus voltage as proposed in [15] and [16]. These converters can have a good performance under wide input conditions, but they have a two-stage structure in their PFC platform alone, which needs more components with more conduction losses. Flexible PFC converters can be employed as in [17]–[23]. The voltage stress of the semiconductors in these converters is low, and the inductor size is small; however, the number of the components is higher than the other options. These converters also suffer from complex control algorithms, inrush current issues at startup, and common-mode interferences in their current version. The last two features can be solved by some additional hardware. These restrictions limit the usage of these kinds of structures in the wide input range PFC applications. Other types of configurable boost converters can also be employed in wide range PFC applications proposed in [24]–[26]. The interesting circuit presented in [24] changes its structure in different input voltage levels to provide high efficiencies throughout the entire operating range. This converter also provides common-mode connection with a new selection of components in the design. Nonetheless, this converter cannot improve the inductor current ripple in high input voltages, which is the same performance as the boost converter. A variable dc-link approach has been used in the PFC converter proposed in [27]. In this converter, the dc-link voltage changes based on the input voltage value, which helps to keep the efficiency high and inductor ripples low under different conditions. This converter, however, transfers the wide gain regulation to the dc/dc stage and requires further control implementation. Therefore, new methods should be used in the isolated dc/dc converters as the second stage to regulate the output voltage with high changes in the dc bus voltage [28]–[33].

Loads with high-power levels use a high dc bus voltage in order to maintain reasonable current magnitudes. Recently, $800\ V_{\rm DC}$ bus voltage is gaining acceptance in the EV market because of weight savings across the vehicle as well as reduced battery charging times [34], [35]. Therefore, a solution with this high-voltage dc bus and wide gain can support the input voltage range variations for high-power applications.

In this article, an extended input voltage range PFC converter is proposed to support the wide input voltage range from 90 to $530\ V_{\rm rms}$. The proposed converter maintains a high efficiency throughout the wide input range and features low input current ripple, which translates into low conduction losses and low total harmonic distortion (THD). Reduced ripple in the inductor current enables the designer to use a smaller inductor in the design compared to a traditional boost converter. In addition, the proposed converter has a path for inrush current at startup and during line surges, and line-frequency connection between the input and output ports, which reduces the common-mode noise. The last two features are beneficiary for an industrial PFC solution. Moreover, the presented converter has a flexible and bridgeless structure in hardware and requires simple control strategies. The proposed converter structure is shown in Fig. 1. Two different modulation schemes are presented in this article for the proposed extended input voltage range PFC structure.

In Section II, the operation of the proposed converter is described along with the related equations. Section III describes the modulation methods as well as the control loop of the proposed converter. Design considerations have been presented in Section IV. Loss breakdown of the selected components has been done in Section V. Experimental results are shown in Section VI for a 2-kW prototype. As part of the validation, the current ripple of the proposed converter, the efficiency,the power factor, and THD have been compared with the traditional totem-pole boost PFC converter's as a benchmark in different input voltages and output power levels.

II. Principles of Operation

In this article, an extended range PFC converter is proposed to support a wide input voltage variation ($90-530\ V_{\rm rms}$). The proposed converter needs a small inductor for its operation in the wide range because of the reduction in the inductor's current ripples. Therefore, the proposed converter can provide a high-efficiency curve in the whole wide input voltage range. The proposed converter has a flexible structure in different input voltages with a bridgeless configuration that can generate a high-voltage dc bus in the output with $800\ V_{\rm DC}$. The extended input voltage range PFC converter has a line frequency connection between the input and output-voltage ports in all of the operating modes resulting in low common-mode noise issues. In addition, the proposed converter has the ability to handle inrush currents to protect the critical components and also to prevent over voltages. In this section, the operation of the proposed converter is studied in different operating modes.

Boost-type converters are conventionally used for PFC applications. In boost-type PFC converters, output voltage cannot be less than the input voltage peak. Therefore, for a wide range of variation in the input voltage ($90-530\ V_{\rm rms}$), the bus voltage cannot remain $400\ V_{\rm DC}$ as in the traditional boost converters. However, the bus voltage can be selected to be $800\ V_{\rm DC}$. In this case, converting $90\ V_{\rm rms}$ to $800\ V_{\rm DC}$ reduces the efficiency drastically in the boost converter. In order to solve this problem, the boost structure can be changed into a voltage doubler boost converter in low line voltages. This helps the boost converter to work with half of the bus voltage at low input voltages in each half-line cycles. This reduces the conduction losses resulting in

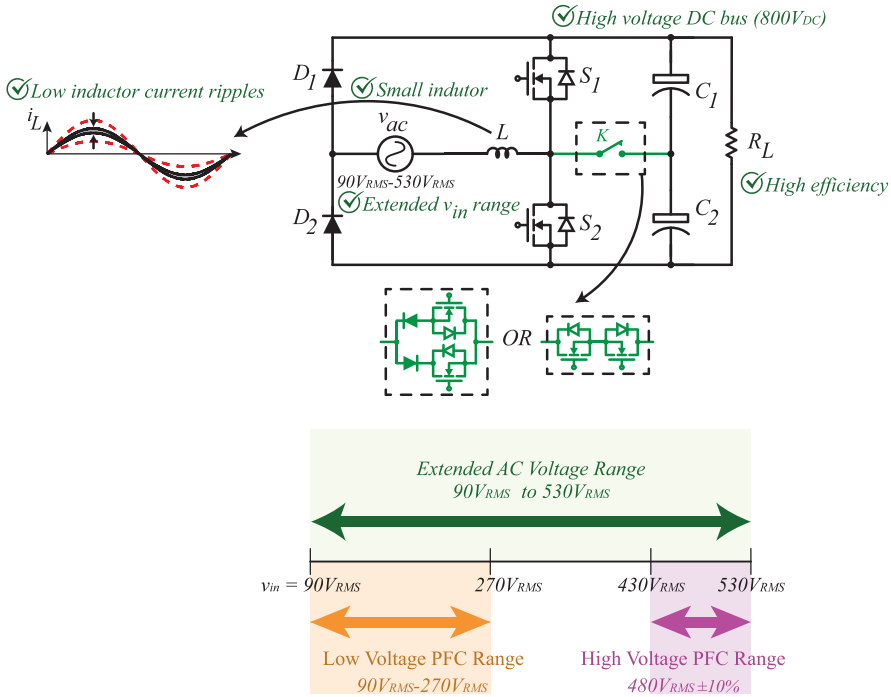


Fig. 1. Proposed extended input voltage range PFC converter.

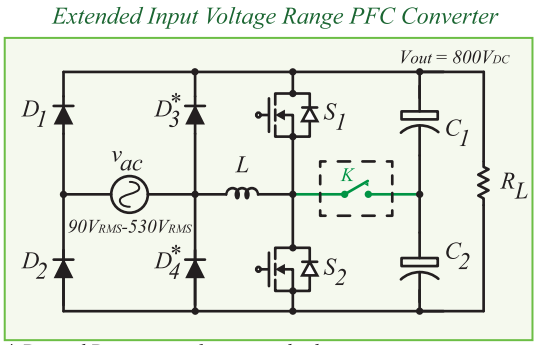
the efficiency to increase significantly [36]. In this article, a new structure has been proposed to support the mentioned wide input voltage range with high efficiencies, as shown in Fig. 1. With different control strategies, the current ripple in the inductor of the converter can be limited, which is an important characteristic resulting in reduction of the size of the inductor, the THD, and also increasing the efficiency even with an 800 V_{DC} bus voltage.

The structure of the proposed converter can be seen in Fig. 1. As seen in Fig. 1, D_1 and D_2 are the slow diodes, rectifying the input voltage in negative and positive half-line cycles, respectively. L is the inductor of the structure. S_1 and S_2 are the semiconductor switches. Output capacitors C_1 and C_2 are placed to filter out the line frequency ripple and the high-frequency switching ripples. The proposed structure has been shown in Fig. 2(a) with more details. Diodes D_3 and D_4 in Fig. 2(a) are also line frequency diodes to limit the impact of the surge current from the source. In other words, these two components are not working in the steady-state operation of the converter and, thus, operate only when there is an inrush current flowing from the source. With the help from these two elements along with D_1 and D_2, the converter elements are not exposed to the high-stress situations caused by inrush and surge currents. For example, during startup, the inrush current flows through D_1-D_4 to charge the output capacitors, which prevents the sensitive high-frequency switches from being exposed to this current pulse and does not allow the output capacitors to resonate with the input inductor, which prevents the output voltage from exceeding the input voltage peak value at the startup [37].

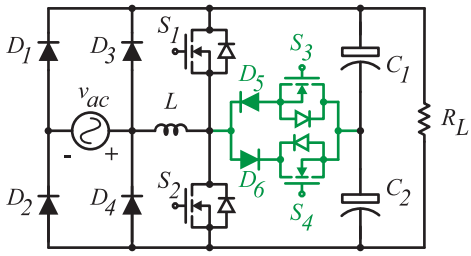
Two different modulations are tested in the proposed converter in Fig. 2(a). The requirements for the semiconductors are different for each of these modulation methods. Therefore, there are two options for the switch network K shown in Fig. 2(b) and (c). In the first option shown in Fig. 2(b), two parallel unidirectional paths each comprising one diode and one switch (S_3 with D_5, S_4 with D_6) replaced K. In the second option demonstrated in Fig. 2(c), two back-to-back switches (S_5 and S_6) are used to support the bidirectional flow of the current. These two modulations are described in the next two sections with related states of operation and equations. In order to make the analysis straightforward, the equivalent series resistors of the capacitors and the inductor are neglected. In addition, for simplifying the analysis, semiconductors are assumed to be ideal. It is also assumed that $C_1 = C_2$; therefore, the steady-state voltage across each of these capacitors is equal to half of the output voltage.

A. First Modulation Method: Low-Frequency Middle Switch

The first modulation method is shown in Fig. 3. The proposed converter has two different modes of operation when operating with the low-frequency middle switch method. The presented structure works like a bridgeless voltage-doubler boost converter at low line voltages ($v_{\mathrm{inpeak}} < \frac{V_{\mathrm{out}}}{2}$). In this modulation method, the bidirectional middle switch, comprising S_3, S_4, D_5, and D_6, is switched ON and OFFin the middle of the half-line cycles at high-voltage levels ($v_{\mathrm{inpeak}} > \frac{V_{\mathrm{out}}}{2}$). With this method, the input current ripples are reduced in high-voltage mode compared to a traditional totem-pole PFC converter. Therefore, the conduction losses decrease both in the inductor and the semiconductors. In this configuration, slow MOSFETs with low R_{dsOn} and high reverse-recovery in the body diodes can be used for S_3 and S_4 as these FETs are only switching with the line frequency cycles. On the other hand, diodes D_5 and D_6 should have low reverse recovery as they are working at the switching frequency levels.



(a)



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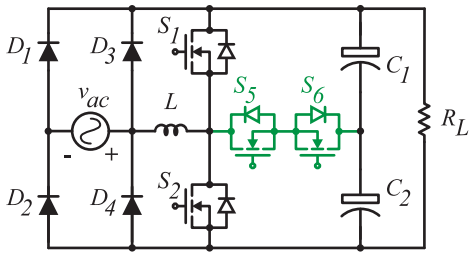

(c)

Fig. 2. (a) Proposed extended input voltage range PFC converter. Different possible configurations for the proposed extended input voltage range PFC converter: (b) First method: The low-frequency middle switch configuration with two 600-V general purpose switches and two 600-V fast recovery diodes. (c) Second method: The high-frequency middle switch configuration with two 600-V SiC switches.

There are two different modes of operation, one at low line voltages shown in Fig. 3(b), and the other one at high line voltages illustrated in Fig. 3(c). These modes are further explained in the remaining part of this section. The proposed converter working with this method has four different operational states shown in Fig. 3(d).

1) Low Input Voltages With $V_{inpeak} < \frac{V_{out}}{2}$: When the input voltage peak value is less than half of the output voltage ($V_{\text{inpeak}} < \frac{V_{\text{out}}}{2}$), the converter switches into low-voltage mode operation. Circuit waveforms for this mode are shown in Fig. 3(b). In this mode, the proposed converter acts like a bridgeless voltage-doubler boost converter. As seen in Fig. 3(b), when the input voltage is positive, the converter works in state III, as shown in Fig. 3(d). In this state, diode D_2 is conducting, S_2 is the switch of the boost converter, and since S_4 is kept ON, D_6 is the diode of the boost. In this situation, the boost converter's output voltage is the voltage across the output capacitor C_2. Therefore, the proposed converter is converting the input voltage into half of the output voltage, which reduces the conversion ratio and, thus, increases the efficiency. On the other hand, when the input voltage is negative, the proposed converter works in state IV, as shown in Fig. 3(d). In state IV, diode D_1 is conducting, S_1 is the switch of the boost, and because S_3 is ON, D_5 is the diode of the boost converter. In this mode, switch S_4 is ON when the input voltage is positive and S_3 is ON when the input voltage is negative. In this mode, the proposed converter acts like a bridgeless voltage-doubler boost converter in which the input voltage and output voltage of the boost structure are the line voltage and the voltage across C_1, respectively. The equivalent circuit schematic of the converter at this mode is shown in Fig. 3(d) in states III and IV. At each of the half-line cycles, one of the output capacitors is charged by the circuit, which causes the proposed converter to have a lower output voltage, decreasing the conversion ratio. The duty cycle of the converter and the inductor's ripple in this mode are shown in (1) and (2), respectively

$$D_{\text{Doubler}} = 1 - 2\frac{|v_{\text{in}}|}{v_o} \tag{1}$$

$$\Delta i_{\text{Doubler}} = \frac{|v_{\text{in}}|(1 - 2\frac{|v_{\text{in}}|}{v_o})}{Lf_{\text{sw}}}. \tag{2}$$

2) High Input Voltage Operation With $V_{inpeak} > \frac{V_{out}}{2}$: When the input voltage peak value is higher than half of the output voltage, the proposed converter works in the high input voltage operation mode. In this mode, the bidirectional switch network is switching in the middle of the half-line cycles. Switching waveforms of the converter at this mode is shown in Fig. 3(c). As seen in Fig. 3(c), switch S_4 is turned ON when the input voltage's instantaneous value is lower than half of the output voltage. Under this condition, the circuit works in state III, as shown in Fig. 3(d). S_4 is kept ON, and thus, S_2 and D_6 are, respectively, the switch and the diode of the boost converter working with the line voltage as the input, and half of the output voltage as the output voltage of the boost converter. Once the line voltage value reaches to half of the output voltage, S_4 is turned OFF by the controller, which causes the converter to work as a totem-pole structure in state I with S_2 as the switch and S_1 as the diode. Once again when the input voltage's instantaneous value goes below $\frac{V_o}{2}$, switch S_4 is turned ON again to take the converter into state III. The same scenario happens at negative line voltage values when the middle switch S_3 changes the configuration of the proposed converter in low line values from totem pole [state II in Fig. 3(d)] to voltage doubler [state IV in Fig. 3(d)]. Since the proposed converter works in both doubler and totem-pole modes in a line cycle under this condition, the duty cycle and

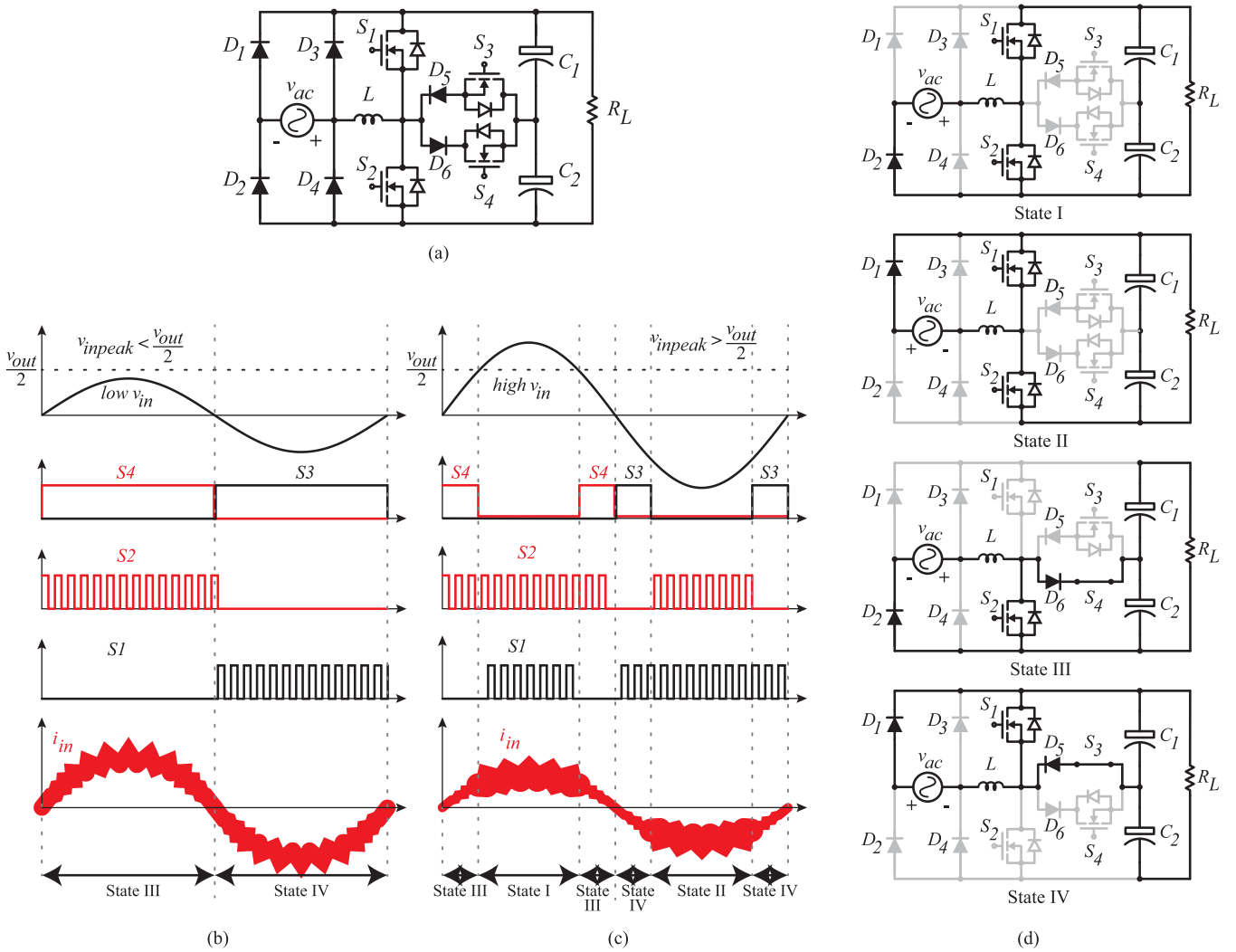

Fig. 3. First modulation method: Low-frequency middle switch, which acts like a voltage doubler at low input voltage levels ($v_{\text{inpeak}} < \frac{V_{\text{out}}}{2}$) and at high input voltage levels ($v_{\text{inpeak}} > \frac{V_{\text{out}}}{2}$), it switches between the voltage doubler and the totem pole in the middle of the half-line cycles with the help from the middle bidirectional switches (S_3 and S_4). (a) Circuit schematic at the first method of operation: Low-frequency middle switch. (b) Circuit waveforms ($V_{\text{inpeak}} < \frac{V_{\text{out}}}{2}$). (c) Circuit waveforms ($V_{\text{inpeak}} > \frac{V_{\text{out}}}{2}$). (d) Different states of operation in the first method.

the current ripples can be calculated in

$$|v_{\text{in}(t)}| < \frac{V_o}{2} \xrightarrow{D_{\text{Doubler}}} \Delta i_L = \Delta i_{\text{Doubler}} = \frac{|v_{\text{in}}|(1-2\frac{|v_{\text{in}}|}{V_o})}{Lf_{\text{sw}}}$$

$$|v_{\text{in}(t)}| > \frac{V_o}{2} \xrightarrow{D_{\text{TotemPole}}} \Delta i_L = \Delta i_{\text{TotemPole}} = \frac{|v_{\text{in}}|(1-\frac{|v_{\text{in}}|}{V_o})}{Lf_{\text{sw}}}. \quad (3)$$

B. Second Modulation Method: High-Frequency Middle Switch

This modulation method is shown in Fig. 4. In this case, the middle switch (K) consists of two back-to-back FETs, as shown in Fig. 2(c). The middle network FETs in this case [S_5 and S_6 in Fig. 4(a)] are different from the ones in the previous modulation method [S_3 and S_4 in Fig. 3(a)]. S_5 and S_6 in Fig. 4(a) should work in the switching frequency speed, which needs a better body diode with lower reverse recovery losses. On the other hand, S_3 and S_4 in Fig. 3(a) can have lower transition speed since they are switching with the line frequency cycles. Low-voltage operation of the proposed converter with the high-frequency middle switch is shown in Fig. 4(b) as well as the high-voltage operation illustrated in Fig. 4(c). The proposed converter in this method has four different states, as shown in Fig. 4(d), with states XI, XII, XIII, and XIV.

1) Low Input Voltages Once $V_{\text{inpeak}} < \frac{V_{\text{out}}}{2}$: When the input voltage peak value is less than half of output voltage, the converter shown in Fig. 4(a) works in the low input voltage mode. Theoretical waveforms of the converter in this mode are shown in Fig. 4(b). As seen in Fig. 4(b), the converter has only two states of operation in this mode shown in Fig. 4(d). When the input voltage is positive, the converter works in state XI, and once the input voltage is negative, it works in state XIII. As stated, in state XI, the converter acts like a voltage doubler charging C_2 with S_2 as the switch, S_6 as the diode, S_1 OFF, and S_5 ON. Similarly once the input voltage is negative, the converter works in state XIII.

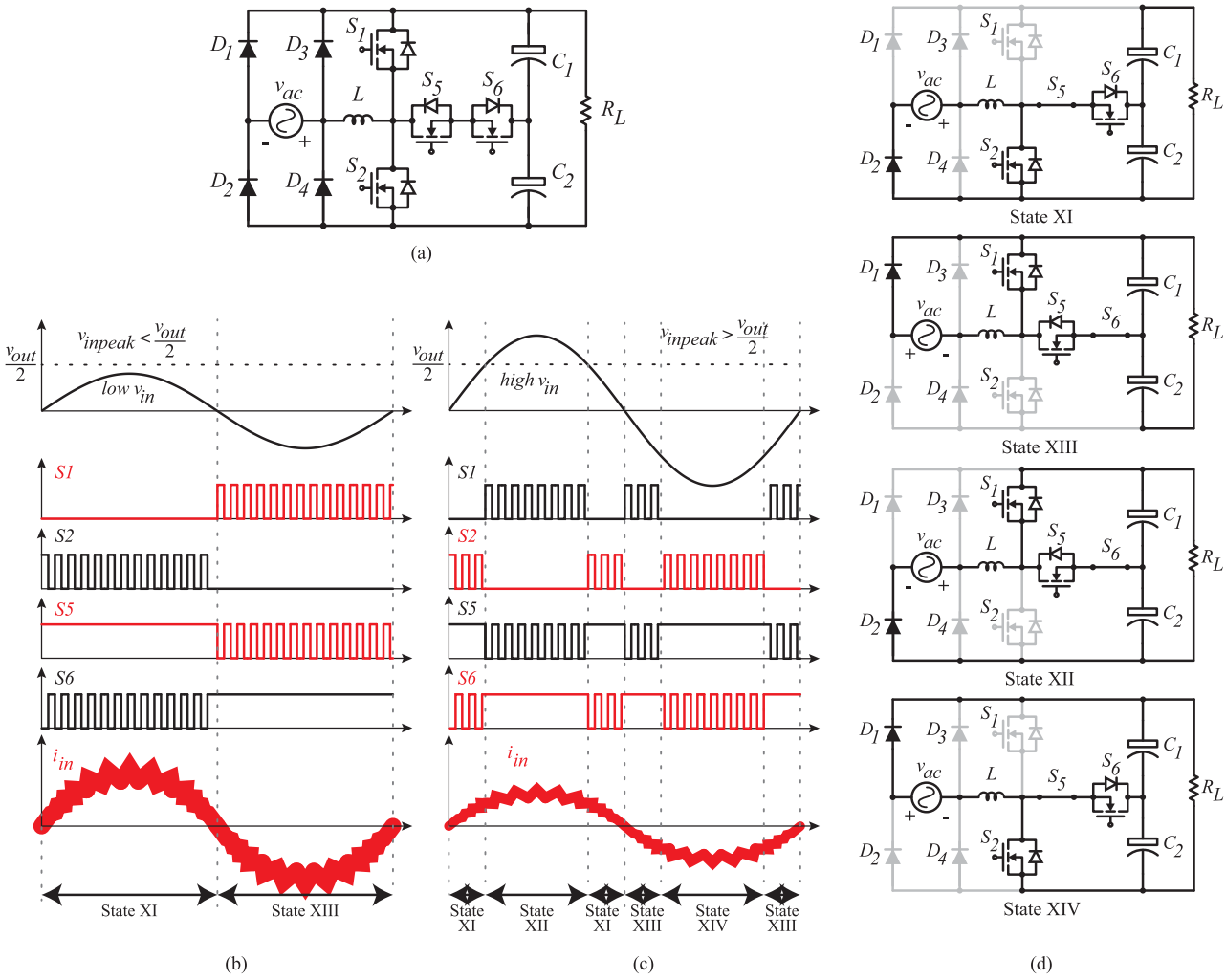

Fig. 4. Second modulation method: High-frequency middle switch, which acts like a voltage doubler at low input voltage levels ($v_{\text{inpeak}} < \frac{V_{\text{out}}}{2}$) and at high input voltage levels ($v_{\text{inpeak}} > \frac{V_{\text{out}}}{2}$), it puts the minimum voltage across the inductor to limit the current ripples in the inductor with the help from the middle bidirectional switches (S_5 and S_6). (a) Circuit schematic at the second method of operation: High-frequency middle switch. (b) Circuit waveforms ($V_{\text{inpeak}} < \frac{V_{\text{out}}}{2}$). (c) Circuit waveforms ($V_{\text{inpeak}} > \frac{V_{\text{out}}}{2}$). (d) Different states of operation in the second method.

In this state, S_2 is remained OFF, S_6 is ON, S_1 is the switch of the boost, and S_5 is the diode of the structure. With this method, the converter can have low ripples in the input current and, thus, the efficiency can be improved. The duty cycle of the converter in this mode is shown in (4) as well as the input current ripples in (5)

$$|v_{\text{in}}| < \frac{v_o}{2} \Rightarrow D_{\text{lowVin\_highf}} = 1 - 2\frac{|v_{\text{in}}|}{v_o} \tag{4}$$

$$|v_{\text{in}}| < \frac{v_o}{2} \xrightarrow{D=D_{\text{Doubler}}} \Delta i_L = \Delta i_{\text{Doubler}} = \frac{|v_{\text{in}}|(1 - 2\frac{|v_{\text{in}}|}{v_o})}{L f_{\text{sw}}}. \tag{5}$$

2) High Input Voltage With $V_{inpeak} > \frac{V_{out}}{2}$: When the input voltage peak value is higher than half of the output voltage, the converter with this method works in the high-voltage mode. The theoretical waveforms of the converter in this mode is shown in Fig. 4(c). When the absolute instantaneous value of the input voltage is less than half of the output voltage, the converter works in state XI at positive input voltages and, in state XIII, at negative input voltages. State XI is similar to state III in the first method. In state XI, S_5 is ON and S_6 acts like the diode of the boost structure. S_2 is the switch of the boost converter in this mode and S_1 is remained OFF. Similarly in state XIII, S_1 is the switch of the boost and S_6 acts like the diode. S_2 is remained OFF and S_6 is ON in this state. State XIII is similar to state IV in the previous modulation method. The proposed converter works in the doubler mode in states XI and XIII, which are similar to the operation of the converter in states III and IV in the previous method. When the input voltage's absolute value gets higher than half of the output voltage, the converter enters into states XII and XIV when the input voltage is positive and negative, respectively. In state XII, S_2 is OFF, S_6 is ON, S_5 is the switch of the boost structure, and S_1 is the diode of the structure. Similarly in state XIV, S_1 is OFF, S_5 is ON, S_6 is the switch of the converter, and S_2 is the diode of the boost structure. With these states of operation in this converter, the voltage across the inductor is always limited to half of the output voltage in all cases, which reduces the input current ripples significantly.

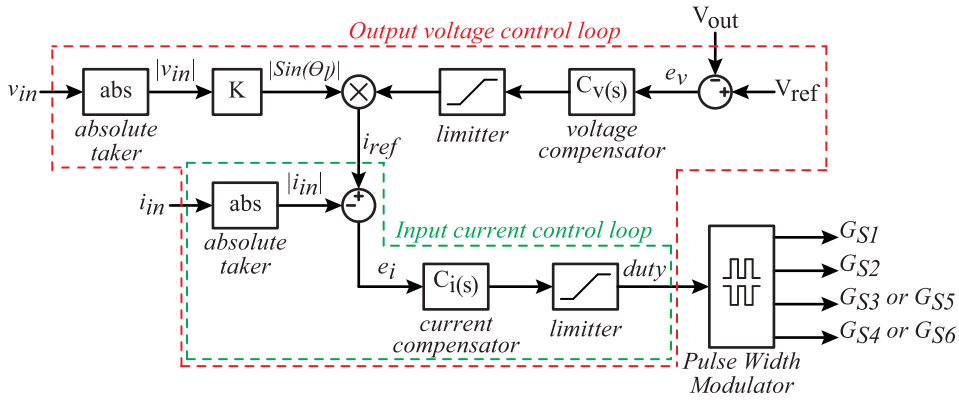

Fig. 5. Control loop of the converter.

The duty cycle of the converter in this mode is variable in different values of the input voltage. When the input voltage absolute value is lower than half of the output voltage, the duty cycle is similar to (1), which is given in (4). The input current ripple is also given in (4). When the absolute instantaneous value of the input voltage is higher than half of the output voltage, with the switch of the boost beingON, the voltage across the inductor is equal to $|v_{\text{in}}| - \frac{V_{\text{out}}}{2}$. Also when the switch is OFF, the voltage across the inductor is $V_{\text{out}} - |v_{\text{in}}|$. The duty cycle can be calculated as done in

$$|v_{\text{in}}| > \frac{V_o}{2} \Rightarrow D_{\text{highVin\_highf}} = 2\left(1 - \frac{|v_{\text{in}}|}{V_o}\right). \tag{6}$$

Also, the inductor current ripples can be calculated in

$$|v_{\text{in}}| > \frac{V_o}{2} \xrightarrow{D\ @(6)} \Delta i_L = \frac{2|v_{\text{in}}|(1 - \frac{|v_{\text{in}}|}{V_o})(1 - \frac{V_o}{2|v_{\text{in}}|})}{L f_{\text{sw}}}. \tag{7}$$

As stated in the first part of this section, it is assumed that the output capacitors have equal capacitance, and hence, the operation of the converter is balanced and symmetrical. In practical cases, there might be some differences between the capacitance of C_1 and C_2, which causes their voltages to be unbalanced. This does not affect the operation of the converter significantly and only causes this split cap structure to reach to a self-balancing state with slightly different voltage levels [38], [39]. There are also many techniques proposed in the literature to relieve the possible unbalanced performance of the structures with split caps [40]–[48].

The operation of the proposed converter was described in this section along with different operating modes with related figures. The control and modulation algorithm of the proposed converter is studied in the next section.

III. Modulation and Control Methods

The extended input voltage range PFC converter introduced in this article provides high efficiencies in a wide input voltage range from 90 V_{rms} up to 530 V_{rms}. It has a high output voltage (800 V_{DC}) suitable for high-power operation. The required inductor is small with low ripples. The presented structure has inrush current handling capabilities as well as the line-frequency common-mode connection between the input and output ports. The control and modulation of the proposed converter is described in this section.

The control loop of the converter is shown in Fig. 5. The control loop is the same for both of the methods presented in Section II. The only difference between the presented methods is the pulsewidth modulation (PWM) module, which is shown in Fig. 5 with the PWM block. As seen in Fig. 5, there are two control loops in the circuit: one for the input current, and the other one to regulate the output voltage. Input current is forced to follow a sinusoidal waveform similar to the input voltage's. The reference of the input current, shown with i_{ref} in Fig. 5, is formed by multiplication of the sinusoidal waveform synchronous to the input voltage ($|\sin(\theta_l)|$) and the v_{out} compensator output. This way, the shape of the input current follows a sinusoidal waveform sampled from the input voltage causing the converter to have a high power factor at the input. Also, the amplitude of this sinusoidal waveform is controlled by the output-voltage compensator in different loading levels, ensuring that the converter will have a constant output voltage value under different conditions. The output of the controller module for the input current is called $duty$ in Fig. 5, which represents the required duty cycle of the converter. This parameter is then received by the modulation module, which depends on different methods being used, as mentioned in Section II.

As stated, different modulation schemes are used in the presented methods in the previous section. First modulation scheme for the low-frequency middle switch method is shown in Fig. 6. As seen in this method, there are three comparators that take the parameter $duty$ as the input. There are two different sawtooth waveforms to be used in this method, as seen in Fig. 6. Sawtooth1 and sawtooth2 are themselves formed by comparing the $duty$ with the dc value of 0.5. As seen, after the comparison made between $duty$ and the sawtooth waveforms, the gating parameters Gate1, Gate2, and Gate3 are formed. These parameters are then used to generate the gate signals needed for the switches. This process includes some multiplexers shown in Fig. 6. Another parameter used in this modulation method comes from the sign of the input voltage. As stated, in the first modulation method, the converter automatically changes its behavior in different input voltages.

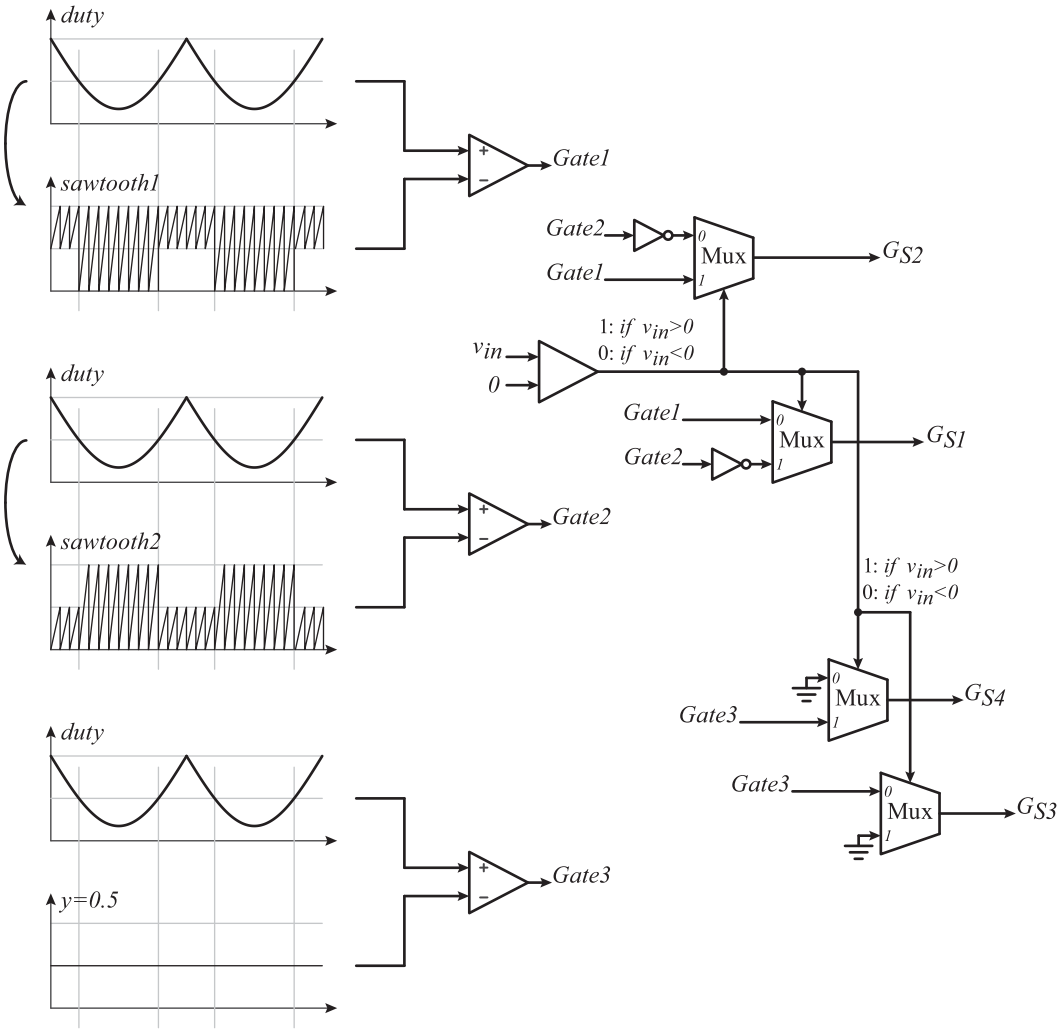

Fig. 6. Modulation method used for the first modulation method: Low-frequency middle switch.

The second modulation method introduced in Section II is shown in Fig. 7. Second modulation method, or the high-frequency middle switch approach, requires a different process for switching the FETs in the design. There are two sawtooth waveforms in this method, as seen in Fig. 7. Sawtooth1 has a frequency equal to the switching frequency with a minimum equals 0.5 and a maximum equals 1. Also, sawtooth2 is a sawtooth waveform with the switching frequency between 0 and 0.5. The parameter $duty$ is compared with these sawtooth waveforms, forming Gate1 and Gate2. As seen in Fig. 7, once the input voltage is positive, Gate1 is connected to the gate signals of the switches S_2 and S_6, and when the input voltage is negative Gate2 is connected to the gates of S_2 and S_6, which are working in the complementary mode. The opposite scenario is happening for the gate signals of S_1 and S_5, which are also working in the complementary mode.

Control method and different modulation schemes for the proposed extended input voltage range PFC converter were discussed in this section. In the next section, a design method is developed for designing the presented converter based on the predefined conditions.

IV. Designing the Proposed Converter

The presented converter in this article has a high efficiency in the wide input voltage range from 90 V_{rms} up to 530 V_{rms}. The output voltage of the proposed converter is regulated at 800 V_{DC} in the whole extended input voltage range. The proposed configuration needs a small inductor, and produces low-current ripples. In addition, the proposed converter has inrush current handling capability and line-frequency common-mode connection between the output and input ports. In this section, the design process of the proposed converter is discussed.

The inductor's current ripple has been calculated in (2), (3), (5), and (7). The proposed converter has different characteristics in each of the modulation methods. The inductor's current ripple ratio to peak is depicted in Fig. 8(a) in the presented modulations at low input voltages when $V_{\text{inpeak}} < \frac{V_{\text{out}}}{2}$. Also the current ripple is shown in Fig. 8(b) at high input voltages, $V_{\text{inpeak}} > \frac{V_{\text{out}}}{2}$. The waveforms in Fig. 8(a) and (b) are illustrated at nominal rms values of low and high input voltages, respectively ($v_{\text{in\_nom\_low}} = 208$ V_{rms} and $v_{\text{in\_nom\_high}} = 480$ V_{rms}) with 2-kW output power and 1-mH inductance. These

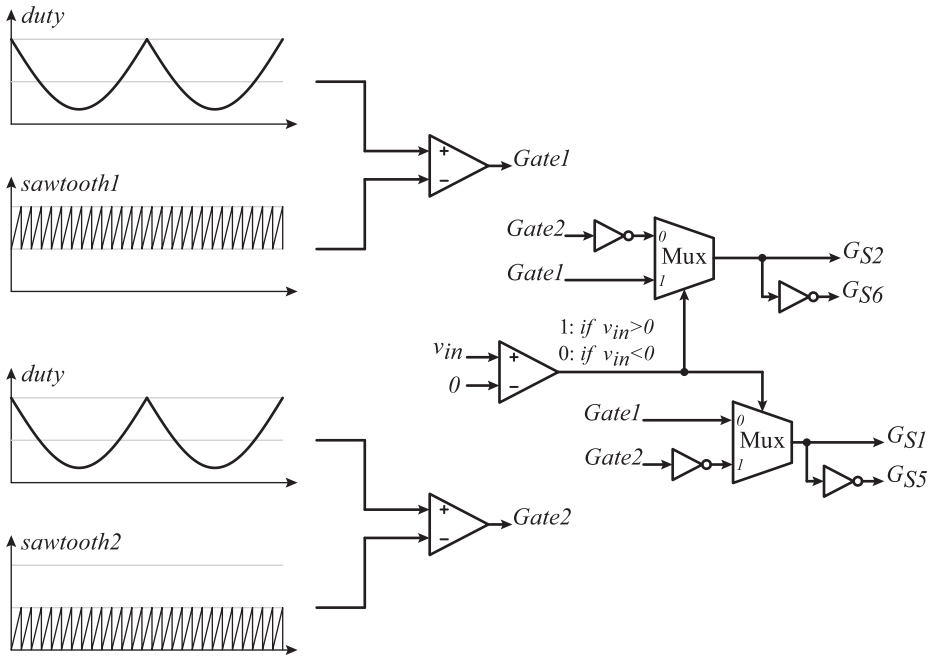

Fig. 7. Modulation method used for the second modulation method: High-frequency middle switch.

waveforms represent similar behavior in different operating points and are given in Fig. 8 as a reference. The inductor's current ripple during the low-frequency middle switch modulation is shown in Fig. 8(a) at low line voltages and, in Fig. 8(b), at high line values. The second modulation method (high-frequency middle switch) is given in Fig. 4 with the modulation scheme shown in Fig. 7. This modulation method represents the lowest ripples in the inductor's current, as seen in Fig. 8. The inductor's current ripple is shown in low input voltage values in Fig. 8(a), and high input voltages in Fig. 8(b). As seen in Fig. 8(a), the inductor's ripple is the same in both of the modulation methods because the converter in both of them is working in the doubler mode. Totem-pole PFC converter's inductor ripple is also shown in Fig. 8 in comparison with the presented modulation methods. The lowest ripple in the inductor, as stated, is happening in the second modulation in both cases of the input voltage values. The highest one is the totem-pole converter's. The first modulation scheme has a moderate ripple value between the second method and the totem-pole PFC technique.

Based on the calculations, the inductance should be higher than 525 μH in order to have a current ripple below 20% at full load and the lowest line voltage. For comparison, if a totem-pole structure is used at low voltages, the minimum value of the inductance to support the maximum 20% ripple should have been 940 μH. Therefore, the inductance value has been decreased nearly 45% with the same value of the current ripple. The maximum current in the inductor is equal to the peak value of the input current plus half of the high-frequency ripple at the peak. Therefore, the maximum current of the inductor is 16.3 A, which happens at the minimum line voltage under full-loading conditions. Two micrometals alloy powder cores have been selected for the required inductance. The part number of the cores are MS-226060-2 and are placed on top of each other,

TABLE I
SPECIFICATIONS OF THE DESIGNED POWER STAGE

Electrical characteristic	Range
Input voltage range (v_{inRMS})	$90 - 530V_{RMS}$
Full power AC input range	$187 - 530V_{RMS}$
Output voltage (v_{out})	$800V_{DC}$
Maximum output power (P_{Omax})	$2kW$
Switching frequency (f_{sw})	$60kHz$
Inductor current ripple ($\frac{\Delta i_L}{I_{Lpeak}}$)	20% @ low line/full load
$120Hz$ ripple of v_{out} (Δv_{out})	40 V_{p-p}
Hold-up time ($t_{hold-up}$)	$10ms$ @ $V_{Omin} = 650V$

which results in higher A_L ($\frac{nH}{N^2}$). Number of the turns are 52 with 6 litz wires of AWG20 or wires with 0.8-mm diameter. Based on this selection, the initial value of the inductance in zero ampere turn (zero crossing) is 745 μH and the value of the inductance at the peak value of the input current is equal to 540 μH. Silicon carbide (SiC) switches have been selected for the main switches of the converter (S_1, S_2). SiC switches are a better match for this converter because these switches have better switching characteristics in higher voltages ($V_{\text{bus}} = 800$ V). The reverse recovery of the body diodes in these switches is lower than silicon types.

There are two factors that need to be considered when selecting the output capacitors for the design: satisfying the hold-up time requirements and also having small low-frequency output voltage ripples. Both of these requirements are mentioned in Table I. Following equation is used for calculating the minimum

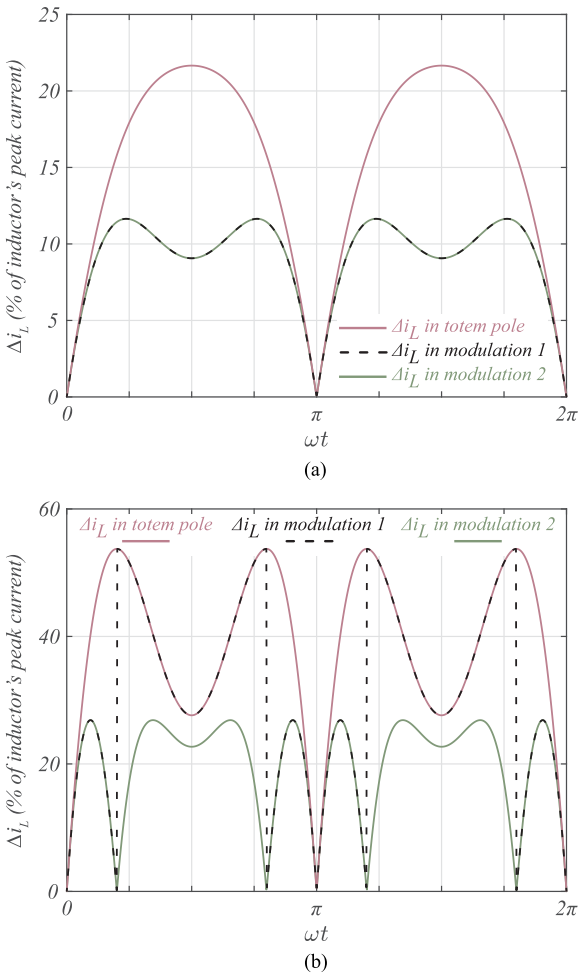

Fig. 8. Inductor's current ripples in the analyzed design cases of totem pole and the proposed modulations 1 and 2 at (a) low input voltage cases ($v_{\text{inpeak}} < \frac{V_{\text{out}}}{2}$), and (b) high input voltage range ($v_{\text{inpeak}} > \frac{V_{\text{out}}}{2}$).

capacitance required for the hold-up time:

$$C_o > \frac{2\,P_{\text{Omax}}\,t_{\text{hold-up}}}{v_{\text{out}}^2 - v_{\text{out\_min}}^2} = 183.9\,\mu\text{F}. \tag{8}$$

Also based on the work in [24], the required capacitance in order to handle the low-frequency output voltage ripple requirements, mentioned in Table I, is given in (9). Equation (9) is considered during the low input voltage mode because the ripples are higher. In addition, (9) is valid for both of the doubler mode and totem-pole mode. Therefore, the output capacitance required for both of the proposed converter and the totem-pole boost PFC is the same

$$C_o > \frac{2I_{\text{Omax}}}{\omega_{\text{line}}\Delta v_{\text{out}}} = 331.7\,\mu\text{F}. \tag{9}$$

Based on (8) and (9), the output capacitance should be higher than the maximum. Therefore, three 220 μF electrolytic capacitors are selected for each of the output caps of C_1 and C_2 in the design. Full list of selected components can be found in Table II. This table includes the part numbers of the components for both of the methods and also some comments regarding the necessary features of the elements. As shown in Fig. 2(b) and (c), the middle switches used in the first method (S_3 and S_4) can be silicon-based FETs. However, in the second method (high-frequency middle switch) the middle switch network should have FETs with low reverse recoveries in their body diodes. Therefore, S_5 and S_6 should be selected from SiC or GaN semiconductors. In the presented prototype, SiC switches have been selected for S_5 and S_6 with the part number shown in Table II. In the next section, an analysis is done for the selected components losses in order to give a better understanding about the performance of the proposed converter compared to the conventional design.

V. Loss Analysis of the Components

In this section, a loss breakdown analysis is done for the proposed converter in both of the high-frequency and low-frequency middle switch modulations. In order to give a better picture about the performance of the proposed converter, the same analysis is also done in a conventional totem-pole boost converter with the same components. As stated in Section IV, the components listed in Table II are selected for the experimental setup. As seen in Fig. 2, the proposed converter has a switch network in its structure, which is the only elements added to the design compared to a totem-pole boost PFC. S_3, S_4, D_5, and D_6 are the middle switch network in the low-frequency mid switch method, as well as S_5 and S_6 in the high-frequency mid switch approach. The proposed converter in these modes have additional losses in these components compared to a totem-pole PFC converter. On the other hand, as mentioned in Section IV, the proposed approaches introduce less ripples in the inductor, which enables the designer to decrease the size of the inductance. But if the same inductor is used in both of the proposed converter and the totem-pole PFC, the conduction and core losses in the inductor would be limited in the proposed one. In addition, since the ac element of the inductor current is reduced, less conduction losses are expected in the main switches of the converter (S_1 and S_2) compared to the totem-pole design. As mentioned in Section IV, the output voltage ripple is the same for both of the proposed converter and the totem-pole design with the same output capacitance value and ratings. However, the ripple current going through each of the output caps are not the same as the totem-pole case. As shown in [24], the current ripple in each of the output caps is higher in the doubler boost converter compared to the regular boost. This causes each of the caps to have higher voltage ripples but the total voltage ripples across the series connection of them are the same as the totem-pole boost structure. Therefore, there are additional losses in the doubler mode compared to the boost mode but the output voltage ripples are the same.

In this section, only conduction and inductance core losses are considered in calculations. The results are shown in Fig. 9. Power losses are illustrated in three cases of low-frequency middle switch converter, high-frequency middle switch converter, and totem-pole boost PFC converter, all with the same components listed in Table II. These converters are compared in the nominal low input voltage of 208 V_{rms} in Fig. 9(a) as well as the high nominal input voltage of 480 V_{rms} in Fig. 9(b). Both of the figures are illustrated in 2-kW power levels. As seen in Fig. 9,

TABLE II
EXPERIMENTAL PARAMETERS

Component(s)	Part number	Comment
L	$540\mu H/12.4Apeak$	-
$C_1,\ C_2$	$3 \times 220\mu\text{F}/500V$	-
$S_1,\ S_2$	LSIC1MO120E0080 (1200V, 25A)	SiC with $V_{ds} > 800V$
$D_1 - D_4$	VS60EPS12M3 (1200V, 60A)	Standard recovery with $V_D > 800V$
$D_5,\ D_6$	RHRG7560 (600V, 75A)	Fast recovery with $V_D > 400V$
$S_3,\ S_4$	IXFX64N60P3 (600V, 64A)	FET with $V_D > 400V$
$S_5,\ S_6$	UJ3C065080K3S (650V, 30A)	SiC with $V_{ds} > 400V$

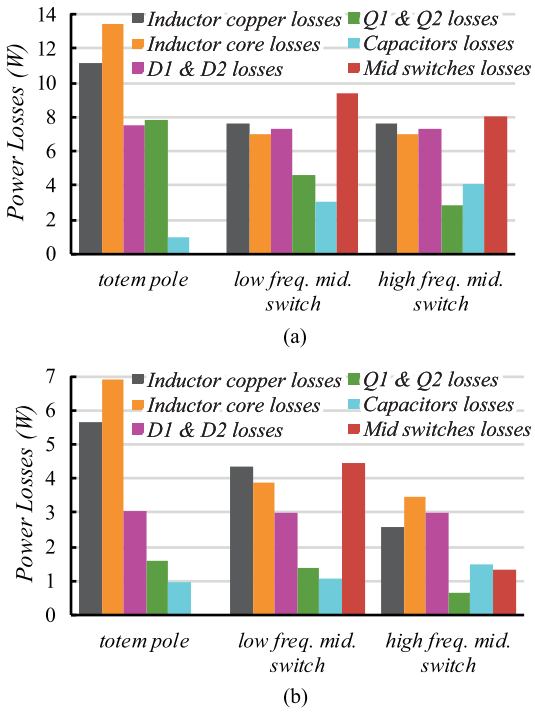

Fig. 9. Loss breakdown of the proposed converter and the conventional totem-pole boost PFC in (a) nominal low input voltage of 208 V_{rms}, and (b) nominal high input voltage of 480 V_{rms}.

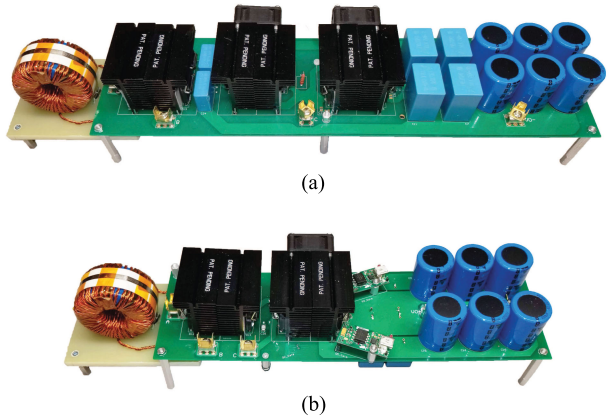

Fig. 10. Photographs of the proposed converter with (a) two MOSFETs and diodes in the middle network to work with low-frequency middle switch modulation (487 mm × 105 mm × 87 mm); (b) two SiC FETs in the middle network to work with high-frequency middle switch modulation (395 mm × 93 mm × 83 mm).

conduction and core losses in the totem-pole boost PFC are higher than the other two converters in both of the cases. In addition, main switches' losses (Q_1 and Q_2) are reduced in the proposed converters. On the other hand, the proposed converters have additional losses because of the middle switch network in their structures. Capacitive losses are also higher in the proposed converter.

Experimental results are given in the next section comparing the performance of the proposed converter in both of the methods with the conventional totem-pole boost PFC converter.

VI. EXPERIMENTAL RESULTS

The proposed extended input voltage range PFC converter supports a wide input voltage range from 90 to 530 V_{rms}. The proposed converter provides a high-efficiency curve in the whole input voltage range with a regulated high output voltage (800 V_{DC}). The studied converter has a small inductor with reduced current ripples. The proposed converter provides a line-frequency common-mode connection between the input and output ports in all of the operating modes. In addition, the proposed converter can handle inrush currents coming from the grid side in order to protect the switches and the inductor. The performance of the proposed converter is analyzed in an experimental setup in this section. The proposed structure has been experimentally tested using the components listed in Table II. These elements are designed and selected in Section IV. The picture of the designed structures are shown in Fig. 10. The first proposed method shown in Fig. 2(a) with the low-frequency middle switch configuration is shown in Fig. 10(a). In addition, second proposed method with the high-frequency middle switch configuration is given in Fig. 10(b). The boxed size of the proposed prototypes have been also shown in Fig. 10. There are two sections in this part of the article. The first one discusses the performance of the proposed methods in an experimental prototype. The second section compares the performance of the proposed modulation methods together and also with a traditional totem-pole PFC structure.

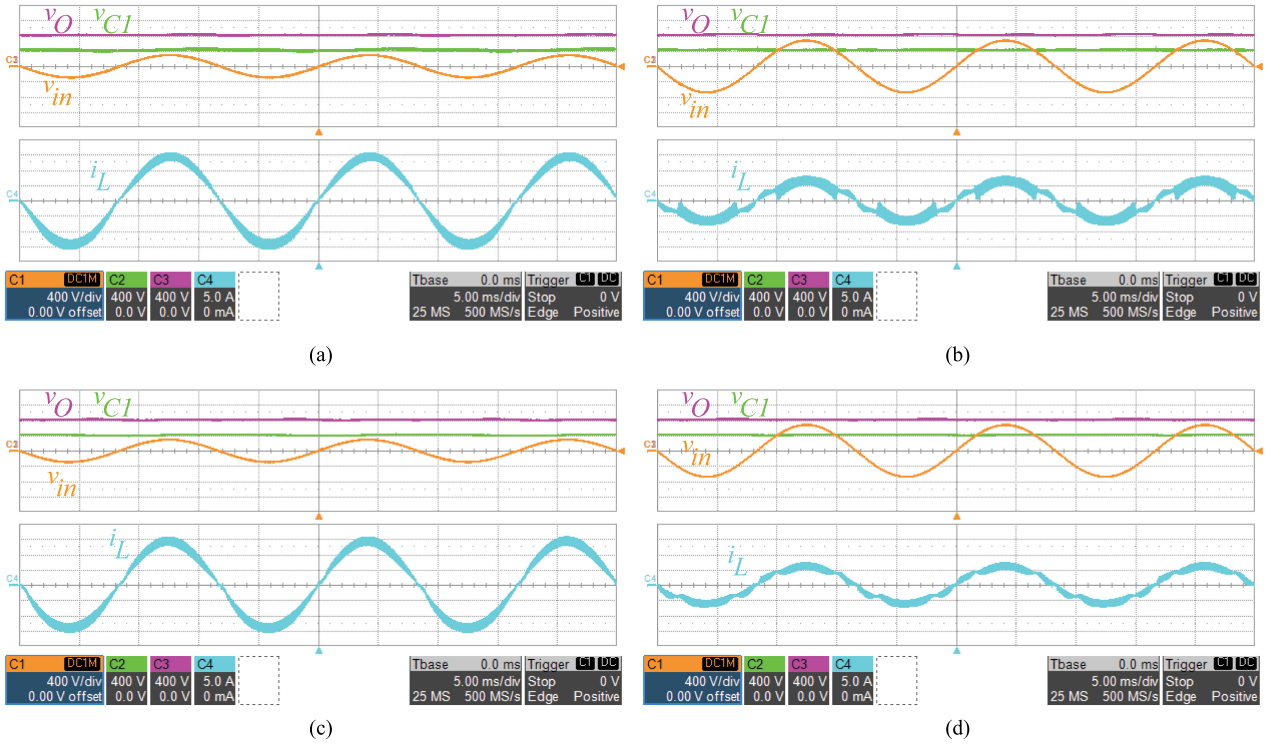

Fig. 11. Experimental captures of the proposed converter in the first modulation method: low-frequency middle switch at (a) 208 V_{rms} ($V_{\text{inpeak}} < \frac{V_{\text{out}}}{2}$), and (b) 480 V_{rms} ($V_{\text{inpeak}} > \frac{V_{\text{out}}}{2}$). Experimental captures of the proposed converter in the 2nd modulation method: high-frequency middle switch at (c) 208 V_{rms} ($V_{\text{inpeak}} < \frac{V_{\text{out}}}{2}$), and (d) 480 V_{rms} ($V_{\text{inpeak}} > \frac{V_{\text{out}}}{2}$).

A. *Performance of the Proposed Converter*

The performance of the proposed converter working with the first modulation method (low-frequency middle switch) is shown in Fig. 11. The waveforms of the proposed converter in this mode are shown at $v_{\text{in}} = 208$ V_{rms} (low input voltage nominal level with $V_{\text{inpeak}} < \frac{V_{\text{out}}}{2}$) in Fig. 11(a) and at $v_{\text{in}} = 480$ V_{rms} (high input voltage nominal level with $V_{\text{inpeak}} > \frac{V_{\text{out}}}{2}$) in Fig. 11(b). These captures are showing the full-load performance of the converter at this mode. In these figures, input voltage (v_{in}), inductor current (i_L), output voltage (v_O), and one of the output capacitor's voltages (v_{C1}) are shown. The efficiency of the converter at full load (2 kW) is measured 97.7% at $v_{\text{in}} = 480$ V_{rms}, and 96.9% at $v_{\text{in}} = 208$ V_{rms}.

The performance of the proposed converter working with the second modulation method (high-frequency middle switch) is shown in Fig. 11. The operation of the proposed converter in this mode is shown at $v_{\text{in}} = 208$ V_{rms} (low input voltage level with $V_{\text{inpeak}} < \frac{V_{\text{out}}}{2}$) in Fig. 11(c) and at $v_{\text{in}} = 480$ V_{rms} (high input voltage level with $V_{\text{inpeak}} > \frac{V_{\text{out}}}{2}$) in Fig. 11(d). The efficiency of the proposed converter in this mode is 98.2% at $v_{\text{in}} = 480$ V_{rms}, and 96.8% at $v_{\text{in}} = 208$ V_{rms}.

As seen in Fig. 11, the ripple in the second modulation method in high voltages is lower than the first modulation technique. This is based on the analytical discussion provided in Section II. As stated in the previous sections, the voltage across the inductor in the second modulation method is limited to half of the output voltage under all conditions. This helps the proposed converter in this mode to have a smaller ripple in the inductor, which results in higher efficiency (lower conduction losses) and higher power factor. On the other hand, the voltage across the inductor in the first modulation method is limited to half of the output voltage in low input voltages but it is the output voltage once the input voltage rms value is high. The switching losses is also limited in the first method because of the high-frequency switching of the diodes (D_5 and D_6) compared to the high-frequency switching in the MOSFETs (S_5 and S_6) in the second method. That is why the efficiency of the converter at low input voltages is higher in the first proposed modulation method. Loss breakdown of the components have been done in Section V. The inductor current ripples shown in Fig. 11 have the same values as calculated in Section IV. In addition, the maximum inductor current value is the same expected value as shown in Section IV with 16 A in low input voltages in Fig. 11(a) and (c).

B. *Comparing the Proposed Converter With Totem-Pole PFC*

In order to compare the performance of the proposed algorithm with an existing PFC system, totem-pole PFC converter is considered. The totem-pole PFC converter should be working with the same input and output voltage and power characteristics for this comparison. Also, the same set of components (L, C_1, C_2, S_1, S_2, and $D_1 - D_4$) are used in the totem-pole PFC to make it easy to compare with the proposed converter. The output voltage of the totem-pole converter is the same as the proposed converter (800 V_{DC}) with the same input voltage range

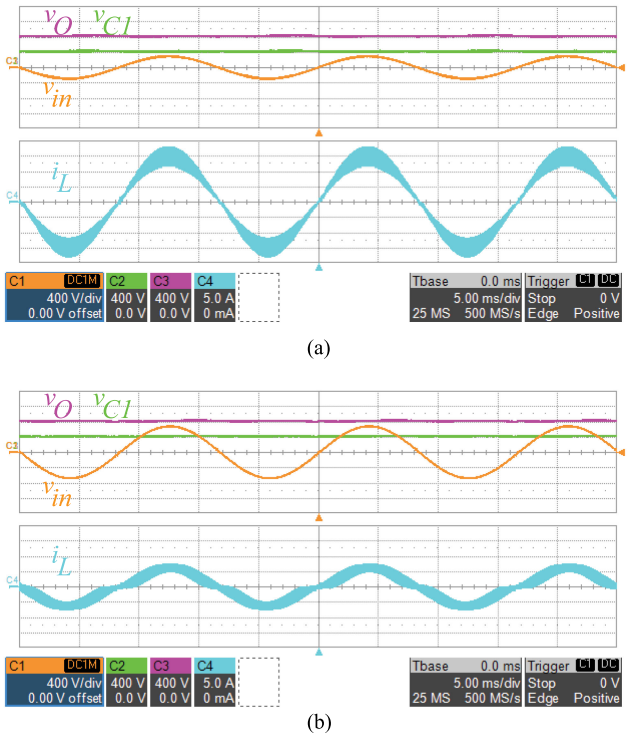

Fig. 12. Experimental captures of the totem-pole PFC converter with the same input and output characteristics. The operational waveforms in (a) 208 V_{rms} ($v_{\text{inpeak}} < \frac{V_{\text{out}}}{2}$), and (b) 480 V_{rms} ($v_{\text{inpeak}} > \frac{V_{\text{out}}}{2}$).

Fig. 13. Comparison of the efficiency of the proposed converters with the traditional totem-pole PFC boost converter with the same electrical characteristics and the same components at (a) $v_{\text{in}} = 480$ V_{rms} and different output power levels, (b) $v_{\text{in}} = 208$ V_{rms} and different output power levels, and (c) $P_{\text{out}} = 2$ kW and different input voltage levels ($v_{\text{in}} = 187-530$ V_{rms}) with derated power levels in $v_{\text{in}} = 90-187$ V_{rms}.

(90−530 V_{rms}). The experimental waveforms of the totem-pole PFC converter is shown in Fig. 12. The experimental captures of the totem-pole PFC converter in low voltage at 208 V_{rms} are shown in Fig. 12(a) and in high input voltage at 480 V_{rms} in Fig. 12(b). As seen in Fig. 12, the ripple in both of the input voltages' cases are higher than the ones seen in Fig. 11. Therefore, the ripple in the proposed solutions are smaller than the conventional totem-pole PFC's. This can be also seen in Fig. 8. The reason behind these advantages in the proposed converter is lower levels of the voltage across the inductor. As shown in Figs. 3 and 4, the proposed modulation methods work like a voltage doubler boost PFC in low input voltages while $V_{\text{inpeak}} < \frac{V_{\text{out}}}{2}$. As a result, the voltage across the inductor in these modes are always limited to half of the output voltage in low line levels. Therefore, the ripple in the inductor will be less than the totem-pole boost's. Since the switching frequency is the same in all of the converters, less voltage across the inductor results in lower ripples in the inductor's current causing the conduction losses to be minimized. The efficiency of the totem-pole PFC at full load with the same conditions as the proposed converter is 97.2% at 480 V_{rms} and 96.2% at 208 V_{rms}, which is lower than the efficiency of the proposed converters in modulation methods 1 and 2.

The efficiency of the proposed converters in modulation methods 1 and 2 are compared with the totem-pole PFC converter's in Fig. 13. The efficiency of the proposed configuration is compared with the totem-pole PFC in the nominal high input voltage ($v_{\text{in}} = 480$ V_{rms}) in Fig. 13(a) as well as the nominal low input voltage ($v_{\text{in}} = 208$ V_{rms}) in Fig. 13(b) both versus output power levels. In addition, the efficiency of the extended input voltage range PFC is presented along with the totem-pole PFC at full load in different input voltage rms values in Fig. 13(c). The converters in this figure are working with nominal power (2 kW) in 187−530 V_{rms}, and also derated power in 90−187 V_{rms}.

As seen in Fig. 13, the efficiency of the proposed techniques in the extended input voltage range PFC is always higher than that of the totem-pole PFC converter's. This is the result of having lower ripples in the inductor of the circuit. Although there are more elements in the proposed converter, which cause

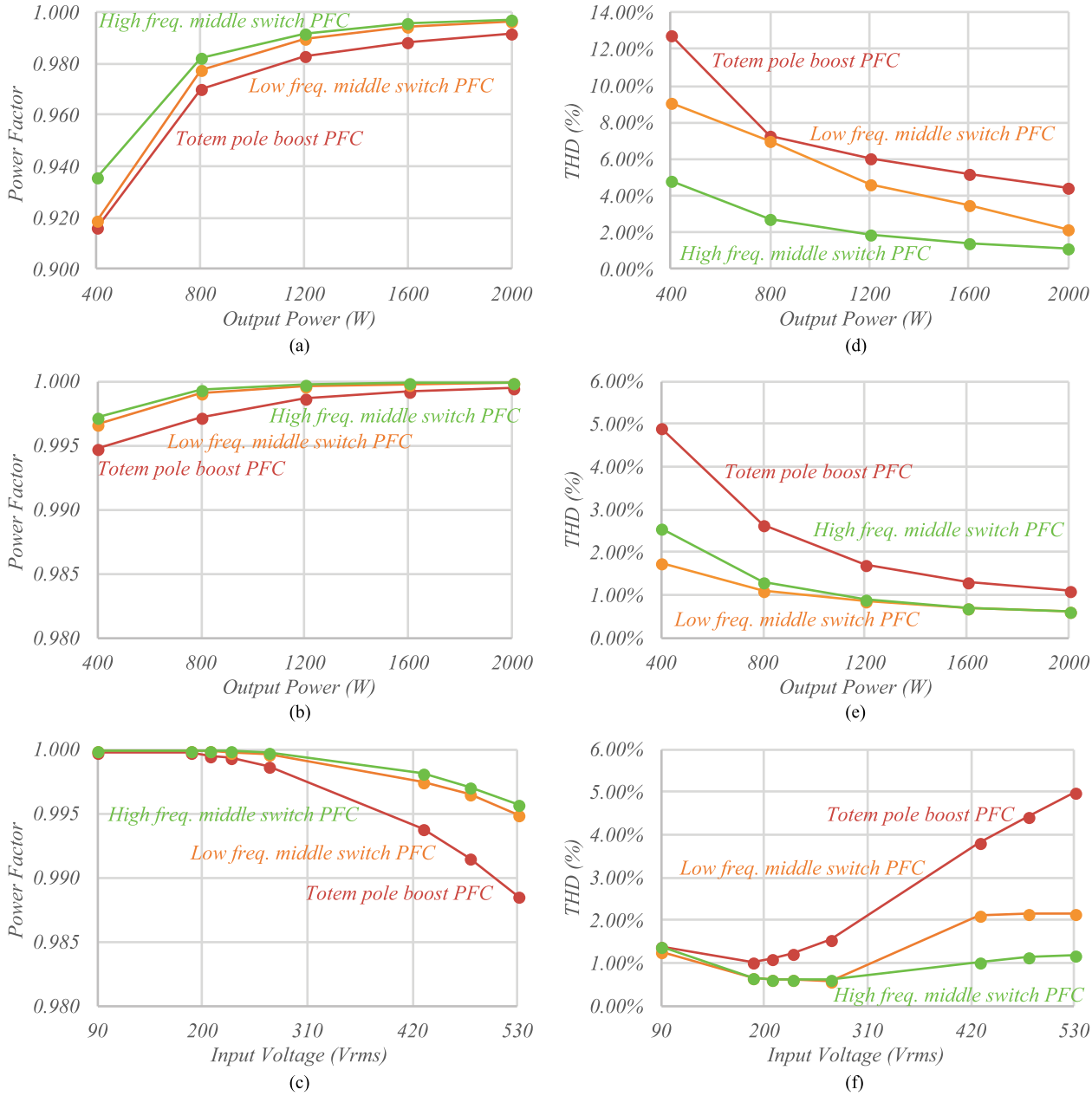

Fig. 14. Comparison of the proposed converters with the traditional totem-pole PFC boost converter with the same electrical characteristics and the same components. Power factor comparison at (a) $v_{in} = 480\ V_{rms}$ and different output power levels, (b) $v_{in} = 208\ V_{rms}$ and different output power levels, and (c) $P_{out} = 2$ kW and different input voltage levels ($v_{in} = 187-530\ V_{rms}$) with derated power levels in $v_{in} = 90-187\ V_{rms}$. THD comparison at (d) $v_{in} = 480\ V_{rms}$ and different output power levels, (e) $v_{in} = 208\ V_{rms}$ and different output power levels, and (f) $P_{out} = 2$ kW and different input voltage levels ($v_{in} = 187-530\ V_{rms}$) with derated power levels in $v_{in} = 90-187\ V_{rms}$.

more losses in the circuit, the reduction of the dissipation in other parts of the circuit is higher than the effect of these extra losses. Therefore, the efficiency of the proposed techniques are higher than the totem-pole PFC converter's. In high input voltages shown in Fig. 13(a), the efficiency of the high-frequency middle switch is higher than the low-frequency middle switch technique. But in low voltages, modulation 1 shows slightly higher efficiencies.

The power factor and THD of the proposed converters in modulation 1 and 2 are compared with the totem-pole PFC converter's in Fig. 14. The power factor of the proposed configuration is compared with the totem-pole PFC in the nominal high input voltage ($v_{in} = 480\ V_{rms}$) in Fig. 14(a) as well as the nominal low input voltage ($v_{in} = 208\ V_{rms}$) in Fig. 14(b) in different output power levels. In addition, the power factor of the extended input voltage range PFC is presented along with the totem-pole PFC at full load in different input voltage rms values in Fig. 14(c). An *LC* filter has been added to the input of the proposed converter and the totem-pole boost PFC to eliminate the high-frequency ripples in the input currents. A 2 μF capacitor and a 50 μH inductor has been used for this purpose. The THD comparison between the proposed converter and the

conventional totem-pole boost PFC are also done in different input voltage and power levels in Fig. 14. THD is compared at 480 V_{rms} and 208 V_{rms} in different output power levels in Fig. 14(d) and (e), respectively. In addition, THD is compared in different input voltage levels when operating at full output power in Fig. 14(f). As seen in Fig. 14, the power factor (THD) of the extended input voltage range PFC converter is always higher (lower) than that of the totem-pole PFC converter's in different input voltages and output power levels. In addition, the power factor (THD) of the modulation technique 2 is higher (lower) than that of the first modulation method at high input voltages. This is mainly because of the lower current ripples in the inductor in the first modulation method compared to other techniques.

VII. Conclusion

Typical commercial utility line voltage ranges (90 to 530 V_{rms}) restrict the attainable efficiency of a single PFC converter. In this article, an extended input voltage range bridgeless PFC converter with high-voltage dc bus and small inductor is proposed. The proposed converter exhibits a high efficiency throughout the entire operating input voltage range. Two modulation methods are presented for the proposed PFC converter. In the first modulation method (low-frequency middle switch) the converter can limit the inductor current ripple in low and high input voltages resulting in lower ripples compared to the totem-pole PFC converter with the same inductance value. The second modulation method (high-frequency middle switch) also demonstrates good performance when subjected to high input voltages when compared to the conventional totem-pole approach and the first modulation method. The proposed structures transform into a voltage doubler PFC converter at low line voltages ($V_{\text{inpeak}} < \frac{V_{\text{out}}}{2}$) and demonstrate different structures in higher line voltages ($V_{\text{inpeak}} > \frac{V_{\text{out}}}{2}$). With these methods, the proposed converter can maintain a high operating efficiency even with an 800 V_{DC} bus voltage throughout the entire input voltage range. Theoretical analysis as well as the experimental results have been presented for a 2-kW power level prototype. The efficiency and the power factor of the proposed PFC converter is compared with the totem-pole PFC converter's in different input voltages and output power levels. At full load, the efficiency of the proposed converter reaches as high as 98.2% at 480 V_{rms} compared to 97.2% in the totem-pole PFC with the same components. Also, the efficiency of the proposed converter is 96.9% at 208 V_{rms} compared to 96.2% in the totem-pole PFC structure. These improvements in the efficiency and also the power factor are the results of the reduction in the inductor current ripples due to the proposed modulation methods. This enables the proposed converter to have a smaller inductor when compared to the totem-pole boost PFC.

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Hamed Valipour (Graduate Student Member, IEEE) was born in Tehran, Iran. He received the B.Sc. and M.Sc. degrees in electrical engineering from the Sharif University of Technology, Tehran, in 2012 and 2014, respectively. He is currently working toward the Ph.D. degree with The University of British Columbia (UBC), Vancouver, BC, Canada.

He has been involved in many research and industrial projects including design and implementation of power electronics circuits in renewable energies, electric vehicles, LED drivers, voltage monitoring relays, and firmware design for numerous applications. His research interests include the design and implementation of power electronic circuits (soft-switching techniques, renewable energies, electric vehicles, high-frequency converters), and firmware development.

Mr. Valipour is the recipient of numerous awards and scholarships for his academic performance including the Four Year Fellowship in 2016, and Graduate Support Initiative Scholarships in 2018 and 2019 from UBC.

Mohammad Mahdavi was born in Isfahan, Iran. He received the B.S, M.S., and Ph.D. degrees in electrical engineering from the Isfahan University of Technology, Isfahan, Iran, in 2006, 2009, and 2013 respectively.

He was an Assistant Professor with Islamic Azad University, Isfahan. He has been a Postdoctoral Research Fellow with the Department of Electrical and Computer Engineering, The University of British Columbia, Vancouver, BC, Canada, since July 2017. He is currently a Power Electronics Engineer with Bombardier Recreational Products (BRP), Valcourt, QC, Canada, where he is developing power converters for electrical vehicle applications. His research interests include power electronics, power factor correction converters, soft-switching techniques, renewable energies, electric vehicles, and high-frequency converters.

Martin Ordonez (Member, IEEE) was born in Neuquen, Argentina. He received the Ing. degree in electronics engineering from the National Technological University, Cordoba, Argentina, in 2003, and the M.Eng. and Ph.D. degrees in electrical engineering from the Memorial University of Newfoundland (MUN), St. Johns, NL, Canada, in 2006 and 2009, respectively.

He is currently a Professor and a Canada Research Chair in Power Converters for Renewable Energy Systems with the Department of Electrical and Computer Engineering, The University of British Columbia, Vancouver, BC, Canada. He is also the holder of the Fred Kaiser Professorship on Power Conversion and Sustainability with UBC. He was an Adjunct Professor with Simon Fraser University, Burnaby, BC, and MUN. His industrial experience in power conversion includes research and development with Xantrex Technology Inc./Elgar Electronics Corporation (now AMETEK Programmable Power, San Diego, CA). With the support of industrial funds and the Natural Sciences and Engineering Research Council, he has contributed to more than 150 publications and R&D reports.

Dr. Ordonez is a Guest Editor for the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS, an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS, and an Editor for the IEEE TRANSACTIONS ON SUSTAINABLE ENERGY. He serves on several IEEE committees, and reviews widely for IEEE/IET journals and international conferences. He was the recipient of the David Dunsiger Award for Excellence in the Faculty of Engineering and Applied Science in 2009 and the Chancellors Graduate Award/Birks Graduate Medal in 2006, and became a fellow of the School of Graduate Studies, MUN.

Peter F. Ksiazek (Member, IEEE) was born in Lethbridge, AB, Canada. He received the Diploma in electrical engineering technology from the Northern Alberta Institute of Technology, Edmonton, AB, Canada, in 2008, the B.Eng. degree in electrical engineering from the University of Victoria, Victoria, BC, Canada, in 2012, and the M.A.Sc. degree in electrical engineering from The University of British Columbia, Vancouver, BC, in 2014.

He is currently a Power Electronics Engineer with Alpha Technologies, Ltd. (an EnerSys Company), Burnaby, BC, Canada, where he assists with the development of high-efficiency and high-reliability power converters for the telecommunications industry. His research interests include power electronic controls, resonant topologies, and renewable energy extraction techniques.

Rahul Madhav Khandekar (Member, IEEE) was born in Mumbai, India. He received the B.E. degree in instrumentation engineering from Mumbai University, Mumbai, India, in 2001, and the M.S. and Ph.D. degrees in electrical engineering from the State University of New York at Binghamton, Binghamton, NY, USA, in 2004 and 2008, respectively.

He is currently with Alpha Technologies, Ltd. (an EnerSys company), Reading, PA, USA, where he is a Manager of research and advanced development. In this role, he manages technology development in power electronics, embedded controls, and power systems as well as partners with universities to advance research for telecom, traffic, and datacenter applications. His work experience spans academic research and industrial research and product commercialization. His research interests include applications of embedded controls in optics, robotics, and power electronics.