Duty Cycle Loss Compensation Method Based on Magnetic Flux Cancelation in High-Current High-Frequency Synchronous Rectifier of *LCLC* Converter

Liangzong He, *Member, IEEE*, Jiazhe Chen, Bing Cheng, and Hongyan Zhou

***Abstract*—With uncertainty of the parasitic parameter in different practical layout, two synchronous rectifiers (SR) with same topology and identical components may exhibit significant difference in driving timing and each SR FET may suffers from the duty cycle loss. In this article, the mutual induction between the voltage detection network of SR controller and the transformer secondary windings is first investigated. Then, a compensation method based on magnetic flux cancellation is proposed to solve the duty cycle loss issue caused by the parasitic inductive coupling, which enables further increase of switching mode power supply efficiency. With the proposed compensation method, only an additional wire turn is required with no need to change the layout, resulting in reducing the difficulty for implementation in practical prototypes. Where, a most compatible method is employed after multiparameter extraction methods comparison and the parasitic parameters are given out. Then, the design process of a specific compensator is proposed. Finally, a prototype of 400 to 14 V, 1.5 kW *LCLC* resonant converter was employed to verify the advantages of the proposed method. An efficiency improvement of 0.8% is achieved. The method can be generally applied to different kinds of SR controllers. This article is accompanied by a video demonstrating operation waveforms.**

***Index Terms*—Duty cycle loss compensation, high current, high efficiency, *LLC* converter, synchronous rectifier (SR).**

I. Introduction

LLC converters, including its derived *LCLC* converter, have been widely used in various fields such as renewable energy, electric vehicle, and telecommunication power supplies in the past ten years. To obtain higher efficiency in high-current application such as on-board dc/dc converter for electric vehicle and server power supply, diode rectifier in the secondary side is usually replaced by the synchronous rectifier (SR).

Due to the phase shift brought by the resonant tank, the control timing of the primary switch is not strictly in phase with the secondary SR during the full operation range. Hence, the primary driving signal cannot be directly applied to drive SR FETs [1]. To obtain the appropriate conduction angle for SR FETs, a self-driven method for *LLC* converter is proposed in [2]. By adding two auxiliary windings to the center-tapped transformer, the SR FETs can be driven by the auxiliary winding. However, due to the leakage inductance in the secondary side, severe conduction loss will be caused by the driving waveforms overlapping. To address the issue, replacing the auxiliary winding with a current-detection transformer (CT) has been proposed in [3]. However, CT in series with the secondary winding will bring in large conduction loss in high-current application. In order to reduce conduction loss, some work focusing on moving the CT to the primary side has been reported [4]–[6]. In these topologies, additional magnetizing current compensation network, such as "magnetizing current detector" and "a compensating winding in CT" are employed to eliminate the magnetizing current from the resonant current. However, the compensation network requires many passive components, which increases system complexity. To simplify the circuit and improve the efficiency, voltage doubling rectifier is applied to reduce the number of CTs in [7], [8]. However, it is not a suitable solution in the low-voltage application.

Generally speaking, the current detection has a large time delay caused by the leakage inductance of CT. Besides, the equivalent resistance of the current sensor brings about additional loss. Hence, the current detection is seldom used nowadays.

A promising driving method is the voltage detection [9]–[13]. The forward drop of the SR FETs is processed by control circuit or SR controller (also named smart IC) to determine the driving timing. However, due to a small amplitude signal, it still has several disadvantages [14], [15]. First, the leakage inductance from the secondary windings of transformer will resonate with the C_{oss} of SR FET at the turn-ON time of SR FET. If the oscillation is longer than the minimum on time (MOT), the SR controller will turn OFF mistakenly. Second, it

Manuscript received January 29, 2020; revised April 24, 2020; accepted June 8, 2020. Date of publication June 14, 2020; date of current version September 4, 2020. This work was supported in part by the Fujian Province Outstanding Youth Fund under Grant 2018J06016, in part by the Natural Science Foundation of China under Grant 61671400, and in part by the Xiamen University Nanqiang Young Top Talents Program under Grant 6001010201. Recommended for publication by Associate Editor Q. Li. *(Corresponding author: Jiazhe Chen.)*

The authors are with the Department of Instrumental and Electrical Engineering, Xiamen University, Xiamen 361005, China (e-mail: hlz190213@163.com; 748482167@qq.com; 1606912765@qq.com; 1140427341@qq.com).

This article has supplementary downloadable material available at https://ieeexplore.ieee.org, provided by the authors.

Color versions of one or more of the figures in this article are available online at https://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2020.3002266

is hard to detect the zero-crossing point of secondary current accurately in the turn-OFF stage. Because the ON-resistance of SR FET is usually small and millivolt threshold voltage is easily drown in electromagnetic noise. Third, due to the package inductance of SR FET, the voltage across SR FET will lead the current. Error voltage signal brings challenge to drive SR FETs precisely. Although, the reliability of these circuits can be improved by employing an *RC* filter, the additional problems such as turn-ON lag, overfiltering, or underfiltering may still be pendent.

In order to overcome above drawbacks, a zero-crossing noise filter (ZCNF) compensation network, containing an *RC* filter and an auxiliary diode, is presented in [16]. However, to ensure that the ZCNF timing is consistent with the SR FETs, the voltage drop of the auxiliary diode should match that of the paralleled body diode.

To drive SR FETs more precisely and universally, some general adaptive driving methods for synchronous rectifier in *LLC* is proposed in [17] and [18]. Digital control enables more intelligent power management but brings about huge computational complexity due to the cycle by cycle detection control strategy. Consequently, the requirement of expensive field-programmable gate array will limit its application. As an improvement, SR digital driving scheme for *LLC* converters using cost-effective microcontrollers is proposed in [19] and [20].

In recent study, various synchronous rectification schemes for *LLC* converter were presented, like resonant capacitor voltage and homopolarity cycle modulation in [21] and [22].

Because there are large quantities of SR controllers in the market, and lower price, SR utilizing SR controllers (smart IC) is still popular in the low-cost *LLC* converter. As described above, how to effectively and steadily correct timing of voltage detection method is still a challenge for the smart *IC*. Until now, the duty cycle loss issue caused by self-parasitic inductance in *LLC* converter has been widely explored. However, few literatures focus on the issue brought by mutual-parasitic inductance, especially for the high-current applications.

This article concentrates on the inductive coupling between the voltage detection network of SR controller and the transformer secondary windings. By applying equivalent circuit to detection network, the duty cycle loss induced by mutual coupling is first analyzed. Moreover, based on magnetic flux cancellation, a compensator employing a wire turn is proposed to solve the duty cycle loss issue caused by parasitic coupling, stray inductance in layouts, and package inductance of SR FETs.

The rest of this article is organized as follows. In Section II, the principle of the secondary rectifier in *LCLC* converter using smart IC is reviewed and the key issue of duty cycle loss induced by mutual inductance in practice is identified. In Section III, a strategy is developed to eliminate the effect of stray parameter and the proposed compensation method is given. In Section IV, the design procedure of a specific compensator is presented. Experimental results obtained from the 1.5-kW *LCLC* prototype are presented in Section V, Finally, the conclusion is given in Section VI.

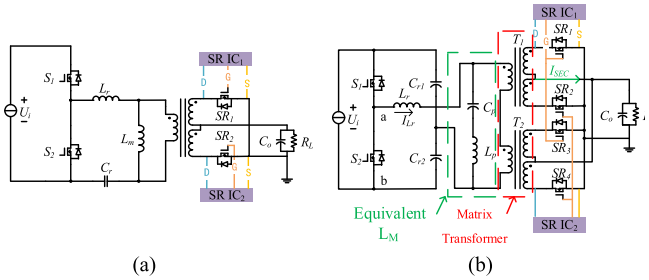


Fig. 1. Schematic of LLC converter. (a) Conventional LLC converter. (b) LCLC converter with matrix transformer.

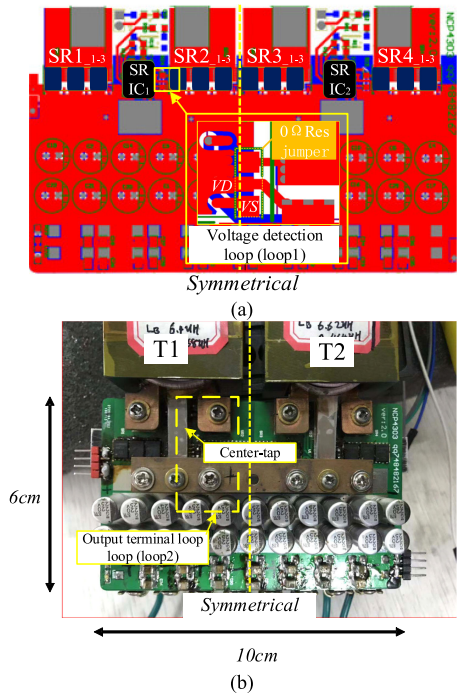


Fig. 2. Image of secondary PCB layout and prototype. (a) PCB layout top side. (b) Secondary prototype.

II. Mutual Parasitic Inductance in Voltage Detection Network of Smart IC

A. Mutual Inductance Between Secondary Windings and Voltage Detection Loop

It is difficult to identify the parasitic inductive coupling parameter unless a practical circuit is considered. Therefore, to state it clearly, the prototype and its secondary side layout is introduced first. A widely used *LLC* topology with SR is showed in Fig. 1(a). And the modified *LLC* topology to expand voltage gain, also called *LCLC*, is showed in Fig. 1(b). The *LCLC* converter could be essentially equivalent to a set of *LLC* converters with different magnetizing inductors that are automatically adjusted for different input voltages [23]. To increase current carrying capability, the single transformer is replaced by a matrix transformer [24], [25]. The PCB layout of prototype secondary side is shown in Fig. 2(a). Considering the conduction loss of on-state resistance, three SR FETs in parallel are utilized

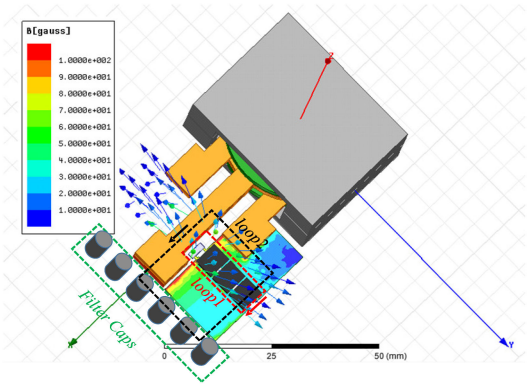


Fig. 3. Magnetic field generated by the secondary windings.

to reduce the on-state resistance. To improve the heat dissipation of surface mounted technology (SMT) components, the thermal vias are provided under the SR FETs. The thermal vias areas need to be installed with a heat-sink for better heat dispassion. The entity of prototype secondary side is shown in Fig. 2(b), as a tradeoff for PCB layout, the center-tap of the transformer is designed to cross the SR IC area. Noticed, longer center-tap will result in larger leakage inductance.

The enlarged part in Fig. 2(a) shows the voltage detection loop (loop1) layout of prototype SR circuit. Taking the demo board in [10] as a reference, the layout of SR circuit still follows the smart IC layout guidelines in datasheet. For example, "keep IC close to SR FETs, obtain Kelvin connection, and keep the gate loop as small as possible."

However, seen from Fig. 3, although the area of loop1 (red lined part) could be optimized to nearly zero by moving IC close to SR FETs, the mutual coupling between loop1 and output terminal loop (loop2, black lined part) still exists. Fig. 3 suggests a small amount of magnetic flux generated by the secondary windings. In other words, there is a parasitic mutual inductance between the voltage detection loop and the secondary windings of the transformer.

B. Duty Cycle Loss Caused by Mutual Parasitic Coupling

In most cases, the mutual inductive coupling has minor influence on converter. However, the effect of mutual coupling cannot be negligible any more if there are two branches with large current difference [26]. In the SR with voltage detection, since loop2 current is several order higher than loop1 current and hundreds of amperes of current flows through loop2, the mutual inductance between loop1 and loop2 will cause severe duty cycle loss for SR FETs.

To explain it clearly, a decoupling equivalent circuit is provided here. Considering complementarily operating for two secondary windings of the center-tapped transformer, part of the SR circuit extracted from Fig. 1 is shown in Fig. 4.

L_1 is the inductance of detection loop. L_2 denotes the secondary leakage inductance of transformer. M_1 is the mutual inductance between L_1 and L_2. The parasitic resistance in loop1 is ignored due to its much smaller value compared with the inductive reactance. When SR FET is ON, the drain-source voltage

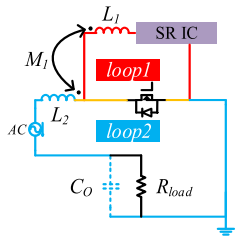


Fig. 4. One phase of SR circuit.

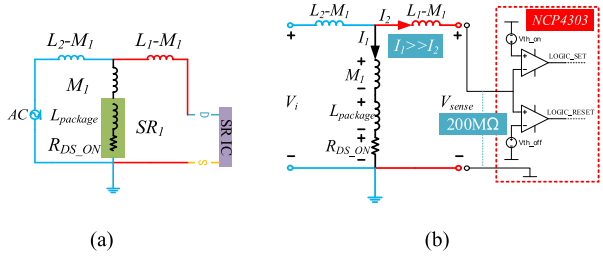


Fig. 5. Equivalent circuit of SR. (a) Decoupling equivalent circuit. (b) Two-terminal equivalent circuit.

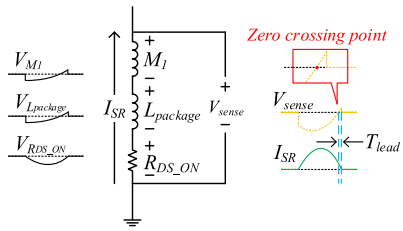


Fig. 6. Mechanism of duty cycle loss.

becomes very small. A small on-resistance R_{DS_ON} in series with MOSFET package inductance L_{package} can be substituted for SR FET. The decoupling equivalent circuit of SR is shown in Fig. 5(a) and two-terminal equivalent circuit is shown in Fig. 5(b). It is assumed that the output filter capacitor C_o is ideal, which will short the load resistor R_{load} under high frequency.

Appling KVL to loop1, the voltage sensed by smart IC V_{sense} can be written as follows:

$$\begin{cases} V_{\text{sense}} = j\omega I_2 (M_1 - L_1) + j\omega I_1 M_1 + V_{DS} \\ V_{DS} = j\omega I_1 L_{\text{package}} + I_1 R_{DS\_ON} \end{cases} \tag{1}$$

$$V_{\text{sense}} = I_1 (j\omega M_1 + j\omega L_{\text{package}} + R_{DS\_ON}). \tag{2}$$

Taking smart IC NCP4303A as an example, the input leakage current of the comparator I_2 is 1 μA at 200 V input bias, meanwhile, the peak value of the current through SR FETs I_1 is about hundreds of amperes. The value of I_2 could be negligible compared to I_1. So, (1) can be simplified to (2) further. Known from (2), the actually detected voltage V_{sense} is the sum of V_{RDS_ON}, V_{M1} and $V_{L\text{package}}$, and the V_{M1} and $V_{L\text{package}}$ will make the zero-crossing point of V_{sense} forward. The mechanism of duty cycle loss is shown in Fig. 6, where the direction of I_{SR} is opposite to that of I_1 in Fig. 5(b).

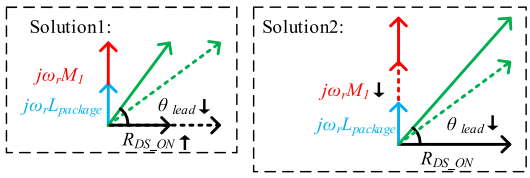


Fig. 7. Vector diagram of two solutions to decrease θ_{lead}.

Since the smart IC will be triggered when the zero-crossing point is detected, if V_{sense} is referenced directly for the driving signals generation, inevitably, the SR FETs will be turn OFF prematurely while they still carry large current. After the SR FETs are turned OFF, the current will go through the parallel body diode, resulting in much body-diode conduction loss further.

Ignoring the voltage drop across L_1 and M_1, the lead angle θ_{lead} and lead time T_{lead} can be derived as (3), where f_r denotes the series-resonant frequency

$$\begin{cases} T_{\text{lead}} = \frac{\theta_{\text{lead}}}{\omega_r} \\ \theta_{\text{lead}} = \tan^{-1}\left(\frac{\omega_r(L_{\text{package}}+M_1)}{R_{DS\_ON}}\right) \\ \omega_r = 2\pi f_r \\ f_r = \frac{1}{2\pi\sqrt{L_r C_r}}. \end{cases} \tag{3}$$

From (3), it is obvious that T_{lead} will be influenced by L_{package}, M_1, and R_{DS_ON}. In practical design, when the package of SR FET is selected, the L_{package} will be determined as well. Only M_1 and R_{DS_ON} can be optimized. Under this premise, there are two possible solutions to decrease θ_{lead} (T_{lead}). Solution1: maintain the layout of loop1 (it means fixed M_1 and L_{package}), an SR FET with larger on-state resistance is employed (R_{DS_ON} increase). Solution 2: keep the SR FET (it means fixed R_{DS_ON} and L_{package}), but the layout of the loop1 is modified to have smaller M_1. The vector diagram of two solutions is shown in Fig. 7.

C. Duty Cycle Loss in High-Current High-Frequency Application

High-frequency converters have become more and more popular in recent years due to their high-power density and integrated magnetics for reduced total cost [27]. However, the reactance of parasitic inductance is proportional to the operation frequency. Aiming for high efficiency, the high-current converter should have smaller output resistance on the secondary side. Hence, SR FET with lower R_{DS_ON} is the best choice. Consequently, the parasitic reactance will become comparable to R_{DS_ON} in high-current high-frequency application.

Based on (3), the possible way to reduce T_{lead} is to reduce M_1 or L_{package}. Although L_{package}, brought by the bonding wire inside the SR FET package, is inevitable, M_1 can be optimized by modifying SR FETs layout.

To reveal the relationship between T_{lead} and arrangement of SR FETs, the finite element analysis (FEA) simulation with/without paralleling SR FETs is carried out. The simulation models are shown in Fig. 8. The value of M_1 in each case obtained by FEA tool is given in Table I. The different loop1 area results in different magnetic flux coupling magnitude. For example, there are three unit space for three SR FETs, "100" means only one SR FET placed on the left side of the PCB trace, its M_1 is small due to a small loop1 area; "001" indicates only one SR FET placed on the right side of the PCB trace, its M_1 is large due to a large loop1 area.

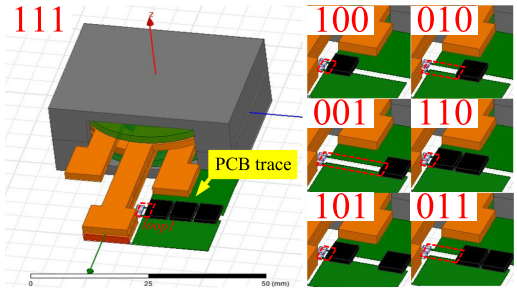


Fig. 8. FEA simulation groups with seven different SR FET arrangements.

TABLE I
PARASITIC PARAMETERS OF SEVEN DIFFERENT ARRANGEMENTS

Arrangements	M_1/nH	R_{DS_ON}/mΩ	T_{lead}/us	D_{lead}
001	5.41	1.4	1.33	42.6%
010	3.12	1.4	1.21	38.7%
011	3.11	1.4/2	1.38	44.2%
100	0.77	1.4	0.77	24.6%
101	0.73	1.4/2	1.08	34.6%
110	0.76	1.4/2	1.09	34.9%
111	0.73	1.4/3	1.23	39.4%

Duty cycle loss rate D_{lead} is defined in (4) to evaluate duty loss level

$$D_{\text{lead}} = \frac{T_{\text{lead}}}{0.5T_r} = 2T_{\text{lead}} f_r. \tag{4}$$

T_{lead} and D_{lead} under specify condition (assuming L_{package} = 0.6 nH, f_r = 160 kHz) are also shown in Table I.

As shown in Table I, from groups "001" "010" "100," the case "100" with the smallest loop1 area demonstrates the best performance (M_1 = 0.77 nH, D_{lead} = 24.6%), hence, the smart IC should be placed more closely to SR FET to minimize loop1 area and reduce parasitic coupling effect. However, seen from groups "100" "110" "111," even loop1 area for them all almost achieves the minimum value, D_{lead} still increases with the R_{DS_ON} decreasing due to the SR FETs in parallel connection.

It is not difficult to determine whether the duty cycle loss of SR FETs is mainly caused by the mutual inductance [28]. Here, the magnetic field sniffer, as depicted in Fig. 9, is employed and the sniffer experiment results are shown in Fig. 10, where I_{SEC} is the current through center-tap, $V_{GS\_SR1,3}$ ($V_{GS\_SR2,4}$) represents the gate driving signal generated from SR IC$_1$ (SR IC$_2$). To detect the induced voltage precisely, the loop area of sniffer wire turn is designed to be several times larger than that of loop1. As the output current flows through the secondary side, the sniffer could capture the magnetic flux surrounding center-tap.

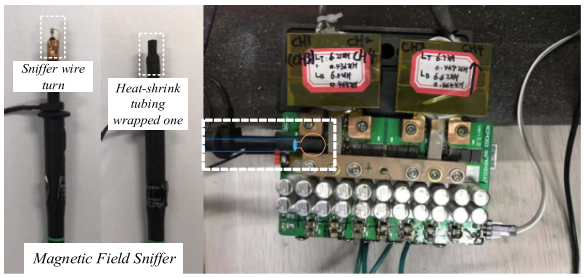


Fig. 9. Photograph of the magnetic field sniffer and experimental set up.

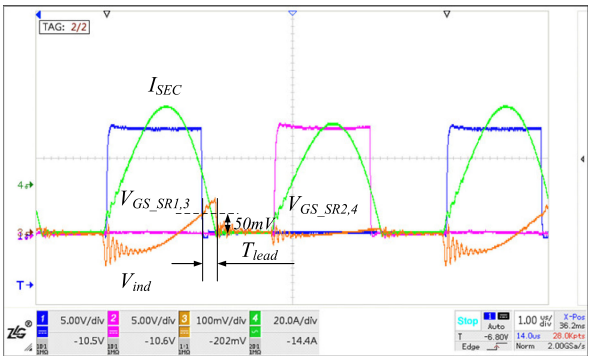


Fig. 10. Experimental waveforms, where $V_{\rm ind}$ from magnetic field sniffer.

The induced voltage $V_{\rm ind}$ can be described in (6), where Φ is magnetic flux flowing sniffer wire turn, B is magnetic flux density, and A is loop area of sniffer, the number of turns $N = 1$.

$$\begin{cases} \Phi = B \times A \\ \psi = N \cdot \Phi \\ M = \dfrac{\psi}{i} \end{cases} \tag{5}$$

$$V_{\rm ind} = \frac{d\psi}{dt} = \frac{dB}{dt} A = M \frac{di}{dt}. \tag{6}$$

As observed from Fig. 10, the induced voltage $V_{\rm ind}$ is about 50 mV at the falling edge of $V_{GS\_SR1,3}$ (blue waveform), which means increasing 50/3 mV to the turn-OFF threshold for the smart IC (on the assumption that the loop area of the sniffer wire turn is 3 times than loop1). As to the voltage detection in SR application, it is quite critical to maintain precision of turn-OFF threshold. Assuming a SR FET with R_{DS_ON} of 1 mΩ, 1 mV error voltage on the $V_{\rm sense}$ may result in 1 A turn-OFF current threshold difference.

The conduction loss caused by body diode is relatively small to be neglected in low-current application. However, in high-current application, the loss cannot be neglected. Moreover, thermal design will become complicated due to large loss, especially for the SMT device.

III. Compensation Turn Developed for Parasitic Parameter Cancellation

For the sake of higher efficiency and stability, the value of M_1 and $L_{\rm package}$ should be reduced. Zhang *et al.* [29] have reported the employment of direct FET to reduce the duty cycle loss, because direct FET has the smallest $L_{\rm package}$. On the other hand, magnetic flux can be shielded by adding a surface mount shield, which helps to reduce M_1. Theoretically, ideal electromagnetic shielding can completely block EMI problem, but it is costly and takes up more space.

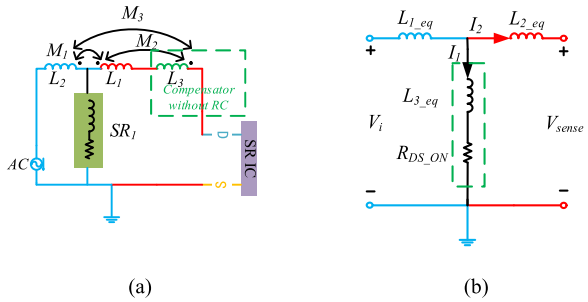


Fig. 11. (a) Schematic of compensator without *RC*. (b) Equivalent circuit.

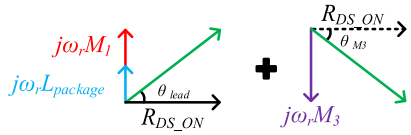


Fig. 12. Vector diagram of proposed compensation method.

To address the duty cycle loss issue caused by M_1 and $L_{\rm package}$, a compensation method based on magnetic flux cancellation is proposed in this section. The basic principle of the proposed method lies in that since error voltage can be introduced by parasitic mutual inductance, a specified mutual inductance M_3 can be designed for voltage compensation.

A. Cancellation Turn Compensator Without RC Filter

An additional cancellation inductance L_3 is added in voltage detection loop. The schematic of the proposed compensation method is shown in Fig. 11(a). M_3 denotes the mutual inductance between L_2 and L_3. In Fig. 11(a), the position of dotted terminals is determined by aiding coupling or opposing coupling between L_2 and L_3. Fig. 11(b) shows its decoupling equivalent circuit, where $L_{1'eq} = L_2 - M_1 + M_3$, $L_{2'eq} = L_1 + L_3 - M_1 - 2M_2 + M_3$, and $L_{3'eq} = M_1 - M_3 + L_{\rm package}$.

To simplify the analysis, the voltage drop brought by L_{2_eq} is ignored. Then, M_3 for the optimal compensation of the proposed compensator without *RC* can be derived as

$$M_3 = L_{\rm package} + M_1. \tag{7}$$

Under the condition, $L_{3\_eq} = 0$, the branch in green dotted square in Fig. 11(b) is a pure resistive network and $V_{\rm sense}$ is in phase with I_1.

The voltage matching method of the proposed compensator without *RC* filter is shown in Fig. 12.

B. Cancellation Turn Compensator With RC Filter

Adjustable MOT is integrated into new generation SR controller, such as NCP4303A and UCC24610. Since the MOT is

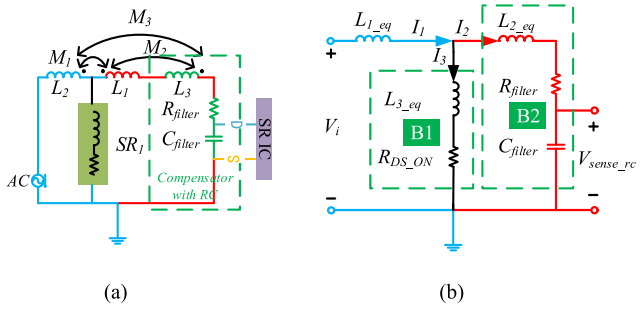


Fig. 13. (a) Schematic of compensator with *RC*. (b) Its equivalent circuit.

set to be longer than ringing time in DCM period, there is unnecessary to add an *RC* filter to avoid false trigging problem caused by parasitic ringing. However, as to the old generation smart SR controller, such as IR11682S, the MOT is internally fixed. In case where a longer filtering time is desired, a small additional *RC* filter should be added across the drain-source to absorb the parasitic ringing of V_{DS} (voltage across the drain-source port) to prevent false-triggering at the turn-ON of SR FETs. To avoid the false triggering problem, the time constant of filter τ_{filter} should be selected a little bit larger than the period of the parasitic ringing [16]. However, at the turn-OFF, an additional *RC* network may introduce delay time with time constant of τ_{filter}. To avoid overcompensation, the *RC* delay time should be taken into account in the design for M_3.

The schematic of compensator with *RC* filter is shown in Fig. 13(a) and its equivalent circuit is shown in Fig. 13(b). In Fig. 13(b), the branch B1 and B2 are shown in the green dotted boxes. Along with a direction of current I_3, B1 consists of equivalent inductance L_{3_eq} and on-state resistance R_{DS_ON}. Along with a direction of current I_2, B2 consists of equivalent inductance L_{2_eq} and *RC* filter. V_{sense_rc} denotes the *RC* filter output voltage.

Taking $\dot{I}_1 = \text{I}_1 \angle 0°$ as the reference and applying a sinusoidal steady-state analysis for the circuit in Fig. 13(b), (8) can be derived, where Z_1 is the impedance of B1, Z_2 is the impedance of B2, and $Z_{c\text{filter}}$ is the impedance of C_{filter}. Rewriting the rectangular form of complex number in (8) into an exponential form to get (9). To ensure V_{sense_rc} to be in phase with I_3, the impedance angle θ_1-θ_2 and θ_3-θ_2 should be equal, equal condition is shown in (10). Equation (10) shows that the equal condition is weakly dependent on angular frequency ω_r due to L_{2_eq}. However, L_{2_eq} has little influence on an *RC* network. In practice, branch B_2 is regarded as an *RC* network instead of an *RLC* network. Hence, voltage drop across L_{2_eq} is neglect

$$\begin{cases} \dot{I}_3 = \dot{I}_1 \frac{Z_2}{Z_1+Z_2} \\ = \dot{I}_1 \frac{R_{\text{filter}}+(\omega_r L_{2\_eq}-\frac{1}{\omega_r C_{\text{filter}}})j}{R_{DS\_ON}+R_{\text{filter}}+(\omega_r L_{3\_eq}+\omega_r L_{2\_eq}-\frac{1}{\omega_r C_{\text{filter}}})j} \\ \dot{V}_{\text{sense\_rc}} = \dot{I}_2 Z_{C\text{filter}} = \dot{I}_1 \frac{Z_1}{Z_1+Z_2} Z_{C\text{filter}} \\ = \dot{I}_1 \frac{\frac{L_{3\_eq}}{C_{\text{filter}}}-\frac{R_{DS\_ON}}{\omega_r C_{\text{filter}}}j}{R_{DS\_ON}+R_{\text{filter}}+(\omega_r L_{3\_eq}+\omega_r L_{2\_eq}-\frac{1}{\omega_r C_{\text{filter}}})j} \end{cases} \tag{8}$$

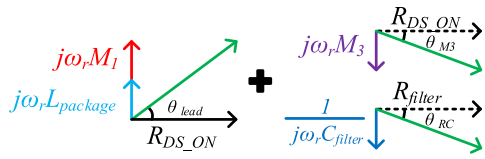


Fig. 14. Vector diagram of proposed compensation method with *RC* filter.

$$\begin{cases} \dot{I}_3 = \dot{I}_1 \frac{r_1 e^{j\theta_1}}{r_2 e^{j\theta_2}} = \frac{r_1}{r_2} e^{j(\theta_1-\theta_2)} \\ \dot{V}_{\text{sense\_rc}} = \dot{I}_1 \frac{r_3 e^{j\theta_3}}{r_2 e^{j\theta_2}} = \frac{r_3}{r_2} e^{j(\theta_3-\theta_2)} \\ r_1 = \sqrt{{R_{\text{filter}}}^2 + (\omega_r L_{2\_eq} - \frac{1}{\omega_r C_{\text{filter}}})^2} \\ \theta_1 = \text{atan}\left(\frac{\omega_r L_{2\_eq}-\frac{1}{\omega_r C_{\text{filter}}}}{R_{\text{filter}}}\right) \\ r_2 = \\ \sqrt{(R_{DS\_ON}+R_{\text{filter}})^2+(\omega_r L_{3\_eq}+\omega_r L_{2\_eq}-\frac{1}{\omega_r C_{\text{filter}}})^2} \\ \theta_2 = \text{atan}\left(\frac{\omega_r L_{3\_eq}+\omega_r L_{2\_eq}-\frac{1}{\omega_r C_{\text{filter}}}}{R_{DS\_ON}+R_{\text{filter}}}\right) \\ r_3 = \sqrt{\left(\frac{L_{3\_eq}}{C_{\text{filter}}}\right)^2 + \left(\frac{-R_{DS\_ON}}{\omega_r C_{\text{filter}}}\right)^2} \quad \theta_3 = \text{atan}\left(\frac{-R_{DS\_ON}}{\omega_r L_{3\_eq}}\right) \end{cases} \tag{9}$$

$$\frac{R_{DS\_ON}}{L_{3\_eq}} = \frac{\frac{1}{C_{\text{filter}}} - {\omega_r}^2 L_{2\_eq}}{R_{\text{filter}}} \tag{10}$$

$$L_{3\_eq} = R_{DS\_ON} R_{\text{filter}} C_{\text{filter}}. \tag{11}$$

According to above assumptions, (10) can be simplified as (11) further. Solving (11) with $L_{3\_\text{eq}} = M_1$-M_3+L_{package}, then, M_3 for optimal compensation of the proposed compensator with *RC* filter can be expressed as

$$M_3 = L_{\text{package}} + M_1 - R_{DS\_ON} R_{\text{filter}} C_{\text{filter}}. \tag{12}$$

Comparing (7) with (12), the (12) has an additional term of $-R_{DS\_ON}R_{\text{filter}}C_{\text{filter}}$. It means that T_{lead}, brought by L_{package} and M_1, is partly offset by *RC* time constant at the turn OFF time of SR FETs. The voltage matching method is shown in Fig. 14.

C. Performance Comparison

As reviewed in the introduction, many solutions have been proposed to improve the SR circuit performance in *LLC* converters. The proposed compensation method is suitable for the occasion with the smart IC utilized. Hence, its counterpart is the SR with smart IC. A performance comparison among some popular smart ICs with compensation method is implemented. These solutions can be roughly divided into two categories: 1) reshaping detection signals by adding passive or active components [12], [14], [16]; 2) regulating on-resistance by applying varying gate driving voltage [13]. The feature of those methods is summarized in Table II.

On reshaping detection signal by capacitive components, Wang and Liu [16] provided a ZCNF for SR in *LLC* converters. It adopts *RC* filter with auxiliary diodes to reshape detection signals. Since the capacitive reactance is always negative, only the premature turn-OFF is compensated. Moreover, the auxiliary

TABLE II
COMPARISONS OF *LLC* SR COMPENSATION METHODS WITH SMART IC

Smart IC SR method	Extra loss	Timing error	Number of components	Paralleled MOSFETs
No compensation	Low	High	None	Support
***RC* compensation [14,16]**	Low	None	1-2 Res 1 Cap 1-3 diodes or 3 switches	Support
Inductor compensation [12]	High	None	1 inductor	Support
Adaptive gate drive [13]	Low	None	None	Not support
Cancellation turn compensator without *RC* filter	Low	None	1 wire turn	Depend on device
Cancellation turn compensator with *RC* filter	Low	Low	1 wire turn 1 Res 1 Cap	Depend on device

switch or passive diode is needed to short *RC* filter at turn-ON time to avoid turn-ON lag. To ensure passive diode operate in phase with SR FET, the voltage drop of passive diode and body-diode should be equal, which will limit the component selection. As to reshaping detection signal by inductive components, literature [12] proposed a smart IC with an internal inverter to reverse voltage across compensation inductance L_{comp}. If the value of L_{comp} is equal to L_{package} the compensation voltage V_{comp} across L_{comp} will be exactly the same as the error voltage caused by L_{package} due to their series connection. The internal analog inverter inverts V_{comp} and offsets the turn-OFF threshold. Thus, the smart IC is able to detect zero-crossing point precisely at the cost of an additional L_{comp}. However, L_{comp} added to terminal of SR FET will increase hardware cost and cause undesirable conduction loss. For adaptive gate drive method proposed in [13], the IC regulates the voltage across SR FET to an absolute level of 50 mV at its conduction. When the voltage drop of SR FET is higher than the absolute level of 50 mV, the output voltage of gate driver will increase to reduce the on-resistance of SR FET until the voltage drop reduces down to the absolute level. Compared with the reshaping signal solution, no additional component is needed and no timing error will be introduced. However, the specific gate signals restrict the employed low-side gate driver. It is worth noting that the low-side gate driver helps to improve driving capability of the paralleled MOSFETs.

The last two columns in Table II demonstrates the feature of proposed method. Comparatively, (11) is similar to duty cycle compensation function $\frac{R_{DS\_ON}}{L_{\text{trace}}} = \frac{1}{R_{\text{filter}} C_{\text{filter}}}$ in ZCNF [16]. The difference lies in a fixed trace inductance L_{trace} in ZCNF, which means a fixed *RC* time constant as well. The fixed *RC* time constant may incur underfiltering and overfiltering. To overcome the conflict between the filter time constant and compensation time constant, diodes and additional filter resistors are utilized to build filter. In (11), L_{3_eq} becomes controllable. It helps to select *RC* parameters since the filter and duty cycle compensation can be designed independently. The other benefit of the proposed compensation method lies in that, compared with inductor compensation, it utilizes the parasitic parameter and no additional in-series compensation inductor in high current branch B1 is required. Therefore, it has both advantages on efficiency and design of PCB layout.

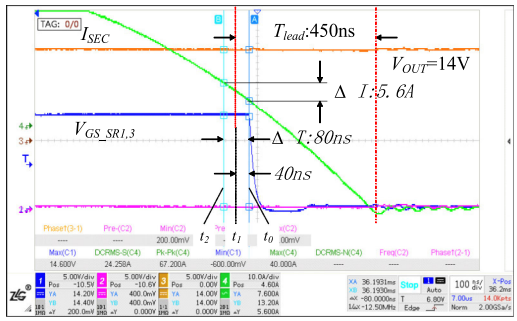


Fig. 15. Waveforms of SR circuit at turn off time t_0.

IV. DESIGN PROCEDURE OF PROPOSED COMPENSATION METHOD

A. Parasitic Parameters Extraction

Generally, there are three methods to extract parasitic parameters: measurement, FEA simulation, and estimation. The measurement method has the best accuracy, however, it is not suitable to do optimization of the layout before the prototype design. Estimation by formula for the self-inductance and mutual-inductance has a simple calculation process, but its accuracy becomes lower in irregular layouts. The accuracy of FEA simulation depends on the modeling and meshing process, whereas the modeling process is relatively complicated.

In this article, two methods based on measurement and one based on FEA simulation are proposed to extract L_{package} and M_1.

For measurement method, the *LCR* meter or impedance analyzer can only obtain the self-inductance, the mutual inductance cannot be obtained directly by measurement. Therefore, two indirect measuring methods are proposed here. Only one voltage probe and one high-frequency current probe are employed.

1) Method 1: Use the relationship between voltage and current: Zoom in on Fig. 10, the waveform at t_0 is shown in Fig. 15. At t_0, $V_{GS\_SR1,3}$ turns OFF. According to the datasheet of smart IC NCP4303A selected in the prototype, the typically turn-OFF delay time from the voltage detection input to the driver is about 40 ns. Therefore, the real zero-crossing time t_1 of V_{sense} (V_{sense} is not shown in Fig. 10) is 40 ns earlier than t_0.

At time t_1, according to (2)

$$V_{off\_th} = \frac{di_{SR1}}{dt}\left(M_1 + L_{\text{package}}\right)\Big|_{t_1} + i_{SR1}(t_1) R_{DS\_ON}. \tag{13}$$

To simplify the analysis, the turn-OFF threshold voltage of SR IC V_{off_th} is assumed to zero. The parasitic inductance (L_{stray}) can be written as

$$L_{\text{stray}} = M_1 + L_{\text{package}} = -\frac{i_{SR1}(t_1) R_{DS\_ON}}{\frac{di_{SR1}}{dt}\Big|_{t_1}}. \tag{14}$$

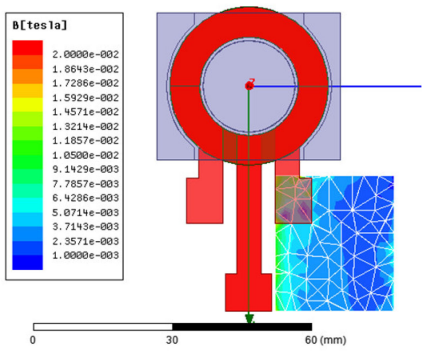


Fig. 16. Magnetic flux density distribution of single transformer.

ΔI and ΔT in Fig. 15 is substituted to $\frac{di_{SR1}}{dt}|_{t_1}$ in (14). According to Fig. 15, i_{SR1} at t_1 is about 36.4 A, and the ON-resistance is 1.4/3 mΩ. By calculating, L_{stray} is 0.242 nH.

2) Method 2: Use the Relationship Between the T_{lead} *and* M_1, $\text{L}_{\text{package}}$.*:* From (3), T_{lead} is related to the L_{package} and M_1. Substituting f_r of 160 kHz, on-resistance of 1.4/3 mΩ, and T_{lead} of 450 ns into (3), L_{stray} of 0.226 nH can be obtained.

3) Method 3: Use FEA Simulation: The accuracy of the FEA is highly relevant to modeling method. In order to improve the modeling accuracy, software ansoft-links is applied in PCB modeling process. First, simplify the PCB layout on the altium designer and generate ansoft neutral files, then translate ansoft neutral files to the solid model by ansoft-links. The mutual inductance M_1 of –0.360 nH is obtained by the FEA tool. L_{package} measured by *LCR* meter is 0.6 nH. Finally, L_{stray} of 0.24 nH can be obtained.

Compared with method 1, the accuracy of method 2 is constrained by load since the smaller load leads the more distortion to the waveform of I_{SEC}. Hence, under light load condition, method 2 is no longer applicable. In addition, the method 1 can avoid the tedious modeling process compared with method 3.

In the end, the L_{stray} of 0.24 nH is employed for the following design procedure.

B. Design of the Compensation Turn

In this section, the design of cancellation turn compensator without *RC* is taken as an example to show how to obtain M_3 based on a wire turn.

Different prototypes own various magnetic flux distribution. Taking the proposed prototype as an example, the magnetic flux density distribution near the voltage detection loop can be obtained by FEA, as shown in Fig. 16. The magnetic flux density distribution of the center-tap of the single transformer is similar to a long straight wire. The magnetic flux density is approximately independent of vertical direction but decreases in horizontal direction.

Five abstract FEA cases about how to place the wire turn is shown in Fig. 17. Center-tap of the transformer in Fig. 16 is simplified to a long straight orange wire, the voltage detection loop and the compensation wire turn in these cases are simplified to a green or a yellow rectangular coil with one turn, respectively.

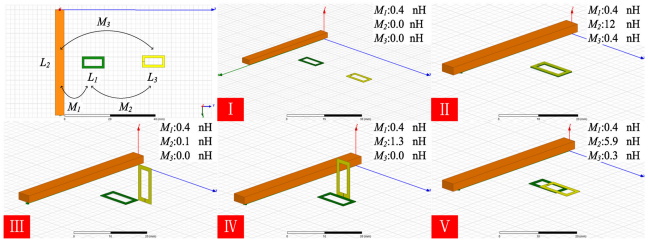


Fig. 17. Five abstract FEA cases of wire turn placement.

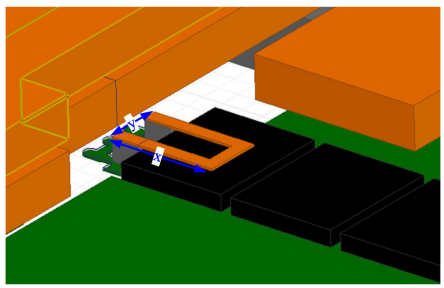


Fig. 18. 3-D layout of the added wire turn.

Among type III and IV, there is little magnetic flux coupling between L_2 and L_3, thus M_3 closes to zero. Type II is a special case where the compensator layout is exactly the same as the detection loop layout, thus $M_1 = M_3$. In the case, the voltage detection loop could be immune to external interference. However, it is difficult to achieve unless a multilayer PCB is utilized in type II. Type V presents a general case, compared with type II, it is easy to be implemented. When the compensation wire turn is moved far away from the voltage detection loop, the coupling between L_1 and L_3 can be ignorable, namely, $M_2 = 0$. In this case, type V is equivalent to type I.

According to the above analysis, M_3 can be generated by a wire turn in type II or V placement. Considering a zero ohm resistor used as a jumper, as shown in enlarged part in Fig. 2(a), it can be replaced by the compensation turn. Hence, the type V placement is selected here finally.

Because the values of L_{package} and M_1 are relatively small, hence M_3 has a small value as well and it can be constructed by one turn coil. A 3/4 rectangle enameled wire turn is in series with the smart IC, and the 3-D layout of the added wire turn is shown in Fig. 18.

Assuming the rectangle wire turn with length of x and width of y, y has a fixed value since the zero ohm resistor with length of 2 mm. The position of the wire turn has been fixed as well, and x becomes the only parameter to be regulated. The relationship between M_3 and x can be obtained by optimetrics option function in ANSYS Maxwell. The FEA simulation result of M_3 is provided in Fig. 19, where x ranges from 2 to 10 mm, step size = 1 mm, and $y = 2$ mm. Take cancellation turn compensator without *RC* filter as an example, to satisfy the (7), M_3 of 0.24 nH should be selected to cancel L_{stray}. From Fig. 19, x should range from 2 to 4 mm. Since the FEA simulation only give a coarse size of wire turn, further size optimization is needed.

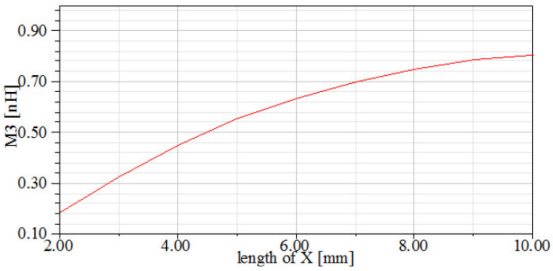


Fig. 19. FEA simulation result of the relationship between x and M_3.

TABLE III
PARAMETERS OF THE PROTOTYPE

Parameters/Specification	Value
U_i	350-450 V
f_r / f_s	160 kHz / 110-150 kHz
P_{out}	1500W
S_1-S_2 / SR_1-SR_4	C2M0040120D / BSC014N06NS×3
C_r C_p L_r L_p	64 nF 80 nF 15 uH 80 uH
V_{out} / I_{out} / R_{load}	14V / 107A / 0.13Ω
C_o	5000 uF
Size of compensator 1	x:3.26 mm y:1.76 mm
Size of compensator 2	x:3.64 mm y:1.76 mm

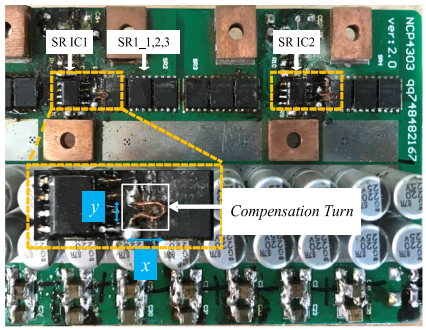
V. EXPERIMENTAL RESULTS

A 400-V input, 14-V output, 150-W half-bridge *LCLC* with SR is employed to verify the mentioned theoretical analysis. The half-bridge *LLC* IC UCC25600 is used as the primary side controller. The secondary side controller NCP4303A is selected to realize synchronous rectification. The resonant frequency f_r is set as 160 kHz, while the switching frequency f_S is set lower than f_r. The circuit parameters of the prototype are shown in Table III.

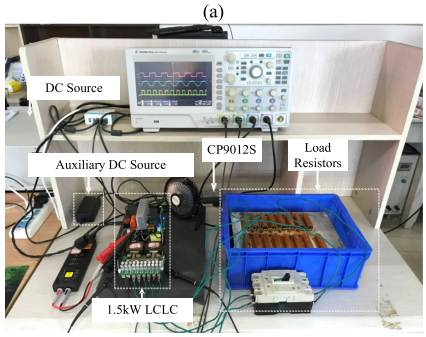
Fig. 20(a) shows the image of secondary side with compensation turn and Fig. 20(b) shows the photograph of test platform. The ac flexible current probe (CP9012S by CYBERTEK) is employed to measure the current I_{SEC}.

Fig. 21 demonstrates the benefits of the proposed method for duty cycle compensation, the waveforms of V_{GS}, I_{SEC}, and V_{ab} are captured for the prototype with/without compensator. In Fig. 21, with a compensator, the ON-time of the SR FETs is significantly extended about 220 ns. Fig. 22 shows waveforms at light load and full load, respectively.

Fig. 23 shows the experimental waveforms of the transient experiment. In Fig. 23(a), the output power of the converter drops from 1200 to 400 W. In Fig. 23(b), the output power rises from 400 to 1200 W. The experimental results suggest that the proposed compensation method can be applied to transient operation well. It is worth noted that there is some unbalance for I_{SEC} in Fig. 23, which may be caused by the asymmetric V_{ab}. Fig. 24 compares the operating efficiency of the prototype with compensator and without compensator at the different loads but the same 400 V input. Efficiency increases obviously, especially, from 94.6% to 95.4% at 1400 W. Equivalently, the loss is reduced by approximately 11 W. The thermal images of secondary side in thermal equilibrium with 400 V input voltage and 1200 W



(a)



(b)

Fig. 20. Image of the proposed prototype. (a) Image of secondary side with compensation turn. (b) Image of test platform.

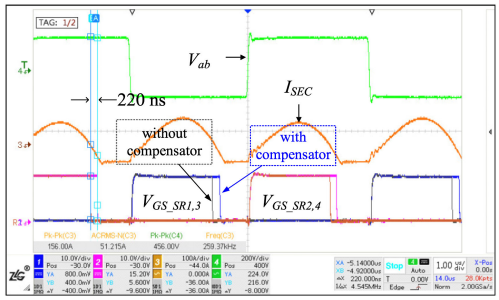
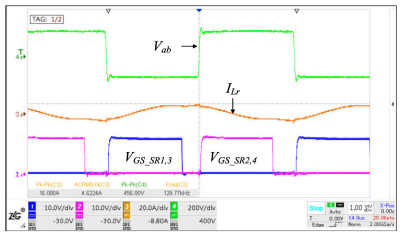
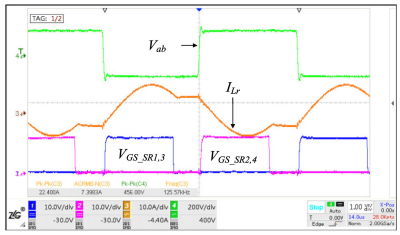


Fig. 21. Steady-state waveforms with $V_o = 14$ V, $V_{in} = 400$ V, $P_o = 1400$ W.



(a)



(b)

Fig. 22. Steady-state experimental waveforms with $V_o = 14$ V, $V_{in} = 400$ V. (a) $P_o = 200$ W. (b) $P_o = 1500$ W.

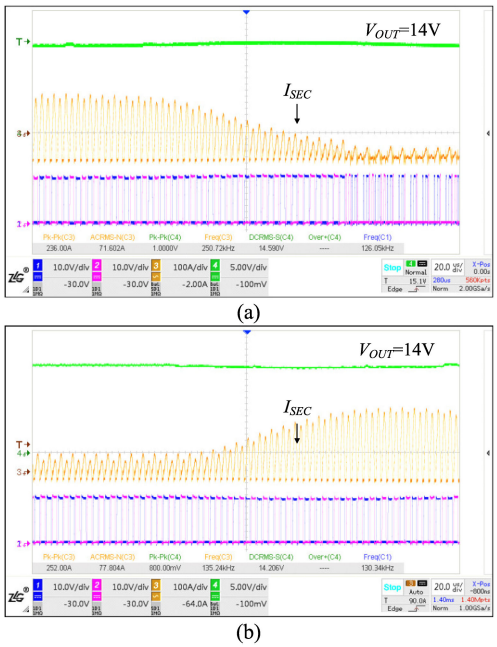


Fig. 23. Transient waveforms with $V_o = 14$ V, $V_{in} = 400$ V. (a) R_L steps from 167 to 500 mΩ. (b) R_L steps from 500 to 167 mΩ.

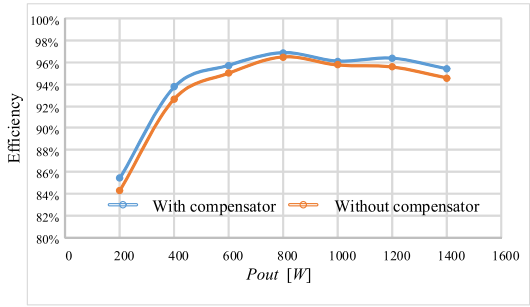


Fig. 24. Efficiency comparison between with/without compensator.

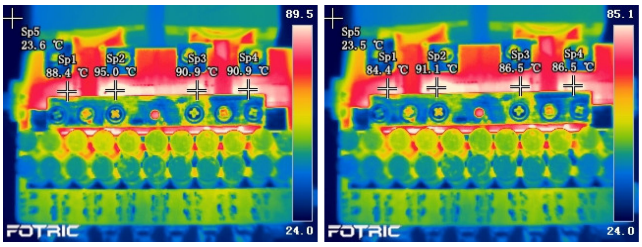


Fig. 25. Thermal images of secondary side with $V_{in} = 400$ V, $P_o = 1200$ W. (a) Without compensator. (b) With compensator.

output power is shown in Fig. 25, the temperature of SR FETs can be reduced by 4 °C with the help of proposed compensator.

VI. Conclusion

In this article, the duty cycle loss issue of SR FETs caused from parasitic parameter effect or inductive coupling effect is discussed. Based on the magnetic flux cancelation principle and vector analysis, a compensator is proposed to eliminate the error voltage from the voltage detection network. The compensator demonstrates such benefits: first, the duty cycle loss caused by both the mutual inductance and stray inductance has been reduced. Second, the SR timing could be corrected without additional passive components. Third, no high current flows through the compensation coil and no additional loss is brought. Fourth, the compensator never brings extra effect to steady and dynamic performance. Fifth, it can be supported by various smart IC and easy to implement. The experimental results suggest that the efficiency increases obviously with the compensator, which proves the correctness and effectiveness of proposed method.

Acknowledgment

This article was carried out by B. Cheng and H. Zhou. The authors would like to acknowledge their invaluable cooperation in preparing the experimental results.

References

[1] Y. Liu, A. Pratt, P. Kumar, M. Xu, and F. C. Lee, "390V input VRM for high efficiency server power architecture," in *Proc. 22nd Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2007, pp. 1619–1624.

[2] Y. Zhang, D. Xu, M. Chen, Y. Han, and Z. Du, "LLC resonant converter for 48 V to 0.9 V VRM," in *Proc. 35th Annu. Power Electron. Spec. Conf.*, 2004, pp. 1848–1854.

[3] X. Xie, J. C. P. Liu, F. N. K. Poon, and M. H. Pong, "A novel high frequency current-driven synchronous rectifier applicable to most switching topologies," *IEEE Trans. Power Electron.*, vol. 16, no. 5, pp. 635–648. Sep. 2001.

[4] X. Wu, B. Li, Z. Qian, and R. Zhao, "Current driven synchronous rectifier with primary current sensing for LLC converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2009, pp. 738–743.

[5] X. Wu, G. Hua, J. Zhang, and Z. Qian, "A new current-driven synchronous rectifier for series–parallel resonant (LLC) DC–DC converter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 289–297, Jan. 2011.

[6] B. Kim, H. Park, S. C. Moon, Y. Kim, D. Kim, and G. Moon, "The novel synchronous rectifier driving method for LLC series resonant converter," in *Proc. 38th Annu. Conf. IEEE Ind. Electron. Soc.*, 2012, pp. 810–813.

[7] J. Zhang, J. Liao, J. Wang, and Z. Qian, "A current-driving synchronous rectifier for an LLC resonant converter with voltage-doubler rectifier structure," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1894–1904, Apr. 2012.

[8] J. Liao, J. Wang, J. Zhang, and Z. Qian, "A novel current driving scheme for LLC resonant converter with synchronized voltage-doubler rectifier," in *Proc. 26th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2011, pp. 566–570.

[9] H. Ding and P. Green, "IR11688 smart rectifier control IC design notes," *Infineon Technol.*, pp. 4–6, Jul. 2015. [Online]. Available: https://www.infineon.com/dgdl/Infineon-ApplicationNote-IR11688-SmartRectifier-Control-IC-DesignNotes-AN-v01_00-EN.pdf?fileId=5546d46253f65057015418afca1d4d20

[10] International Rectifier, "IR11682S: Dual smart rectifier driver IC," pp. 13–15. Jul. 2017. [Online]. Available: https://www.infineon.com/dgdl/ir11682spbf.pdf?fileId=5546d462533600a4015355c47188165a

[11] ST Microelectronics, "Synchronous rectifier smart driver for LLC resonant converters," pp. 9–16, May 2017. [Online]. Available: https://www.st.com/resource/en/datasheet/srk2000a.pdf

[12] ON-semiconductor, "Secondary side synchronous rectification driver for high efficiency SMPS topologies," pp. 1–30, Apr. 2015. [Online]. Available: https://www.onsemi.com/pub/Collateral/NCP4303-D.PDF

[13] NXP Semiconductors, "TEA1995T green chip dual synchronous rectifier controller," pp. 5–8, Dec. 2017. [Online]. Available: https://www.nxp.com/docs/en/data-sheet/TEA1995T.pdf

[14] D. Fu, Y. Liu, F. C. Lee, and M. Xu, "A novel driving scheme for synchronous rectifiers in LLC resonant converters," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1321–1329, May 2009.

[15] J. Wang, J. Zhang, G. Zhang, M. Xu, and Z. Qian, "Research on key application issues of smart synchronous rectifier driver IC in LLC resonant converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2011, pp. 2765–2770.
[16] D. Wang and Y. Liu, "A zero-crossing noise filter for driving synchronous rectifiers of LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1953–1965, Apr. 2014.
[17] Chen, "Adaptive synchronous rectification control circuit and method thereof," U.S. Patent 7 495 934, Feb. 24, 2009.
[18] W. Feng, F. C. Lee, P. Mattavelli, and D. Huang, "A universal adaptive driving scheme for synchronous rectification in LLC resonant converters," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3775–3781, Aug. 2012.
[19] C. Fei, W. Feng, F. C. Lee, and Q. Li, "State-trajectory control of LLC converter implemented by microcontroller," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 1045–1052.
[20] C. Fei, Q. Li, and F. C. Lee, "Digital implementation of adaptive synchronous rectifier (SR) driving scheme for high-frequency LLC converters with microcontroller," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5351–5361, Jun. 2018.
[21] J. Hsu, M. Ordonez, W. Eberle, M. Craciun, and C. Botting, "LLC synchronous rectification using resonant capacitor voltage," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10970–10987, Nov. 2019.
[22] M. Mohammadi and M. Ordonez, "Synchronous rectification of LLC resonant converters using homopolarity cycle modulation," *IEEE Trans. Ind. Electron.,* vol. 66, no. 3, pp. 1781–1790, Mar. 2019.
[23] Y. Chen, "LCLC converter with optimal capacitor utilization for hold-up mode operation," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2385–2396, Mar. 2019.
[24] J. Chen, L. He, and B. Cheng, "Optimized parameter design method for wide-input-voltage LLC converter with frequency-based self-adapted magnetizing inductance," in *Proc. IEEE Int. Symp. Predictive Control Elect. Drives Power Electron.*, 2019, pp. 1–4.
[25] D. Huang, S. Ji, and F. C. Lee, "LLC resonant converter with matrix transformer," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4339–4347, Aug. 2014.
[26] S. Wang, R. Chen, F. C. Lee, and J. D, "Improved passive filter configurations for high-frequency conducted EMI in power electronics," in *Proc. Euro. Conf. Power Electron. Appl.*, 2005, p. 1–16.
[27] D. Fu, B. Lu and, and F. C. Lee, "1MHz high efficiency LLC resonant converters with synchronous rectifier," in *Proc. IEEE Power Electron. Specialists Conf.*, 2007, pp. 2404–2410.
[28] S. Maniktala, *Switching Power Supplies A – Z*, 2nd edition. New York, NY, USA: Elsevier, 2012, pp. 597–620.
[29] J. Zhang, "Choosing the right power MOSFET package," *Infineon Technol.*, pp. 1–6, Feb. 2004. [Online]. Available: https://www.infineon.com/dgdl/mosfetpackageeepn0204.pdf?fileId=5546d462533600a40153574455f93f58

Liangzong He (Member, IEEE) was born in Hunan, China, in 1984. He received the B.Sc. degree from Jilin University, Changchun, China, in 2006, and the Ph.D. degree from the Huazhong University of Science and Technology, Wuhan, China, in 2012.

From November 2009 to August 2011, he was a Joint Ph.D. Education Student with Michigan State University, East Lansing, MI, USA. In September 2012, he joined as an Assistant Professor with Xiamen University, Xiamen, China, where he has been a Professor since August 2019. His research interests include dc–dc converters, switched-capacitor converters, Z-source converters, wireless power transmission, and microgrids.

Jiazhe Chen was born in Fujian, China, in 1993. He received the B.E. degree from the College of Physics and Information Engineering, Fuzhou University, Fuzhou, China, in 2016. He is currently working toward the master's degree with the School of Aerospace Engineering, Xiamen University, Xiamen, China.

His research interests focus on the topology and control of resonant converters.

Bing Cheng was born in Henan, China, in 1996. He received the B.E. degree from Xiamen University, Xiamen, China, in 2018. He is currently working toward the master's degree with the Department of Instrumental and Electrical Engineering, Xiamen University, Xiamen, China.

His research interests include modeling and control of wireless power transfer and power electronics.

Hongyan Zhou was born in Hebei, China, in 1998. He received the B.E. degree from Xiamen University, Xiamen, China, in 2019. He is currently working toward the master's degree with the Department of Instrumental and Electrical Engineering, Xiamen University, Xiamen, China.

His research interests include system stability analysis and power electronics.