Letters

Dual-Path Three-Level Buck Converter With Loop-Free Autocalibration for Flying Capacitor Self-Balancing

Woojoong Jung, *Student Member, IEEE*, Se-Un Shin, *Member, IEEE*, Sung-Wan Hong, *Member, IEEE*, Sung-Min Yoo, Tae-Hwang Kong, Jun-Hyeok Yang, Sang-Ho Kim, Michael Choi, Jongshin Shin, *Member, IEEE*, and Hyung-Min Lee, *Member, IEEE*

***Abstract*—This letter proposes a loop-free autocalibration technique for self-balancing of flying capacitors in a three-level dc–dc buck converter. The proposed converter utilizes a dual-path power stage with balancing switches that adaptively short flying capacitors at de-energizing phases. Thus, the dual-path three-level converter ensures that flying capacitor voltages are self-balanced at half the input voltage without using additional feedback calibration loops, leading to robust operation and competitive efficiencies. The prototype was fabricated in the 0.13-μm CMOS BCD process and adopted two flying capacitors of 4.7 μF each and an inductor of 10 μH with a dc resistance of 128 mΩ. When an 8-V input was converted to a 3-V output voltage with a load current of 400 mA, the measured efficiency was 88.6% at 800 kHz switching while flying capacitors are automatically balanced.**

***Index Terms*—Dual path, flying capacitor, loop-free calibration, self-balancing, three-level buck converter.**

I. Introduction

NOWADAYS, the demand for step-down dc–dc converters is rapidly growing as many products need different specifications, such as battery-charging and battery-powered products [1]. Battery-powered systems typically operate at low supply voltages to minimize power consumption. For example, the typical voltage of a Li–ion battery is 3.7 V, but Internet of Things products are powered by a 1-V supply converted from a Li–ion battery [2]. Thus, a step-down converter with a low conversion ratio (CR) (e.g., $V_{\rm OUT}/V_{\rm IN} < 0.45$) is highly desired.

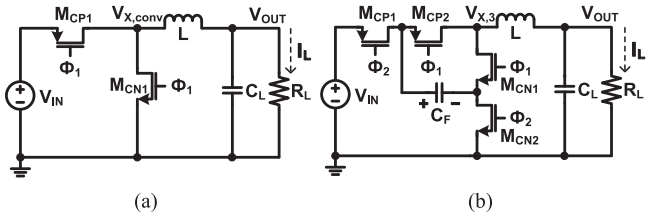

Fig. 1. Conventional (a) two-level and (b) three-level buck converters.

However, a conventional two-level buck converter, shown in Fig. 1(a), with a low CR has two primary disadvantages. First, the buck converter needs high-voltage transistors (e.g., >8 V) to endure a high supply voltage without breakdown. Such transistors are large and suffer from high switching losses due to their large parasitic capacitance. Second, the converter suffers from large inductor current ripple, leading to high conduction losses. While the inductance and operating frequency can be chosen to satisfy the ripple demands, $V_{X,\rm conv}$ of the buck converter swings $V_{\rm IN}$ to GND, which induces a large voltage difference between $V_{X,\rm conv}$ and $V_{\rm OUT}$, and thus a large inductor current ripple. The power dissipation at an inductor dc resistance $P_{\rm LDC}$ is related to a square term of the current ripple, which can be expressed as

$$P_{\rm LDC} = I_{L,\rm RMS}^2 \times R_{\rm LDC} = \left(\sqrt{I_L^2 + \Delta i_L^2/12}\right)^2 \times R_{\rm LDC} \tag{1}$$

where $I_{L,\rm RMS}$ is a root-mean-square value of a load current I_L and $R_{\rm LDC}$ is an inductor dc resistance. Large inductor current ripple Δi_L increases $I_{L,\rm RMS}$ and $P_{\rm LDC}$, limiting the efficiency of the two-level buck converter. Thus, the voltage difference between $V_{X,\rm conv}$ and $V_{\rm OUT}$ needs to be reduced to increase efficiency.

A three-level buck converter in Fig. 1(b) initially charges a flying capacitor C_F to half $V_{\rm IN}$ and makes the swing range of a switching node $V_{X,3}$ becomes half, i.e., either between $V_{\rm IN}$ and $V_{\rm IN}/2$ or between $V_{\rm IN}/2$ and GND. Moreover, the effective switching frequency is doubled compared with that of the two-level buck converter. Thus, normalized inductor current

Manuscript received April 1, 2020; revised May 5, 2020 and June 3, 2020; accepted June 15, 2020. Date of publication June 17, 2020; date of current version September 4, 2020. This work was supported by Samsung Electronics, South Korea. *(Corresponding authors: Hyung-Min Lee; Se-Un Shin.)*

Woojoong Jung and Hyung-Min Lee are with the School of Electrical Engineering, Korea University, Seoul 02841, South Korea (e-mail: dneld156@korea.ac.kr; hyungmin@korea.ac.kr).

Se-Un Shin is with the Department of Display Engineering, Dankook University, Cheonan 330-714, South Korea (e-mail: seuns@dankook.ac.kr).

Sung-Wan Hong is with the Department of Electronics Engineering, Sookmyung Women's University, Seoul 140-742, South Korea (e-mail: hsw0930@sookmyung.ac.kr).

Sung-Min Yoo, Tae-Hwang Kong, Jun-Hyeok Yang, Sang-Ho Kim, Michael Choi, and Jongshin Shin are with the Foundry Business, Samsung Electronics, Hwaseong 18448, South Korea (e-mail: sungmin.yoo@samsung.com; t.h.kong@samsung.com; jh0812.yang@samsung.com; sh35.kim@samsung.com; michael.b.choi@samsung.com; jongshin.shin@samsung.com).

Color versions of one or more of the figures in this article are available online at https://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2020.3003519

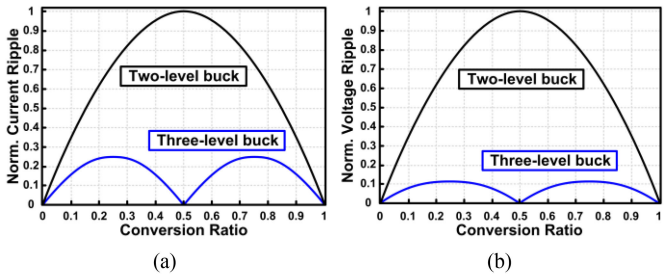

Fig. 2. Comparison of the normalized (a) current ripple and (b) voltage ripple.

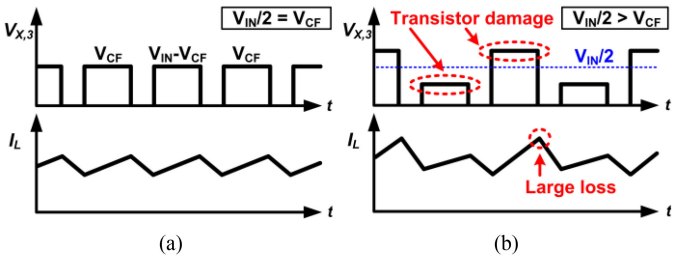

Fig. 3. Waveforms of (a) ideal and (b) practical three-level buck converters.

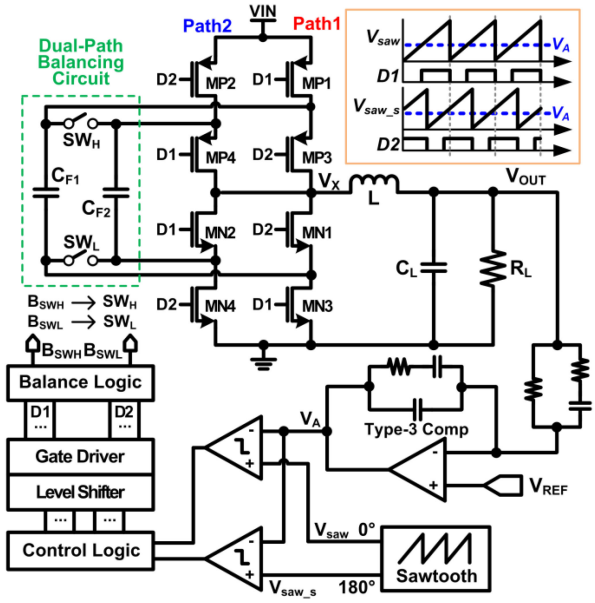

Fig. 4. Block diagram of the proposed dual-path three-level buck converter.

and output voltage ripples of the three-level buck converter are reduced by four times and eight times, respectively, as shown in Fig. 2(a) and (b), thus reducing the conduction losses of the converter [3], [4].

An additional benefit of the three-level converter is that switching loss is also reduced. High-voltage transistors (e.g., 8-V Tr.) used for power switches can be replaced with low-voltage transistors (e.g., 5-V Tr.), which can provide smaller gate capacitance and lower ON-resistance, because the voltages across transistors decrease to below half the input voltages, as shown in Fig. 3(a). However, the practical operation of the three-level converter suffers from parameter mismatches in power transistors, leakages, gate signal timing, and parasitic capacitors, which lead to voltage variations in C_F during phase transition [4]. The switching node voltage $V_{X,3}$ can then be different at each operation phase, as shown in Fig. 3(b), increasing inductor current ripples and conduction losses. In addition, the power transistors can breakdown if voltage differences across transistors exceed the tolerable range due to unbalancing of the flying capacitor voltage.

To prevent this issue and minimize the inductor current ripple, state-of-the-art papers have suggested calibration techniques to balance the flying capacitor voltages in three-level buck converters [5]–[7]. However, the techniques utilized additional feedback control loops to sense the capacitor voltage and adjust the gate signals of power switches, which were complicated to design with additional area and power consumption. Moreover, those feedback loops can be susceptible to operating conditions, such as load variations, affecting the converter operation. To overcome these limitations, this letter proposes a dual-path three-level buck converter with loop-free autocalibration, whose parallel power paths operate in a complementary fashion to automatically balance flying capacitors without using any feedback loops.

II. System Architecture

Fig. 4 shows the block diagram of the proposed dual-path three-level buck converter that adopts loop-free self-balancing of flying capacitors $C_{F1,2}$. Power switches $M_{CN1,2}$ and $M_{CP1,2}$ and a flying capacitor C_F of the original three-level converter in Fig. 1(b) are divided into two paths M_{P1}-M_{P3}-M_{N1}-M_{N3} with C_{F1} and M_{P2}-M_{P4}-M_{N2}-M_{N4} with C_{F2} while two balancing switches SW_H and SW_L are added between C_{F1} and C_{F2}. The total size of the divided power transistors $M_{N1\text{-}4}$ and $M_{P1\text{-}4}$ and flying capacitors $C_{F1,2}$ in Fig. 4 can be similar to the total size of power transistors $M_{CN1,2}$ and $M_{CP1,2}$ and the flying capacitor C_F in Fig. 1(b), respectively, because the same load current I_L is evenly divided into the dual paths. Thus, the area occupied by power switches can be maintained similar to the allocated area for the original three-level converter except two additional balancing switches while their sizes are relatively smaller than power switches, leading to small decrease in power density. The converter adopts type-3 compensation to ensure a stable feedback loop for output regulation.

In the dual-path structure, the power transistors of paths 1 and 2 operate complementary; the operation mode is depicted in Fig. 5. This letter focuses on when CR is lower than 0.5 with logic signals for power transistors in Fig. 6(a). The operation mode comprises four phases: P1 and P3 are for energizing and P2 and P4 are for de-energizing and balancing.

First, suppose that there is no parameter mismatch and the flying capacitors are initially charged to $V_{IN}/2$. During P1 phase, $M_{N3,P3}$ on path 1 and $M_{N2,P2}$ on path 2 turn ON. Half of I_L flows from V_{IN} to the load via the flying capacitor C_{F2} on path 2, and the charged voltage of C_{F2} increases. The rest of I_L flows from GND to the load via the flying capacitor C_{F1} on path 1, and then the charged voltage of C_{F1} decreases. At the end of this phase, C_{F2} is higher than $V_{IN}/2$ and C_{F1} is lower than $V_{IN}/2$. We can infer that one of $C_{F1,2}$ is charged and the other is discharged

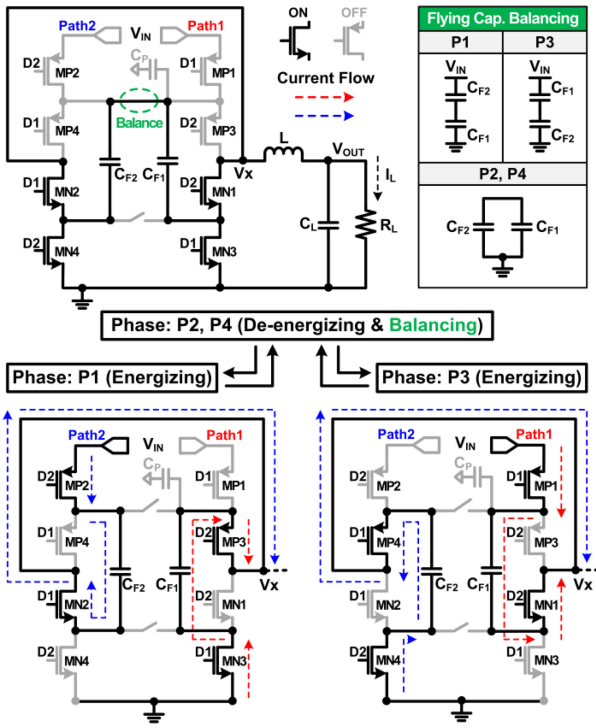

Fig. 5. Operation of the proposed dual-path three-level buck converter when CR $<$ 0.5.

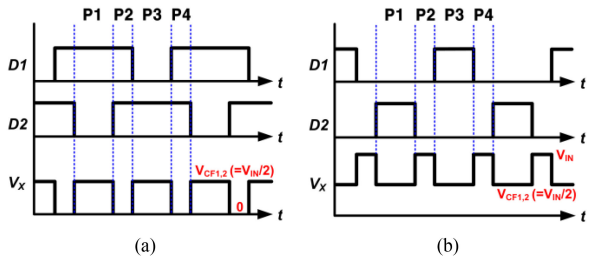

Fig. 6. Gate logic signals when (a) CR $<$ 0.5 and (b) CR $>$ 0.5.

from $V_{\rm IN}/2$ in energizing phases; this characteristic can be used in the following phase to fix balance.

In P2 phase, all NMOS transistors on both paths turn ON and all PMOS transistors turn OFF for de-energizing. Thus, the bottom of $C_{F1,2}$ is connected to GND. In this phase, $\rm SW_H$ also turns ON for balancing, which shorts C_{F1} and C_{F2} with the same voltage converging to $V_{\rm IN}/2$. It is noted that all PMOS transistors are surely OFF before $\rm SW_H$ turns ON. Moreover, the power losses across $\rm SW_H$ during balancing can be negligible since C_{F1} and C_{F2} are balanced with almost same voltage levels, minimizing the inrush current through $\rm SW_H$.

For P3 phase, $\rm M_{N3,P3}$ on path 1 and $\rm M_{N2,P2}$ on path 2 turn OFF and all other power transistors turn ON. That is, the switch operation and current direction are exactly the opposite of P1 phase. At the end of this phase, C_{F1} is higher than $V_{\rm IN}/2$ and C_{F2} is lower than $V_{\rm IN}/2$ while energizing the inductor. Then, the next phase, P4, operates the same as P2, which performs both de-energizing and balancing. It should be noted that the balancing switches operate at every de-energizing phase, and the capacitor voltages are gradually balanced to about half $V_{\rm IN}$ within multiple cycles through repetitive charge redistribution.

Even if any mismatches between path 1 and path 2, such as leakage, timing, or parasitic capacitance (e.g., C_P in Fig. 5), exist, the proposed converter still ensures that flying capacitors hold the same voltage that is approximately $V_{\rm IN}/2$, which can be proved by following equations. First, the voltages of two flying capacitors $V_{\rm CF1}$ and $V_{\rm CF2}$ are defined as follows:

$$V_{\rm CF1} = V_{\rm IN}/2 + \Delta V_1\,, \quad V_{\rm CF2} = V_{\rm IN}/2 + \Delta V_2 \tag{2}$$

where ΔV_1 and ΔV_2 are arbitrary error values in C_{F1} and C_{F2}, respectively, which are not correlated. Then, the relationship between $V_{\rm CF1}$ and $V_{\rm CF2}$ during the energizing phases P1 and P3 can be expressed as

$$P1:\ V_{\rm IN} - V_{\rm CF2} = V_{\rm CF1}\,, \quad P3:\ V_{\rm IN} - V_{\rm CF1} = V_{\rm CF2}. \tag{3}$$

Also, $V_{\rm CF1}$ and $V_{\rm CF2}$ during the de-energizing and balancing phases P2 and P4 can be expressed as

$$P2,\ P4:\ V_{\rm CF1} = V_{\rm CF2}. \tag{4}$$

By substituting (2) in (3) and (4), following equations about ΔV_1 and ΔV_2 can be derived:

$$\Delta V_1 + \Delta V_2 = 0\,, \quad \Delta V_1 = \Delta V_2 \tag{5}$$

$$\Delta V_1 = \Delta V_2 = 0. \tag{6}$$

From the above equations, ΔV_1 and ΔV_2 converge to zero, and $V_{\rm CF1}$ and $V_{\rm CF2}$ become $V_{\rm IN}/2$ through the entire operation. In short, voltages of $V_{\rm CF1,2}$ can be of equal level by arranging parallel connection of $C_{\rm F1}$ and $C_{\rm F2}$ through balancing switches in P2 and P4, but they may converge to either below or above $V_{\rm IN}/2$. In P1 and P3, however, the sum of $V_{\rm CF1}$ and $V_{\rm CF2}$ is recharged to $V_{\rm IN}$ by arranging series connection of C_{F1} and C_{F2}, resulting in self-balancing of $V_{\rm CF1}$ and $V_{\rm CF2}$ to the voltage level of $V_{\rm IN}/2$.

If CR is higher than 0.5, all PMOS transistors and the balancing switch $\rm SW_L$ are turned ON in P2 and P4 with the gate logic signals in Fig. 6(b). In this case, the self-balancing mechanism is still the same; the sum of $V_{\rm CF1}$ and $V_{\rm CF2}$ is charged to $V_{\rm IN}$ in the energizing phases, and they are rebalanced in the de-energizing phases. The voltage range of V_X changes, as shown in Fig. 6(a) and (b), and V_X is connected to either GND (CR $<$ 0.5) or $V_{\rm IN}$ (CR $>$ 0.5) in P2 and P4. It is noted that the proposed balancing technique can also be effective in dynamic transitions since the balancing switches automatically operate during de-energizing periods of the converter. That is, the balancing technique does not need additional periods but shares the existing periods, P2 and P4, which are determined through the converter control loop.

III. Circuit Details and Design Consideration

Fig. 7 depicts the circuit details of the balancing switches $\rm SW_H$ and $\rm SW_L$ and logic operation. $\rm SW_{H,L}$ consist of two series transistors in each switch to prevent the reverse current. In case of CR $<$ 0.5, if $\rm SW_H$ has only one transistor, the reverse current would flow because the voltage difference between $\rm N_{P1}$ and $\rm N_{P2}$ can be $V_{\rm IN}/2$ and $-V_{\rm IN}/2$ in phases P1 and P3, respectively.

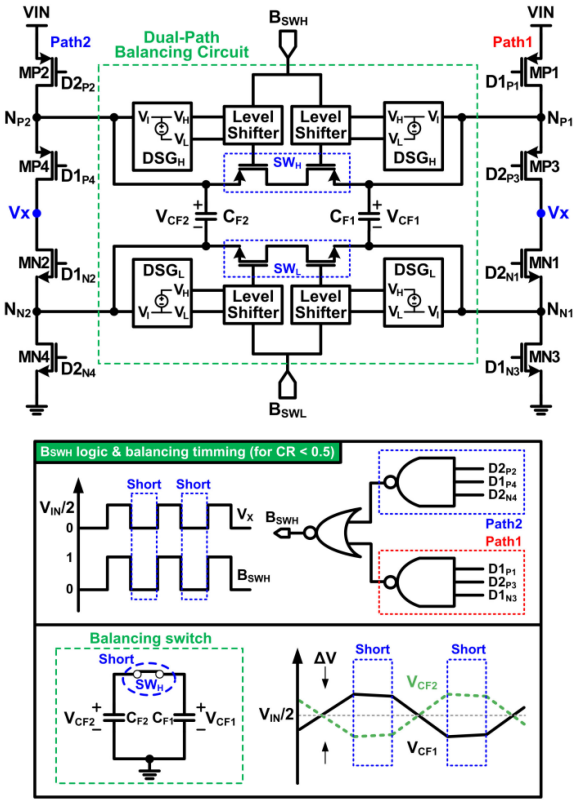

Fig. 7. Schematic diagram of balancing switches and logic operation.

The balancing logic signals B_{SWH} and B_{SWL} for $\mathrm{SW_H}$ and $\mathrm{SW_L}$, respectively, can be generated based the gate logic signals of power switches. For example, a logic circuit for B_{SWH} comprises two 3-NAND and one NOR for CR $<$ 0.5. B_{SWH} guarantees an accurate balancing timing at which $\mathrm{N_{P1,2}}$ are disconnected from V_{IN} and $\mathrm{N_{N1,2}}$ are connected to GND by sharing the gate logic signals $D1$ and $D2$. Thus, $\mathrm{SW_H}$ and $\mathrm{SW_L}$ do not turn ON during the phase transition between P1,3 and P2,4, which otherwise leads to shoot-through currents and power losses.

B_{SWH} and B_{SWL} are made with the logic supply voltage, which is typically lower than the main supply voltage. Thus, the logic signals need to be level shifted to drive $\mathrm{SW_H}$ and $\mathrm{SW_L}$ with suitable voltage levels. For example, the level shifters for $\mathrm{SW_H}$ need two levels of supply voltages V_H and V_L, which can be generated from a dynamic supply generator (DSG). The DSG for $\mathrm{SW_H}$ provides the high supply voltage V_H from $\mathrm{N_{P1,2}}$ voltages and the low supply voltage V_L by shifting down $\mathrm{N_{P1,2}}$ voltages as low as the PMOS balancing switches can fully turn ON while not exceeding the breakdown voltage.

IV. Measurement Results

Fig. 8 shows the die micrograph fabricated in a 0.13-μm CMOS BCD process. The core size is 3.7 $\times$ 3.7 mm^2, and the total size including pads is 4.5 $\times$ 4.5 mm^2. The layout utilized a symmetric structure for dual power paths to match the timing of gate signals for power switches as well as flying capacitor connections. The 10 μH inductor with DCR $=$ 128 mΩ was

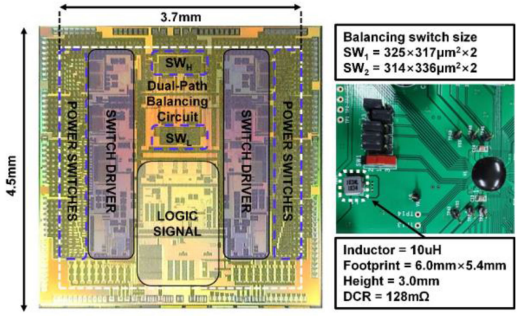

Fig. 8. Die micrograph of the proposed dual-path three-level buck converter.

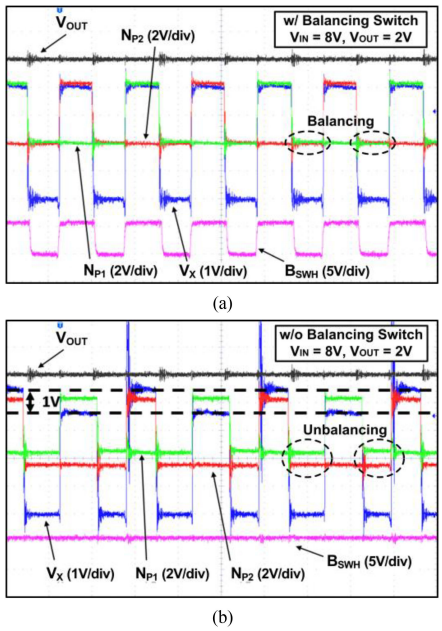

Fig. 9. Waveform of (a) with and (b) without balancing logic when CR $<$ 0.5.

chosen considering current ripple, power losses, and form factor. Each flying capacitor had 4.7 μF to decrease the voltage ripple below 50 mV and thus minimize power losses across balancing switches. Power and balancing switches utilized 5- and 12-V transistors, respectively.

Fig. 9 depicts the effects of balancing switches for autocalibration of voltages in $C_{\mathrm{F1,2}}$. When the balancing switches operate, as shown in Fig. 9(a), the $\mathrm{N_{P1,2}}$ nodes swing the same voltage levels from $V_{\mathrm{IN}}/2$ to V_{IN} but are phase shifted by 180° with each other. V_X also swings from GND to $V_{\mathrm{IN}}/2$, verifying that V_{CF1} and V_{CF2} are self-balanced. However, if the balancing switches are deactivated in the dual-path structure by intentionally turning OFF $\mathrm{SW_H}$ and $\mathrm{SW_L}$, as shown in Fig. 9(b), V_X varies irregularly due to inherent parameter and timing mismatches, implying that the balance of flying capacitors is broken. In this case, the duty cycle changes depending on V_X levels, e.g., when V_X is higher than $V_{\mathrm{IN}}/2$, duty becomes short. This unbalancing leads to not only efficiency degradation but also risk of damages in power transistors.

Fig. 10 shows the measured efficiencies when sweeping I_L and V_{OUT}. In Fig. 10(a), V_{IN} and V_{OUT} were fixed at 8 and

TABLE I
THREE-LEVEL BUCK CONVERTER BENCHMARKING

	2016 [1]	2012 [3]	2016 [5]	2018 [6]	**This work**
Process	0.13µm	0.13µm	0.5µm (120V)	0.65µm	**0.13µm (BCD)**
Topology	two-level	three-level	three-level	three-level	**three-level**
Inductor	-	1 nH/phase	1.5 µH	100 nH	**10 µH**
Flying cap.	Not required	18 nF	1 µF	5 nF	**4.7 µF × 2**
Frequency	1.5 MHz	50-200 MHz	~2 MHz	50 MHz	**0.8 - 1 MHz**
V_{IN}	6 - 16 V	2.4 V	12 - 100 V	5 V	**8 V**
V_{OUT}	2.5 - 4.2 V	0.4 - 1.4 V	10 V	0.6 - 4.2 V	**1.8 - 3.3 V**
Max. P_{OUT}	6 W	1 W	5 W	3 W	**1.35 W**
Peak efficiency	87% (V_{IN} = 9V)	77%	90%	90%	**88.6%**
Flying cap. Balancing	Not required	-	Feedback loop control	Feedback loop control	**Dual path + Loop-free calibration**

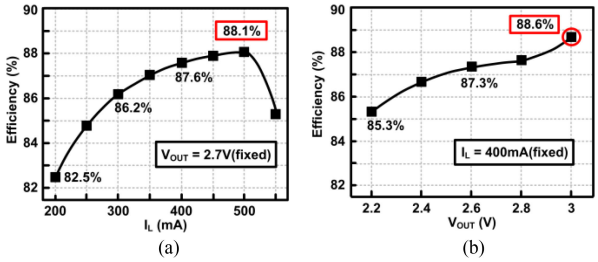

Fig. 10. Measured efficiencies when sweeping (a) I_L and (b) $V_{\rm OUT}$ at $V_{\rm IN} = 8$ V.

2.7 V, respectively, whereas I_L varies from 200 to 550 mA. The peak efficiency of 88.1% was measured at $I_L = 500$ mA. The efficiency drops at $I_L > 500$ mA resulted from increased conduction losses due to larger current flowing through power transistors. In Fig. 10(b), $V_{\rm OUT}$ varies from 2.2 to 3 V when $V_{\rm IN}$ and I_L were fixed to 8 V and 400 mA, respectively. The peak efficiency was achieved as 88.6% at $V_{\rm OUT} = 3$ V because larger $V_{\rm OUT}$ decreases the inductor current ripple, reducing RMS losses across inductor DCR and power transistors. When $V_{\rm IN} = 8$ V, $V_{\rm OUT} = 2.7$ V, and $I_L = 500$ mA, the simulation results show that the voltage difference between C_{F1} and C_{F2}, which is ΔV in Fig. 7, can be up to 45 mV. In case the balancing period becomes too short depending on CR (e.g., $0.45 <$ CR < 0.5), ΔV increases, which may limit the balancing operation. Then, each capacitor voltage increases or decreases by about 3 mV during the balancing period, leading to the total energy consumption of 0.65 nJ. Thus, the average power consumption required for balancing operation at switching frequency of 800 kHz is about 0.52 mW, which is negligible compared to the output power of 1.35 W. In case PMOS power switches have intended size mismatches up to 30%, the balancing switches still operate properly, resulting in similar power dissipation that is still negligible.

Table I benchmarks the proposed converter with state-of-the-art works. The proposed dual-path converter operates with low CR, i.e., $V_{\rm IN} > 8$ V and $V_{\rm OUT} = 1.8$–3.3 V, which can be utilized for various applications, such as fast battery charger and vehicle electronics. Unlike previous three-level converters that need additional feedback loops for flying capacitor balancing, the proposed converter adopts a loop-free autocalibration method, which enables a simple and robust structure for self-balanced three-level operation. The total size of power transistors and the total capacitance of flying capacitors in the dual paths can be similar to those in the original converter since divided currents flow through each path and flying capacitor. While the proposed converter enables loop-free self-balancing with the dual-path topology, it also achieved competitive efficiencies up to 88.6% compared to other three-level converters even considering that [5] had much higher input/output voltage ranges and [6] used an integrated flying capacitor at higher switching frequency.

V. CONCLUSION

The proposed three-level buck converter utilizes a dual-path power stage with two flying capacitors and adopts loop-free balancing switches between them to automatically calibrate the capacitor voltages. The balancing switches adaptively short flying capacitors at every de-energizing phase while not affecting the converter operations, ensuring that capacitor voltages are self-balanced at half the input voltage without requiring an additional feedback calibration loop. Consequently, the proposed converter guarantees simple and robust three-level operation with low-voltage transistors, which decreases inductor current ripples and improves power efficiencies, especially for applications where the input voltage is much higher than the target output voltage.

REFERENCES

[1] M.-G. Jeong, S.-H. Kim, and C. Yoo, "Switching battery charger integrated circuit for mobile devices in a 130-nm BCDMOS process," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7943–7952, Nov. 2016.
[2] S. S. Amin and P. P. Mercier, "A fully integrated Li-ion-compatible hybrid four-level DC–DC converter in 28-nm FDSOI," *IEEE J. Solid State Circuits*, vol. 54, no. 3, pp. 720–732, Mar. 2019.
[3] W. Kim, D. Brooks, and G.-Y. Wei, "A fully-integrated 3-level DC-DC converter for nanosecond-scale DVFS," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 206–219, Jan. 2012.
[4] X. Liu, P. K. T. Mok, J. Jiang, and W.-H. Ki, "Analysis and design considerations of integrated 3-level buck converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 5, pp. 671–682, May 2016.
[5] J. Xue and H. Lee, "A 2 MHz 12–100 V 90% efficiency self-balancing ZVS reconfigurable three-level DC-DC regulator with constant- frequency adaptive-on-time V^2 control and nanosecond-scale ZVS turn-on delay," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2854–2866, Dec. 2016.
[6] X. Liu and P. K. T. Mok, "A high-frequency three-level buck converter with real-time calibration and wide output range for fast-DVS," *IEEE J. Solid-state Circuit.*, vol. 53, no. 2, pp. 582–595, Feb. 2018.
[7] E. Abdelhamid, L. Corradini, P. Mattavelli, G. Bonanno, and M. Agostinelli, "Sensorless stabilization technique for peak current mode controlled three-level flying-capacitor converters," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 3208–3220, Mar. 2020.