Determination of RMS Current Load on the DC-Link Capacitor of Voltage Source Converters Using Direct Current Control

Sebastian Raab, Andreas Krämer, and Ansgar Ackva

***Abstract*—RMS current load is one of the most important design criteria for the dc-link capacitors of voltage source converters. In the literature, determination of this rms current load is well documented for state-of-the-art modulation schemes, such as space vector modulation. But the methods presented cannot be applied for direct current control algorithms. Therefore, this article introduces a new approach especially for direct current controllers, which reflects and compares to the state-of-the-art calculation method for space vector modulation. As direct current control is a feedback control, no closed-form solution can be given. Instead, the dc-link capacitor rms current load is determined by an iterative calculation scheme as a function of the modulation level and the phase angle. Although the scheme presented is applied to a three-phase two-level voltage source converter, it can be adapted to any voltage source converter topology. An example is presented applying the calculation method to one specific direct current control algorithm. The calculated results are verified via a digital simulation model as well as test bench measurements showing good correlation. For correct comparison, different effects are considered and discussed between simulation, calculation, and measurement results. These contain transients, the commutation process between insulated gate bipolar transistor (IGBT) and diode, the current-dependent voltage drop of the semiconductors, and the stationary current error of the hysteresis control. The dc-link capacitor current load for space vector modulation is calculated analytically as a reference by using the state-of-the-art method. The comparison of results obtained in this article and the reference are very similar, which is discussed in the conclusion.**

***Index Terms*—AC-DC power converters, converters, current control, DC-AC power converters, electric variables control, power electronics, power engineering and energy.**

I. Introduction

IN INDUSTRIAL as well as automotive drive trains, two-level voltage source converters (VSCs) can be considered as state-of-the-art technology. For proper operation of VSCs, their dc voltage needs to be stabilized by the use of capacitors, as shown exemplarily in Fig. 1. The kind of capacitor strongly depends on the application. For example, in automotive traction drive trains, efforts are made in lowering the capacitors footprint and costs that cause 14% to 16% of the total costs of the traction drive VSC [1]. For correct capacitor specification, the current load I_{C1} as well as the capacitor ripple voltage $U_{\mathrm{C1}\sim}$ have to be determined precisely.

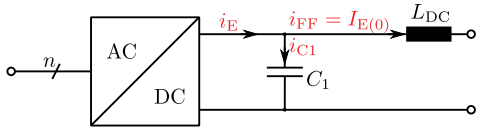

Fig. 1. VSC with dc-link capacitor.

In [2], a method for the analytical calculation of dc-link capacitor current load is described by means of a space vector modulation (SVM) controlled VSC. For this purpose, the root-mean-square (rms) value of the distortion current at the VSCs dc-side $I_{\mathrm{E}\sim}$ is a valid measure. $I_{\mathrm{E}\sim}$, often called the ripple current, is determined from the rms value I_{E} and its dc component $I_{\mathrm{E(0)}}$ according to (1). Assuming ideal filtering given for the conditions in (2), $I_{\mathrm{E}\sim}$ can be interpreted as I_{C1}

$$I_{\mathrm{E}\sim} = \sqrt{I_{\mathrm{E}}^2 - \mathrm{I}_{\mathrm{E(0)}}^2} \tag{1}$$

$$I_{\mathrm{E}\sim} = I_{\mathrm{C1}} \text{ for } \omega L_{\mathrm{DC}} >> \frac{1}{\omega C_1}. \tag{2}$$

Equation (1) can be applied to various pulsewidth modulation (PWM) schemes. Literature can be found where $I_{\mathrm{E}\sim}$ is also used to determine the dc-link capacitor current load for interleaved VSC systems [3]. In [4], the normalized distortion current load factor of the dc-link is defined as

$$K_{\mathrm{DC}} = \frac{I_{\mathrm{E}\sim}^2}{I_n^2} \text{ with } n = \mathrm{U}, \mathrm{V}, \mathrm{W} \tag{3}$$

where I_n represents the rms values of the VSCs three-phase ac-side currents. The rms values of the phase currents are assumed to be equal, so $I_n = I_{\mathrm{N}}$.

In [4], it is shown that the unitless distortion current load factor K_{DC} is independent of the ac current. It only depends on the modulation level m_{a} and the phase displacement angle φ. Therefore, it is suitable for comparing the impact of different modulation as well as direct control methods on the dc-link capacitor current load [5], [6]. In [7], K_{DC} is applied and calculated

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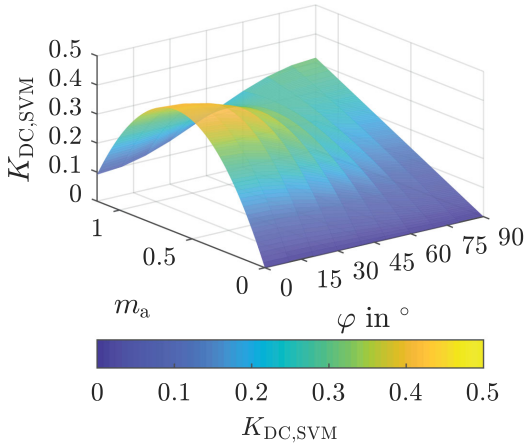

Fig. 2. Normalized distortion current load factor of the dc-link for SVM.

for the reduced common mode voltage PWM, a PWM technique specifically developed to alleviate common mode voltages.

In Fig. 2, K_DC for SVM is shown depending on m_a defined by (4) and φ. Here, $\hat{u}_{n(1)}$ with $n = \mathrm{U,V,W}$ describes the amplitude of the VSC neutral point output voltage u_n at fundamental frequency

$$m_\mathrm{a} = \frac{2\hat{u}_{n(1)}}{u_{\mathrm{C1}}}. \tag{4}$$

Since SVM is the most widely used modulation method for VSCs, the calculated characteristic values are subsequently used as a reference for comparison.

The capacitor ripple voltage $U_{\mathrm{C1}\sim}$ can also be determined analytically for SVM according to Dahono *et al.* [8]. The general solution is given as follows:

$$\begin{aligned} U_{\mathrm{C1}\sim} &= \sqrt{\frac{3}{\pi}\int_{\varphi_\mathrm{U}}^{\varphi_\mathrm{U}+\pi/3} U_{\mathrm{C1}\sim,\mathrm{Tp}}\,\mathrm{d}\varphi_\mathrm{U}} \\ U^2_{\mathrm{C1}\sim,\mathrm{Tp}} &= \frac{1}{T_\mathrm{P}}\int_0^{T_\mathrm{P}} u^2_{\mathrm{C1}\sim}\,\mathrm{d}t \\ u_{\mathrm{C1}\sim} &= \frac{1}{C_1}\int I_{\mathrm{E}(0)} - i_\mathrm{E}\,\mathrm{d}t. \end{aligned} \tag{5}$$

So, the knowledge of $i_{\mathrm{E}\sim}$ in every operation point is fundamental for dimensioning of the dc-link capacitor because current load as well as ripple voltage can be derived from it. $i_{\mathrm{E}\sim}$ in turn depends on the switching timings of the VSC.

In Sections II and III, a method to calculate $I_{\mathrm{E}\sim}$ for direct current controlled VSCs is described step by step.

1) In Section II, direct current control is introduced. Its different switching conditions in comparison to SVM are declared using an exemplary direct current control method called scalar hysteresis control (SHC).
2) a) In Section III-A, a calculation method for the total switch-ON times is given for SHC.
   b) In Section III-B, the relative switch-ON times are derived from the total switch-ON times proofing the calculation method presented is hardware independent. Therefore, the expression pulse group with duration t_PG is established.
   c) In Section III-C, $I_{\mathrm{E}\sim}$ is calculated for SHC, depending only on modulation level m_a and phase displacement angle φ.

II. Direct Current Control

The aim of any feedforward modulation method mentioned in Section I is the generation of pulse patterns for setting the target voltage u^*_n with $n = \mathrm{U,V,W}$ given by a higher leveled controller. In many applications, this higher leveled controller is used to tune the ac current. Due to this architecture, these methods are also referred as indirect current control. In contrast, for direct current control, the set current i^*, the measured current i, and the fundamental voltage at the VSC ac-side are taken into account for directly triggering a switching action in order to keep the current error i_ε inside a predefined tolerance area.

A. Hysteresis Control

A well-known direct current control method is the two-point hysteresis control [9, p. 205]. A tolerance area for the current error $i_{\varepsilon,n}$ in phase n consisting of an upper limit $I_{\epsilon,\mathrm{high}}$ and a lower limit $I_{\epsilon,\mathrm{low}}$ is defined [see (6)]. For the three-phase two-point hysteresis controller, the current error $i_{\varepsilon,n}$ is calculated separately in each phase of the VSC according to (6). If $i_{\varepsilon,n}$ exceeds the limits of the tolerance area, a switching action defined in (7) is triggered. Therefore, a switch position is selected, which reduces the current error in the corresponding phase. The output voltage u_n is defined in (8)

$$i_{\varepsilon,n} = i_n - i^*_n, \text{ for } n = \mathrm{U,V,W} \tag{6}$$

$$s_n = \begin{cases} +1, & \text{for } i_{\varepsilon,n} > I_{\epsilon,\mathrm{high}} \\ -1, & \text{for } i_{\varepsilon,n} < I_{\epsilon,\mathrm{low}} \end{cases} \tag{7}$$

$$u_n = s_n\frac{u_{\mathrm{C1}}}{2}. \tag{8}$$

For three-phase VSCs, in the most simple case, all three phase currents are regulated independently from each other. However, this leads to an overdetermination of the system in case of a nonconnected neutral point.

For control reasons, the current error for three-phase applications can be converted into the $\alpha\beta$-system by means of Clarke transformation to solve the mentioned issue of overdetermination [10].

B. Relation Between Voltage and Current Vector

Hereafter, the voltage as well as the current are described in the $\alpha\beta$-system for the three-phase direct current control methods. In Fig. 3, the relationship between voltage $\underline{u}'_{\alpha\beta}$, set current $\underline{i}^*_{\alpha\beta}$, and measured current $\underline{i}_{\alpha\beta}$ are shown. The vector $\underline{u}'_{\alpha\beta}$ represents the mean value of the VSC output voltage normalized to the intermediate circuit voltage u_{C1}. It is defined as follows

$$\begin{aligned} \underline{u}'_{\alpha\beta} &= |\underline{u}'_{\alpha\beta}|\,(\cos(\varphi_U) + \mathrm{j}\sin(\varphi_U)) \\ \text{with } |\underline{u}'_{\alpha\beta}| &= \frac{1}{2}m_\mathrm{a} = \frac{\hat{u}_{n(1)}}{u_{\mathrm{C1}}} \\ \text{and } \varphi_U &= \arg(\underline{u}'_{\alpha\beta}) = \int 2\pi f\,\mathrm{d}t \end{aligned} \tag{9}$$

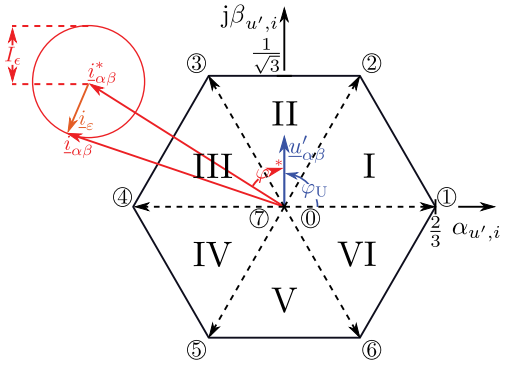

Fig. 3. Graphical illustration of the relationship between normalized voltage and current phasors in the $\alpha\beta$ plane. Tolerance circle for SHC.

The current $\underline{i}_\varepsilon$ describes the current error, defined in (10). In the example representation in Fig. 3, the tolerance area is drawn as a circle with radius I_ϵ, but may take different forms depending on the control method used. For example, in [11], the tolerance area forms a square using three active space vectors (SVs) and the zero voltage vectors (ZVVs) to control $\underline{i}_{\alpha\beta}$

$$\underline{i}_\varepsilon = \underline{i}_{\alpha\beta} - \underline{i}^*_{\alpha\beta}. \tag{10}$$

C. Scalar Hysteresis Control

The SHC method presented in [12] represents the development of a relative new direct current controller. Only those two SVs adjacent to $\underline{u}'_{\alpha\beta}$ as well as the ZVVs are used to control the current $\underline{i}_{\alpha\beta}$ under steady-state conditions.[1] The areas with identical SVs form triangles and define the limits of the voltage sectors I to VI.

The individual SVs are determined by evaluating the vector of the current error $\underline{i}_\varepsilon$ in the alpha–beta plane (see Fig. 3). For the maximum of $\underline{i}_\varepsilon$, a tolerance circle with radius I_ϵ is defined, as shown in Fig. 3. Once the limit of this area is exceeded, a switching operation is triggered and the SV is selected, which best moves $\underline{i}_\varepsilon$ back into the circle [13]. Equations (11) and (12) describe the vector choice for the exemplary case of voltage sector II with $\pi/3 \le \varphi_\mathrm{U} \le 2\pi/3$

$$k = \underset{k=0,2,3}{\arg\min}\, \Re\big((\underline{u}'_{\mathrm{SV}k} - \underline{u}'_{\alpha\beta})\bar{\underline{i}}_\varepsilon\big) \tag{11}$$

$$\begin{aligned} \underline{u}'_{\mathrm{SV0}} &= 0 \\ \underline{u}'_{\mathrm{SV2}} &= \frac{2}{3}\mathrm{e}^{\pi/3} \\ \underline{u}'_{\mathrm{SV3}} &= \frac{2}{3}\mathrm{e}^{2\pi/3}. \end{aligned} \tag{12}$$

In order to compare the dc ripple current for this direct current controller type with SVM, the distortion current load factor $K_{\mathrm{DC,SHC}}$ has to be determined as a function of modulation level and phase angle. For the calculation of the rms value of the distortion current $I_{\mathrm{E}\sim}$, at first, the general approach for SVM presented in [2] is chosen and adapted to the attributes of direct current control.

[1]For dynamic operations a second, greater tolerance area is defined.

III. Calculation of RMS Current Load on the DC-Link Capacitor

At first, an adapted generic form of the approach in [2] is given. The rms value as well as the dc component of i_E are calculated from the switching functions $s_{\mathrm{SVx},n}$ and $s_{\mathrm{SVy},n}$ as well as from the ac currents i_n. This calculation shown in (13) results the rms value of the dc-side distortion current over one pulse period $I_{\mathrm{E}\sim,\mathrm{Tp}}$ with duration T_P. The variables δ_x and δ_y represent the relative on times of the SV's x and y during one switching period.

Due to geometrical issues, the rms value of $I_{\mathrm{E}\sim,\mathrm{Tp}}$ over one arbitrary voltage sector results the global rms value of the dc-side distortion current $I_{\mathrm{E}\sim}$ shown in (14). Indices x and y correspond to the name of the active SV's used to emulate the voltage vector $\underline{u}_{\alpha\beta}$

$$\begin{aligned} I^2_{\mathrm{E}\sim,\mathrm{Tp}} = &\left(\delta_\mathrm{x}(\varphi_\mathrm{U}) \sum_{n=\mathrm{U,V,W}} \left(\frac{s_{\mathrm{SVx},n}-1}{2}\cdot i_n^2\right)\right. \\ &+ \delta_\mathrm{y}(\varphi_\mathrm{U}) \sum_{n=\mathrm{U,V,W}} \left(\frac{s_{\mathrm{SVy},n}-1}{2}\cdot i_\mathrm{n}^2\right) \\ &- \left(\delta_\mathrm{x}(\varphi_\mathrm{U}) \sum_{n=\mathrm{U,V,W}} \left(\frac{s_{\mathrm{SVx},n}-1}{2}\cdot i_\mathrm{n}\right)\right. \\ &\left.\left. + \delta_\mathrm{y}(\varphi_\mathrm{U}) \sum_{n=\mathrm{U,V,W}} \left(\frac{s_{\mathrm{SVy},n}-1}{2}\cdot i_\mathrm{n}\right)\right)^2 \right. \end{aligned} \tag{13}$$

$$I^2_{\mathrm{E}\sim} = \frac{3}{\pi}\int_{\Phi_\mathrm{U}}^{\Phi_\mathrm{U}+\pi/3} I^2_{\mathrm{E}\sim,\mathrm{Tp}}\mathrm{d}\varphi_\mathrm{U}. \tag{14}$$

Due to the mentioned switching vector selection for the SHC method taking into account only the two adjacent SVs as well as the ZVV, the parameters required for the calculation of (14) can be determined. For voltage sector II, the general switching functions $s_{\mathrm{SVx},n}$ and $s_{\mathrm{SVy},n}$ can be substituted

$$\begin{aligned} s_{\mathrm{SVx},n} &= s_{\mathrm{SV3},n} = [-1+1-1] \\ s_{\mathrm{SVy},n} &= s_{\mathrm{SV2},n} = [+1+1-1]\,. \end{aligned} \tag{15}$$

With (15), the general form given in (13) can be simplified

$$I^2_{\mathrm{E}\sim,\mathrm{Tp}} = \delta_3 i_\mathrm{V}^2 + \delta_2 i_\mathrm{W}^2 - (\delta_3 i_\mathrm{V} - \delta_2 i_\mathrm{W})^2. \tag{16}$$

The fundamentals of the phase currents i_n are defined according to (17) with amplitude $\hat{I}_N$ and phase displacement angle φ

$$\begin{aligned} i_{\mathrm{U}(1)} &= \hat{I}_N \cos(\varphi_\mathrm{U} - \varphi) \\ i_{\mathrm{V}(1)} &= \hat{I}_N \cos(\varphi_\mathrm{U} - \frac{2\pi}{3} - \varphi) \\ i_{\mathrm{W}(1)} &= \hat{I}_N \cos(\varphi_\mathrm{U} + \frac{2\pi}{3} - \varphi). \end{aligned} \tag{17}$$

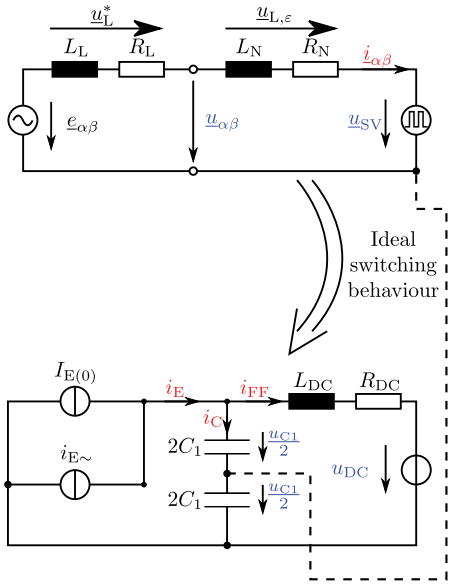

Fig. 4. Equivalent circuit diagram of the dc (bottom) and ac (top) side of a VSC, assuming ideal sinusoidal output voltage $u_{\alpha\beta}$ and reverse voltage $e_{\alpha\beta}$.

If the limit of the tolerance area is violated, a new SV is selected and applied until the ac-side distortion current $\underline{i}_\varepsilon$ again exceeds the tolerance area. Thus, the duration of the SV is dependent on the travel speed of $\underline{i}_\varepsilon$, i.e., the current slope $\mathrm{d}/\underline{i}_\varepsilon \mathrm{d}t$.

The upper part of the equivalent circuit diagram in Fig. 4 describes the VSC ac-side considering the load voltage $\underline{e}_{\alpha\beta}$, the load impedance L_L and R_L, as well as the filter impedance L_N and R_N. With $L_\mathrm{N} >> L_\mathrm{L}$, the distortion of the VSC output voltage $\underline{u}_\mathrm{SV}$ is set equal to the voltage $\underline{u}_{\mathrm{L}\varepsilon}$. So, it becomes clear that the current slope is related to $\underline{u}_{\mathrm{L}\varepsilon}$. The lower part describes the VSC dc-side considering the dc voltage source u_DC, the dc line impedance L_DC and R_DC, as well as the dc-link capacitor C_1. $I_{\mathrm{E}(0)}$ represents the dc component of the VSC dc-side input current, $i_{\mathrm{E}\sim}$ its distortion.

A. Determination of on Times

For the computation of the on time t_SV between one violation of the tolerance area at time t_0 and the subsequent at t_1, the course of $\underline{i}_\varepsilon$, as shown in Fig. 5, has to be determined. For the calculations presented, following are assumed.

1) The voltage $\underline{u}_{\mathrm{L}\varepsilon}$ is only applied to the inductance L_N, i.e., $R_\mathrm{N} = 0\,\Omega$.
2) The reverse voltage $\underline{e}_{\alpha\beta}$ during the on time of an SV is constant. Thus, the current slope for a switching state can be assumed to be constant.

In [14], a method for the computation of $\underline{i}_\varepsilon(t)$ depending on the selected SV is introduced and used for predictive current control. This method can subsequently be applied to determine t_SV.

Provided that t_SV is defined by

$$t_\mathrm{SV} = t_1 - t_0. \tag{18}$$

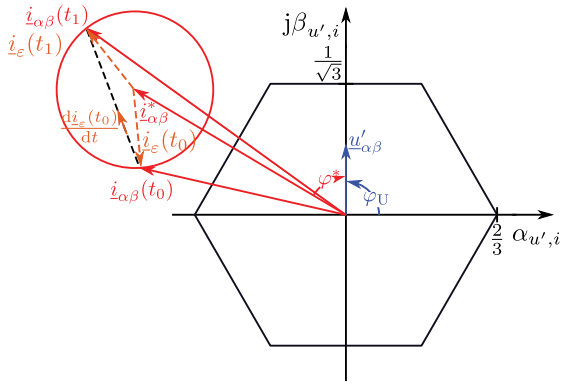

Fig. 5. Calculated course of the current error using the approach presented in [14].

The current error is already defined in (10). At time t_1, $\underline{i}_\varepsilon$ hits the limit of the tolerance area again. This represents the necessary criterion for triggering a new switching action.

The following relations (19)–(21) describe the course of the square of the current error magnitude i_ε^2. These relations as well as the auxiliary quantities a_1 and a_2 are taken from Holtz [14]. Here, the current error vector $\underline{i}_\varepsilon$ is divided into its real component $i_{\varepsilon,\alpha}$ and its imaginary component $i_{\varepsilon,\beta}$. The same is done with the current slope vector $\mathrm{d}\underline{i}_\varepsilon/\mathrm{d}t$

$$\begin{aligned} i_\varepsilon^2(t_1) = {} & i_\varepsilon^2(t_0) - a_1(t_0)\cdot(t_1 - t_0) \\ & + a_2(t_0)\cdot(t_1 - t_0)^2 \end{aligned} \tag{19}$$

$$\begin{aligned} a_1(t_0) = 2\Bigg(& i_{\varepsilon,\alpha}(t_0)\cdot\frac{\mathrm{d}i_{\varepsilon,\alpha}}{\mathrm{d}t}(t_0) \\ & + i_{\varepsilon,\beta}(t_0)\cdot\frac{\mathrm{d}i_{\varepsilon,\beta}}{\mathrm{d}t}(t_0)\Bigg) \end{aligned} \tag{20}$$

$$a_2(t_0) = \left(\frac{\mathrm{d}i_{\varepsilon,\alpha}}{\mathrm{d}t}(t_0)\right)^2 + \left(\frac{\mathrm{d}i_{\varepsilon,\beta}}{\mathrm{d}t}(t_0)\right)^2. \tag{21}$$

Depending on the selected SV, the chronological sequence of the current $\underline{i}_\varepsilon(t)$ can take any secant of the error circle with radius I_ϵ. To determine $\underline{i}_\varepsilon(t)$, the slope of $\underline{i}_\varepsilon(t)$ is calculated for $t = t_0$, as shown in (22). It indicates the absolute value and the direction of the chronological sequence of $\underline{i}_\varepsilon(t)$ for $t_0 \le t < t_1$

$$\frac{\mathrm{d}\underline{i}_\varepsilon}{\mathrm{d}t}(t_0) = \frac{\underline{u}_{\mathrm{L}\varepsilon}}{L_\mathrm{N}}. \tag{22}$$

After expiration of t_SV, the current error reaches the limit of the tolerance area and a new SV needs to be selected and applied. The resulting quadratic function (19) provides information about the number of possible solutions for t_1. A detailed calculation of t_SV is given in (23)–(25). The results coincide with [14].

General solution for $t_{1,1/2}$

$$t_{1,1/2} = \frac{2a_2(t_0)t_0 - a_1(t_0) \pm \sqrt{d}}{2a_2(t_0)}. \tag{23}$$

Provided that discriminant d is covered by

$$d = a_1^2(t_0) + 4a_2(t_0)I_\epsilon^2 - 4a_2(t_0)i_\varepsilon^2(t_0). \tag{24}$$

Special solution for $i_\varepsilon^2(t_0) = i_\varepsilon^2(t_1) = I_\epsilon^2$

$$t_{1,1/2} = \frac{2a_2(t_0)t_0 - a_1(t_0) \pm a_1(t_0)}{2a_2(t_0)}.$$

$$\begin{aligned} &\text{Solution 1: } t_1 = t_0 \Rightarrow t_{\mathrm{SV}} = 0 \\ &\text{Solution 2: } t_1 = t_0 - \frac{a_1}{a_2} \Rightarrow t_{\mathrm{SV}} = -\frac{a_1}{a_2} \\ &\text{with } t_{\mathrm{SV}} = t_1 - t_0. \end{aligned} \tag{25}$$

Using the determined on time and the calculated current slope, the current error for $t = t_1$, when $\underline{i}_\varepsilon$ again exceeds the limit of the tolerance area, can be calculated as

$$\begin{aligned} \underline{i}_\varepsilon(t_1) &= \underline{i}_\varepsilon(t_0) + \Delta\underline{i}_\varepsilon \\ \text{with } \Delta\underline{i}_\varepsilon &= \frac{\mathrm{d}\underline{i}_\varepsilon}{\mathrm{d}t}(t_0) \cdot t_{\mathrm{SV}} \\ \Delta\underline{i}_\varepsilon &= -\frac{2i_{\varepsilon,\alpha}(t_0)u_{\mathrm{L}\varepsilon,\alpha} + 2i_{\varepsilon,\beta}(t_0)u_{\mathrm{L}\varepsilon,\beta}}{u_{\mathrm{L}\varepsilon,\alpha}^2 + u_{\mathrm{L}\varepsilon,\beta}^2}\underline{u}_{\mathrm{L}\varepsilon}. \end{aligned} \tag{26}$$

Using (26), $\underline{i}_\varepsilon(t_1)$ is recalculated iteratively to reconstruct the course of $\underline{i}_\varepsilon(t)$ over any number of switching operations, as shown in (27). The starting point for the very first calculation $\underline{i}_\varepsilon(t_{m-1})$ at $m = 1$ is set to an arbitrary point at the limits of the tolerance area

$$\begin{aligned} \underline{i}_\varepsilon(t_m) &= \underline{i}_\varepsilon(t_{m-1}) + \frac{\mathrm{d}\underline{i}_\varepsilon}{\mathrm{d}t}(t_{m-1}) \cdot t_{\mathrm{SV}m} \\ &\forall\{m \in \mathbb{N}\}. \end{aligned} \tag{27}$$

The on times $t_{\mathrm{SV}m}$ can also be calculated iteratively according to

$$t_{\mathrm{SV}m} = -2L_{\mathrm{N}}\frac{i_{\varepsilon,\alpha}u_{\mathrm{L}\varepsilon,\alpha} + i_{\varepsilon,\beta}u_{\mathrm{L}\varepsilon,\beta}}{u_{\mathrm{L}\varepsilon,\alpha}^2 + u_{\mathrm{L}\varepsilon,\beta}^2}. \tag{28}$$

B. Pulse Groups

To determine the relative on times δ_{x} and δ_{y}, the period duration must be determined first. Indirect control procedures have a fixed pulse period duration T_{P}. It represents the time between two identical sequences of SVs, provided that the relative switch-ON time of the vectors is variable.

Direct current control methods do not have such a fixed pattern of identical sequences. Therefore, the term period duration cannot be used. However, in order to form the ratio of the on times of successive SVs $t_{\mathrm{SV}m}$, these are combined into a pulse group with duration t_{PG}. The number of vectors a pulse group contains is defined equal to the number of SVs available within the considered voltage sector and is denoted with M

$$t_{\mathrm{PG}}(\varphi_{\mathrm{U}}) = \sum_{m=1}^{M} t_{\mathrm{SV}m}. \tag{29}$$

For SHC, $M = 3$. This means, t_{PG} is calculated according to (29) summing up three successive calculations of $t_{\mathrm{SV}m}$ that create a pulse group.

For the considered example of voltage sector II from Fig. 3, the relative on times $\delta_2(\varphi_{\mathrm{U}})$ and $\delta_3(\varphi_{\mathrm{U}})$ needed for solving (16) are redefined as the ratios between total on times of equal active SVs in one pulse group and t_{PG}. In (30), the relative on time δ_2 is calculated exemplarily from the absolute on time t_2 defined in (31). δ_3 is determined analogously. In (31), the absolute on time t_2 for one pulse group is calculated iteratively using the switching criterion k of the SHC given in (11). k defines the decision criterion, which voltage SV is set to reduce the current error. It is recalculated step by step, i.e., for every step m that represents a violation of the current-tolerance area

$$\delta_2(\varphi_{\mathrm{U}}) = \frac{t_{\mathrm{SV2}}(\varphi_{\mathrm{U}})}{t_{\mathrm{PG}}(\varphi_{\mathrm{U}})} \tag{30}$$

$$t_{\mathrm{SV2}}(\varphi_{\mathrm{U}}) = \sum_{m=1}^{M} t_{\mathrm{SV}m} \quad \forall\{m|k(m) = 2\}. \tag{31}$$

Substituting $t_{\mathrm{SV}m}$ in (29) and (31) by means of (28) and inserting the expressions in (30), it can be seen that $\delta_2(\varphi_{\mathrm{U}})$ is independent of L_{N}. Therefore, the voltage $\underline{u}_{\mathrm{L}\varepsilon}$ can be substituted by the unitless variable $\underline{u}'_{\mathrm{L}\varepsilon}$, which can be determined according to (32). As $|\underline{i}_\varepsilon(t_m)| = |\underline{i}_\varepsilon(t_{m-1})|$, $\delta_2(\varphi_{\mathrm{U}})$ is also independent of I_ϵ as long as $I_\epsilon > 0$ A. This proves that the method presented is hardware independent

$$\underline{u}'_{\mathrm{L}\varepsilon} = \underline{u}'_{\alpha\beta}(\varphi_{\mathrm{U}}) - \underline{u}'_{\mathrm{SV}k}. \tag{32}$$

In (14), φ_{U} is assumed to be constant during the pulse period duration T_{P}. This assumption is also made for the pulse group duration t_{PG}. Now, the rms value of the distortion current over one pulse group $i_{\mathrm{E}\sim,t_{\mathrm{PG}}}$ can be calculated analogously to (16) by substituting T_{P} with t_{PG}, as shown in the following:

$$i_{\mathrm{E}\sim,}^2 t_{\mathrm{PG}}(\varphi_{\mathrm{U}}) = \delta_3 i_{\mathrm{V}}^2 + \delta_2 i_{\mathrm{W}}^2 - (\delta_3 i_{\mathrm{V}} - \delta_2 i_{\mathrm{W}})^2. \tag{33}$$

C. Calculation of the Global RMS Value

To calculate the global rms value of the distortion current $I_{\mathrm{E}\sim}$, the rms value of $i_{\mathrm{E}\sim,t_{\mathrm{PG}}}$ for one arbitrary sector is calculated. For the iterative algorithm presented, the integral in (14) cannot be solved analytically. Therefore, it is solved numerically, using the step size $\Delta\Phi_{\mathrm{U}}$ and the number of steps G according to the following:

$$\begin{aligned} I_{\mathrm{E}\sim}^2 &= \frac{1}{G}\sum_{g=0}^{G} i_{\mathrm{E}\sim,t_{\mathrm{PG}}}^2(\Phi_{\mathrm{U}} + g\Delta\Phi_{\mathrm{U}}) \\ \Delta\Phi_{\mathrm{U}} &= \frac{\pi}{3\,G} \quad \forall\{G \in \mathbb{N}\}. \end{aligned} \tag{34}$$

Assuming φ_{U} to be constant during the pulse group duration t_{PG}, φ_{U} is recalculated for every pulse group. The course of $\underline{i}_\varepsilon(t_m)$ is calculated iteratively for $0 \le g \le G$. Therefore, a case-differentiation for its starting point at $m = 1$ needs to be defined according to the following:

$$\begin{aligned} \underline{i}_\varepsilon(t_m, \varphi_{\mathrm{U}}) &= \underline{i}_\varepsilon(t_{m-1}, \varphi_{\mathrm{U}}) + \frac{\mathrm{d}\underline{i}_\varepsilon}{\mathrm{d}t}(t_{m-1}) \cdot t_{\mathrm{SV}m} \\ \underline{i}_\varepsilon(t_0, \varphi_{\mathrm{U}}) &= \begin{cases} I_\epsilon \mathrm{e}^{\mathrm{j}0} & \varphi_{\mathrm{U}} = \Phi_{\mathrm{U}} \\ \underline{i}_\varepsilon(t_M, \varphi_{\mathrm{U}} - \Delta\Phi_{\mathrm{U}}) & \varphi_{\mathrm{U}} > \Phi_{\mathrm{U}} \end{cases}. \end{aligned} \tag{35}$$

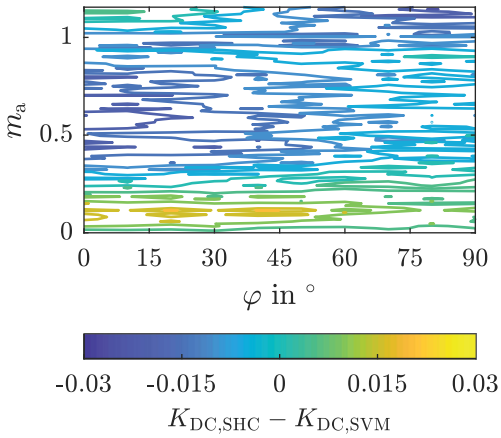

Fig. 6. Distortion current load factor when using the SHC method in comparison to the SVM used as a reference.

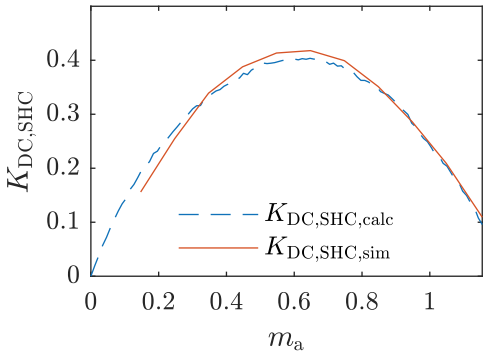

Fig. 7. Comparison of simulation and calculated results for the distortion current load factor using SHC.

The precision of this solution depends on the choice of the step size $\Delta\Phi_U$. For the results presented, the number of steps is set to $G = 100$ resulting in $\Delta\Phi_U = \pi/300$. Using the given relations, the distortion current load factor $K_{DC,SHC}$ can be calculated. A comparison of $K_{DC,SHC}$ and $K_{DC,SVM}$ is shown in Fig. 6.

IV. Verification of the Results Using Digital Simulation

To verify the calculated results from Section III, a digital simulation model was created. Fig. 7 shows the comparison results for $0 < m_a \leq 2/\sqrt{3}$ and $\varphi = 0°$.

1) Calculation method presented: Curve $K_{DC,SHC,calc}$.
2) Simulation model accounting current commutation of the VSC: Curve $K_{DC,SHC,sim}$.

The comparison shows good correlation between simulation and calculation. For $m_a \to 0$, the shape of the curve $K_{DC,SHC,calc}$ deviates from $K_{DC,SHC,sim}$. This deviation can be addressed to the current commutation.

Calculation does not take into account the current commutation process and the delay time t_D, it takes switching from one SV to another. This time delays the switch-ON timing of the SV in comparison to the switch-ON command from the SHC. Until the time t_D has elapsed, the SHC sends no further switching commands to the VSC. This ensures that the minimum on time of an SV is set to t_D. As this issue also arises when comparing calculated results with experimental results, a more detailed analysis is given in Section V-B.

TABLE I
Parameters of Hardware Setup for Test Bench, With $n = U, V, W$

Current setpoint	$\hat{I}_N^*(50\,\text{Hz}) = 20\,\text{A}$
Grid filter	$L_n(100\,\text{Hz}) = 1{,}2\,\text{mH}$ $R_n = 1\,\text{m}\Omega$
Copper Rails	$Z_{R,n}(100\,\text{Hz}) =$ $0{,}1\,\text{m}\Omega + \text{j}\omega 140\,\text{nH}$
Snubber capacitors	$C_{S,n}(100\,\text{Hz}) = 470\,\text{nF}$
Connection plate	$Z_P(100\,\text{Hz}) =$ $0{,}24\,\text{m}\Omega + \text{j}\omega 250\,\text{nH}$
DC-link capacitor	$C_1(100\,\text{Hz}) = 4{,}6\,\text{mF}$
DC Coupling	$L_{DC1}(100\,\text{Hz}) = 34{,}5\,\mu\text{H}$
DC-link voltage	$U_{DC(0)} = 300\,\text{V}$

V. Experimental Results

To verify the calculated and the simulative results, the VSC dc-side current i_E is measured on an experimental setup. Fig. 8 shows a schematic of the test bench. The device under test (DUT) is a three-phase insulated gate bipolar transistor (IGBT) power module. To absorb the distortion current, the electrolytic capacitor C_1 and three snubber capacitors $C_{S,n}$ are used. The ac-side output voltage is filtered by the inductances L_n. To generate a sinusoidal load voltage, a power grid simulator is used. For providing the constant dc voltage, a dc source/sink is applied to the test bench. The amplitude of the three phase ac-side load voltages of the power grid simulator $\hat{e}_N$ is varied to adjust different modulation levels. As the current setpoint is kept constant, the power handled by the VSC varies from 630 VA at $m_a = 0.1$ to 7000 VA at $m_a = 1.15$. Parameters of the hardware setup are given in Table I.

In order to achieve a low inductance connection between the dc-link capacitor and the DUT, the dc bus bar is bolted directly on the half bridge modules, including three snubber foil capacitors. The dc current i_E describes the sum of three half bridge dc currents $i_{DC,n}$. To measure i_E correctly, the current sensors are placed in between the DUT and the snubber capacitors, as shown in Fig. 8. This is done because the currents $i_{S,n}$ of the snubber capacitors $C_{S,n}$ significantly influence the measurements. For this purpose, U-formed copper rails with impedance $Z_{R,n}$ are inserted between the dc connection point of the three half bridges and the snubber capacitors, as shown in Fig. 9. The impedance of the dc bus bar, which connects $C_{S,n}$ to C_1, is called Z_P. The impedances of the passive components given in Table I were measured via a programmable *LCR* bridge. According to datasheet, the *LCR* bridge has a following measuring range:

1) 0,01 mΩ to 100 MΩ for resistive load;
2) 0,01 pF to 100 mF for capacitive load;
3) 10 nH to 100 kH for inductive load.

The frequency ranges from 20 Hz up to 100 kHz. Measurement is done via four-wire measurement. Results presented were obtained at a measurement signal frequency of 100 Hz.

To measure the current i_E, three clamp-on probes are applied to the test bench. According to datasheet, the bandwidth of these probes ranges from dc to 10 MHz. The amplitude accuracy is stated $\pm 1\,\%$ of reading. The rise time is stated to be 35 ns

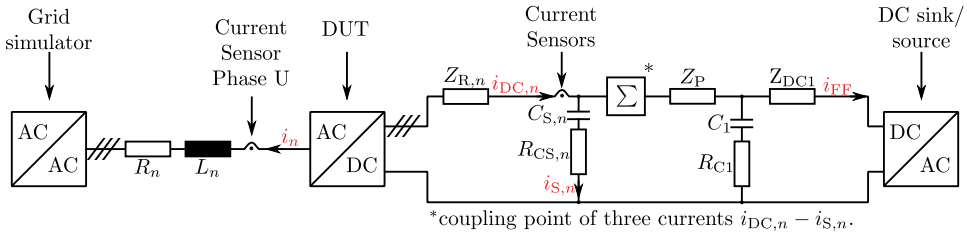

Fig. 8. Schematic of the test bench used for verification of the calculated results.

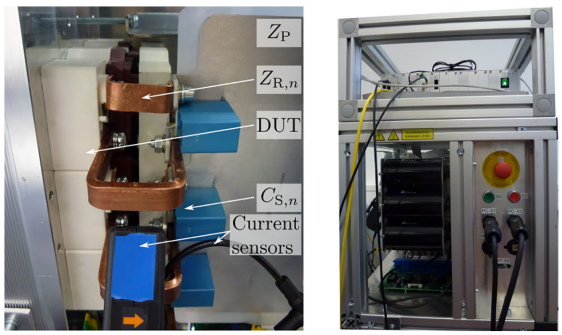

Fig. 9. Coupling of the VSC and its dc-link for measurement of i_E (left-hand side picture). Experimental setup of VSC used as DUT (right-hand side picture).

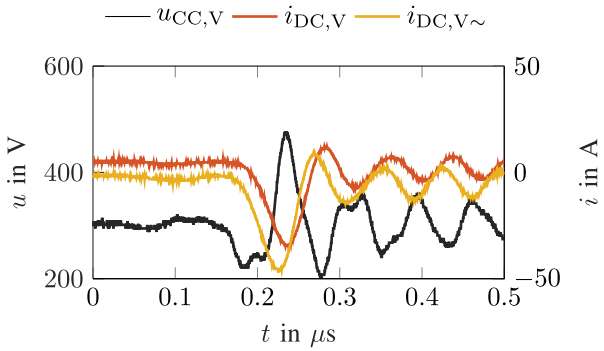

Fig. 10. Comparative current measurement between Rogowski coil and clamp-on probe, measured in phase V. DC-side current and voltage during one switching action of the DUT.

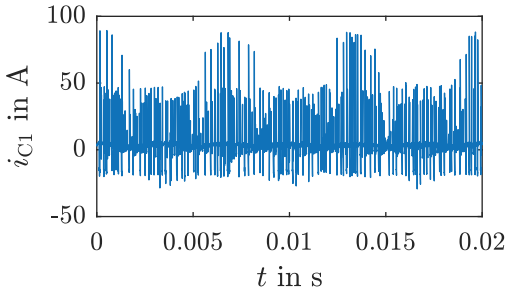

Fig. 11. Measured capacitor current over one fundamental period of 20 ms.

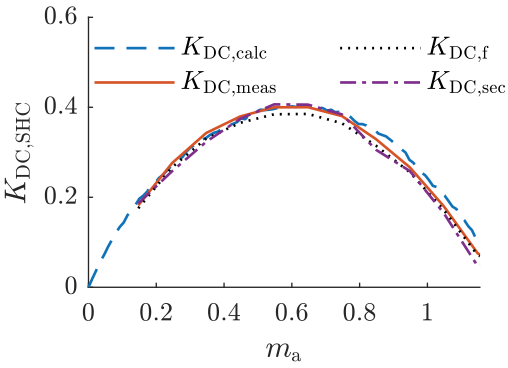

Fig. 12. Comparison of measured test bench results with calculation results.

or less. The current i_E during the switching action presented in Fig. 10 means a phase accuracy of only 65 %. i_E contains high-frequency components due to the VSC switching transients. Correct measurement data acquisition of the clamp-on probes for those high-frequency distortions is validated. For this purpose, a comparative measurement is performed using a Rogowski coil with an HF bandwidth of 30 MHz. The stated maximum current rise that can be detected is 20 ka/μs. The results of the comparison measurement between Rogowski coil ($i_{DC,V\sim}$) and clamp-on probe ($i_{DC,V}$) are shown in Fig. 10 presenting dc-side currents for phase V during one switching action of the DUT. It can be seen that the transient effect is similar for both probes proving the bandwidth of the clamp-on probe is sufficient. Fig. 10 also shows the voltage overshoot $u_{CC,V}$ caused by the impedance $Z_{R,V}$, which has to be kept as low as possible to avoid damage to the IGBT modules of the DUT. Compared to the collector emitter saturation voltage of 1200 V stated in the datasheet of the DUT, the measured voltage overshoot is reasonable.

In Fig. 11, also the measurement results of the capacitor current i_C over one fundamental period of 20 ms is shown. As i_C cannot be measured directly, it is calculated from the ac parts $i_{DC,n\sim}$ of the currents $i_{DC,n}$ with $n = U, V, W$, as stated in (36). The operating point for the measurement is $\varphi = 0°$ and $m_a = 1$

$$i_C = i_{DC,U\sim} + i_{DC,V\sim} + i_{DC,W\sim}. \tag{36}$$

Fig. 12 shows the following comparison of results:

1) results from calculation method presented: $K_{DC,analyt}$;
2) unfiltered measurement: $K_{DC,meas}$;
3) filtered measurement: $K_{DC,f}$;
4) filtered measurement neglecting the switching actions at the sector transition: $K_{DC,sec}$.

For correct comparison between measurement and simulation or calculated results, respectively, some effects have to be considered. These are explained from Sections V-A to V-E.

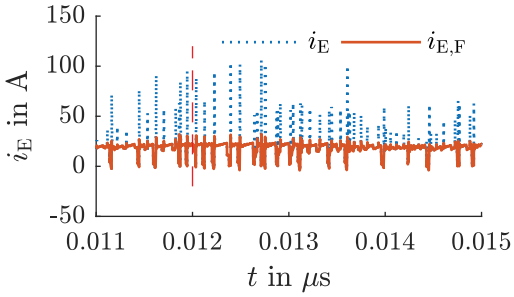

Fig. 13. Comparison of the unfiltered current i_E with the filtered current $i_\mathrm{E,F}$.

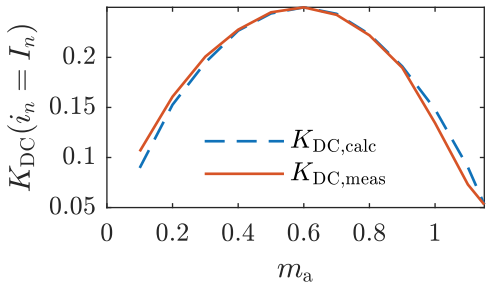

Fig. 14. Comparative result of $K_\mathrm{DC}(i_n = I_\mathrm{N})$ for calculation ($K_\mathrm{DC,calc}$) and measurement ($K_\mathrm{DC,meas}$).

A. Transient Effects

To minimize the distortion in the measurement caused by the necessary hardware intervention as described, the course of $K_\mathrm{DC,SHC}$ was additionally determined with a filtered current signal of i_E. In Fig. 13, the unfiltered current at operating point $m_\mathrm{a} = 1$ is shown. Fig. 13 also shows the filtered current, which is used for computing $K_\mathrm{DC,f}$, as shown in Fig. 12. For filtering purpose, a first-order low pass with a cutoff frequency of 5 MHz is used. As expected, the filtered value of $K_\mathrm{DC,SHC}$ is lower than the calculated one using the unfiltered current i_E over the entire course. Especially in the middle of the modulation range, $K_\mathrm{DC,SHC,f}$ is also lower than the results determined by calculation or simulation, respectively. Considering these results, subsequent filtering does not give an advantage compared to accepting the additional distortion caused by the hardware intervention.

B. Current Commutation

This issue is already encountered in Section IV by comparing calculated results with those from nonideal simulation. The deviation arising from this can be calculated on the basis of different relative switch-ON times of the active SVs δ_a or the ZVV δ_0. In addition, the current error changes during the commutation process due to the commutation current. This results in a shift of the switch-ON times of the SV required by the controller. The correlations between modulation level and relative switch-ON time can be depicted for $\varphi = 0°$ as follows:

$$\lim_{m_\mathrm{a}\to 0} \delta_0 = 1 \tag{37}$$

$$\lim_{m_\mathrm{a}\to 2/\sqrt{3}} \delta_0 = 0. \tag{38}$$

If the phase currents i_n are set equal to its rms value I_n and I_n set equal for all three phases ($I_n = I_\mathrm{N}$), the relative on times of the active SVs can be summed up to one common relative on time for all active SVs δ_a. Accepting these simplification, the normalized distortion current load factor of the dc-link can be recalculated to

$$K_\mathrm{DC}(i_n = I_\mathrm{N}) = \frac{\delta_\mathrm{a} I_\mathrm{N}^2 - (\delta_\mathrm{a} I_\mathrm{N})^2}{I_\mathrm{N}^2}$$

$$\text{with } 1 - \delta_\mathrm{a} = \delta_0$$

$$K_\mathrm{DC}(i_n = I_\mathrm{N}) = \delta_0 \cdot \delta_\mathrm{a}. \tag{39}$$

Due to the definition of $K_\mathrm{DC}(i_n = I_\mathrm{N})$ and the relations between δ_0 and m_a, it becomes clear that deviations of the relative switch-ON times are particularly noticeable at the limits of the modulation range and have a significant impact on the result.

Fig. 14 shows the results of $K_\mathrm{DC}(i_n = I_\mathrm{N})$ for calculation and measurement. The results prove that the visible deviations for $m_\mathrm{a} > 0.8$ and $m_\mathrm{a} < 0.3$ can be explained by the neglection of the current commutation process time t_D for the calculation method presented.

C. Stationary Current Error

SHC remains a stationary error in its ac currents i_n. The phenomenon of remaining error is a known issue for hysteresis control, discussed for dc values in [15, Ch. 3, p. 182]. The calculation method presented considers this issue. But, mainly caused by t_D, the stationary current error of the test bench results differs from calculated results. Based on the observed deviations, the rms value of the ac-side current I_N is measured by a current probe instead of being calculated from the set current. I_N is needed to compute the measured curve of $K_\mathrm{DC,SHC}$.

D. VSC and Filter Voltage Drop

The calculation method presented does not take into account current-dependent voltage drop on the ac-side filter as well as the voltage drop u_CE of the DUTs IGBT modules: To consider the voltage drops of the real system, the modulation level $m_\mathrm{a,meas}$ is calculated as stated in (40). The value for u_CE is taken from the corresponding datasheet of the power module and is set to $u_\mathrm{CE} = 1,7\,\mathrm{V}$ for evaluation

$$m_\mathrm{a,meas} = \frac{2\hat{e}_\mathrm{N}}{u_\mathrm{DC} - 2u_\mathrm{CE} - 2R_\mathrm{N} I_\mathrm{N}}. \tag{40}$$

E. Voltage Sector Selection

In [12, Ch. 5, p. 100], it is stated that the SHC method depends on reliable information regarding the position of $\underline{u}'_{\alpha\beta}$ in order to ensure correct sector selection. In particular, the change of the sector serving as the basis for the SV selection presents a challenge. Because of this, the sensorless acquisition of $\underline{u}'_{\alpha\beta}$ for the purpose as pilot control of the SHC method was described in [16, Ch. 4, p. 63]. Both in the implementation on the test bench and in the simulation model, the method developed in the framework of Hofmann [16] is used for pilot control of the SHC

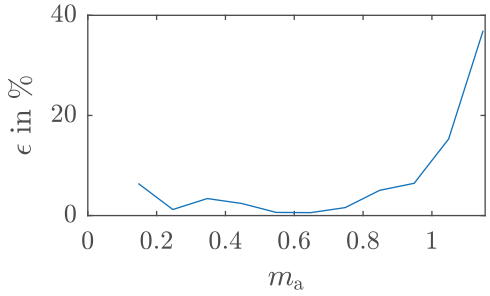

Fig. 15. Relative error of the calculated results in comparison to experimental results.

method. To hide the influence of sector transitions, the filtered measurement result is computed by considering sections of 54° in the middle of the 60° sectors. This result is named $K_{\mathrm{DC,sec}}$ in Fig. 12. The result shows only a slight difference in distortion current load factor, which confirms the results of precise sector transitions described in [16].

VI. Accuracy in Comparison to State-of-the-Art Methods

In [2], for $\varphi = 0^\circ$ and $0 \leq m_\mathrm{a} \leq 1,15$, the average error ε between calculated and measured results is stated as follows.

1) $\epsilon = 5\,\%$ for low ac ripple current ($\kappa = 0,1$).
2) $\epsilon = 9\,\%$ for high ac ripple current ($\kappa = 0,8$).

The relative amplitude of the ac-side ripple current for pulsewidth modulated VSCs is calculated in [2] as follows:

$$\kappa = \frac{1}{\hat{I}_\mathrm{N}} \cdot \frac{U_\mathrm{DC} T_\mathrm{P}}{8 L_\mathrm{N}}. \tag{41}$$

In order to keep the absolute amplitude of the ac-side ripple current constant using the direct current controller SHC, the mean switching frequency is not constant over the modulation level. Instead, the switch-ON time t_SV is adjusted

$$\frac{U_\mathrm{DC} t_\mathrm{SV}}{8 L_\mathrm{N}} = 8 I_\epsilon. \tag{42}$$

The maximum error current is set to $I_\epsilon = 1\,\mathrm{A}$. Applied to the relative ripple current as stated in [2], κ can be calculated as follows:

$$\kappa = \frac{I_\epsilon}{\hat{I}_\mathrm{N}}. \tag{43}$$

The relative error between measurement and calculation is shown in Fig. 15 for $\varphi = 0^\circ$ and $0 \leq m_\mathrm{a} \leq 1,15$. It shows an accuracy of better than 8% for $m_\mathrm{a} < 0,9$. The lower relative accuracy for higher modulation levels can be traced back to the neglection of the current commutation process, as stated in Section V. For the experimental setup, $I_\mathrm{N} = 20\,\mathrm{A}$ resulting $\kappa = 0,4$. The mean average error $\epsilon = 7,3\,\%$. From simulation results in [2], it can be seen that the error goes nearly linear with κ. Assuming this, the error of Kolar and Round [2] would be 6.7 % at $\kappa = 0.4$, which is quite close to the error of the proposed method. This shows with regard to accuracy that the results for the method proposed for direct current controlled VSCs are comparable to state-of-the-art methods for pulsewidth modulated VSCs.

VII. Conclusion and Future Work

A calculation scheme for determining the dc-link capacitor rms current load for direct current control methods is presented. As an example, the approach is applied to the SHC, a direct current control algorithm operating in the $\alpha\beta$ plane.

As a reference, the dc-link capacitor rms current load for SVM $K_{\mathrm{DC,SVM}}$ is calculated using state-of-the-art methods. The comparison between results for SVM and SHC shows a striking similarity over the whole operation area, as shown in Fig. 6. This can be justified by the identical sector-dependent SV selection and indicates that, even with no fixed pulse period, the behavior of SHC is very similar to the behavior of SVM. As SVM is considered to exactly adjust the set voltage, slight deviations can be traced back to the stationary current error of SHC.

The calculated results for $K_{\mathrm{DC,SHC}}$ are verified by digital simulation and test bench measurements and show good correlation. The post treatment of the measurement results are explained. These are as follows:

1) filtering of transient effects caused by the necessary hardware intervention for measurement;
2) current commutation process not considered in the calculation method presented;
3) stationary current error of direct current controllers;
4) IGBT/diode voltage drop causing need for recalculation of m_a;
5) Voltage sector selection using pilot control for SHC.

With the pilot control described in Section V-E, the influence of voltage sector selection is negligible. By comparing Figs. 14 and 12, it becomes clear that the remaining deviation between calculated and measured results can be addressed to the current commutation process. But as the behavior of semiconductors is dependent on many parameters, accounting this process in the generalized, hardware independent calculation method presented does not seem expedient.

Although, it is applied to a specific algorithm, the method presented is a general approach and can be applied to any direct current controller. In contrast to pure numerical simulation, the proposed method provides results in closed-form expressions that are new and useful for the design/component development process.

The derivation of the calculation method presented analytically proves that the global rms value of the dc-side input current I_E for the exemplary utilized SHC is independent of the following:

1) the radius of the tolerance area I_ϵ;
2) the ac-side filter components.

The calculation method presented does not determine the instantaneous dc current waveform, such as in numerical simulation. Determination of the instantaneous dc current waveform implicates calculation of the absolute on times. This causes high computation effort due to the very high frequency components and nonlinearities of the instantaneous dc current waveform

without any benefit for the rms value calculation. Instead, the calculation method presented calculates the normalized distortion current load factor K_{DC} by only determining the relative on times. This causes very less computation effort and, therefore, is a great advantage of the calculation method presented compared to numerical simulation (approximately 570 times faster).

Even though, the article presented focuses on calculation of the dc-link capacitor current load, preliminary work is done for calculating the capacitor ripple voltage of direct current controlled VSCs. This refers to the determination of total on times in Section III-A needed for calculating the capacitor ripple voltage according to the generic approach, as stated in (5). This issue will be focused in future work.

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