Characterization of 3.3-kV Reverse-Blocking SiC Modules for Use in Current-Source Zero-Voltage-Switching Converters

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***Abstract*—Silicon carbide (SiC) MOSFETs with ratings of 3.3 to 15 kV represent a dramatic improvement over available silicon devices, enabling the realization of medium-voltage converters in demanding applications such as solid-state transformers. Typical voltage-source converter configurations realize significant reduction in switching loss with SiC devices, but high *dv/dt* of 30–50 kV/μs generates high levels of electromagnetic interference (EMI) and displacement currents. Current-source based zero-voltage switching (CS-ZVS) converters such as the soft-switching solid-state transformer (S4T), dramatically reduce switching loss using ZVS, thus realizing both controlled *dv/dt* and low EMI. CS-ZVS converters require reverse blocking (RB) modules that are realized using series connection of a diode and a MOSFET. However, no data are available from manufacturers or from literature on RB module characterization under ZVS conditions. This article presents detailed characterization results and model extraction for a 3.3 kV 45 A and a 1.7 kV 10 A SiC RB module, under both hard switching and ZVS modes. A novel double-pulse testbed is designed and built for this characterization of RB devices under both hard switching and ZVS conditions. Significantly, it is shown that when the RB modules are used in CS-ZVS converters, the dynamic voltage sharing between the RB modules in a phase leg and within the RB module (between the diode and the switch) results in a unique voltage stress. Modulation strategies to address this unique voltage stress are proposed and verified through experiment results, using a S4T prototype rated at 1.5 kV, 10 kVA.**

***Index Terms*—Current-source (CS) inverter, device characterization, double-pulse test (DPT), reverse-blocking (RB) modules, soft-switching.**

Manuscript received July 27, 2019; revised December 30, 2019 and March 15, 2020; accepted May 19, 2020. Date of publication June 3, 2020; date of current version September 4, 2020. This work was supported in part by Power America, in part by ARPA-E under DE-AR0000899, and in part by Center for Distributed Energy at Georgia Tech. This article was presented in part at the IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Atlanta, GA, USA, Oct.–Nov. 2018. Recommended for publication by Associate Editor J. Wang. *(Corresponding author: Xiangyu Han.)*

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Digital Object Identifier 10.1109/TPEL.2020.2999878

I. Introduction

MEDIUM-VOLTAGE (MV) and high-voltage (HV) power converters are important assets for control and operation of power grid. Their applications are ranged from HVdc converter stations to flexible ac transmission system controllers, grid interfaces for energy storage devices and renewable energy resources (such as onshore/offshore wind farms and string solar inverters), solid-state distribution transformers, fast battery charging stations, and traction systems. Realization of those converters based on low-voltage Si devices necessitates series-connection of semiconductor devices, which in turn increases the complexity in control and deteriorates the efficiency [1], [2]. Alternatively, the use of HV Si IGBTs (3.3 kV or higher) limits the switching frequency to under 500 Hz, thereby dramatically impacting the size and performance of the converter [3]. Silicon carbide (SiC) devices, compared to their Si counterparts, offer superior electrical and thermal characteristics in terms of efficiency, power density, switching frequency, and operating temperature [4], [5]. SiC devices rated at $>$3.3 kV and 50–200 A can simplify the design of MV and HV converters [6]–[11]. However, simple drop-in replacement of Si devices with SiC ones can result in issues such as electromagnetic interference (EMI) caused by large dv/dt (30–50 kV/μs) [12].

A recently proposed current-source based zero-voltage switching (CS-ZVS) converter with modularity and scalability features, i.e., soft-switching-solid-state transformer (S4T) has been shown to offer significant benefits, including absence of switching losses, reduced, and controlled dv/dt, and benign fault modes [13], for MV applications. CS-ZVS converters, such as S4T, require reverse-blocking (RB) modules that can be realized using series connection of a diode and a MOSFET. The RB module here refers to a standard switch and diode, connected in series either at die level or at discrete package level and not a fundamentally RB device [13]. However, very little is known about the detailed behavior of such RB modules, especially when used in CS converters with ZVS. In [14] and [15], the behavior of RB SiC modules under hard-switching conditions is discussed. However, clear understanding of the characteristics and performance of RB SiC modules under soft-switching conditions have not been yet reported in the literature. The use of 3.3-kV SiC RB modules is contingent upon a deep

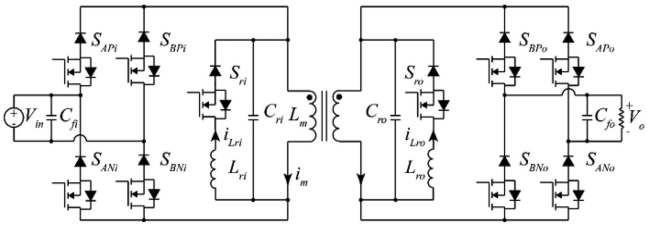

Fig. 1. Circuit diagram of the S4T for dc–dc applications.

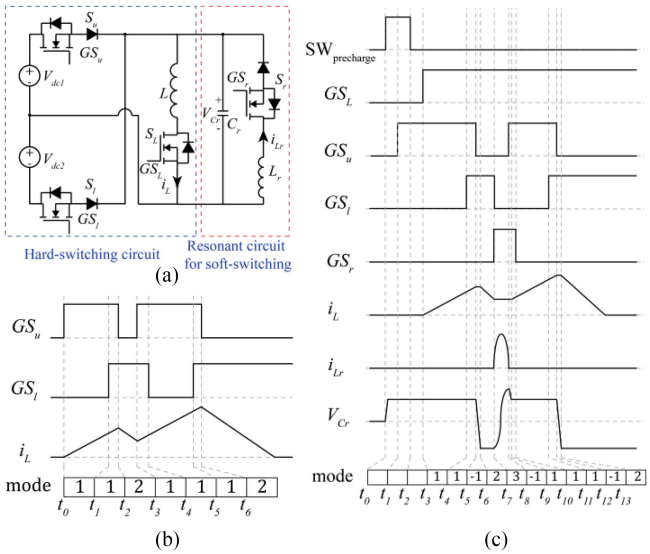

Fig. 2. (a) Schematic of the proposed DPT circuit. (b) Conceptual waveforms under hard-switching. (c) Conceptual waveforms under soft-switching.

understanding of the switching transients of 3.3 kV RB SiC MOSFETs/diodes under soft-switching conditions and a comparison of their switching performance under hard-switching and soft-switching conditions, including switching losses, stresses, EMI, etc. In addition, to exploit the full benefits of 3.3 kV RB modules in CS-ZVS converters, such as the S4T, their practical integration issues in terms of gating sequences and switching stresses need to be explored and resolved prior to using them.

This article, first presents the design of a novel double-pulse test (DPT) circuit, which can be used to characterize the SiC RB modules under both hard-switching and soft-switching conditions. A 3.3-kV 45-A SiC module and 1.7-kV 10-A SiC module are both characterized in this article. The 3.3-kV module is configured in RB mode at die level, while the 1.7-kV module is configured in RB mode using discrete packages. The experimental waveforms, analysis of the switching transients, and switching performance comparison between hard switching and soft switching in terms of switching losses, *dv/dt*, and stresses are presented. A unique phenomenon with RB modules, i.e., device dynamic voltage sharing between the RB modules in a phase leg and within the RB module (between the diode and the switch) resulting in additional voltage stress, is discussed in detail. Switching schemes to limit this unique voltage stress when the RB modules are used in such converters are presented and verified, using the S4T as an example, at 1.5 kV and 10 kVA.

II. Soft-Switching DPT

The S4T is a universal converter that can be configured to convert a single- or three-phase ac or a dc input to a single- or three-phase ac or dc output, featuring bidirectional power transfer, buck-boost capabilities, high-frequency isolation, low EMI through low dv/dt, and soft switching over the full operating load range. The S4T is a "minimal topology" comprised of a single-stage solid-state transformer with two current source inverter bridges on both sides of a high frequency (HF) transformer with relatively low magnetizing inductance L_m, and two auxiliary resonant circuits to achieve ZVS, as shown in Fig. 1 [13]. Because of the current source feature of the S4T, RB-modules are required to realize both the main switches and the resonant switches. As shown in Fig. 1, each RB module is comprised of a series-connected pair of a MOSFET and a diode. Hereinafter, the MOSFET of *i*th RB-module (S_i) is called M_i and the diode is called D_i.

To characterize the RB module performance in the S4T circuit under soft-switching conditions, a novel DPT circuit is proposed, whose schematic is shown in Fig. 2(a). Compared to Fig. 1, the DPT circuit is a simplified circuit of the S4T. The two RB modules ($S_{\rm APi}$, $S_{\rm BNi}$) used for charging L_m are reduced to one RB module (S_u) while the other switch pair ($S_{\rm APo}$, $S_{\rm BNo}$) used for discharging L_m are reduced to one (S_l). The two resonant circuits comprised of resonant capacitors (C_{ri}, C_{ro}), resonant inductors ($L_{\rm ri}$, $L_{\rm ro}$), and resonant switches ($S_{\rm ri}$, $S_{\rm ro}$) on both sides of the HF transformer are reduced to one resonant circuit (C_r, L_r, S_r). The HF transformer with a relatively low magnetizing inductance (L_m) is simplified to an inductor (L). The current through L_m (I_m) is replaced by the inductor current (I_L). Compared to the conventional DPT circuits, the proposed circuit can be easily configured to characterize the RB-switches under either soft-switching or hard-switching conditions by adding or removing the resonant circuit, as shown in Fig. 2.

The operation of the proposed DPT is similar to that of a flyback converter, as is the case with the S4T. As shown in Fig. 2(b), under hard-switching condition, when the gate of S_u (GS_u) is high, the DPT operates in charging mode (mode 1) where $V_{\rm dc1}$ charges L and inductor current (i_L) flows through S_u. When the gate of S_l (GS_l) is high and GS_u is low, the DPT operates in discharging mode (mode 2) where $V_{\rm dc2}$ discharges L and i_L flows through S_l. Fig. 2(c) illustrates the operation of the circuit under soft-switching condition. Under soft-switching conditions, the voltage of C_r ($V_{\rm Cr}$) in the DPT needs to be initialized. Before S_u is turned ON, C_r is precharged to $V_{\rm dc1}$ using an initialization circuit comprised of $SW_{\rm precharge}$, $R_{\rm precharging}$, and S_L as shown in Fig. 4 to ensure soft-switching for the first pulse. For subsequent pulses, soft switching can be achieved using the resonant circuit. At t_0, the mechanical relay $\rm SW_{precharge}$ turns ON and C_r is charged to $V_{\rm dc1}$ through $R_{\rm precharge}$. Then, S_u is turned ON with zero voltage at t_1 with no inrush current flowing through S_u. Subsequent to the completion of precharging, $\rm SW_{precharge}$ is turned OFF at t_2. During these subintervals and switching transitions, i_L needs to be maintained at zero before initialization is done. Therefore, switch S_L is

used, which is turned ON after $SW_{precharge}$ is turned OFF. The initialization completes before t_3. At t_3, when S_L is turned ON, the DPT operates in mode 1. Once mode 1 ends at t_5 when S_u turns OFF, the DPT enters ZVS mode (mode –1) to ensure ZVS turn-OFF of S_u and ZVS turn-ON of S_l. In this mode, since C_r is effectively in parallel with the parasitic capacitors of S_u and S_l, the voltage of S_u (V_{Su}) is charged slowly by i_L and V_{Su} increases negligibly while its current drops to zero. Meanwhile, although GS_l is high at t_5, S_l cannot conduct i_L until V_{Cr} is discharged by i_L to $-V_{dc2}$ at t_6 when the voltage of S_l (V_{Sl}) becomes zero and i_L starts flowing through S_l. Therefore, both S_l and S_u are switched ON/OFF with ZVS at this moment. The DPT operates in mode 2 from t_6 to t_7 and in mode –1 after t_7. S_l is turned OFF in the same manner as S_u. The second pulse starts at t_8. At the beginning of the second pulse, the DPT enters mode 3 in which the negative V_{Cr} is flipped to a positive V_{Cr} higher than V_{dc1} by the resonant circuit. GS_u is turned high once mode 3 ends. Mode 3 is followed by mode –1 in which V_{Cr} is discharged by i_L to V_{dc1} and ZVS turn-ON of S_u is achieved. The rest of the second pulse is the same as the aforementioned discussion. At the end of the second pulse, S_u is turned OFF and S_l is turned ON. Therefore, $-V_{dc2}$ is applied to L and inductor current is discharged to 0.

III. Experimental Setup and Results

A. Hardware Implementation

Fig. 4 shows the circuit diagram of the experimental setup. S_u is the DUT. Voltage and current probes are placed to measure V_{RB} and I_{RB} of the DUT, as shown in Fig. 4. Fig. 3(a) shows a custom 3.3 kV RB SiC module developed by Wolfspeed. The module consists of five identical RB switches with each switch consisting of one 3.3 kV SiC MOSFET and one 3.3 kV SiC diode connected in series. Fig. 3(b) shows a custom 1.7 kV RB SiC module using discrete devices in which a 1.7 kV discrete RB-module is realized by using a discrete 1.7 kV SiC MOSFET in series with a discrete 1.7 kV SiC Schottky diode. The 1.7 kV and 3.3 kV modules are almost the same in terms of their layouts except that the 3.3 kV module has a Kelvin source while 1.7 kV one does not. One of the reasons for using a 1.7 kV module is to have access to the diode and switch interconnection, which is not available in the 3.3 kV module. The diode-switch interconnection point is needed to evaluate the dynamic voltage sharing between the diode and the switch. Fig. 3(c) shows the internal connection of the 1.7 and 3.3 kV modules. Three of the five switches are used in the DPT. Fig. 3(d) shows the photo of the experimental setup. By connecting/disconnecting the resonant circuit, the setup can be easily configured for hard-switching or soft-switching characterization. To suppress the current overshoot under hard switching that also exist in the traditional DPT [16] and to protect the device, a ferrite bead is added as shown in Fig. 4. The bead is also installed under soft-switching conditions to have a fair comparison of the switching performances. The power stage is designed as shown in Fig. 4. The overall test setup is designed to characterize the 3.3 kV RB modules at 2 kV, 25 A condition. In the setup, the

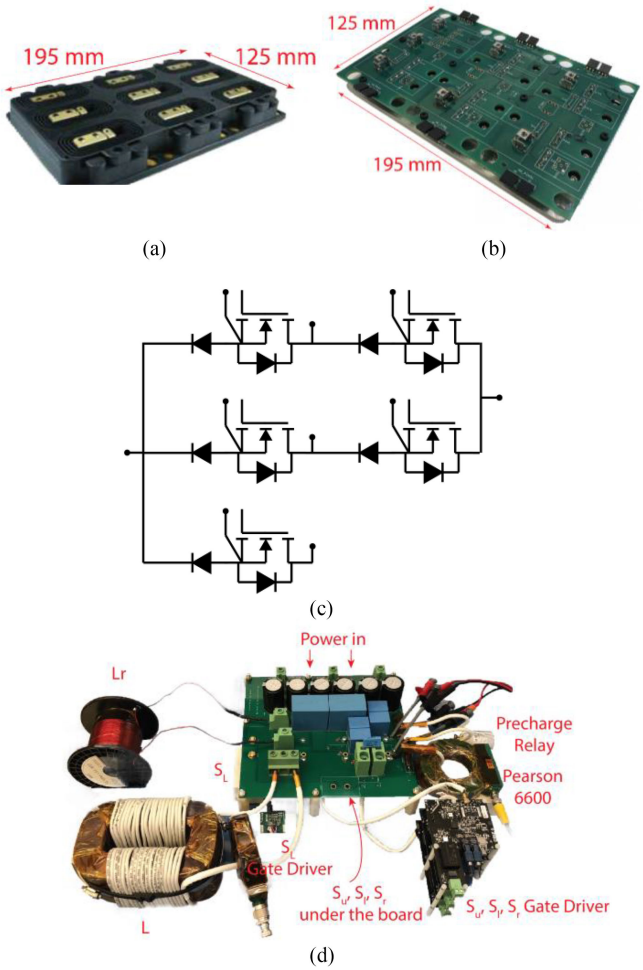

Fig. 3. (a) 3.3 kV, 45 A Wolfspeed RB-device module. (b) 1.7 kV, 10 A module. (c) Schematic of the modules. (d) Image of the 2 kV, 25 A DPT.

core of the inductor L is grounded. The main components used in the DPT are listed in Table I.

B. Experimental Results

The waveforms for both hard switching and soft switching at 1.6 kV 25 A are shown in Figs. 5(a) and 6(a), respectively. Figs. 5(b) and (c) and 6(b) and (c) illustrate magnified portions of the hard-switching and soft-switching waveforms during the turn-ON and turn-OFF switching transitions. Delay in the IRB probe compared to voltage probe is 15 ns and is compensated in loss calculation. Due to the resonant circuit, the DUT is turned ON with zero voltage across it, thus the turn-ON loss is zero. The turn-OFF loss depends on the value of dv/dt, which can be controlled by appropriate selection of Cr. In this test, Cr is chosen to achieve a dv/dt of 0.6 kV/μs compared to 25–30 kV/μs under hard-switching condition.

C. Power Losses

The main switching modules (S_u and S_l) are characterized under different voltage and current levels up to 2 kV, 25 A.

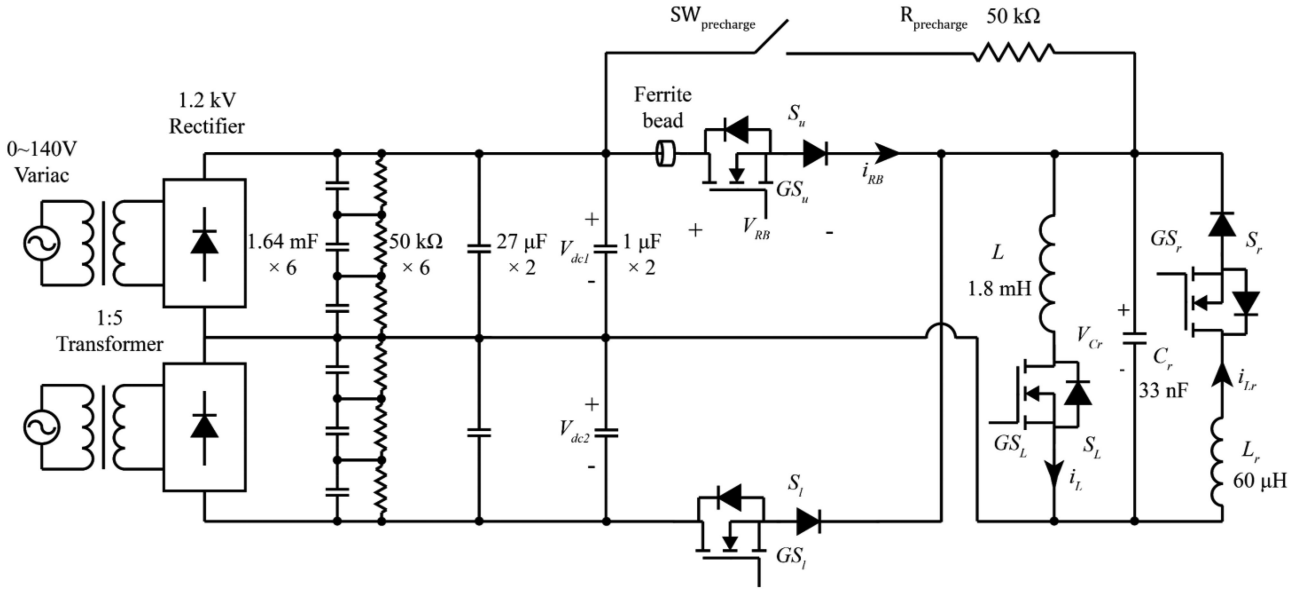

Fig. 4. Circuit diagram of the experimental setup for the DPT.

TABLE I
MAIN COMPONENT OF THE DPT

Element	Description
RB module	3.3 kV, 45A Wolfspeed module Or 1.7 kV, 10A module Wolfspeed C2M1000170D GeneSiC GB10MPS17
RB module Gate Driver	3.3 kV Wolfspeed Gate Driver Or 1.7 kV Wolfspeed CRD-001
L	1.8 mH
L_r	60 μH
C_r	33 nF KEMET CKC33C223KJGACTU
Voltage Probe	Teledyne Lecroy HVD3605 BW=100MHz
Current Probe	Pearson 6600 BW=120MHz

Turn-ON and turn-OFF losses are calculated by

$$E_{\text{on}} = \int_{10\%\ of\ I_{L,pk}}^{90\%\ of\ I_{L,pk}} V_{\text{RB}} \cdot I_{\text{RB}} dt \tag{1a}$$

$$E_{\text{off}} = \int_{90\%\ of\ I_{L,pk}}^{10\%\ of\ I_{L,pk}} V_{\text{RB}} \cdot I_{\text{RB}} dt \tag{1b}$$

$$E_{\text{sw}} = E_{\text{on}} + E_{\text{off}} \tag{1c}$$

Since S_u turns ON when its voltage is zero, E_{on} is zero and soft-switching losses only include the turn-OFF losses. The losses during turn-OFF transition are comprised of device losses and energy stored in the parasitic loop inductance (L_{loop}), which is dissipated in the loop resistance. At 1.6 kV, 25 A, the total turn-OFF losses are 26.9 μJ, of which 3.7 μJ is due to the device characteristic while the remaining 23.2 μJ due to the energy trapped in the L_{loop}. Compared to the device losses, L_{loop} energy dominates the turn-OFF losses, which is discussed in the following section. Device losses are dependent on the value of dv/dt selected, which is 0.6 kV/μs in this case. Fig. 7 shows the

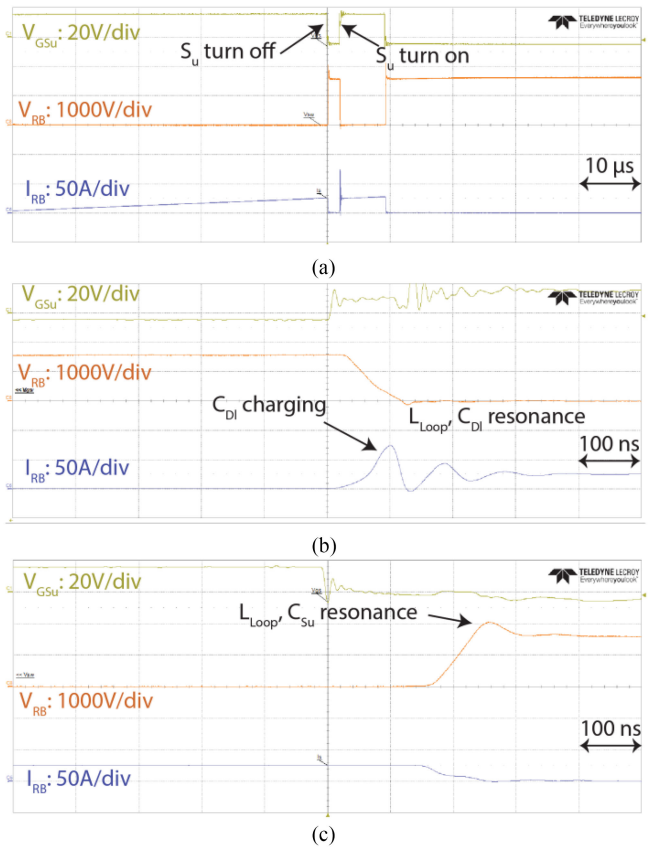

Fig. 5. Experimental results of the 3.3 kV SiC RB module under hard-switching at 1.6 kV, 25A (a) overall voltage and current waveforms, and (b), (c) turn-ON and turn-OFF switching transients, respectively.

total switching losses E_{sw} under different voltage and current levels for both hard switching and soft switching. As compared to hard switching, soft switching shows significant power loss

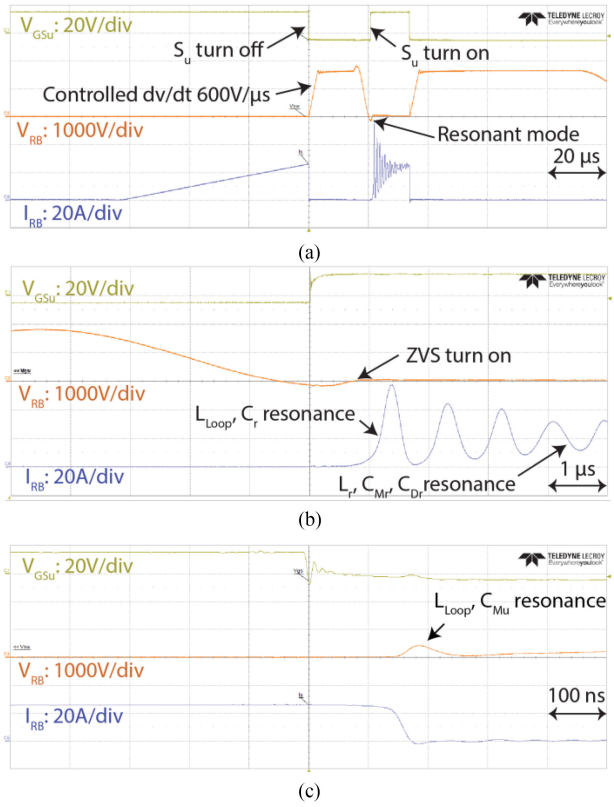

Fig. 6. Experimental results of the 3.3 kV SiC RB module under soft-switching at 1.6 kV, 25 A (a) overall voltage and current waveforms, and (b), (c) turn-ON and turn-OFF switching transients, respectively.

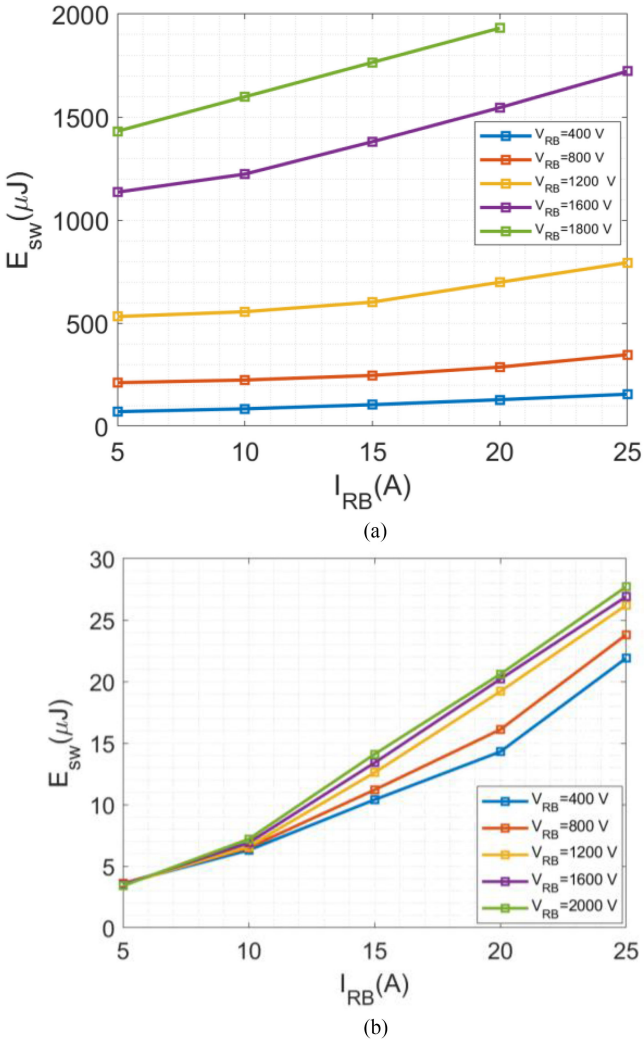

Fig. 7. Power loss comparison of 3.3 kV RB-device (a) hard-switching losses and (b) soft-switching losses.

reduction in the main switching modules, i.e., 98.5%, as shown in Fig. 7.

It is noticeable that the resonant RB module S_r is turned ON and OFF at ZCS due to the presence of L_r, which limits the *di/dt* and its RB characteristic. However, when S_r is turned ON, M_r is blocking $V_{\rm Cr}$ and the capacitive energy associated with the device parasitic capacitor appears as the switching loss of S_r. This portion of energy is lost internally in the device and cannot be measured (the current does not appear at the terminals). At 2 kV, the device output capacitance is 50 pF and this energy is estimated to be 100 μJ, which equals to $\frac{1}{2}CV^2$.

D. Current and Voltage Stresses

As shown in Figs. 5 and 6, under hard switching, the maximum device voltage and current stresses are 2 kV and 75 A, respectively, while under soft switching, those stresses are 1.8 kV and 56 A, respectively. It is also noticed that the maximum gate voltage stress is larger than 20 V under hard- switching condition compared to 15 V under soft-switching condition. Table II summarizes a comparison between hard- switching and soft-switching conditions at 1.6 kV, 25 A.

TABLE II
COMPARISON BETWEEN HARD-SWITCHING AND SOFT-SWITCHING CONDITIONS AT 1.6 kV, 25A USING 3.3 kV SiC RB MODULE

	Hard-switching	Soft-switching
Total Switching losses (μJ)	1722	26.9
dv/dt (kV/μs)	25	0.6
di/dt (A/μs)	500	550
S_u voltage stress (kV)	2	1.8
S_u current stress (A)	75	56
S_u gate voltage stress (V)	>20	16

E. Resonance Caused by Parasitics

As observed in Figs. 5 and 6, resonance occurs at the instant when the devices are switched. Like the conventional DPT, $L_{\rm loop}$ and device capacitance cause these unwanted resonances. The various parasitic elements causing these resonances are identified and labeled in Figs. 5 and 6. By observing the resonant frequency in Figs. 5 and 6, $L_{\rm loop}$ that is comprised of devices internal inductance ($L_{\rm device}$), wiring inductance ($L_{\rm wire}$) and equivalent series inductance of the dc bus capacitance, is estimated as labeled in Fig. 8.

It is noticeable that when the device is turning OFF, a voltage bump appears on the device voltage, as shown in Fig. 6(c). The energy trapped in $L_{\rm loop}$ before turn-OFF is transferred to the capacitance of S_u at this instant and is appeared as a part

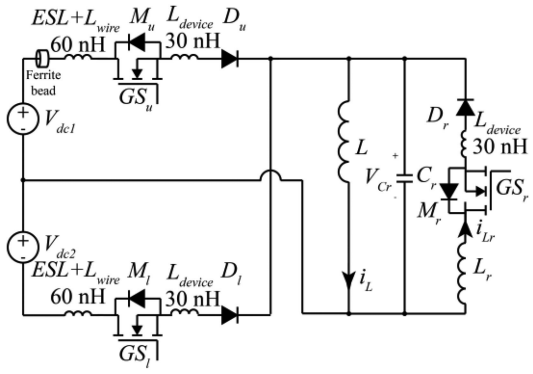

Fig. 8. Schematic of the DPT including the parasitic inductance.

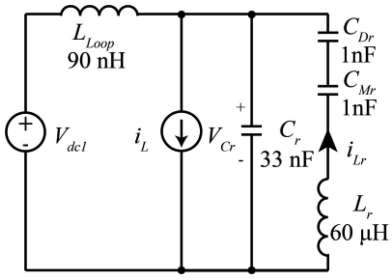

Fig. 9. Equivalent circuit of turn-ON resonance.

of the turn-OFF losses when using *V–I* integration. Therefore, lower $L_{\rm loop}$ will decrease $L_{\rm loop}$ energy, which will decrease the total switching losses consequently. Fig. 6(b) shows a significant resonance in the device current after the resonant mode when S_u turns ON. The equivalent circuit of this instant is shown in Fig. 9. When S_r turns OFF and S_u turns ON, two resonances occur at the same time. If there is any energy left in L_r, it will trigger the first resonance between L_r and $C_{\rm Mr}$ and $C_{\rm Dr}$. On the other hand, a second resonance between $L_{\rm loop}$ and C_r occurs at the same time. Considering the value of L_r, $C_{\rm Mr}$, $C_{\rm Dr}$, $L_{\rm loop}$, and C_r, the critical damping resistance for the two resonances can be calculated by

$$\mathrm{R}_{\rm damp,1} = 2\sqrt{\frac{L_r}{C_{Mr}||C_{Dr}}} \tag{2a}$$

$$\mathrm{R}_{\rm damp,2} = 2\sqrt{\frac{L_{\rm loop}}{C_r}}. \tag{2b}$$

$R_{\rm damp,1}$ is much larger than $R_{\rm damp,2}$, which means that the first resonance is harder to be damped compared to the second one. If S_r is properly controlled to switch at zero current, the first resonance (L_r, $C_{\rm Mr}$, $C_{\rm Dr}$) can be minimized and the total resonance can be easily damped. Fig. 10 shows the turn-OFF transients of S_r with different initial currents in L_r under 400 V, 5 A test condition.

F. Characterization of 1.7 kV SiC RB Modules

Besides the characterization of 3.3 kV Wolfspeed SiC reverse-blocking module, the custom 1.7 kV SiC RB module using discrete devices is characterized using the same test bench

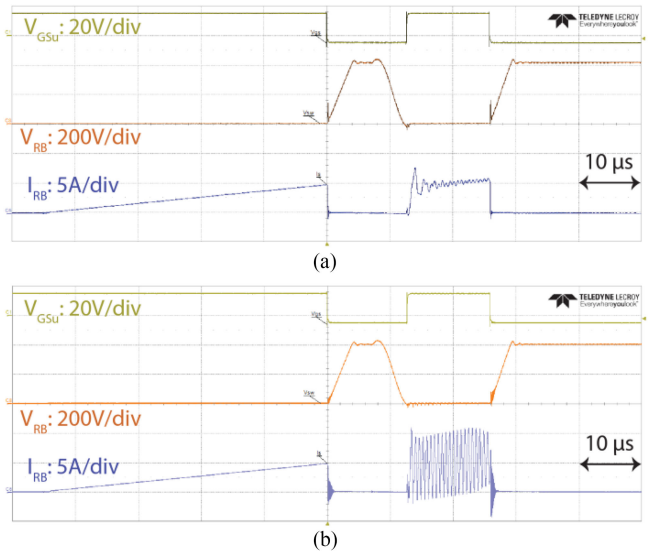

Fig. 10. Turn-OFF transient of S_r with (a) low $I_{\rm Lr}$ and (b) high $I_{\rm Lr}$.

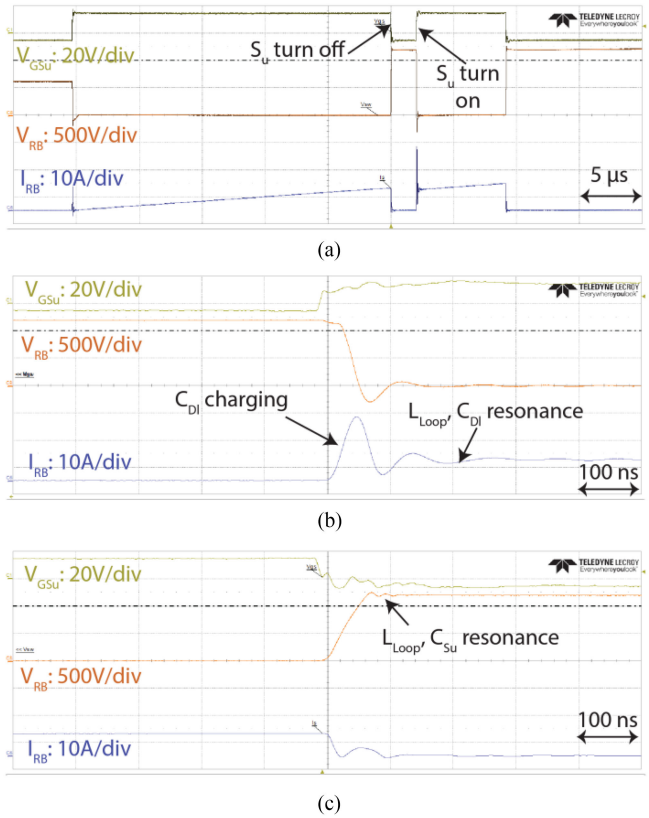

Fig. 11. Experimental results of the 1.7 kV SiC RB module under hard-switching at 1.2 kV, 8 A (a) overall voltage and current waveforms, and (b), (c) turn-ON and turn-OFF switching transients, respectively.

and test procedure. The waveforms for both hard switching and soft switching at 1.2 kV 8 A are shown in Figs. 11(a) and 12(a), respectively. The magnified portions of the hard-switching and soft-switching waveforms during the turn-ON and turn-OFF switching transitions are shown in Figs. 11(b) and (c), and Fig. 12(b) and (c). Similar to the 3.3 kV RB-module, the

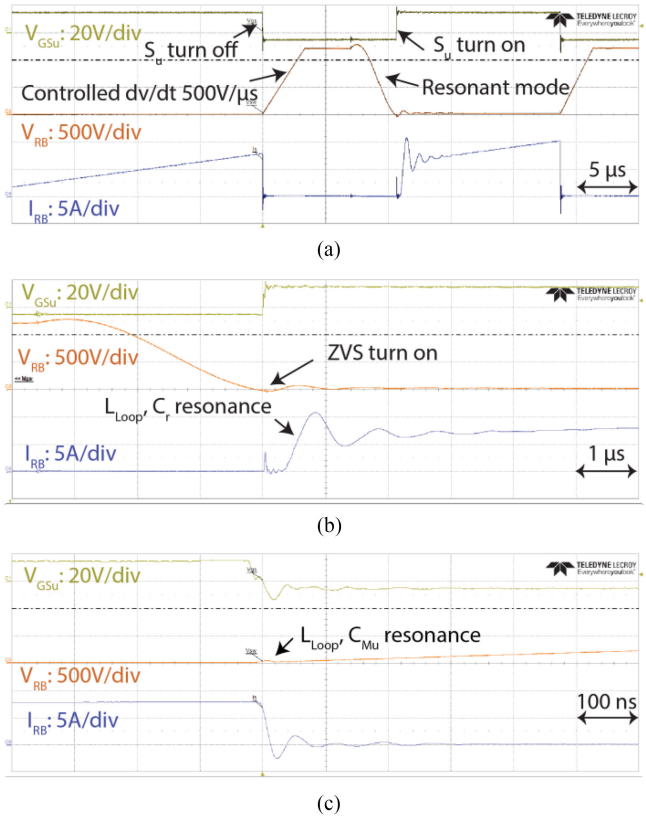

Fig. 12. Experimental results of the 1.7 kV SiC RB module under soft-switching at 1.2 kV, 8 A (a) overall voltage and current waveforms, and (b), (c) turn-ON and turn-OFF switching transients, respectively.

TABLE III
COMPARISON BETWEEN HARD-SWITCHING AND SOFT-SWITCHING CONDITIONS AT 1.2 kV, 8 A USING 1.7 kV MODULE

	Hard-switching	Soft-switching
Total Switching losses (μJ)	254.6	3.2
dv/dt (kV/μs)	30	0.5
di/dt (A/μs)	460	490
S_u voltage stress (kV)	1.25	1.3
S_u current stress (A)	24	11
S_u gate voltage stress (V)	18	18

turn-ON loss of the DUT is zero. In addition, turn-OFF *dv/dt* of 0.5 kV/μs is achieved. Compared to the 3.3 kV Wolfspeed SiC RB-module, the custom module has higher internal parasitic inductanc, which is 60 nH calculated by the same method, described in the previous section. Table III summarizes a comparison between hard-switching and soft-switching conditions at 1.2 kV, 8 A. Similar to the 3.3 kV module, the stresses are less under soft-switching conditions. The di/dt is 490 A/ns when *Rg* is 5 Ω while it is 180 A/ns when *Rg* is 25 Ω. The total switching losses $E_{\rm sw}$ under different voltage and current levels up to 1.2 kV, 8 A for both hard switching and soft switching are shown in Fig. 13. As compared to hard switching, soft switching shows 98.7% power loss reduction in the main switching modules, which is similar to the 3.3 kV module.

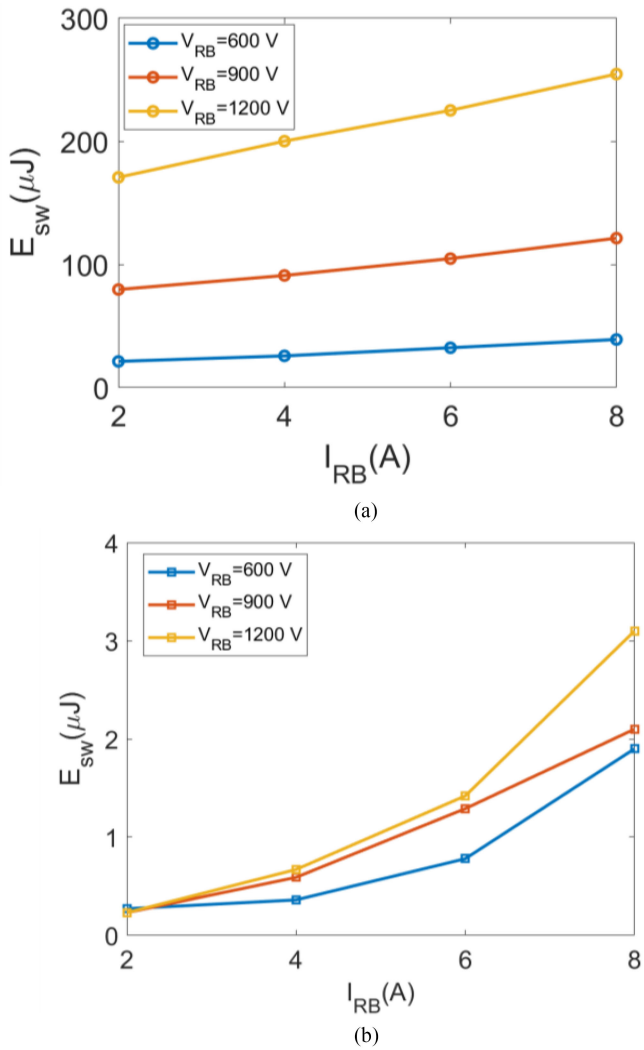

Fig. 13. Power loss comparison of 1.7 kV RB-device (a) hard-switching losses and (b) soft-switching losses.

IV. DYNAMIC VOLTAGE SHARING DURING TURN-ON

The 1.7 kV SiC RB module built based on using discrete switch and diode, enables evaluating the dynamic voltage sharing between the diode and the switch. Although, as shown in Figs. 6(b) and 12(b), the total voltage across RB module S_u is zero during turn-ON, the voltages across M_u and D_u are not zero. Fig. 14(a) shows a turn-ON transition of S_u while Fig. 15(a) shows the equivalent circuit.

Prior to L_r and C_r resonance

$$V_{Su} = V_{\rm dc1} + V_{\rm dc2} \tag{3a}$$

$$V_{Du} = 0. \tag{3b}$$

During resonance, due to the existence of device capacitors $C_{\rm Mu}$ and $C_{\rm Du}$, a small portion of the current flows through $C_{\rm Mu}$ and $C_{\rm Du}$. This current charges $C_{\rm Du}$ and discharges $C_{\rm Mu}$. Therefore, when the resonant stage ends, as shown in Fig. 14(a), $V_{\rm Su}$ is 500 V and $V_{\rm Du}$ is –500 V when the test condition is 1.2 kV and 8 A, indicating that $C_{\rm Mu}$ and $C_{\rm Du}$ both store energy based

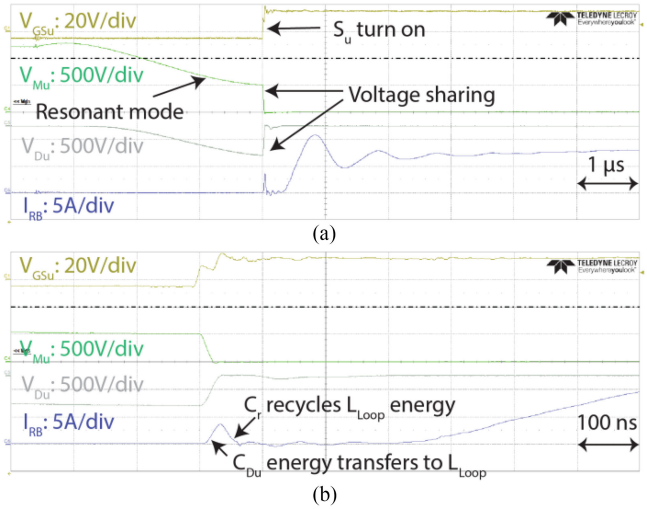

Fig. 14. Voltage sharing during turn-ON transition using discrete 1.7 kV MOSFET/Diode.

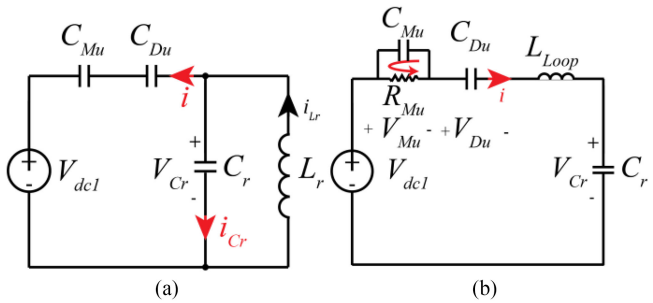

Fig. 15. Equivalent circuit during (a) resonant mode and (b) S_u turn-ON transition.

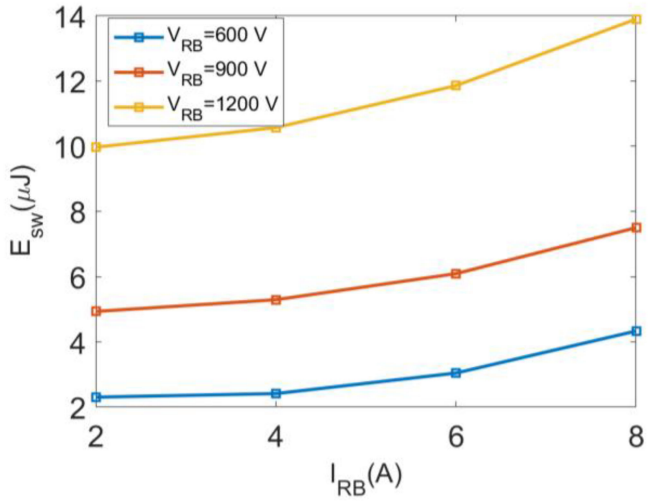

Fig. 16. Power loss of 1.7 kV RB-device under soft-switching condition considering turn-ON voltage sharing.

on

$$V_{Mu} + V_{Du} = V_{\mathrm{dc1}} - V_{Cr},$$

$$i = -C_{eq}\frac{d\left(V_{Mu}+V_{Du}\right)}{dt} = C_{eq}\frac{dV_{Cr}}{dt} \tag{4a}$$

$$V_{Cr}\ (0) = -V_2, V_{Cr}\ (\infty) = V_{\mathrm{dc1}} \tag{4b}$$

where $C_{eq} = C_{Mu}\,||C_{Du}$. V_{Du} and V_{Mu} are calculated by the following:

$$V_{Mu} = V_{Mu}\ (0) - \frac{1}{C_{Mu}}\int idt, V_{Mu}\ (0) = V_{\mathrm{dc1}} + V_{\mathrm{dc2}} \tag{5a}$$

$$V_{Mu} = \frac{C_{Mu}}{C_{Mu}+C_{Du}}\left(V_{\mathrm{dc1}}+V_{\mathrm{dc2}}\right) \tag{5b}$$

$$V_{Du} = V_{Du}\ (0) - \frac{1}{C_{Du}}\int idt, \quad V_{Du}\ (0) = 0 \tag{5c}$$

$$V_{Du} = -\frac{C_{Mu}}{C_{Mu}+C_{Du}}\left(V_{\mathrm{dc1}}+V_{\mathrm{dc2}}\right). \tag{5d}$$

Based on (4), the values of C_{Mu} and C_{Du} determine the final voltage V_{Mu} and V_{Du} as well as the stored energy. Fig. 14(b) shows a zoomed portion of Fig. 14(a). As shown in Fig. 14(b), when M_u is turned ON, V_{Mu} and V_{Du} drop to zero and there is a bump in the device current. The equivalent circuit of this instant is shown in Fig. 15(b). As shown in Figs. 14(b) and 15(b), when M_u is turned ON, energy stored in C_{Mu} is lost and energy in C_{Du} is transferred into parasitic inductance, therefore driving a current bump. Part of this energy is lost in M_u while the rest is retrieved by the resonant capacitor. Device currents during these two submodes are determined as follows.

During the time where V_{Du} drops to zero

$$I_{sw} = e^{-\alpha t}\frac{V_{Cr0}}{L\omega_d}\sin\left(\omega_d t\right) \tag{6a}$$

During the time where energy is recycled by C_r

$$I_{sw} = \frac{V_{c0}}{L\omega_d} - \frac{V_{\mathrm{diff}}}{L_{\mathrm{loop}}}t \tag{6b}$$

where $\alpha = \frac{R}{2L_{\mathrm{loop}}}$, $\omega_d = \sqrt{\frac{1}{L_{\mathrm{loop}}C_{D1}} - \frac{R^2}{4L_{\mathrm{loop}}^2}}$, $V_{\mathrm{diff}} = V_{Cr,pk} - V_{\mathrm{dc1}}$, and R is the lumped wire resistance. Switching losses calculated by (1) only include the losses driven by C_{Du} rather than C_{Mu}. Because of lack of access to the device channel current, the part of switching losses caused by C_{Mu} is not measurable by (1). Therefore, calculation of capacitor stored energy before turning M_u ON is an estimation for this loss, which is 5 μJ under the 1.2 kV, 8 A test condition.

Switching losses of the 1.7 kV device are calculated under different voltage and current levels, with consideration of the turn-ON voltage sharing phenomenon, as shown in Fig. 16. Comparing the power losses calculated at 1.2 kV, 8 A for both soft- and hard-switching scenarios, the power losses under soft switching are reduced by 94.5%. Total switching losses under soft-switching condition are 13.9 μJ of which 10.8 μJ is originating from C_{Su} and C_{Du} voltage sharing. Soft switching helps to reduce majority portion of the switching losses while turn-ON voltage sharing contributes to a major portion of the overall switching losses. In the 3.3 kV module, because of the lack of access to individual MOSFETs or diodes, turn-ON losses

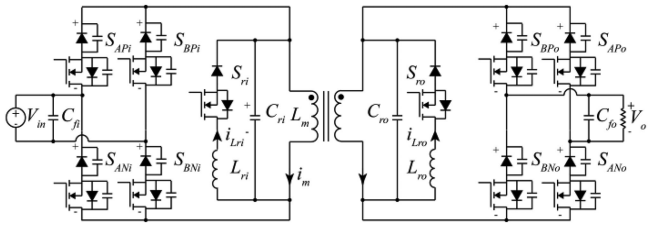

Fig. 17. Circuit diagram of the S4T with parasitic capacitances.

cannot be calculated. However, using the same mechanism as described in (6) for the 1.7 kV module, the turn-ON losses in the 3.3 kV module can be estimated as 75 μJ, which result in a 96% switching losses reduction at 1.6 kV, 25A.

V. Dynamic Voltage Sharing Between RB Modules and Guidance to Use the RB-Modules in the S4T

In the previous section it was shown that the dynamic voltage sharing between the diode and the switch within an RB module causes a slightly increased switching loss even under soft switching conditions. The same phenomenon when extended to two RB modules results in a much larger problem, an increased voltage stress. In a traditional voltage source converter, the free-wheeling diodes (FWDs) limit the maximum voltage across any devices to be equal to the dc bus voltage. In a current source converter, such as S4T, two RB modules together have to block $V_{\rm in}-V_{\rm Cr}$. Please note that $V_{\rm Cr}$ varies from $+V_{\rm in}$ to $-V_{\rm in}$. Hence, the two RB modules have to block a maximum of $2*V_{\rm in}$. There is no FWD equivalent in CSCs to ensure $2*V_{\rm in}$ voltage is shared equally between the two RB modules. This section explains the dynamic voltage sharing issue between two RB modules, using a dc–dc S4T converter as an example. In addition, modified gating strategy for the RB modules in S4T, which enables fully realizing the benefits of soft switching, is presented.

A. Dynamic Voltage Sharing Between RB Modules

Conventionally, switching devices of the S4T that are expected to carry the current, are turned ON and OFF at the beginning and end of that particular conduction mode, respectively [13]. However, this gating strategy can result in additional voltage stress across the devices because of the dynamic voltage sharing issues discussed in the previous section. Fig. 17 shows the circuit diagram of the S4T for dc–dc applications where device parasitic capacitances and voltage polarities are represented. Fig. 18(a) shows the voltage of each RB module using the conventional gating strategy. At t_2, the S4T is in the charging mode with $S_{\rm APi}$ and $S_{\rm BNi}$ being ON. The charging mode ends at t_3 with turning $S_{\rm ANi}$ ON and turning $S_{\rm BNi}$ OFF while the state of $S_{\rm APi}$ remains the same. The two devices on the lower half of the input bridge are discharged in ZVS mode and $S_{\rm BNi}$ blocks the input voltage at t_4. After t_5, the freewheeling mode is over, and the input bridge is inactive with all its devices turned OFF. Therefore, all devices of the input bridge are discharged in ZVS mode and ΔV of each RB module during the ZVS mode from t_5 to t_6 is half of the $\Delta V_{\rm Cr}$. When the input and output voltages are

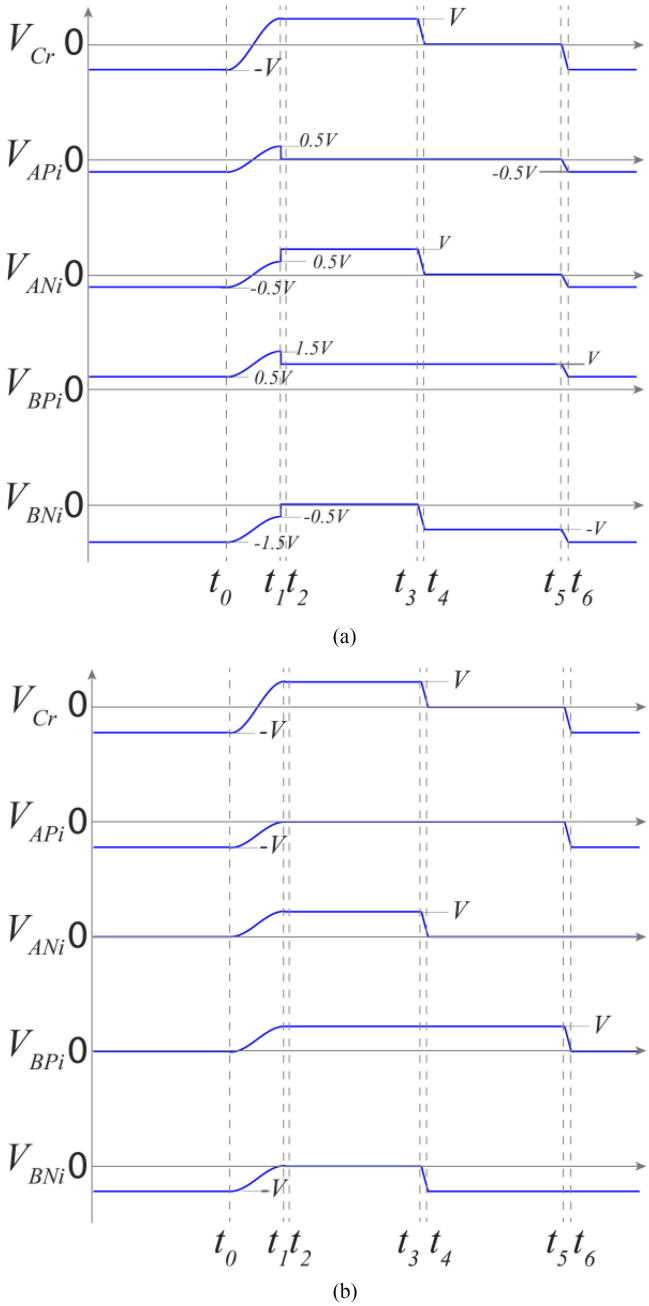

Fig. 18. Voltage of each RB-device of the input bridge of S4T using (a) the conventional gating strategy showing 1.5 p.u. voltage stress and (b) the proposed turn-ON scheme.

the same, $S_{\rm BNi}$ is blocking 1.5 p.u. voltage at t_6 compared to the nominal operating voltage, as shown in Fig. 18(a). At t_1, when the resonant mode is over and prior to turning $S_{\rm APi}$ and $S_{\rm BNi}$ ON, $V_{\rm APi}$ and $V_{\rm BNi}$ are not zero and their turn-ON losses are not negligible. Therefore, the benefits of the S4T in terms of controlled dv/dt and absence of switching losses are not achieved when relying on the conventional gating strategy. The root cause of this phenomenon is the unequal voltage sharing of the upper- and lower-side RB modules even though the total voltage is controlled by C_r. A proper gating sequence is

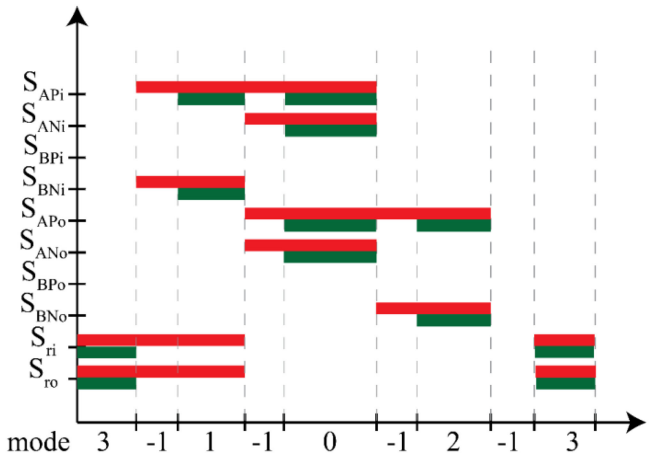

Fig. 19. Proposed switching sequence of S4T.

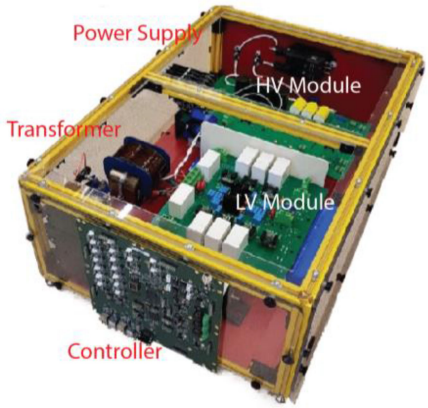

Fig. 20. Image of the 25 kVA 2.5 kV dc/ 600 V dc S4T module.

required to control the voltage sharing of each RB module. When the input bridge is inactive, instead of turning both S_{APi} and S_{Ani} OFF, only S_{APi} is turned OFF, as shown in Fig. 18(b). By keeping S_{ANi} ON, only the upper-side RB modules of the input bridge are discharged in ZVS mode from t_5 to t_6. Consequently, the additional voltage stress is eliminated and V_{API} and V_{BNi} become zero prior to turning ON at t_1. The same strategy can be applied to the output bridge. When the output bridge is inactive, S_{ANo} is turned ON to control the voltage sharing of each device.

B. Proposed Switching Sequence of the S4T

Based on the previous discussion, the switching sequence of the conventional voltage/flyback type CS converters, such as the one presented in [17]–[19] cannot be applied to S4T. To fully utilize the benefit of the S4T, a new switching sequence is proposed. Fig. 19 shows the gate signals applied to each RB modules of the S4T for dc–dc application in which a red bar shows when the gate-source voltage of a specific device is high while a green bar shows when the dc-link current is flowing through a specific device. The nomenclature of modes is similar to that shown in Fig. 2, in which mode 1 is the the charging mode, mode 2 is the discharging mode, mode 3 is resonant mode, mode –1 is ZVS mode, and mode 0 is freewheeling mode. The proposed gating strategy can be generalized to other applications with more operating modes.

C. Converter Verification

The proposed switching sequence is applied to a 25 kVA 2.5 kV dc/600 V dc S4T prototype, shown in Fig. 20. The schematic of the S4T which operates in the dc–dc mode is shown in Fig. 1. Fig. 21 shows the voltage sharing impact on the RB module voltage during the turn-ON transition. Fig. 21(a) shows the waveforms of the S4T using the conventional switching sequence at 100 V. As shown, the RB module is turned ON with hard-switching and the dv/dt is high. Module S_{BPi} has a voltage stress of 1.5 p.u. because of which the experiment was not extended to higher voltages. Fig. 21(b) and (c) shows the waveforms of the S4T using the proposed switching sequence

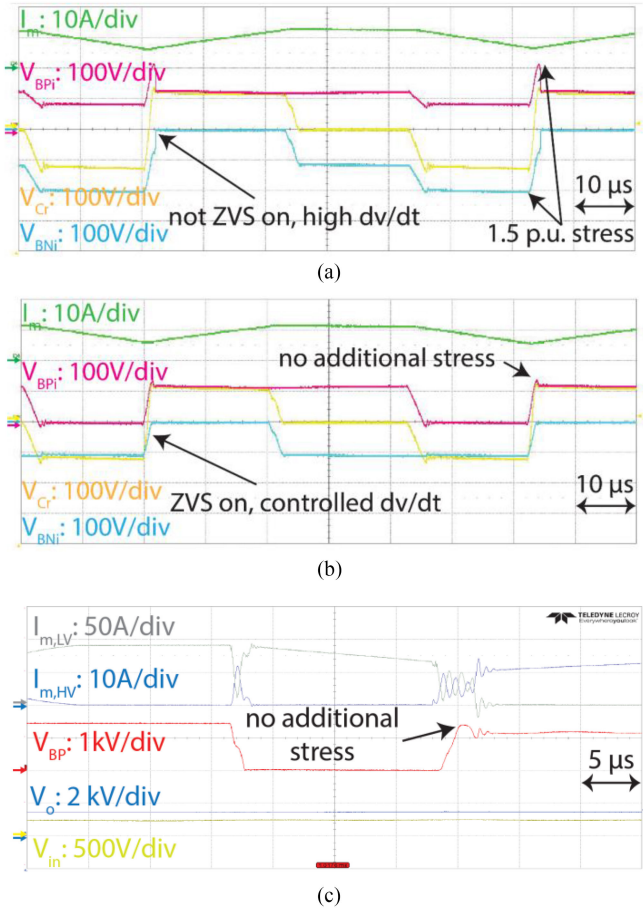

Fig. 21. Waveforms of total RB-device voltage in the S4T using (a) the traditional switching sequence at 100 V; and (b) the proposed switching sequence at 100 V (c) the proposed switching sequence at 1.5 kV, 10 kVA.

at 100 and 1500 V, respectively. In Fig. 21(c), $I_{\mathrm{m,HV}}$ and $I_{\mathrm{m,LV}}$ are the HV and LV side winding current of the transformer, respectively. All the RB modules achieve ZVS, controlled *dv/dt* and stress $\leq$1.0 p.u. Hence, the effectiveness of the proposed gating strategy in achieving ZVS across all modules and in limiting the voltage stress to 1.0 p.u. is verified.

VI. Conclusion

There is a pressing need to build HV power converters, such as solid-state transformers, for direct grid-connected applications. This has been driving the development and adoption of SiC power devices rated at 3.3 to 15 kV. However, SiC device operation in typical voltage source converters is accompanied by high *dv/dt* of 30–50 kV/μs, causing severe EMI problems in real converters. New topologies such as the S4T appear attractive because they realize ZVS giving low switching loss and low EMI but require RB devices operating under ZVS conditions in a CS structure—data for which is simply not available from manufacturers or from literature. Most of the available device characterization data has been for devices with anti-parallel diodes, not with series-connected diodes.

This article presents detailed test results and model extraction for 3.3 kV 45 A SiC module with five RB devices in the package. A novel test-bed was designed and built for this characterization and model extraction of RB devices under both hard-switching and ZVS conditions. The testing helped to generate a parasitic and loss model for the RB devices, showing that switching losses are reduced by as much 96%, while *dv/dt* is reduced from 30 to $<$1 kV/μs. The testing also helped to identify unexpected dynamic voltage sharing issues between the series diode and MOSFET. It was shown that this voltage sharing issue within an RB module (between the switch and the diode) results in a marginally higher switching loss. In addition, it was shown that the same phenomenon of dynamic voltage sharing, when extended to two RB modules (one upper RB module and one lower RB module), causes additional voltage stress (up to 1.5 p.u.) across each RB module. Modified switching schemes to limit this voltage stress when the RB modules are used in such converters presented and verified through an S4T prototype at 1.5 kV, 10 kVA.

References

[1] M. Stieneker and R. W. D. Doncker, "Dual-active bridge dc-dc converter systems for medium-voltage DC distribution grids," in *Proc. IEEE 13th Brazilian Power Electron. Conf. 1st Southern Power Electron. Conf.*, 2015, pp. 1–6.

[2] S. P. Engel *et al.*, "Comparison of the modular multilevel DC converter and the dual-active bridge converter for power conversion in HVDC and MVDC grids," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 124–137, Jan. 2015.

[3] N. Soltau, H. Stagge, R. W. D. Doncker, and O. Apeldoorn, "Development and demonstration of a medium-voltage high-power DC-DC converter for DC distribution systems," in *IEEE 5th Int. Symp. Power Electron. Distrib. Gener. Syst.*, 2014, pp. 1–8.

[4] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, "SiC versus Si—Evaluation of potentials for performance improvement of inverter and DC–DC converter systems by SiC power semiconductors," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2872–2882, Jul. 2011.

[5] K. Shenai, "Future prospects of wide-band-gap (WBG) semiconductor power switching devices," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 248–257, Feb. 2015.

[6] A. Marzoughi, J. Wang, R. Burgos, and D. Boroyevich, "Characterization and evaluation of the state-of-the-art 3.3 kV 400 A SiC MOSFETs," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8247–8257, Oct. 2017.

[7] A. Marzoughi, R. Burgos, and D. Boroyevich, "Characterization and performance evaluation of the state-of-the-art 3.3 kV 30 A full-SiC MOSFETs," *IEEE Trans. Industry Appl.*, vol. 55, no. 1, pp. 575–583, Jan. 2019.

[8] J. Wang *et al.*, Characterization, modeling, and application of 10-kV SiC MOSFET, *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 1798–1806, Aug. 2008.

[9] S. Hazra *et al.*, "High switching performance of 1700-V, 50-A SiC power MOSFET over SI IGBT/BIMOSFET for advanced power conversion applications," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4742–4754, Jul. 2016.

[10] S. Ji, S. Zheng, Z. Zhang, F. Wang, and L. M. Tolbert, "Protection and temperature-dependent switching characterization of latest generation 10 kV SiC MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf. Expos.*, 2017, pp. 783–788.

[11] X. She, P. Losee, H. Hu, W. Earls, and R. Datta, "Performance evaluation of 1.5 kV solar inverter with 2.5 kV silicon carbide MOSFET," *IEEE Trans. Industry Appl.*, vol. 55, no. 6, pp. 7726–7735, Nov/Dec. 2019.

[12] H. Chen and D. Divan, "High speed switching issues of high power rated silicon-carbide devices and the mitigation methods," in *Proc. IEEE Energy Convers. Congr. Expo.*, pp. 2254–2260, 2015.

[13] H. Chen and D. Divan, "Soft-switching solid-state transformer (S4T)," *IEEE Trans. Power Electron.s*, vol. 33, no. 4, pp. 2933–2947, 2018.

[14] A. De, S. Roy, S. Bhattacharya, and D. M. Divan, "Performance analysis and characterization of current switch under reverse voltage commutation, overlap voltage bump and zero current switching," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2013, pp. 2429–2435.

[15] A. De, S. Roy, S. Bhattacharya, and D. M. Divan, "Characterization and performance comparison of reverse blocking SiC and Si based switch," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl.*, 2013, pp. 80–83.

[16] Y Ren, M. Xu, J. Zhou, and F. C. Lee, "Analytical loss model of power MOSFET," *IEEE Trans. Power Electron.s*, vol. 21, no. 2, pp. 310–319, Mar. 2006.

[17] A. K. Gupta and A. M. Khambadkone, "A space vector PWM scheme for multilevel inverters based on two-level space vector PWM," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1631–1639, Oct. 2006.

[18] J. W. Kolar, T. Friedli, J. Rodriguez, and P. W. Wheeler, "Review of three phase PWM AC–AC converter topologies," *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 4988–5006, Nov. 2011.

[19] H. Chen, A. Prasai, and D. Divan, "Dyna-C: A minimal topology for bidirectional solid-state transformers," *IEEE Trans. Power Electron.s*, vol. 32, no. 2, pp. 995–1005, Feb. 2017.

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