Analysis, Design, and Implementation of Junction Temperature Fluctuation Tracking Suppression Strategy for SiC MOSFETs in Wireless High-Power Transfer

Ruoyin Wang, *Student Member, IEEE*, Linlin Tan, Chengyun Li, *Student Member, IEEE*, Tianyi Huang, *Student Member, IEEE*, Haoze Li, *Student Member, IEEE*, and Xueliang Huang, *Member, IEEE*

***Abstract*—In order to improve system reliability and reduce device thermal fatigue failure in multiload wireless power transfer (WPT) systems for electric vehicles, the implementation of the junction temperature fluctuation suppression strategy for SiC MOSFETs is necessary. However, current methods are relatively lacking, and active thermal management has not been used in WPT systems. In this article, the relationship between circuit parameters and junction temperature of SiC MOSFET is analyzed. In particular, a junction temperature fluctuation tracking suppression strategy for SiC MOSFETs is proposed, which consists of a coarse and a fine adjustment stage. As for the former, a shunt capacitor bank switching method is implemented. In order to compensate for the coarse adjustment defects in the small adjustment range and poor effect, in fine adjustment stage, a changing driving voltage method is used. Finally, a 5-kW multiload WPT system is built for verification. Experimental results show that the proposed strategy has obvious effect on the suppression of junction temperature fluctuation and keeps temperature near the target temperature. Benefiting from this, the maximum 13.9 °C junction temperature fluctuation is completely eliminated when the power fluctuations are within 36.1% of the rated power, and the heat load of each SiC MOSFET can be independently adjusted.**

***Index Terms*—Changing driving voltage method (CDVM), junction temperature fluctuation tracking suppression (TFTS) strategy, shunt capacitor bank switching method (SCSM), wireless power transfer (WPT).**

I. INTRODUCTION

WIRELESS power transfer (WPT) technology is a safe and flexible charging method. Due to its outstanding advantages, this technology has been widely applied in the transportation [1], medical [2] and consumer electronics [3], underwater equipment [4], mobile devices [5], electric vehicles [6], etc., with the power ranging from a few to dozens of kilowatts.

The performance of a WPT system is determined by the three following indicators: high efficiency, long distance, and high power [7]. The operating frequency of a magnetically coupled resonant WPT (MCR-WPT) system is generally tens of kilohertz or above. In particular, in such systems the high-frequency inverter is a key device. As the operating frequency increases, the switching and the gate losses of the semiconductor devices increase with the square of the frequency [8]. Moreover, the temperature rise of the system is more prominent under high-power cycling. An efficient thermal management must be therefore carefully considered. Third-generation semiconductor materials represented by SiC have many incomparable advantages compared to Si [9]. Indeed, it has great practical significance to investigate the application of SiC MOSFETs to develop high-frequency and high-power WPT power supplies, with the aim of applying this new design strategy to new technologies.

The growing application of SiC MOSFETs in WPT systems for electric vehicles clearly indicates that both frequency and power will increase to higher levels. The dynamic behavior of SiC MOSFETs is affected by many nonlinear capacitors, and the dynamic characteristics calculated by classical methods have obvious limitations. Moreover, at present, a systematic research study on the dynamic losses of high-speed switching SiC MOSFET power devices is lacking. Indeed, the reliability problem caused by a high-frequency and high-power operation must be considered. Power devices subject to large power fluctuations [10] will result in a strong reduction of their expected service life with respect to other equipment [11].

The superior electrothermal properties of SiC devices are compared with Si devices. However, the reliability of SiC power modules has been identified as a major area of uncertainty in applications that require high reliability. Due to direct contact of materials with different coefficients of thermal expansion, the elements of the packaging are subjected to thermal stresses caused by the variation of temperature during operation of the devices [12]. The thermal stresses will cause degradation of the weaker elements of the packaging system, leading to device

Manuscript received January 28, 2020; revised April 2, 2020 and May 28, 2020; accepted June 21, 2020. Date of publication June 24, 2020; date of current version September 4, 2020. This work was supported by the National Key Research and Development Project under Grant 2018YFB0106300. Recommended for publication by Associate Editor J.-I. Itoh. *(Corresponding author: Linlin Tan.)*

The authors are with the School of Electrical Engineering, Southeast University, Nanjing 210096, China, and also with the Key Laboratory of Smart Grid Technology and Equipment in Jiangsu Province, Zhenjiang 212000, China (e-mail: ruoy_wang@yahoo.com; tanlinlin@seu.edu.cn; 1427418960@qq.com; 220182746@seu.edu.cn; 220192808@seu.edu.cn; xlhuang@seu.edu.cn).

Color versions of one or more of the figures in this article are available online at https://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2020.3004922

failure [13]. And the higher thermal conductivity and Young's modulus of SiC may cause higher stresses on the die-attach solder layer during power changing [14]. In some applications, SiC devices may be suffering from higher temperature changing caused by power changing, that is, temperature fluctuations [15], [16]. During the temperature fluctuations, the plastic strain and creep may cause the solder fatigue [17]–[19]. Although the SiC devices are suitable to operate at high temperatures, the variation of temperature can cause significant thermal stresses on the solder layer, leading to substantial fatigue [19]–[21]. Experimental results show that the shear stress in a SiC die-attach is higher than that in a Si device [22], and strain energy density tends to concentrate at the chip edge where the difference is 1.5 times between the SiC and Si devices under comparable conditions. It is considered that the in-service lifetime of SiC solder layer is only a third of the benchmark Si device [14]. It has been confirmed that the temperature fluctuations ΔT_j affects SiC device life more than Si device [12]. It means that SiC devices are more susceptible to temperature fluctuations.

Although the SiC device is suitable for higher temperature, the power variation in the actual application scenario results in constant variation of junction temperature. Within the SiC device, the variation of temperature can cause significant thermal stress on the solder layer leading to substantial fatigue, which eventually leads to device failure. Therefore, compared with the challenges of continuous high temperature, widespread and frequent junction temperature fluctuations have a greater impact on the life of the SiC MOSFET.

Power fluctuations can be classified as fast and slow cycling. Fast power fluctuations mainly affect the reliability of the die-attach solder layer [23]. Meanwhile, the slow fluctuations mainly produce fatigue on the baseplate solder layer [12]. Therefore, the reliability of SiC MOSFET will be affected regardless of whether it is fast or slow as long as power fluctuations exist. As long as the power fluctuations exist, i.e., as long as the ΔT_j exists, the life of SiC MOSFET will be affected. Researchers have established the lifetime models of SiC device and Si device, which can be concluded that the lifetime is not only affected by the value of ΔT_j [24], [25]. In the field of practical wireless charging application, the power fluctuation of SiC MOSFET is random. This phenomenon indicates that ΔT_j is also random and has an irregular fluctuation. Accordingly, the factor of random thermal stress is introduced, thereby further affecting the lifetime of SiC MOSFET. The reliability of SiC devices due to power fluctuation (i.e., temperature fluctuation) has been tested in the relevant literature; the literature verified the correctness of the life model and confirmed that SiC MOSFET has a long lifetime only when ΔT_j approaches zero [23]. Finally, a special note is needed: From the finite element (FE) analysis the thermal stresses of a SiC device can be significantly higher than those of the comparative Si device under the same junction temperature profile, particularly for low ΔT_j values [12]. This proves again that the in-service lifetime of SiC solder layer is only a third of the benchmark Si device [14].

Junction temperature fluctuations make SiC MOSFET continuously bear the alternating thermal stress shock and, thus, leading to thermal fatigue failure, which greatly reduces the system reliability and service life. And the impact is more than ordinary Si devices. This may compromise the safety of the whole high-frequency, high-power wireless charging system. Therefore, a suppression strategy for junction temperature fluctuations of SiC MOSFETs is urgently needed to reduce thermal shock damage and stabilize the junction temperature fluctuations caused by the power fluctuations in WPT.

Power fluctuations exist in both static and dynamic wireless charging systems for electric vehicles. In the static wireless charging system, the receiving and the transmitting coils may have the deviation. And different charging loads have different deviations. Even the same battery load requires different amounts of power at various charging times, as measured by the battery's charging curve. All these phenomena will cause the system power fluctuation problem. In a multiload static wireless charging system, the input power of the system will fluctuate when different loads are connected and cut off. In a dynamic wireless charging system, the problem of power fluctuation during dynamic wireless charging is also proposed [26]. The coupling degree of the receiving and transmitting coils frequently fluctuates with the driving of the EV, thereby resulting in significant power fluctuations. Therefore, the SiC MOSFETs in a WPT system are vulnerable to power fluctuations, resulting in junction temperature fluctuations. However, it is worth to note that there are no studies on thermal management of WPT systems in electric vehicles. The characteristics of the MCR-WPT system should be considered when designing the temperature control strategy.

In recent years, the research study on junction temperature management technologies has gradually increased in both academia and industry. Studies in [27]–[29] proposed to increase or decrease the switching losses by changing the switching frequency, in order to improve the control of device junction temperature. However, this strategy cannot individually adjust the junction temperature of a single semiconductor element. In addition, by adjusting the switching frequency, the WPT system resonance is lost. In addition, the temperature controller strategy based on switching frequency needs to change the switching frequency within a large range, which affects the output waveform of the converter and has poor effect. In [30], a junction temperature management of a reactive power cycle based on a three-level parallel converter was proposed to adjust switching losses by controlling the reactive current cycle. However, this method can only be used in parallel converter systems, and it increases the thermal load of the diode. The discontinuous pulsewidth modulation strategy reported in [31] reduces the loss in semiconductor devices, thereby lowering the average junction temperature. The biggest drawback of this method is to decrease the output quality of the converter. In [32], a temperature control method based on power distribution was proposed, which controls the device temperature by limiting the power of the converter. However, this method requires multiple converters to be used in parallel, and each converter is used in frequency reduction condition and, thus, reducing the power density. In [33], in order to fix the frequent fluctuations of junction temperature in photovoltaic inverters due to rapid changes in lighting conditions, the maximum power point tracking algorithm was optimized in order to limit the possible thermal stress/shock of the power electronics in the dc/dc converter. The control strategy of this method is complex, and it is not suitable for high-frequency occasions, such as the WPT. For the traditional air cooling technology, on the one hand, the purpose of this study is not simply to reduce the junction temperature but to suppress the junction temperature fluctuations. On the other hand, the additional cooling design increases the system cost and volume. In summary, most of the existing junction temperature controlling methods have some drawbacks, such as output waveform quality reduction, control complexity, easy-to-detune of WPT system, unavailable individual-level single device adjustment, and nonobvious adjustment. Therefore, it is necessary to design a set of junction temperature fluctuation suppression strategy suitable for the MCR-WPT system.

In this article, a junction temperature fluctuation tracking suppression (TFTS) strategy for SiC MOSFETs in a multiload wireless charging system of electric vehicles is proposed for the first time, which belongs to an active thermal management technology. The TFTS strategy tracks the junction temperature and controls the variation trend of the junction temperature through the case temperature, which helps to eliminate the design of the additional air cooling and reduce the volume and cost of the system. The TFTS strategy is divided into a coarse and a fine adjustment stage. The former proposes a shunt capacitor bank switching method (SCSM). In the fine adjustment stage, a changing driving voltage method (CDVM) is used. The combination of SCSM and CDVM is unique, outstanding, and complementary to the strengths of the two methods, which greatly improves the reliability of SiC MOSFETs. The switching losses are reduced and compensated by adjusting the buffer capacitance and drive voltage to stabilize the junction temperature fluctuation of SiC MOSFETs. Then, the temperature of any SiC MOSFET can be controlled separately. In addition, the TFTS strategy does not change the output property of the high-frequency inverter. This strategy does not make the WPT system off-resonant. Thus, it is extremely suitable for the WPT system. Finally, the feasibility of the proposed TFTS strategy is verified by taking the 5-kW WPT prototype as an example. As a result, the final temperature of each SiC MOSFET is stabilized near the target temperature without reducing the output quality of the power converter. This control method helps simplify the cooling design and reduce the cooling cost.

The rest of this article is organized as follows. Section II describes the system architecture and the working principle of the LCC-S multiload WPT system. The relationships among the switching losses, the control variables, and the junction temperature are given in Section III, by modeling the dynamic characteristics of the SiC MOSFET. Section IV deals with the TFTS strategy and the hardware implementation methods in building the designed system. Section V reports on the experimental prototype and experimental results, which confirm the feasibility and effectiveness of the proposed TFTS strategy. Finally, Section VI concludes this article.

II. SYSTEM ARCHITECTURE

In order to suppress SiC MOSFET junction temperature fluctuations in the multiload WPT system, a tracking suppression strategy for junction temperature fluctuation is proposed. The main purpose is to reduce or even eliminate the junction temperature fluctuation caused by power fluctuations through a control strategy rather than single heat dissipation and cooling. In addition, this article does not involve the accurate measurement of junction temperature but tracks the variation trend of junction temperature by detecting the case temperature. Complete control is accomplished through the combination of the SCSM and the CDVM. Because the capacitance is difficult to adjust linearly and continuously, if only the coarse adjustment method is used, the adjustment range would be narrow, and the suppress effect would not be the ideal one. Besides, the coarse adjustment is in the open loop, and both the control effect and the interference suppression performance are relatively poor. Furthermore, the SCSM cannot individually adjust the temperature of each SiC MOSFET in the bridge topology. In order to improve these drawbacks, a closed-loop fine adjustment, based on a CDVM, is used downstream of the coarse adjustment stage. The CDVM can further improve the temperature fluctuation and make the control mode flexible. If CDVM is used alone and the current temperature is far from the target temperature, then the processor will keep the upper or lower limit of the output due to the limiting treatment of the proportional–integral control system, thereby resulting in a saturation problem. This situation will reduce the dynamic performance of the system and even lead to the instability of the closed-loop system and poor temperature adjustment effect. In this article, the SCSM and CDVM are combined to integrate their advantages for the first time.

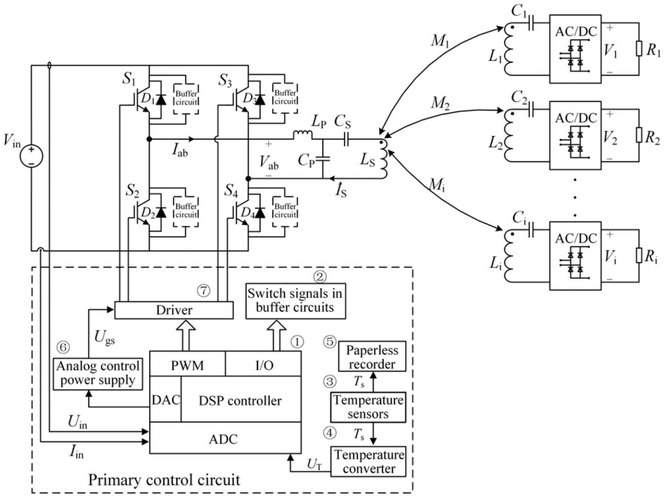


Fig. 1. System architecture relevant to the implemented junction temperature closed-loop control strategy for a multiload wireless charging system of electric vehicles.

The overall system architecture is shown in Fig. 1. The high-frequency full-bridge inverter contains four SiC MOSFETs (namely, S_1, S_2, S_3, and S_4). The resonant system consists of the primary coil L_S, the resonant inductor L_P, and the resonant capacitors C_S and C_P. L_S produces the high-frequency alternating magnetic field to induce a voltage in the secondary-side coil L_i. The direct current output voltage V_i, which is supplied to the load resistances R_i, is generated by a series connection of resonant capacitors C_i and full-bridge rectification stages.

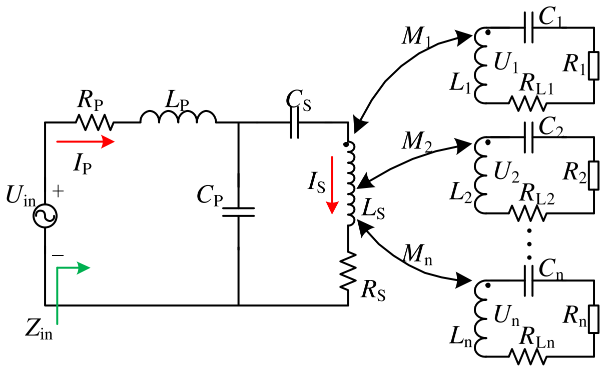


Fig. 2. LCC-S type multiload WPT system.

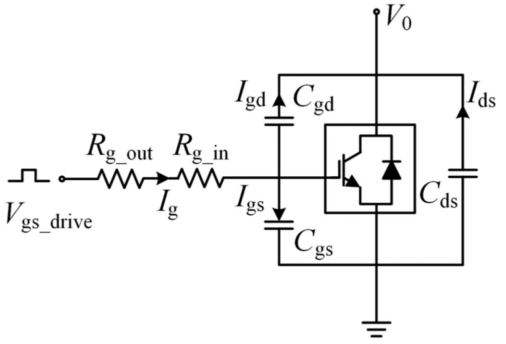


Fig. 3. Equivalent input circuit of the SiC MOSFET gate.

The system control circuit can be divided into two parts: the coarse and the fine adjustment control circuits. The coarse control circuit consists of two modules, labeled (①②) in Fig. 1. The DSP controller (①) collects the input voltage and current of the system. Then, the switching signal in the buffering circuit (②) is determined according to the range of the input power.

The fine control circuit consists of six modules, labeled (①③④⑤⑥⑦) in Fig. 1. The real-time junction temperatures T_s of each SiC MOSFET are measured through the temperature sensor module (③). The real-time temperature is recorded by paperless recorder (⑤), and the voltage signal U_T is obtained via the temperature converter module (④). The DSP controller collects U_T for the proportional integral differential (PID) operation to generate a gate drive signal, whose driving voltage is output through the digital to analog converter (DAC) module of the DSP controller to generate the final driving voltage by means of the analog control power supply module (⑥). Module ⑦ is the driver module.

III. BASIC THEORY ANALYSIS

Due to the different characteristics of the SiC MOSFETs compared with the conventional Si devices, a specific model to analyze the relationship between the SiC MOSFET switching losses and the correlation control variables has been developed, as described in the following sections.

A. Modeling of the Multiload WPT System

The LCC-S type multiload wireless power transfer system is shown in Fig. 2. The impedance of each load branch is given as follows:

$$Z_i = R_i + R_{\mathrm{Li}} + j\omega L_i + \frac{1}{jwC_i}. \tag{1}$$

The total reflected impedance of the multiload system is given as follows:

$$Z_r = \sum_{i=1}^{n} \frac{\omega^2 {M_i}^2}{Z_i} = \sum_{i=1}^{n} \frac{\omega^2 {M_i}^2}{R_i + R_{\mathrm{Li}} + j\omega L_i + 1/jwC_i} \tag{2}$$

and the system input impedance can be expressed as

$$Z_{\mathrm{in}} = R_P + j\omega L_P + \frac{1 - \omega^2 L_S C_S + jwC_S R_S + jwC_S Z_r}{j\omega(C_S + C_P - \omega^2 C_S C_P L_S) - \omega^2 R_S C_P C_S - Z_r \omega^2 C_P C_S}. \tag{3}$$

It follows that the system resonance condition is

$$\omega = \sqrt{\frac{1}{C_P L_P}} = \sqrt{\frac{1}{C_i L_i}} = \sqrt{\frac{C_S + C_P}{C_S C_P L_S}}. \tag{4}$$

After neglecting parasitic parameters as follows:

$$\begin{cases} Z_{\mathrm{in}} = \frac{\omega^2 C_S L_S - 1}{Z_r \omega^2 C_S C_P} \\ \dot{I}_P = \dot{I}_{\mathrm{in}} = \frac{\dot{U}_{\mathrm{in}}}{Z_{\mathrm{in}}} \end{cases} \tag{5}$$

the system input power is given by

$$P_i = |\dot{I}_P \dot{U}_{\mathrm{in}}| = \frac{|\dot{U}_{\mathrm{in}}|^2}{Z_{\mathrm{in}}}. \tag{6}$$

Summing up, as the load number *n* increases, the system input impedance Z_{in} decreases, whereas the input power P_{in} increases. Conversely, as the load number *n* decreases, Z_{in} increases and P_{in} decreases. Therefore, the change of load may cause the power fluctuation of the multiload WPT system.

B. Dynamic Modeling of the SiC MOSFETs

Before designing any temperature stability control strategy, it is necessary to analyze the dynamic characteristics of SiC MOSFETs in order to estimate the switching losses. The traditional measurement method to estimate losses uses the integrals of switching waveforms measured by an oscilloscope. Such a procedure is very likely to introduce a parasitic inductance, leading to a significant deviation in the integrand function, which is particularly obvious for SiC MOSFETs. In addition, the switching loss measured by this method does not take into account the discharge currents of C_{gd} and C_{ds}, and the displacement current is wrongly regarded as a shutdown loss.

In this article, a specific dynamic modeling for the SiC MOSFET switching process is established. The simplified gate input circuit is shown in Fig. 3, where V_{gs_drive} is the driving voltage, R_{g_in} and R_{g_out} are the grid parasitic and the applied resistances, respectively, I_g is the driving current, C_{gd} and C_{gs} are the gate–drain and the gate–source parasitic capacitances, respectively, I_{gd}, I_{ds}, and I_{gs} are the currents flowing through C_{gd}, $C_{ds,}$ and

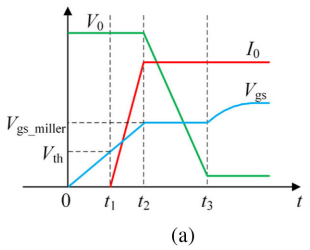


Fig. 4. Waveforms relevant to the SiC MOSFET switching process. (a) Opening process. (b) Closing process.

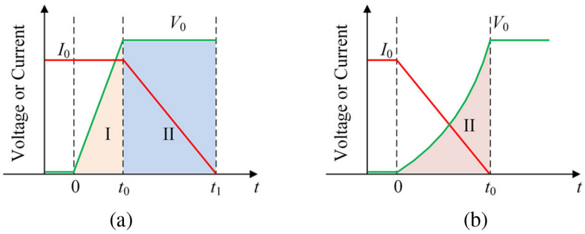


Fig. 5. Current and voltage waveforms when the SiC MOSFET is OFF (a) without the *RC* buffer circuit and (b) with the *RC* buffer circuit.

C_{gs}, respectively, and V_0 is the drain voltage. The square wave V_{gs_drive} is equivalent to the step input excitation, and the gate current is $I_g = I_{gs} + I_{gd}$. It results in the following:

$$\frac{V_{gs\_\text{drive}} - V_{gs}}{R_{g\_\text{out}} + R_{g\_\text{in}}} = C_{gs}\frac{dV_{gs}}{dt} + C_{gd}\frac{dV_{gd}}{dt} \tag{7}$$

where $dV_{gd} = d(V_{gs} - V_{ds}) = dV_{gs}$. From the initial condition $V_{gs} = 0$ V, we have

$$V_{gs} = V_{gs\_\text{drive}}(1 - e^{-t/\tau}). \tag{8}$$

Fig. 4 illustrates the SiC MOSFET switching process. V_{gs_miller} is the Miller platform voltage. The time constant is $\tau = (C_{gs} + C_{gd})(R_{g\_\text{out}} + R_{g\_\text{in}})$. By combining the timeline reported in Fig. 4 with (7), the times in the switching process of the SiC MOSFET are given as

$$t_1 = \tau \ln[V_{gs\_\text{drive}}/(V_{gs\_\text{drive}} - V_{\text{th}})] \tag{9}$$

$$t_2 = \tau \ln[V_{gs\_\text{drive}}/(V_{gs\_\text{drive}} - V_{gs\_\text{miller}})] \tag{10}$$

$$t_3 = Q_{gd} \cdot (R_{g\_\text{out}} + R_{g\_\text{in}})/(V_{gs\_\text{drive}} - V_{gs\_\text{miller}}) \tag{11}$$

$$t_4 = \tau \ln(V_{gs\_\text{drive}}/V_{gs\_\text{miller}}) \tag{12}$$

$$t_5 = Q_{gd} \cdot (R_{g\_\text{out}} + R_{g\_\text{in}})/V_{gs\_\text{miller}} \tag{13}$$

$$t_6 = \tau \ln(V_{gs\_\text{miller}}/V_{\text{th}}) \tag{14}$$

where Q_{gd} is the gate–drain (Miller) charge, which can be obtained from SiC MOSFET's datasheet.

C. SiC MOSFET Switching Loss Analysis

The opening process loss is given by

$$E_{\text{on}} = \int_0^{t_2+t_3} I_0 V_0 dt = I_0 V_0 \cdot (t_2 + t_3)/2. \tag{15}$$

From (9) and (10), E_{on} decreases if V_{gs_driver} increases, and vice versa. The closing process loss is

$$E_{\text{off}} = \int_0^{t_5+t_6} I_0 V_0 dt = I_0 V_0 \cdot (t_5 + t_6)/2. \tag{16}$$

By combining (12) and (13), the aforementioned equation does not explicitly display the relationship between E_{off} and V_{gs_drive}. Further analysis is therefore required, and g_{fs} is the transconductance of the SiC MOSFET. In this article, I_{mos} and V_{mos} represent the current and voltage of the SiC MOSFET, respectively

$$I_{\text{mos}} = g_{fs} V_{gs} \tag{17}$$

$$\begin{cases} dI_{\text{mos}}/dt = [g_{fs}(V_{\text{EE}} - V_{\text{th}}) - I_0]/C_{gs}R_g \\ dV_{\text{mos}}/dt = [I_0 + g_{fs}(V_{\text{th}} - V_{\text{EE}})]/C_{gd}R_g g_{fs}. \end{cases} \tag{18}$$

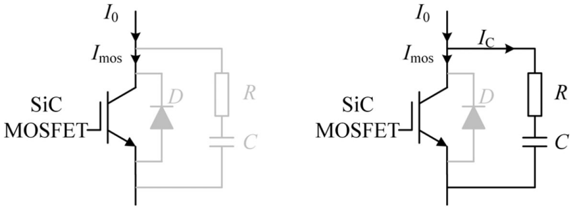
Here, V_{EE} is the shutdown voltage of the SiC MOSFET, and E_{off} by (15) can be rewritten as:

$$E_{\text{off}} = \frac{I_0 V_0}{2}\left(\frac{I_0}{|dI_{\text{mos}}/dt|} + \frac{V_0}{dV_{\text{mos}}/dt}\right). \tag{19}$$

Since $V_{\text{EE}} < 0$, it results in $-V_{\text{EE}} = |V_{\text{EE}}|$. An increase in the switching voltage, which means an increase in $-V_{\text{EE}}$, results in an increase in both dV_{mos}/dt and $|dI_{\text{mos}}/dt|$, so that E_{off} decreases. In summary, the switching loss of the SiC MOSFET decreases as the absolute value of the driving voltage increases and vice versa.

D. Buffer Capacitance and Shutdown Loss Analysis

Fig. 5(a) and (b) displays the loss distribution as a function of time without and with the *RC* buffer circuit connected, respectively. When the buffer circuit is not connected, since the dead zone S_2 is not open, the switch S_1 is OFF (see Fig. 1). As the load current cannot suddenly change, it can only be continued through the diode D_2. However, before the voltage of switch S_1 rises to the bus voltage, the diode cannot be conducted under the reverse voltage drop, so the current flowing through S_1 can only pass through D_2 after its voltage rises to the bus voltage. As shown in Fig. 5(a), t_0 indicates the time when the voltage on switch S_1 rises to the bus voltage V_0, and t_1 is the time when the current on switch S_1 falls to 0. Without the *RC* buffer circuit, the losses are therefore distributed in regions I and II. When the *RC* circuit is connected, the direction of current flow when the switch S_1 is turned ON is shown in Fig. 6(a). The buffer circuit is short circuited, and the current flows through S_1. When S_1 is shutdown, as shown in Fig. 6(b), before the diode D_2 is turned ON, the current I_0 flowing through S_1 can be split through the *RC* buffer circuit. I_0 will immediately decrease, and the switching loss will also be reduced. As shown in Fig. 5(b), no loss occurs in region I; therefore, the *RC* buffer circuit reduces the overall turn-off loss. Moreover, by adding the *RC* buffer circuit, the SiC MOSFET current drop time does not change. The same considerations mentioned above apply to S_3 and S_4 switches.



(a) (b)

Fig. 6. Schematic circuits showing the current flow direction for the SiC MOSFET when adding the *RC* buffer circuit (a) when turned ON and (b) at shutdown.

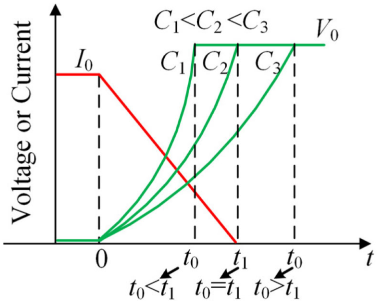


Fig. 7. Shutdown waveforms for different values of the buffer capacitance.

Assuming the current that flows through the buffer circuit to be I_C, the current and voltage of SiC MOSFET are

$$\begin{cases} I_{\text{mos}} = I_0 - I_{\text{C}} = I_0 - I_0 \cdot t/t_1 \\ V_{\text{mos}} = V_{\text{C}} + V_{\text{R}} = (t + 2CR) \cdot I_0 \cdot t/2Ct_1. \end{cases} \tag{20}$$

As shown in Fig. 7, the larger the buffer capacitance, the slower the voltage rises, i.e., the longer the time for the voltage to rise to V_0. If $t_0 < t_1$, the energy loss is given as

$$E_{\text{off}} = \int_0^{t_0} \left(\frac{I_0}{2Ct_1}t^2 + \frac{I_0 R}{t_1}t\right)\left(I_0 - \frac{I_0}{t_1}t\right) dt + \frac{I_0 V_0 (t_1 - t_0)}{2t_1}. \tag{21}$$

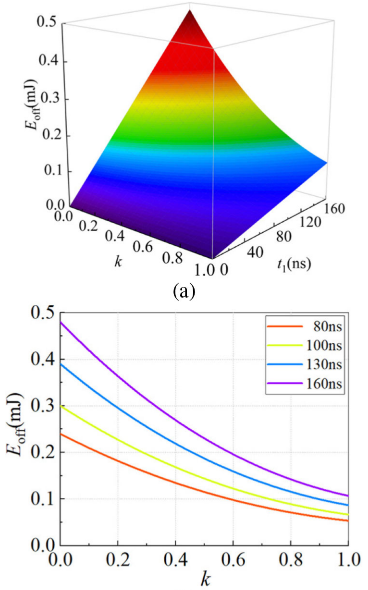
At t_0, V_{mos} has risen to V_0. Combining (20) with (19), and assuming $t_0 = kt_1$ $(0 \leq k \leq 1)$, E_{off} can be expressed as a function of k when $t_0 < t_1$

$$E_{\text{off}} = \frac{I_0}{12}(-8t_1V_0k + 3t_1V_0k^2 + 2Rt_1I_0k^2 - RI_0t_1k^3 + 6V_0t_1). \tag{22}$$

If $t_0 \geq t_1$, then E_{off} is given by

$$E_{\text{off}} = I_0 t_1 \left(\frac{I_0 t_1}{24C} + \frac{I_0 R}{6}\right) t_0 \geq t_1. \tag{23}$$

When $t_0 \geq t_1$, it is easy to note that E_{off} decreases as C increases. If $t_0 < t_1$, the dependence of E_{off} on the circuit parameters can be explained based on the analysis of E_{off} as a function of k and time t_1. A three-dimensional plot of E_{off} versus k and t_1 is displayed in Fig. 8(a), where $I_0 = 20$ A, $V_0 = 300$ V, and $R = 5\ \Omega$. As a matter of fact, each SiC MOSFET has a different t_1. For a specific SiC MOSFET, E_{off} monotonically decreases as k (or C) increases, as illustrated in Fig. 8(b), which shows E_{off} as a function of k for various types of SiC MOSFETs, i.e., different values of t_1.



(a)

(b)

Fig. 8. (a) E_{off} as a function of k and t_1. (b) E_{off} as a function of k for different values of t_1.

In summary, for any SiC MOSFET model, the shutdown loss decreases as the buffer capacitance increases. Compared with the non-*RC* buffer circuit, the SiC MOSFET with the *RC* buffer circuit not only reduces the shutdown loss in zone II, but also eliminates the loss in zone I. Moreover, a variation of the buffer capacitance can regulate the loss in zone II.

E. Switching Loss and Junction Temperature Analysis

In addition to establishing the relationship between circuit parameters (drive voltage and buffer capacitance) and switching losses (E_{on} and E_{off}), it is necessary to establish the relationship between switching losses and junction temperature of SiC MOSFET

$$T_j = P_{\text{loss}}(R_{j-c} + R_{c-a}) + T_a \tag{24}$$

where T_j is the junction temperature of SiC MOSFET. P_{loss} is the power consumption of SiC MOSFET. R_{j-c} is the thermal resistance between the junction and the case. R_{c-a} is the thermal resistance between the case and the ambient. T_a is the ambient temperature.

P_{loss} is dominated by switching losses and conduction losses because the conduction losses are mainly affected by the conduction resistance R_{don} of the SiC MOSFET. Meanwhile, the conduction resistance of SiC MOSFET is low and is less affected by temperature variation. Therefore, the change of switching losses has great influence on the change of the P_{loss}

$$P_{\text{loss}} \approx P_{\text{on}} + P_{\text{off}} = f_{\text{sw}}(E_{\text{on}} + E_{\text{off}})k_{\text{I}}k_{\text{U}} \tag{25}$$

where P_{on} and P_{off} are the turn-ON power loss and turn-OFF power loss, respectively. f_{sw} is the switching frequency. E_{on}

and E_{off} are the turn-ON energy loss and turn-OFF energy loss, respectively. k_I and k_U represent the conversion coefficients of the current and voltage of SiC MOSFET, respectively. The ambient temperature is fixed. Therefore, the following equation can reflect the relationship between junction temperature and energy loss

$$T_j = f_{\text{sw}}(E_{\text{on}} + E_{\text{off}})k_{\text{I}}k_U(R_{j-c} + R_{c-a}) + T_a. \tag{26}$$

Equation (26) reflects the relationship between switching loss and junction temperature of SiC MOSFET. The junction temperature increases with the increase in switching loss and decreases with the decrease of switching loss.

Therefore, in Section III, the relationship between circuit parameters and junction temperature can be obtained, which lays a foundation for subsequent control strategies.

IV. SYSTEM CONTROL STRATEGY AND HARDWARE IMPLEMENTATION

The process of the proposed closed-loop SiC MOSFET junction temperature control strategy is first coarse adjustment and then fine adjustment.

A. Coarse Adjustment Based on SCSM

As described in the previous section, changing the value of the capacitor in the *RC* buffer circuit can reduce and compensate for the SiC MOSFET turn-OFF loss. However, in the practical application, the capacitance value is difficult to be adjusted linearly and continuously. The system designed in this article implements a buffer capacitor bank switching according to input power range. Different ranges of the input power correspond to different capacitance values.

Fig. 9 shows the hardware and processor architectures that implements the SCSM. It is difficult to realize that each power point corresponds to a different capacitance value because adjusting the capacitance value linearly and continuously is difficult. Therefore, this study sets different capacitors corresponding to different power ranges and changes the switch signal in the buffer circuit through the range of the input power. As shown in Fig. 10, the processor collects the input current and voltage of the system to obtain the input power P_{in}. Thereafter, a comparison is made. *m* means that the input power is divided into *m* ranges that correspond to *m* groups of different switching signals. That means, there are *m* different buffer capacitance values. The switch signal $S_w = [T_1, T_2 \cdots T_n]$ is input into the drive circuit of the four buffer capacitor switches at the same time, the parallel number of buffer capacitors is changed, and the synchronous adjustment of the four buffer capacitors is completed.

B. Fine Adjustment Based on CDVM

In this article, a new strategy for junction temperature fine adjustment based on CDVM is proposed. It consists in controlling the junction temperature by changing the MOSFET opening and closing voltages. When the junction temperature rises, the absolute value of the opening and closing voltages is increased in order to reduce the switching loss, which in turn can low down the junction temperature. Conversely, as the junction temperature decreases, the absolute value of the opening and closing voltages is reduced to increase the switching loss, which in turn will increase the junction temperature.

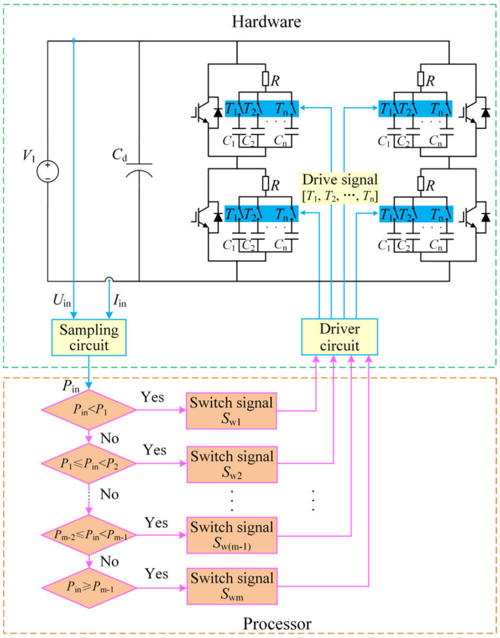


Fig. 9. Schematic diagram of coarse adjustment control strategy based on the SCSM.

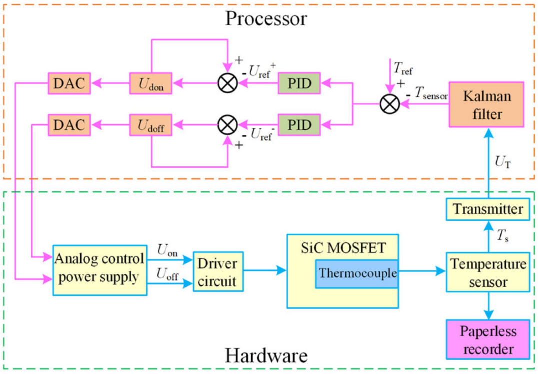


Fig. 10. Schematic diagram of the closed-loop junction temperature fine adjustment control strategy based on the CDVM.

It is worth to point out that a temperature collection module that collects the temperature recordings is necessary, no matter what kind of junction temperature adjustment method is used. For the junction temperature estimation, several methods are currently available.

1) Direct measurement, such as infrared technology [34], [35], which has high precision and relatively simple operation. The main disadvantage of this technique is the need to open the module, which is not convenient for online application, is easy to affect the normal operation of the device, and cannot be used to measure the metal surface. Moreover, the required measurement equipment is expensive.

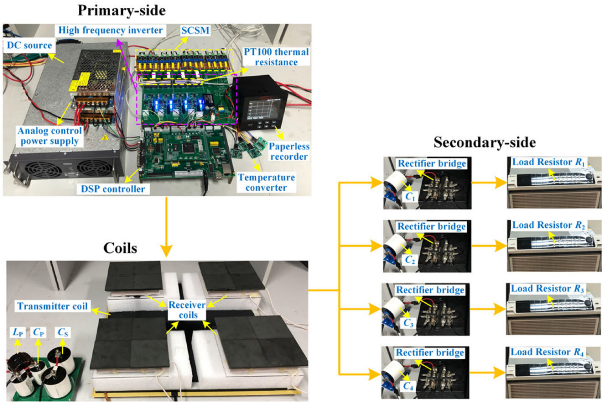


Fig. 11. Experimental prototypes.

2) Indirect measurement, e.g., by thermocouples or thermistors [36], which is a high accuracy noninvasive online measurement method. However, this strategy requires prior calibration.

3) Junction temperature calculation [37] by means of electrothermal modeling or finite-element analysis, which is, of course, a noncontact measurement method. However, the calculated parameters will change with the aging time, and the calculation error is large.

In summary, by considering costs, convenience, and accuracy, the indirect measurement method is adopted in this article

Fig. 10 shows the hardware and processor architectures implementing the junction temperature fine adjustment method based on the CDVM. The SiC MOSFET junction temperature T_s is collected through a real-time paperless recorder and is converted to the voltage U_T through the temperature transmitter to the primary-side DSP controller. In order to reduce noise and interference in measuring junction temperature signals, a Kalman filter is implemented. The obtained temperature T_{sensor} is compared with the target temperature T_{ref}, and two PID operations are then performed. The results of PID operations are limited within the SiC MOSFET opening and closing voltage range $U_{\text{ref}+}$ and $U_{\text{ref}-}$. U_{don} and U_{doff} are the driving voltages corresponding to the digital output from the processor and are fed to the DAC module, which has no driving capability. By feeding the analog signal to the analog control power supply module, the driving signals U_{on} and U_{off}, i.e., the actual opening and closing voltages, are finally obtained, thereby achieving the SiC MOSFET driving voltage real-time adjustment.

V. EXPERIMENTAL VERIFICATION

A. Experimental Prototype

In order to verify the feasibility and the effectiveness of the proposed junction temperature closed-loop control method, a 5-kW experimental prototype was realized, as shown in Fig. 11. The prototype mainly includes a dc source, a high-frequency inverter, a transmitter coil, and four receiver coils with their own load circuit in secondary side. The high-frequency inverter uses SiC power MOSFETs (IXFN50N120SiC), and the specific experimental parameters are listed in Table I.

TABLE I
PARAMETERS OF THE EXPERIMENTAL WPT SYSTEM PROTOTYPE

Symbol	Purpose	Value
L_1	Primary compensating inductor	20μH
C_1	Primary compensating capacitor	175.3nF
L_P	Transmitter coil self-induction	103.5μH
C_P	Transmitter coil compensating capacitor	41.99nF
R_1	Transmitter coil ESR	0.12Ω
f	Resonant frequency	85kHz
L_i	Receiver coil self-induction	28.06μH
C_i	Receiver coil compensating capacitor	125nF
M_i	Mutual inductance	8.1μH
R_i	Load resistors	0Ω~100Ω
V_{in}	Input DC voltage	250V
V_i	Voltage of load resistor	110V
T_a	Ambient temperature	25°C

ESR: Equivalent series resistance.

TABLE II
POWER FLUCTUATION SEQUENCE

Sequence	Input power	Input current
1	3600W	14.4A
2	5000W	20A
3	2200W	9.2A
4	3000W	12A
5	5000W	20A
6	2300W	9.2A
7	3000W	12A

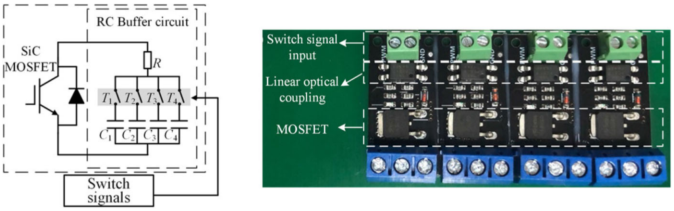


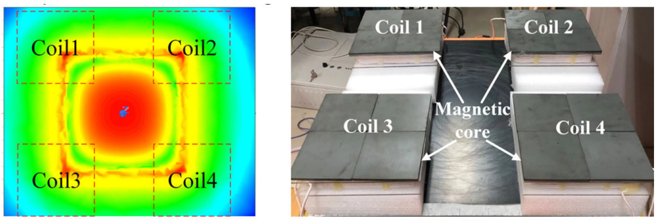
Fig. 12. Schematic of the *RC* buffer circuit and optical photograph, with indication of the main components.

B. Hardware Design and the Experimental Analysis

The LCC-S multiload WPT system has the characteristic of constant pressure for the receiving coil. The load resistance used in this study is the electronic load (Chroma_63200A), which is a programmable electronic load. The combination and switching of different loads can be realized by programming. Four electronic loads are used in this study. By adjusting the load resistance and the amount of load, the input power P_{in} of the system is changed to simulate the power fluctuation problem in the practical multiload wireless charging system. The sequence of power fluctuations is shown in Table II.

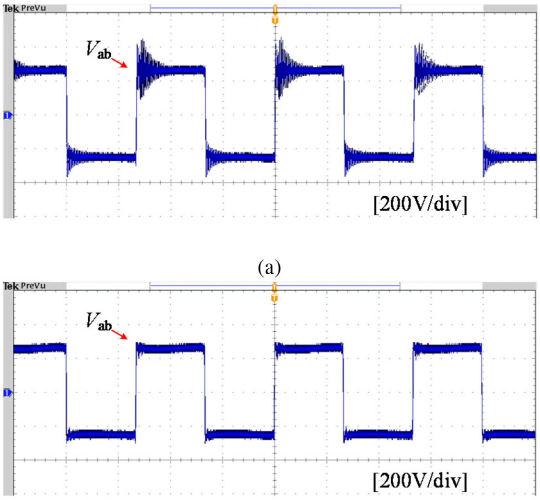
1) Shunt Capacitor Bank Switching Method: The value of the buffer capacitance can be adjusted by increasing or decreasing the number of shunt capacitors by adding switches in the buffer capacitor branch, as shown in Fig. 12. A STB24NM60N MOSFET (600 V/17 A) is used as a switch. The switching signal is fed after judging the range of input power.

In the multiload experiment, in order to ensure that the self-induction of each transmitter coil is the same as the receiver coil, an electromagnetic simulation by using ANSYS Maxwell



(a) (b)

Fig. 13. (a) Simulation of the magnetic field of the transmitter coil. (b) Optical photograph of the transmitter and receiver coils.



(b)

Fig. 14. (a) The output voltage of the inverter when $C < 25$ nF. (b) The output voltage of the inverter when $25 \text{ nF} \leq C \leq 140$ nF.

tool is first performed, in order to find the equivalent position of the magnetic field for placing the receiver coil. The simulation results are shown in Fig. 13(a). The red dashed line is the position of the receiver coils, which are placed at the four corners of the transmitter coil. An optical photograph of the system is shown in Fig. 13(b).

After testing, the output voltage of the rectifier bridge is 110 V. Section III deduces the relationship between the buffer capacitor C and E_{off}. E_{off} decreases with the increase in the buffer capacitor, whereas the limit of the buffer capacitor in practical application needs to be limited. On the one hand, the buffer capacitance is too small to suppress the voltage oscillation on the device caused by high frequency, as shown in Fig. 14(a). On the other hand, excessive buffer capacitance leads to severe heating of the resistance of the buffer circuit, which requires additional cooling design, thus undoubtedly increasing the volume and cost of the system. Therefore, after testing, when the buffer capacitance is less than 25 nF, oscillation becomes evident, as shown in Fig. 14(a). When the buffer capacitance is at [25 nF,140 nF], the oscillation suppression effect is better, as shown in Fig. 14(b). Therefore, different input power intervals in this article correspond to different buffer capacitances, as shown in Table III. According to the sequence presented in Table II, the value of the buffer capacitor is set to 99, 132, 33, 66, 132, 33, and 66 nF.

TABLE III
LOAD SWITCHING SEQUENCE

Input power P_{in}	Buffer capacitance
P_{in}<2500W	33nF
2500W≤P_{in} <3500W	66nF
3500W≤P_{in} <4500W	99nF
P_{in}≤4500W	132nF

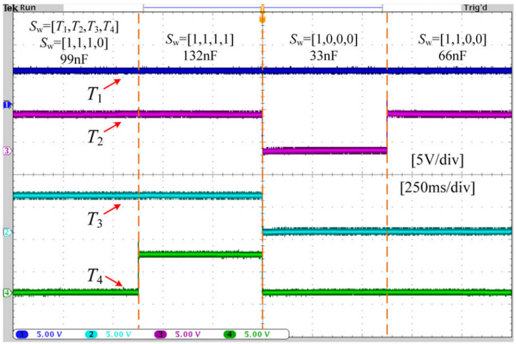
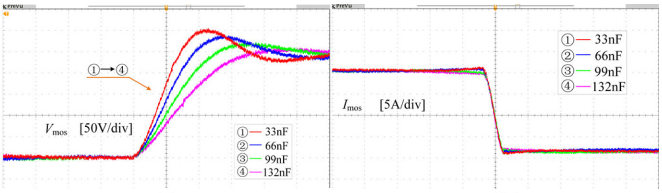


Fig. 15. The switching signal S_w in the buffer circuit.



(a) (b)

Fig. 16. (a) Turn-OFF voltage waveform of SiC MOSFET with different buffer capacitances. (b) Turn-OFF current waveform of SiC MOSFET with different buffer capacitances.

The switching signals $S_w = [T_1, T_2, T_3, T_4]$ in the buffer circuit is tested by programming the electronic loads and setting the conversion time of the input power. As shown in Fig. 15, the sequence is 99, 132, 33, and 66 nF.

In this study, the current and voltage waveforms of SiC MOSFET with different buffer capacitances are tested. As shown in Fig. 16(b), the addition of the buffer circuit decreases the current of SiC MOSFET rapidly. The higher the capacitance is, the lower the rising slope of the turn-OFF voltage is, as shown in Fig. 16(a). The conclusion presented in Section III has been verified. However, different buffer capacitors do not affect the descending slope of the turn-OFF current.

In this study, the output voltage V_{ab} and current I_{ab} of the inverter are also tested when the buffer capacitance is switched, as shown in Fig. 17. The waveform of V_{ab} and I_{ab} can not only represent the voltage and current across a single SiC MOSFET, but also observe the overall output quality of the high-frequency inverter. For the convenience of observation, two fixed switching times of the electronic load are set here to simulate different input powers and to observe the switching signals in the buffer circuit and the output of the inverter. Since the input voltage of the system is constant, the change of input power can be expressed

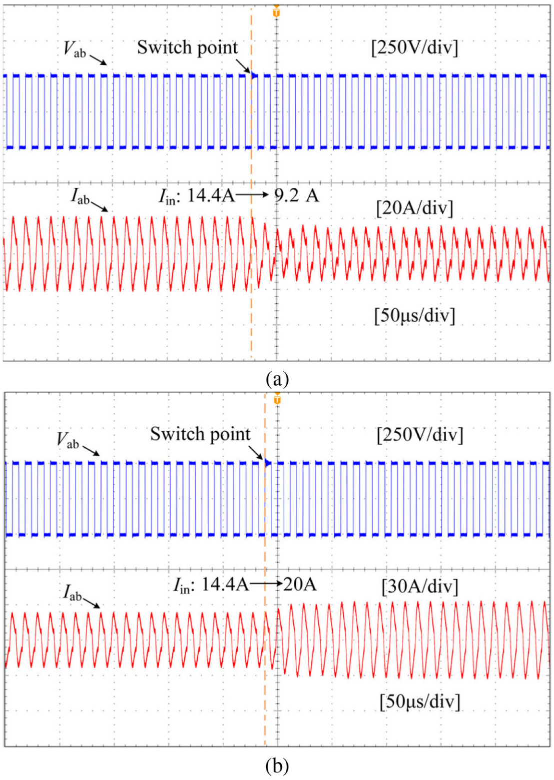


Fig. 17. Output voltage and current waveform of the high-frequency inverter. (a) I_{in} is transformed from 14.4 to 9.2 A. (b) I_{in} is transformed from 14.4 to 20 A.

by the input current I_{in}. Fig. 17(a) shows output voltage and current of the inverter when the input current is transformed from 14.4 to 9.2 A. Fig. 17(b) shows output voltage and current of the inverter when the input current is transformed from 14.4 to 20 A. A slight voltage wobble can be found only at the moment of switching. This slight jitter has little effect on the system because the buffer capacitance needs not be changed frequently. Therefore, the proposed SCSM does not sacrifice the output quality of the high-frequency inverter and is suitable for MCR-WPT system extremely.

2) Changing Driving Voltage Method: As discussed above, Fig. 10 illustrates the junction temperature fine adjustment method proposed in this article. The real-time junction temperature of each SiC MOSFET is collected. The time constant of the thermal resistance *RC* found by datasheet is ms level. A good mapping relationship between junction temperature and case temperature is found, which means that the case temperature can be effectively used to track the junction temperature. In this article, a PT100 sensor is used to measure the temperature of each SiC MOSFET. The real-time temperature is recorded by the paperless recorder and transmitted to the processor after being converted into the voltage signal U_T by the temperature transmitter. In this article, we focus on the suppression of the junction temperature fluctuation caused by power fluctuations. By setting the system target temperature T_{ref} to 66 °C at the input current of 14.4 A, the SiC MOSFET opening voltage is limited from +12 to +22 V, and the shutdown voltage is limited from −6 to −1 V.

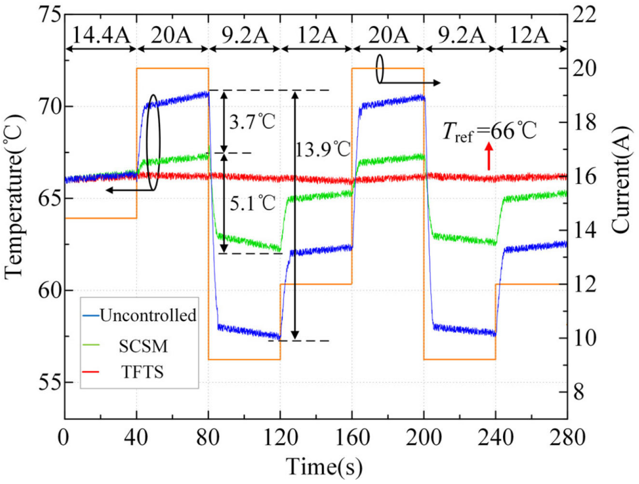


Fig. 18. Junction temperature fluctuation under different control strategies.

3) Experimental Results: The sequence of power fluctuations is shown in Table II, each different load combination causes the system input power to fluctuate. As a result, the input current fluctuates in order of 14.4, 20, 9.2, 12, 20, 9.2, and 12 A. The resulting current fluctuation is shown by the two-way horizontal arrows in Fig. 18. The target temperature T_{ref} at 14.4 A is set to 66 °C. That is, the rated power is set as 3600 W, and the rated current is set as 14.4 A in this study. The blue line in Fig. 18 represents the case without any junction temperature stability control strategy. The junction temperature fluctuates randomly as the load changes, and the maximum junction temperature difference reaches 13.9 °C. The green line is the result of the proposed SCSM, i.e., the coarse junction temperature adjustment. It can be clearly observed that the junction temperature still fluctuates significantly, and the maximum junction temperature fluctuation reaches 5.1 °C. However, due to the open-loop control, at each time period, the temperature shows continuous rising or falling, and the overall temperature trend is not smooth. The junction temperature fluctuation suppress effect is therefore not ideal. The red line is the result of the TFTS strategy proposed in this article. Under the same conditions, the fluctuation of the junction temperature can be stabilized around the set target temperature of 66 °C. The maximum junction temperature fluctuation of 13.9 °C is completely eliminated, and the maximum junction temperature adjustment ability is increased by 63.3%, compared with using only the coarse method. Indeed, when the power fluctuation is 36.1% of the rated power (3600 W/14.4 A), or less, the junction temperature fluctuation can be adjusted to be completely stable. The junction temperature fluctuation suppress effect is therefore obvious. Moreover, the final temperature error after full adjustment is less than 0.3 °C, which can effectively reduce the thermal stress shock of the SiC MOSFET.

To verify the ability of this method to adjust four SiC MOSFETs (S_1, S_2, S_3, and S_4) thermal loads independently, four reference temperatures are set (66 °C, 65 °C, 64 °C, and 63 °C). The results are shown in Fig. 19, which indicates that the proposed TFTS strategy has excellent independent regulation ability. The error is less than 0.3 °C.

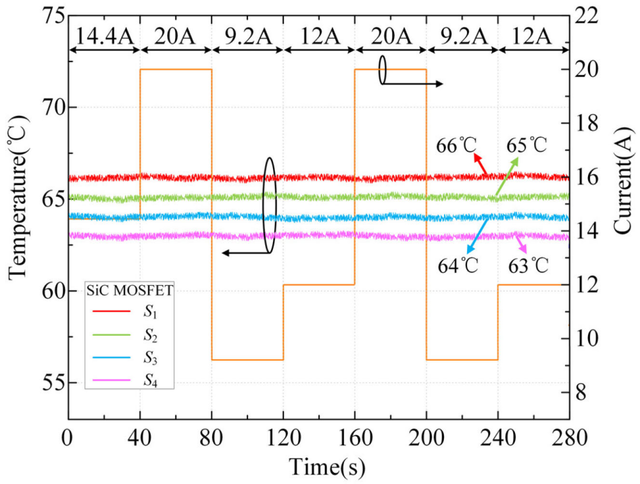


Fig. 19. Junction temperature fluctuation on different SiC MOSFETs.

VI. CONCLUSION

In this article, a novel and active temperature control method is proposed to suppress high-frequency inverter SiC MOSFET junction temperature fluctuations caused by power fluctuations in the high-power electric vehicle WPT system. The developed strategy implements the SiC MOSFET junction TFTS by means of both a coarse and a fine adjustment stages. The SCSM and the CDVM are proposed respectively for these two adjustment stages in the TFTS strategy. As for the former, the SCSM is proposed for junction temperature coarse adjustment. A junction temperature fine adjustment method based on the CDVM is proposed to compensate for the limited adjustment range and the low accuracy of the coarse adjustment method alone. The combination and complementarity of these two methods not only expands the regulation range and makes the control system more stable but also individually adjusts the junction temperature of each SiC MOSFET flexibly. By means of the developed temperature stability control method, the maximum 13.9 °C junction temperature fluctuation observed during validation tests is completely eliminated. The maximum temperature error after adjustment is less than 0.3 °C. Further studies will be needed to find out the practical use of the proposed TFTS strategy in the junction temperature and loss compensation ranges of SiC MOSFETs in electric vehicle wireless charging systems.

REFERENCES

[1] O. C. Onar, M. Chinthavali, S. L. Campbell, L. E. Seiber, and C. P. White, “Vehicular integration of wireless power transfer systems and hardware interoperability case studies,” *IEEE Trans. Ind. Appl.*, vol. 55, no. 5, pp. 5223–5234, Sep. 2019.

[2] X. Li, Y.-P. Li, C.-Y. Tsui, and W.-H. Ki, “Wireless power transfer system with $\Sigma\Delta$-modulated transmission power and fast load response for implantable medical devices,” *IEEE Trans. Circuits Syst. II, Express Brief*, vol. 64, no. 3, pp. 279–283, Mar. 2017.

[3] B. Sim *et al.*, “Core-shared-repeater (CSR) coil scheme for low EMI and efficient WPT system in ultra-thin digital TV,” in *Proc. IEEE Wireless Power Transfer Conf.*, Montreal, QC, Canada, 2018, pp. 1–4.

[4] Z. Yan *et al.*, “Frequency optimization of a loosely coupled underwater wireless power transfer system considering eddy current loss,” *IEEE Trans. Ind. Electron.*, vol. 66, no. 5, pp. 3468–3476, May 2019.

[5] X. Ye, X. Zong, and Z. Nie, “A novel adaptive focusing for wireless energy transfer to mobile devices in complex environment,” in *Proc. IEEE Int. Conf. Comput. Electromagn.*, Shanghai, China, 2019, pp. 1–3.

[6] Y. Jiang, L. Wang, Y. Wang, J. Liu, M. Wu, and G. Ning, “Analysis, design, and implementation of WPT system for EV’S battery charging based on optimal operation frequency range,” *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6890–6905, Jul. 2019.

[7] A. Zakerian, S. Vaez-Zadeh, and A. Babaki, “A dynamic WPT system with high efficiency and high power factor for electric vehicles,” *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 6732–6740, Jul. 2020.

[8] D. J. Perreault *et al.*, “Opportunities and challenges in very high frequency power conversion,” in *Proc. 24th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2009, pp. 1–14.

[9] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, “A survey of wide bandgap power semiconductor devices,” *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[10] S. Li, L. Wang, Y. Guo, and C. Tao, “Optimization of T-type compensation network for a certain power fluctuation tolerance of the dynamic wireless power transmission,” in *Proc. IEEE 4th Southern Power Electron. Conf.*, 2018, pp. 1–5.

[11] J. A. Anderson, C. Gammeter, L. Schrittwieser, and J. W. Kolar, “Accurate calorimetric switching loss measurement for 900 V 10 m Ω SiC MOSFETs,” *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 8963–8968, Dec. 2017.

[12] B. Hu *et al.*, “Failure and reliability analysis of a SiC power module based on stress comparison to a Si device,” *IEEE Trans. Device Mater. Rel.*, vol. 17, no. 4, pp. 727–737, Dec. 2017.

[13] M. Ciappa, “Selected failure mechanisms of modern power modules,” *Microelectron. Rel.*, vol. 42, no. 4/5, pp. 653–667, Apr. 2002.

[14] C. Herold, M. Schaefer, F. Sauerland, T. Poller, J. Lutz and O. Schilling, “Power cycling capability of modules with SiC-diodes,” in *Proc. 8th Int. Conf. Integr. Power Electron. Syst.*, Nuremberg, Germany, 2014, pp. 1–6.

[15] S. Liebig and J. Lutz, “Efficiency and lifetime of an active power filter with SiC-MOSFETs for aerospace application,” in *Proc. Eur. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, Nuremberg, Germany, 2014, pp. 1–9.

[16] S. Liebig, A. Engler, and J. Lutz, “Design and evaluation of state of the art rectifiers dedicated for a 46 kW E-ECS aerospace application with respect to power density and reliability,” in *Proc. 14th Eur. Conf. Power Electron. Appl.*, 2011, pp. 1–10.

[17] W. W. Lee, L. T. Nguyen, and G. S. Selvaduray, “Solder joint fatigue models: review and applicability to chip scale packages,” *Microelectron. Rel.*, vol. 40, no. 2, pp. 231–244, Feb. 2000.

[18] I. Kim and S. Lee, “Reliability and failure analysis of lead-free solder joints for PBGA package under a cyclic bending load,” *IEEE Trans. Compon. Packag. Technol.*, vol. 31, no. 2, pp. 478–484, Jun. 2008.

[19] F. P. McCluskey, M. Dash, Z. Wang, and D. Huff, “Reliability of high temperature solder alternatives,” *Microelectron. Rel.*, vol. 46, no. 9/11, pp. 1910–1914, Sep. 2006.

[20] J. A. Dicarlo, “Creep of chemically vapour deposited SiC fibres,” *J. Mater. Sci.*, vol. 21, no. 1, pp. 217–224, Jan. 1986.

[21] S. Zhu, M. Mizuno, Y. Kagawa, J. Cao, Y. Nagano, and H. Kaya, “Creep and fatigue behavior of SiC fiber reinforced SiC composite at high temperatures,” *Mater. Sci. Eng., A*, vol. 225, no. 1/2, pp. 69–77, Apr. 1997.

[22] L. A. Navarro *et al.*, “Thermomechanical assessment of die-attach materials for wide bandgap semiconductor devices and harsh environment applications,” *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2261–2271, May 2014.

[23] T. Herrmann, M. Feller, J. Lutz, R. Bayerer, and T. Licht, “Power cycling induced failure mechanisms in solder layers,” in *Proc. Eur. Conf. Power Electron. Appl.*, Aalborg, Denmark, 2007, pp. 1–7.

[24] F. Blaabjerg, K. Ma, and D. Zhou, “Power electronics and reliability in renewable energy systems,” in *Proc. IEEE Int. Symp. Ind. Electron.*, Hangzhou, China, May 2012, pp. 19–30.

[25] R. Bayerer, T. Herrmann, T. Licht, J. Lutz, and M. Feller, “Model for power cycling lifetime of IGBT modules—Various factors influencing lifetime,” in *Proc. 5th Int. Conf. Integr. Power Electron. Syst.*, Nuremberg, Germany, 2008, pp. 1–6.

[26] H. Liu *et al.*, “Dynamic wireless charging for inspection robots based on decentralized energy pickup structure,” *IEEE Trans. Ind. Inf.*, vol. 14, no. 4, pp. 1786–1797, Apr. 2018.

[27] A. Saleki, M. Changizian, S. Rezazade, and M. T. Bina, “Lifetime extension by varying switching frequency of inverters based on junction temperature estimation,” in *Proc. 9th Annu. Power Electron., Drives Syst. Technol. Conf.*, Tehran, Iran, 2018, pp. 259–264.

[28] T. A. Polom and B. Wang, “Control of junction temperature and its rate of change at thermal boundaries via precise loss manipulation,” *IEEE Trans. Ind. Appl.*, vol. 53, no. 5, pp. 4796–4806, Sep. 2017.

[29] M. Ouhab, Z. Khatir, A. Ibrahim, J.-P. Ousten, R. Mitova, and M.-X. Wang, “New analytical model for real-time junction temperature estimation of multichip power module used in a motor drive,” *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5292–5301, Jun. 2018.

[30] K. Ma, M. Liserre, and F. Blaabjerg, “Reactive power influence on the thermal cycling of multi-MW wind power inverter,” *IEEE Trans. Ind. Appl.*, vol. 49, no. 2, pp. 922–930, Mar. 2013.

[31] P. Zanchetta, S. Bifaretti, J. Clare, A. Watson, A. Bellini, and L. Tarisciotti, “Distributed commutations pulse-width modulation technique for high-power AC/DC multi-level converters,” *IET Power Electron.*, vol. 5, no. 6, pp. 909–919, Jul. 2012.

[32] H. Wang, A. M. Khambadkone, and X. Yu, “Control of parallel connected power converters for low voltage microgrid—Part II: Dynamic electrothermal modeling,” *IEEE Trans. Power Electron.*, vol. 25, no. 12, pp. 2971–2980, Dec. 2010.

[33] J.-C. Wang, Y.-L. Su, K.-C. Kuo, J.-C. Shieh, and J.-A. Jiang, “A novel multipoint direct-estimation method for the maximum power point tracking of photovoltaic modules under partially shaded irradiation conditions,” in *Proc. IEEE Int. Energy Conf. Exhib.*, Florence, Italy, 2012, pp. 13–19.

[34] N. Baker, L. Dupont, S. Munk-Nielsen, and M. Liserre, “IR camera validation of IGBT junction temperature measurement via peak gate current,” *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 3099–3111, Apr. 2017.

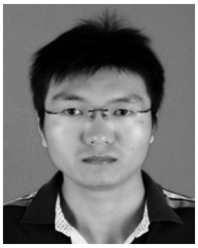
[35] B. Shi, S. Feng, L. Shi, and H. Zhu, “Junction temperature measurement method for power MOSFETs using turn-on delay of impulse signal,” *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5274–5282, Jun. 2018.

[36] K. Wei, D. D.-C. Lu, C. Zhang, Y. P. Siwakoti, J. L. Soon, and Q. Yao, “Modeling and analysis of thermal resistances and thermal coupling between power devices,” *IEEE Trans. Electron Devices*, vol. 66, no. 10, pp. 4302–4308, Oct. 2019.

[37] R. Kibushi, T. Hatakeyama, S. Nakagawa, and M. Ishizuka, “Calculation of temperature distribution of power Si MOSFET with electro-thermal analysis the effect of boundary condition,” in *Proc. Int. Conf. Electron. Packag.*, Toyama, Japan, 2014, pp. 567–571.

Ruoyin Wang (Student Member, IEEE) was born in Zhenjiang, Jiangsu, China, in 1991. He received the M.S. degree in electrical engineering from Jiangsu University, Jiangsu, China, in 2018. He is currently working toward the Ph.D. degree in electrical engineering with Southeast University, Nanjing, China.

His research interests include wireless power transfer, wide bandgap power devices, coil positioning, and temperature control technology.



Linlin Tan received the B.S. degree in electrical engineering and automation from Harbin Engineering University, Harbin, China, in 2008, and the Ph.D. degree in electrical engineering from Southeast University, Nanjing, China, in 2014.

He is currently an Associate Professor with the School of Electrical Engineering, Southeast University. He has authored more than 20 papers. His interests include wireless power transfer, wireless charging for electric vehicle, and wireless vehicle-to-grid.

Chengyun Li (Student Member, IEEE) was born in Shandong, China, in 1997. He received the B.S. degree in electrical engineering in 2019 from Southeast University, Nanjing, China, where he is currently working toward the M.S. degree in electrical engineering.

His research interests include wireless power transfer, coil positioning technology, and high-efficiency power technology.

Tianyi Huang (Student Member, IEEE) was born in Jiangsu, China, in 1997. He received the B.S. degree in electrical automatization from the Nanjing Institute of Technology, Nanjing, China, in 2018. He is currently working toward the M.S. degree in electrical automatization with Southeast University, Nanjing, China.

His research interests include wireless power transfer and advanced power semiconductors.

Haoze Li (Student Member, IEEE) was born in Jiangsu, China, in 1997. He received the B.S. degree in electrical engineering and automatic chemistry from Jiangsu University, Zhenjiang, China, in 2019. He is currently working toward the M.S. degree in electrical engineering with Southeast University, Nanjing, China.

His research interests include wireless power transfer and high-frequency and high-power electronic conversion devices.

Xueliang Huang (Member, IEEE) was born in Zhoushan, Zhejiang, China, in 1969. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Southeast University, Nanjing, China, in 1991, 1994, and 1997, respectively.

From 2002 to 2004, he was a Postdoctoral Researcher with the University of Tokyo. Since 2004, he has been a Professor with the Electrical Engineering Department, Southeast University. He has authored four books, more than 150 articles, and more than 40 inventions. He holds one PCT patent. His research interests include novel wireless power transfer systems, analysis of electromagnetic field, applied electromagnetics, intelligent electricity technology, etc.

Prof. Huang is an Editor for the *Journal Transactions of China Electrotechnical Society*.