Adaptive Hysteresis Current Based ZVS Modulation and Voltage Gain Compensation for High-Frequency Three-Phase Converters

Boran Fan, *Member, IEEE*, Qiong Wang, *Member, IEEE*, Rolando Burgos, *Member, IEEE*, Agirman Ismail, and Dushan Boroyevich, *Life Fellow, IEEE*

***Abstract*—This article proposed a systematic approach for the control of three-phase bidirectional zero-voltage switching (ZVS) converters. Combining the adaptive hysteresis-band current control and turn-ON delay modifications, ZVS conditions are realized in full line-cycle in all loading conditions like active power, reactive power, light load, and heavy load. The soft-switching resonant period is carefully analyzed, and the current band is designed accordingly, which minimized the additional conduction loss. Meanwhile, a zero-sequence voltage injection control is included in the approach, which compensates the voltage gain by 15% and narrows down the switching frequency variation range. The hardware design approach is also provided including the *LCL* filter design and a low-cost high-bandwidth high-accuracy current sensor design. A highly integrated 5-kW silicon carbide implemented three-phase ZVS converter prototype with printed circuit board integrated inductors and customized current sensors is designed. All the control is implemented in a single microcontroller unit, which achieves a high electromagnetic compatibility. The designed prototype achieves a total power density of 5.5 kW/L and a peak efficiency of 98.5%. All the analysis and the proposed control approach are experimentally verified on the designed prototype.**

***Index Terms*—Critical conduction mode (CRM), current sensor, hysteresis current control, silicon carbide (SiC), soft switching, three-phase bidirectional ac–dc converter, variable switching frequency.**

I. Introduction

In THE recent decade, power electronics technology took a big step forward thanks to the developments on wide-bandgap (WBG) semiconductor devices. Due to the highly improved figure-of-merit, WBG devices like silicon carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs) and gallium nitride high-electron mobility transistors can operate at much higher switching frequency than Si counterparts, which benefits the size reduction of passive filter components. However, the turn-ON loss is still significant for several hundred kilohertz switching [1], [2]. In order to further reduce the switching loss, the zero-voltage switching (ZVS) technique [3] that eliminates turn-ON loss of semiconductor devices is preferred. For single-phase ac–dc applications, critical conduction mode (CRM) [4], also referred as triangular current mode [5], is widely adopted to achieve ZVS due to its simplicity. Liu *et al.* [4] demonstrated a ZVS GaN-based totem-pole power factor correction (PFC) rectifier power converter that operates in MHz range with 99% peak efficiency.

For higher power applications like motor driver, on-board charger, or PV inverters, three-phase instead of single-phase implementations are preferred. In bidirectional three-phase ac–dc applications, ZVS could be achieved with [6] or without [7]–[9] auxiliary circuits. Like in single-phase applications, the CRM technique that eliminates auxiliary circuits gains more interest.

Fig. 1 shows three-phase two-level converters with *LCL* filter at the ac side. In applications of active front-end (AFE) converters, L_s is the grid-side inductor and v_{ga}, v_{gb}, and v_{gc} are the grid voltages. In applications of motor drives, L_s is the motor leakage inductance and v_{ga}, v_{gb}, and v_{gc} are the motor back electromotive force. Three topologies are considered here: Topology 1 when SN12 and SN23 are OFF, Topology 2 when SN12 and SN23 are ON, and Topology 3 when SN12 is ON and SN23 is OFF.

Huang *et al.* [9] and Haryani *et al.* [10] demonstrated the three-phase ZVS operation using Topology 1. Since when SN12

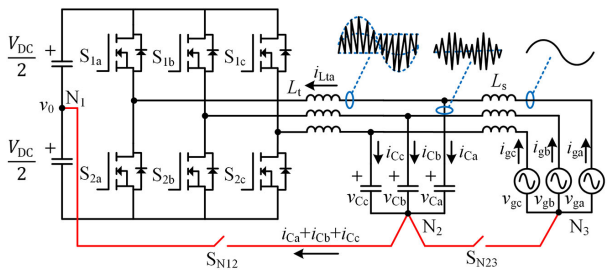

Fig. 1. ZVS three-phase two-level converters. Topology 1: SN12 OFF and SN23 OFF. Topology 2: SN12 ON and SN23 ON. Topology 3: SN12 ON and SN23 OFF.

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and SN23 are off, only two phases among the three are independent. The current ripple in each of the phases is influenced by all the three-phase switching actions, therefore CRM operations cannot be used separately for three phases. A modulation approach combining the CRM, discontinuous conduction mode (DCM), and clamping mode was proposed in [9] and [10]. The combination rotates alternatively among three phases in every 30° in a line-cycle and the switching pattern is calculated based on the inductor current zero-crossing instant. Due to the use of DCM, the four devices in the CRM and DCM phase-legs are all in OFF-state in the soft-switching resonant period. Therefore the control approach has to deal with a complicated fourth-order system consisting of two phase inductors (L_t) and two device junction capacitors [9]. In [11] and [12], a more implementation-friendly approach was proposed for Topology 1 based on the three-phase five-segment space vector pulsewidth modulation (PWM). The DCM in the modulation combination was replaced by the over-ZVS mode and the soft-switching period resonance is determined by a second-order system instead of a fourth-order system. Meanwhile, a current ripple prediction [13] based ZVS operation was introduced and there is no need for current zero-crossing detection (ZCD) circuit. The ZVS operation is achieved by keeping the switching frequency below the boundary switching frequency [11], [12]. A parallel interleave was also investigated, which demonstrated an effectively reduced current ripple [14]. However, replacing the DCM with over-ZVS mode is at the cost of additional conduction loss. In the above two control approaches, the ZVS realization of a certain phase-leg is always influenced by the other two phase-legs and special designs are required for different loading conditions, like with or without reactive power [15], [16].

One way to overcome this is to decouple three phases by splitting capacitors at the dc link and connecting the dc-side midpoint (N1) to the ac-side neutral points (N2 and N3), as shown in Fig. 1 Topology 2, which is reported in the literature [8], [17], [18]. With the decoupling, CRM can be realized independently on three phases and in the ZVS soft-switching period, the fourth-order circuit in Topology 1 is simplified as a second-order circuit even if DCM is used. A 400-W three-phase microinverter was demonstrated with a peak efficiency of 98.4% in [8].

Hysteresis-band instantaneous current control technique is widely adopted due to its simplicity of implementation, fast response, and inherent peak limiting capability [19], [20]. It has also been proved that hysteresis-band approach can bring convenience on ZVS modulations [16]. Different current band designs were discussed for Topology 2, which results in different switching frequency variation and system efficiency [17]. However, in these works, the resonance between inductor L_t and device junction capacitance happened in the ZVS soft-switching period was simplified as a first-order system. Since the inductance value L_t can be designed to be very small for a couple hundred kilohertz switching, neglecting the resonance between L_t and the device junction capacitance in the switching period will result in losing ZVS conditions. In addition, the *LCL* filter design, which heavily affects the system efficiency, was not fully discussed in the previous work.

TABLE I
TOPOLOGY COMPARISONS FOR ZVS OPERATIONS

	Topology1		Topology2	Topology3
(SN12, SN23)	(0, 0)		(1, 1)	(1, 0)
ac-side neutral point	Not required		Required	Not required
ZVS resonant period	4th order circuit	2nd order circuit	2nd order circuit	2nd order circuit
Modulation combination	Clamp +CRM +DCM [9], [10]	Clamp +CRM+ OverZVS [11], [12]	CRM +DCM*	CRM +DCM*
Modulation ratio	<1		<0.866	<1

*DCM is optional

One disadvantage of Topology 2 is that a neural point is required at the ac side, which is not always accessible. The other disadvantage comes from the modulation ratio/voltage gain limitation. Owning to the pseudo-single-phase operation, the phase-to-neutral voltage magnitude at the ac side must be smaller than half of the dc-link voltage, therefore the modulation ratio is limited to 0.866. In this article, points N2 and N3 in Fig. 1 are further split (Topology 3) and a zero-sequence voltage is injected between points N2 and N3 [23], which boost the modulation ratio by 15%. Meanwhile, CRM can still be realized independently among three phases. It is worth mentioning that DCM is also optional for Topologies 2 and 3, which helps with improving efficiency especially at light load conditions, but the clamping mode is not feasible for Topologies 2 and 3 because the ac capacitors limit any instant zero-sequence voltage jump. The topology comparisons are summarized in Table I.

The objective of this article is to propose a hysteresis current based approach for the control of a three-phase bidirectional ZVS converter (Topology 3 in Fig. 1). The ZVS should be realized in full line-cycle in all loading conditions like active power, reactive power, light load and heavy load conditions. The article is organized as follows. In Section II, the soft-switching resonant period is carefully analyzed, and the hysteresis-band current control and turn-ON delay are designed accordingly. In Section III, a zero-sequence voltage injection control is included in the approach, which compensates the voltage gain by 15% and narrows down the switching frequency variation range. The hardware design approach is provided in Section IV including the *LCL* filter design and the current sensor design. Section V provides the overall control diagram. In Section VI, all the analysis and the proposed control approach are experimentally verified on a custom-built highly integrated 5-kW SiC-implemented three-phase ZVS converter prototype. Finally, Section VII concludes this article.

II. PROPOSED ADAPTIVE HYSTERESIS-BAND CURRENT CONTROL FOR THREE-PHASE ZVS MODULATIONS

A. Current Band Design for ZVS Operation

In Topology 3, the connection between the dc-link midpoint N1 and the ac capacitor neutral-point N2 decouples the three

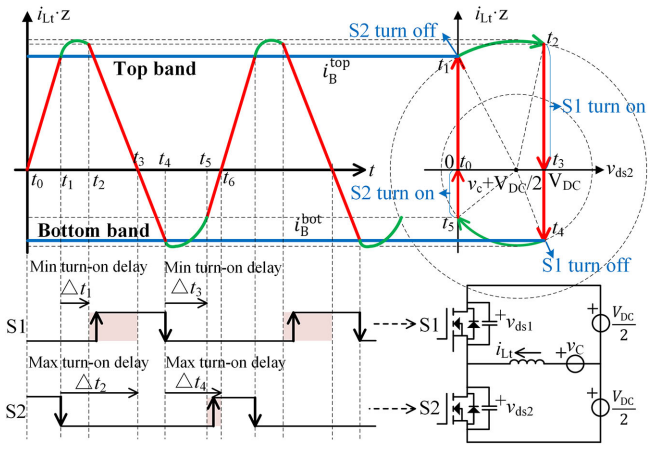

Fig. 2. ZVS condition analysis when $v_c > 0$. Clockwise from top left: inductor current, state-plane plot, single phase-leg topology, and the gate signals for both the top (S1) and bottom (S2) devices.

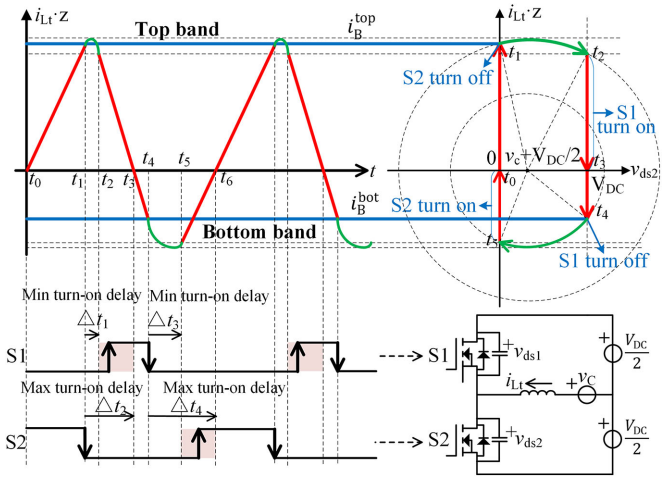

Fig. 3. ZVS condition analysis when $v_c < 0$. Clockwise from top left: inductor current, state-plane plot, single phase-leg topology, and the gate signals for both the top (S1) and bottom (S2) devices.

phases and the ZVS operation can be applied separately on different phases. Therefore, the following ZVS condition analysis is performed on each single phase-leg. Since the inductance L_t is small, the resonance between L_t and the device junction capacitance is not negligible. In order to ensure the ZVS operation, it is important to clearly analyze this resonance period.

Fig. 2 shows the ZVS condition analysis when the ac capacitor voltage is positive ($v_c > 0$). In Fig. 2, clockwise from top left, the figures are inductor current, state-plane plot, single phase-leg circuit topology, and the gate signals for both the top (S1) and bottom (S2) devices. In the state-plane plot, the two states are selected as the bottom device drain–source voltage v_{ds2} and the inductor current i_{Lt}. In the single phase-leg circuit, the ac capacitors and dc-link capacitors are assumed as voltage sources for simplicity and in Section V-C, the *LCL* filter is designed to ensure this assumption.

As shown in Fig. 2, at t_0 moment, S2 is ON and the inductor is being charged. At t_1 moment, the inductor current touches the top band and S2 turns OFF. In period t_1 to t_2, resonance happens between the inductor L_t and the device junction capacitor. The resonance frequency ω_r is shown in (1). The C_{oss}^{S1} and C_{oss}^{S2} are the charge equivalence of the top and bottom device junction capacitance and $C_{oss_{\rm eq}}$ is the parallel capacitance of C_{oss}^{S1} and C_{oss}^{S2}

$$\omega_r = \frac{1}{\sqrt{L_t C_{oss_{\rm eq}}}},\ C_{oss_{\rm eq}} = C_{oss}^{S1} + C_{oss}^{S2}. \tag{1}$$

At t_2 moment, the drain–source voltage on S2 (v_{ds2}) resonant to $V_{\rm DC}$ and the drain–source voltage on S1 (v_{ds1}) resonant to zero and the body diode of S1 starts to conduct. S1 should turn ON within period of t_2 to t_3 to ensure a ZVS turn-ON. If S1 turns ON before t_2, v_{ds1} is not zero yet and if S1 turns ON after t_3, DCM instead of CRM is applied (valley switching instead of ZVS). Meanwhile, the turn-ON moment should be close to t_2 moment to reduce conduction loss. After t_2 moment, the inductor L_t starts to discharge. At t_4 moment, the inductor current touches the bottom band and S1 turns OFF. In the period of t_4 to t_5, resonance happens again between the inductor and the device junction capacitor. It is not difficult to conclude from the state-plane plot that in order to achieve ZVS operation, there must be enough negative current on inductor L_t before S1 turns OFF. The absolute value of the minimum current is given by (2), as derived in the Appendix. $i_{\rm zvs0}$ is named as "ZVS extension current" in this article

$$i_{\rm zvs0} = \sqrt{\frac{2C_{oss_{\rm eq}} V_{\rm DC}\,|v_C|}{L_t}}. \tag{2}$$

In sum, when $v_c > 0$, the ZVS operation requires the bottom current band $i_B^{\rm bot}$ must be small than $-i_{\rm zvs0}$, as given by the following equation:

$$i_B^{\rm bot} < -i_{\rm zvs0}. \tag{3}$$

At t_5 moment, v_{ds2} resonant to zero and the body diode of S2 starts to conduct. The inductor current starts to charge. S2 should turn ON within period of t_5 to t_6 to ensure a ZVS turn-ON and the turn-ON moment should be closer to t_5 to help reducing the conduction loss.

The analysis when the ac capacitor voltage is negative ($v_c < 0$) is similar. Fig. 3 shows the ZVS condition analysis when $v_c < 0$. In Fig. 3, clockwise from top left, the figures are inductor current, state-plane plot, single phase-leg topology, and the gate signals for both the top (S1) and bottom (S2) devices. In the state-plane plot, the two states are selected as v_{ds2} and i_{Lt}.

At t_0 moment, S2 is ON and the inductor $L_{\rm t}$ is being charged. At t_1 moment, the inductor current touches the top band and S2 turns OFF. In period t_1 to t_2, resonance happens between L_t and the device junction capacitor. It is not difficult to conclude from the state-plane plot that in order to achieve ZVS operation, there must be enough positive current on inductor L_t before S2 turns OFF. The minimum current is the same as given by (2). In sum, when $v_c > 0$, the ZVS operation requires the top current band $i_B^{\rm top}$ must be larger than $i_{\rm zvs0}$, as given by the following equation:

$$i_B^{\rm top} > i_{\rm zvs0}. \tag{4}$$

At t_2 moment, v_{ds2} resonant to V_{DC} and v_{ds1} resonant to zero and the body diode of S1 starts to conduct. S1 should turn ON within period of t_2 to t_3 to ensure a ZVS turn-ON. Meanwhile, the turn-ON moment should be closer to t_2. After t_2 moment, the inductor L_t starts to discharge. At t_4 moment, the inductor current touches the bottom band and S1 turns OFF. In the period of t_4 to t_5, resonance happens again between the inductor and the device junction capacitor. At t_5 moment, v_{ds2} resonant to zero and the body diode of S2 starts to conduct. The inductor current starts to charge. S2 should turn ON within period of t_5 to t_6 to ensure a ZVS turn-ON and the turn-ON moment should be closer to t_5.

According to the above-mentioned analysis, the ZVS condition is determined by v_c polarity. In summary, the ZVS operation requires the current band satisfying the following conditions:

1) when $v_c > 0$, $i_B^{\text{top}} \geq 0, i_B^{\text{bot}} = -\sigma \cdot i_{\text{zvs0}}, \sigma \geq 1$;
2) when $v_c < 0, i_B^{\text{top}} = \sigma \cdot i_{\text{zvs0}}, i_B^{\text{bot}} \leq 0,\ \sigma \geq 1$.

The parameter σ is a relaxation factor. It helps reducing the parameter sensitivity for the ZVS operation. For instance, when $v_c > 0$, if $\sigma = 1$, then in Fig. 2, t_5 becomes equal to t_6 and S2 must turn ON at the exact instant t_5 to ensure ZVS condition. This is not applicable in real systems since there are always error on inductance value and voltage/current sensing. With $\sigma \geq 1$, the ZVS turn-ON instant becomes a range, therefore the ZVS condition is easier to realize. However, an exaggerated σ will result in additional conduction loss. In addition to the ZVS conditions, the top and bottom current band also satisfy (5), where i_{Lt}^{avg} is the required average current on inductor L_t

$$i_{Lt}^{\text{avg}} \approx \frac{1}{2}\left(i_B^{\text{top}} + i_B^{\text{bot}}\right). \tag{5}$$

To realize ZVS operations, the band design approach is summarized in Fig. 4 before the dashed line. As shown in Fig. 4, the first step is to calculate i_{zvs0}. If $i_{Lt}^{\text{avg}} > 0$, then the top and bottom band are set as $i_B^{\text{top}} = 2i_{Lt}^{\text{avg}}$, $i_B^{\text{bot}} = 0$, otherwise $i_B^{\text{top}} = 0$, $i_B^{\text{bot}} = 2i_{Lt}^{\text{avg}}$. If $v_c > 0$, the bottom band needs to be checked to make sure $i_{\text{B}}^{\text{bot}} < -\sigma i_{\text{zvs0}}$. In case the ZVS condition is not met, the i_B^{bot} is modified as $-\sigma i_{\text{zvs0}}$ and i_B^{top} as $2i_{Lt}^{\text{avg}} + \sigma i_{\text{zvs0}}$. If $v_c < 0$, the top band needs to be checked to make sure $i_B^{\text{top}} > \sigma i_{\text{zvs0}}$. In case the ZVS is not met, the i_B^{top} is modified as σi_{zvs0} and i_B^{bot} as $2i_{Lt}^{\text{avg}} - \sigma i_{\text{zvs0}}$.

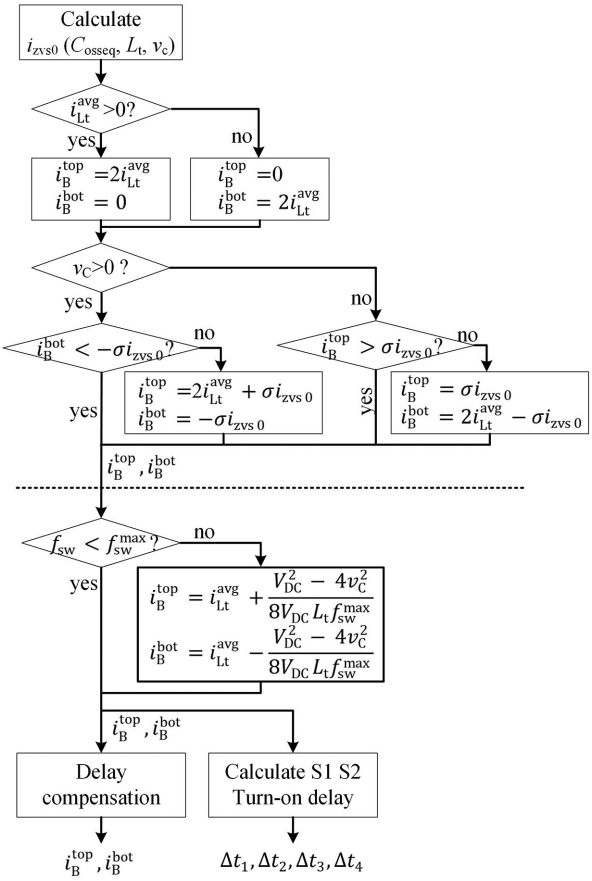

Fig. 4. Flowchart for the current band and turn-ON delay design.

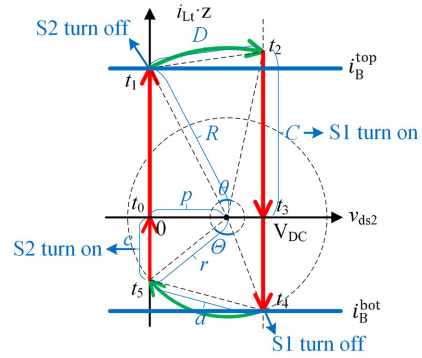

Fig. 5. State-plane plot for the ZVS turn-ON delay calculation. S1 and S2 turn ON along trajectory *C* and *c*, respectively.

B. Turn-on Delay Calculation

In Figs. 2 and 3, simple turn-OFF logic is presented: when inductor current touches the top band, S2 turns OFF and when inductor current touches the bottom band, S1 turns OFF. In order to realize the ZVS turn-ON, as analyzed in the previous section, the turn-ON moment of S1 should be located within period t_2 to t_3 and the turn-ON moment of S2 should be located within period t_5 to t_6. As shown in Figs. 2 and 3, the S1 turn-ON delay relevant to the S2 turn-OFF moment t_1 should be in the range of $[\Delta t_1, \Delta t_2]$ and the S2 turn-ON delay relevant to the S1 turn-OFF moment t_4 should be in the range of $[\Delta t_3, \Delta t_4]$. Fig. 5 shows the state-plane plot for the turn-ON delay calculations. The circle center p is given by (6). S1 and S2 turn ON along trajectory *C* and *c*, respectively

$$p = v_C + \frac{V_{\text{DC}}}{2}. \tag{6}$$

The calculation of Δt_1 to Δt_4 based on the state-plane plot is elaborated in Table II, where $z = \sqrt{\frac{L_t}{C_{\text{osseq}}}}$.

TABLE II
TURN-ON DELAY CALCULATION

S1 turn-on delay	S2 turn-on delay
$R=\sqrt{p^2+\left(z\cdot i_{\mathrm{B}}^{\mathrm{top}}\right)^2}$	$r=\sqrt{(V_{\mathrm{DC}}-p)^2+\left(z\cdot i_{\mathrm{B}}^{\mathrm{bot}}\right)^2}$
$C=\sqrt{R^2-(V_{\mathrm{DC}}-p)^2}$	$c=\sqrt{r^2-p^2}$
$D=\sqrt{{V_{\mathrm{DC}}}^2+\left(C-z\cdot i_{\mathrm{B}}^{\mathrm{top}}\right)^2}$	$d=\sqrt{{V_{\mathrm{DC}}}^2+\left(c-z\cdot i_{\mathrm{B}}^{\mathrm{bot}}\right)^2}$
$\vartheta=\operatorname{acos}\left(\frac{2R^2-D^2}{2R^2}\right)$	$\theta=\operatorname{acos}\left(\frac{2r^2-d^2}{2r^2}\right)$
$\Delta t_1=\frac{\vartheta}{\omega_r}$	$\Delta t_3=\frac{\theta}{\omega_r}$
$\Delta t_2=\frac{\vartheta}{\omega_r}+\frac{C}{z}\cdot\frac{2L_{\mathrm{t}}}{V_{\mathrm{DC}}+2v_{\mathrm{C}}}$	$\Delta t_4=\frac{\theta}{\omega_r}+\frac{c}{z}\cdot\frac{2L_{\mathrm{t}}}{V_{\mathrm{DC}}-2v_{\mathrm{C}}}$

C. Switching Frequency Limitation

Based on the analysis in the previous section, the switching frequency is given by the following equation:

$$f_{\mathrm{sw}}=\frac{1}{\Delta t_1+\Delta t_3+\frac{2L_t\left(c+i_B^{\mathrm{top}}\right)}{V_{\mathrm{DC}}+2v_C}+\frac{2L_t\left(C-i_B^{\mathrm{top}}\right)}{V_{\mathrm{DC}}-2v_C}}. \tag{7}$$

When the average inductor current is close to zero, according to (5), the absolute value of the top and bottom current band becomes very small; therefore, the switching frequency is mostly determined by resonant periods and becomes very high. In order to reduce the switching frequency, the current band should be slightly enlarged. For simplicity, neglecting the resonant period, the switching frequency can be simplified as the following equation:

$$f_{\mathrm{sw}}\approx\frac{V_{\mathrm{DC}}^2-4v_C^2}{4V_{\mathrm{DC}}L_t\left(i_B^{\mathrm{top}}-i_B^{\mathrm{bot}}\right)}. \tag{8}$$

Assuming the allowed highest switching frequency is $f_{\mathrm{sw}}^{\max}$. If the calculated current band from Section II-A results in a switching frequency higher than $f_{\mathrm{sw}}^{\max}$, based on (8), the current band can be modified as

$$i_B^{\mathrm{top}}=i_{Lt}^{\mathrm{avg}}+\frac{V_{\mathrm{DC}}^2-4v_C^2}{8V_{\mathrm{DC}}L_tf_{\mathrm{sw}}^{\max}} \tag{9}$$

$$i_B^{\mathrm{bot}}=i_{Lt}^{\mathrm{avg}}-\frac{V_{\mathrm{DC}}^2-4v_C^2}{8V_{\mathrm{DC}}L_tf_{\mathrm{sw}}^{\max}}. \tag{10}$$

Since the resonant period is neglected in (8), with the modified current band, the actual switching frequency will be slightly lower than $f_{\mathrm{sw}}^{\max}$. It is worth mentioning that the band enlarging is not the only way to reduce the switching frequency. DCM operation is an alternative strategy but with a more complicated design. Due to the length of the article, the DCM operation will be discussed in a future work.

D. Band Delay Compensation

In real implementation, the digital and analog delay in the system is unavoidable. The delay period is denoted as t_d. As shown in Figs. 2 and 3, S1 should turn OFF the instant when the inductor current touches the bottom band and S2 should turn OFF the instant when the inductor current touches the top band. However, the existence of t_d will result in delayed turn-OFF instants, which makes the inductor currents exceed the top and the bottom band. It not only introduces additional conduction losses but also changes the ZVS conditions. The delay can be compensated by adding an additional term on the top and the bottom band as given by

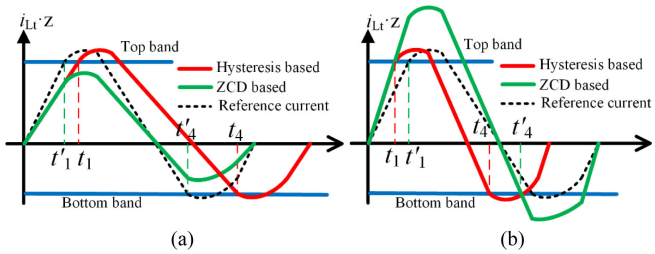

Fig. 6. Comparison of the hysteresis current based and ZCD-based implementation. (a) Inductance L_t is larger. (b) Inductance L_t is smaller. Hysteresis-based modulation exhibits a better current loop performance.

$$i_B^{\mathrm{top}}=i_B^{\mathrm{top}}-t_d*\frac{V_{\mathrm{DC}}+2v_C}{2L_t} \tag{11}$$

$$i_B^{\mathrm{bot}}=i_B^{\mathrm{bot}}+t_d*\frac{V_{\mathrm{DC}}-2v_C}{2L_t}. \tag{12}$$

It worth mentioning that the turn-ON delays (Δt_1, Δt_2, Δt_3, Δt_4) are relevant to the turn-OFF instant. Therefore, once the current bands are compensated, the turn-OFF instants are accurate and there is no need to compensate the turn-ON delays. The approaches discussed in Sections II-B, II-C, and II-D are summarized in Fig. 4 below the dashed line. Based on the calculated current band from Section II-A, the bands are modified further to make sure the switching frequency is lower than $f_{\mathrm{sw}}^{\max}$. Then, the compensated bands and turn-ON delays are calculated accordingly.

E. Comparison With ZCD-Based ZVS Implementation

As shown in Fig. 4, the proposed approach is a hysteresis current based online design method, which is not limited by certain loading conditions. It worth mentioning that hysteresis current control is not the only way for ZVS implementation. ZCD-based methods can also be implemented, as used in single-phase totem-pole converter [24]. All the turn-ON and turn-OFF instants can be precalculated and implemented based on the inductor current zero-crossing point. The band comparison logic mentioned above can be eliminated. However, in mass production, error on inductance value L_t is unavoidable. Since the ZCD-based method uses precalculated switching instants. It becomes vulnerable for these errors. As shown in Fig. 6, the precalculated S2 and S1 turn-OFF moments are t'_1 and t'_4, respectively. In Fig. 6(a), the inductance value is larger than the theoretical value, and therefore all rising and falling edges become slower, which results in a smaller average current when ZCD-based method is used. In Fig. 6(b), the inductance value is smaller and results in a larger average current when ZCD-based method is used.

Compared to the ZCD-based method, the hysteresis current based implementation is more robust to the inductance error. Since the switching instants are determined by the current band touching moment, the inductance error will not change the average current in a switching cycle. Therefore, the current loop performance is better. This is a lot helpful for the three-phase operation, since the hysteresis control allows a larger unbalance on three-phase inductance value, which simplifies the manufacturing process.

III. Voltage Gain Compensation for Three-Phase Operations

For three-phase converters, the modulation ratio is an important factor, which indicates how effectively the dc-link voltage can be used. In Fig. 1, phase *a* of the ac-side voltages is given by (13). It is assumed that the three-phase voltages are balanced, and phases *b* and *c* are $\frac{2}{3}\pi$ and $\frac{4}{3}\pi$ delayed reference to phase *a*

$$v_{ga} = v_m \cos(\omega_1 t + \theta_g). \tag{13}$$

The modulation ratio is defined as (14). For conventional three-phase continuous current mode (CCM) converter, theoretically the maximum modulation ratio is "1" [25]

$$m = \frac{\sqrt{3} v_m}{V_{\rm DC}}. \tag{14}$$

Since the voltage drop on the line impedance L_s is usually small, the differential-mode voltages on the ac capacitor tank (on v_{Ca}, v_{Cb}, v_{Cc}) are close to the differential-mode voltages on v_{ga}, v_{gb}, v_{gc} but the common-mode/zero-sequence voltages can be different. Assuming the zero-sequence voltage of v_{ga}, v_{gb}, and v_{gc} is zero and the zero-sequence voltage of v_{ca}, v_{cb}, and v_{cc} is v_0, the capacitor tank voltages are given by the following equation:

$$v_{Cx} = v_{gx} + v_0, \quad x = a, b, c. \tag{15}$$

For the three-phase ZVS converter, the capacitor voltage magnitude must be smaller than half of the dc-link voltage to maintain a voltage margin for charging and discharging the inductor L_t. In case there is no zero-sequence voltage injected ($v_0 = 0$), the maximum voltage magnitude of v_{ga} (v_m) is VDC/2 and the maximum modulation ratio is 0.866. Like traditional three-phase converters, by injecting appropriate zero-sequence voltage, the three-phase ZVS converter modulation ratio can be improved to "1" [25]. The difference is that the zero-sequence voltage is established across the ac capacitor tank in Topology 3, so it is critical to make sure the designed zero-sequence voltage is continuous. Any instant voltage jumping is not achievable. In this article, a third-harmonic injection is used, as given by the following equation:

$$v_0^{\rm ref} = -\frac{1}{6} v_m \cos(3\omega_1 t + 3\theta_g). \tag{16}$$

Required zero-sequence current that flows through each capacitor is given by (17), where *C* is the capacitance of ac capacitors

$$i_0^{\rm cal} = C \frac{dv_0^{\rm ref}}{dt} = \frac{1}{2} \omega_1 C v_m \sin(3\omega_1 t + 3\theta_g). \tag{17}$$

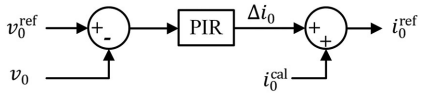

Fig. 7. Zero-sequence voltage injection control.

Assuming the ac-side three-phase reference currents are i_a, i_b, and i_c. The three-phase average reference current on L_t has both the differential-mode components and common-mode components. The differential-mode components are i_a, i_b, and i_c. In order to establish the required zero-sequence voltage, $i_0^{\rm cal}$ in (17) should be used as the common-mode components. Meanwhile, due to the parameter errors, a closed-loop control for the capacitor voltages is necessary, as shown in Fig. 7.

In Fig. 7, v_0 is the measured zero-sequence voltage, as given by (18). The error between $v_0^{\rm ref}$ and v_0 will be regulated by a proportional–integral–resonant (PIR) regulator, the resonant frequency of the PIR regulator is $3\omega_1$. Combining the PIR regulator output Δi_0 and the open-loop reference current $i_0^{\rm cal}$, the zero-sequence current reference is given by (19)

$$v_0 = \frac{1}{3}(v_{Ca} + v_{Cb} + v_{Cc}) \tag{18}$$

$$i_0^{\rm ref} = i_0^{\rm cal} + \Delta i_0. \tag{19}$$

Combining the differential-mode components and the common-mode components, the average inductor L_t reference currents are given by the following equation:

$$i_{Ltx}^{\rm avg} = i_x - i_0^{\rm ref}, \quad x = a, b, c. \tag{20}$$

With the zero-sequence voltage injection, combining (13)–(16), the capacitor voltage of phase *a* is given by (21). Since the ac capacitor voltage magnitude is reduced, according to (8), the minimum switching frequency is increased and the switching frequency variation range is narrowed

$$v_{Ca} = \frac{m V_{\rm DC}}{\sqrt{3}} \left(\cos(\omega_1 t + \theta_g) - \frac{1}{6} \cos(3\omega_1 t + 3\theta_g) \right). \tag{21}$$

Although, theoretically the modulation ratio can reach 1. In ZVS operations, as aforementioned a voltage margin between the ac capacitor voltage and the half dc-link voltage should be reserved for applying charging and discharging voltage on inductor L_t. When modulation ratio is close to 1, this voltage margin becomes trivial and results in a very small switching frequency, which will cause large ac capacitor voltage ripple and distorted currents at the ac side. In order to avoid this, the switching frequency must be several times higher than the corner frequency of the *LC* filter (L_t and *C*). In order to comply with certain total harmonic distortion (THD) requirements, (22) should be satisfied, where the minimum switching frequency is chosen to be *k* times (e.g., $k = 5$) higher than the corner frequency where the switching frequency is calculated according to (8)

$$\min f_{\rm sw} \ (v_{Ca}) \geq k \cdot \frac{1}{2\pi \sqrt{L_t C}}. \tag{22}$$

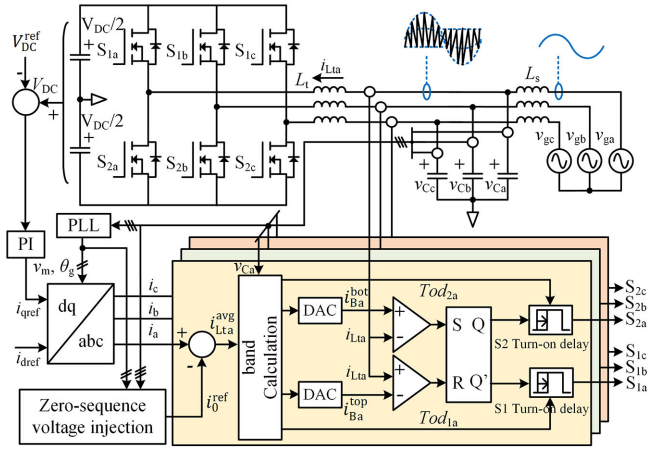

Fig. 8. Overall control diagram.

It worth mentioning that the modulation ratio limitation is also true for conventional CCM hard-switching three-phase converters. There must be voltage margin reserved for the voltage drop on the grid side inductor or the motor leakage inductor. In addition, in CCM converters, the passive components are implemented with much higher impedance due to the lower switching frequency, which can result in a larger voltage drop and a reduced modulation ratio. Therefore, from modulation ratio perspective, the CCM three-phase converter and ZVS three-phase converter are comparable.

IV. Overall Control Strategy

A. Overall Control Diagram

To summarize the proposed control approach, using the AFE converter application as an instance where the dc-link voltage needs to be regulated, the overall control diagram is shown in Fig. 8.

In Fig. 8, the difference between the measured dc-link voltage $V_{\rm DC}$ and the reference dc-link voltage $V_{\rm DC}^{\rm ref}$ is regulated by a proportional–integral regulator, which provides the reference current on q-axis, $i_{\rm qref}$. The d-axis reference $i_{\rm dref}$ is given by the reactive power command. With the measured capacitor voltages v_{Ca}, v_{Cb} and v_{Cc}, a phase-locked loop is used for getting the grid-side voltage magnitude v_m and the angle θ_g. A dq to abc transformation is then performed to get the ac-side reference currents i_a, i_b and i_c. As discussed in Section III, a zero-sequence voltage injection module, as shown in Fig. 7, is then applied to provide the zero-sequence current reference $i_0^{\rm ref}$. Combining i_a, i_b, i_c, and $i_0^{\rm ref}$, the average reference currents on three-phase inductor L_t are $i_{Lta}^{\rm avg}$, $i_{Ltb}^{\rm avg}$, and $i_{Ltc}^{\rm avg}$. Band calculations are performed on three phase-legs, respectively, according to the flowchart in Fig. 4, as explained in Section II. The calculated digital top and bottom bands need to be converted into analog signals by digital-to-analog conversion (DAC) modules. The measured inductor i_{Ltx} $(x = a, b, c)$ and the analog bands then go into a band comparison logic including two comparators and an SR flip–flop logic. Finally, the turn-ON edge of the generated S1 and S2 gate signals are delayed by turn-ON delay modules.

TABLE III
Circuit Parameters

Parameter	Symbol	Value
dc-link	$V_{\rm DC}$	700 V
Junction capacitance	$C_{\rm osseq}$	147 pF
Inductance	$L_{\rm t}$	20 µH
ac capacitance	C	2.4 µF
ac-side frequency	$f_{\rm l}$	50 Hz
ac-side voltage rms value (Line-line)	-	380 V
ac-side voltage magnitude	$v_{\rm m}$	311 V
Relaxation factor	σ	1.2
Maximum switching frequency	$f_{\rm sw}^{\rm max}$	400 kHz

The turn-ON delays are calculated online for ZVS operation as explained in Section II-B, where Tod_{1a} is the S1 turn-ON delay in phase a and Tod_{1a} is in range of $[\Delta t_1, \Delta t_2]$. Tod_{2a} is the S2 turn-ON delay in phase a and Tod_{2a} is in range of $[\Delta t_3, \Delta t_4]$. As for motor driver applications, the only difference is the $i_{d\rm ref}$ and $i_{q\rm ref}$ come from motor drive requirements instead of the dc-link regulation. The rest of the control remains the same.

B. Current Band, Turn-ON Delay, and Switching-Frequency Variation for Different Loading Conditions

Table III lists the main parameters of a 5-kW three-phase ZVS converter. Based on the parameters in Table III, Fig. 9(a) and (b) demonstrates the proposed implementation for both rectifier and inverter mode operation in nominal power. From top to bottom, the figures are phase a S1 and S2 turn-ON delay, dc-link voltage, ac capacitor voltage, phase a current bands, and the switching frequency. The active power flows from ac side to dc side in Fig. 9(a) and from dc side to ac side in Fig. 9(b). There is no reactive power at the ac side in Fig. 9.

As discussed in Section II, by introducing a relaxation factor σ, the turn-ON delay for ZVS operation becomes a range, $[\Delta t_1, \Delta t_2]$ for S1 and $[\Delta t_3, \Delta t_4]$ for S2 as shown in the top figure. In the figure of ac capacitor voltages, the dashed line shows the injected zero-sequence voltage. The ac capacitor voltage magnitude is reduced by 15% due to the zero-sequence voltage injection. In the figure of the current band design, the dashed lines are the compensated current band considering a t_d of 100 ns, as discussed in Section II-D. Compared to the rectifier implementation, the inverter implementation has a larger turn-ON delay range and a narrower current band. It is because in inverter mode operation, when $v_c > 0$ the average reference inductor current is negative, the instantaneous value of this current could be enough for ZVS operation, therefore no need for the ZVS extension current (i_{zvs0}). The bottom current band can be set as zero. However, in rectifier mode, when $v_c > 0$, the average reference inductor current is positive, additional negative i_{zvs0} is always required for ZVS operation. When $v_c < 0$, the conclusion is the same. This is only true when a high average current exhibit on inductor L_t. Around current zero-crossing point and in light load condition, additional i_{zvs0} current is still prerequisite even for inverter mode operation. At ac current zero-crossing point, in order to reduce the switching frequency, current bands are enlarged according to Section II-C and the switching frequency is controlled below the maximum frequency of 400 kHz, as shown in the bottom figure in Fig. 9.

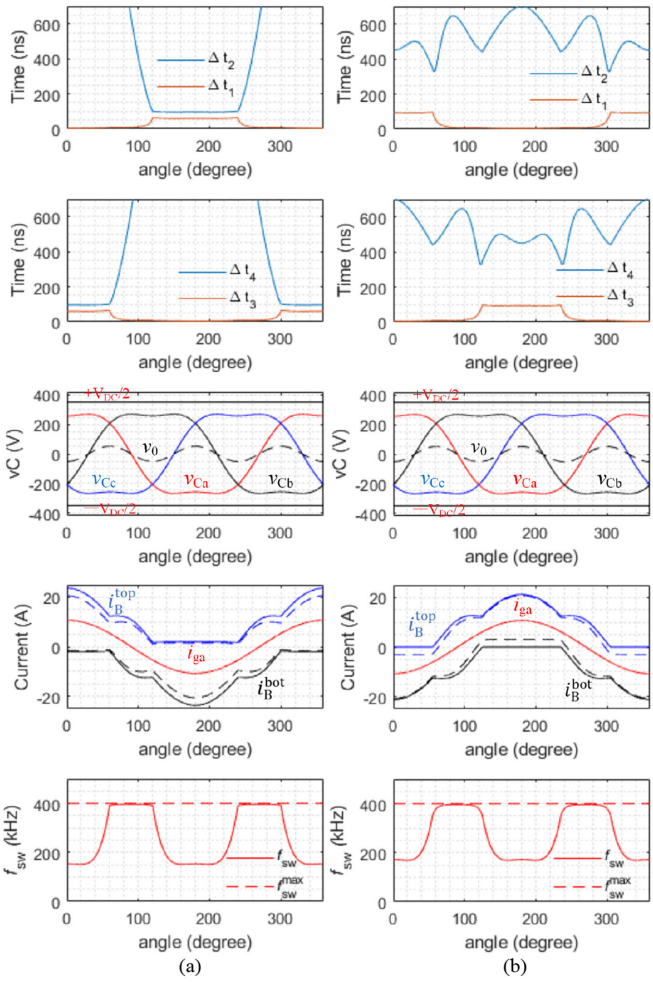

Fig. 9. (a) Rectifier implementation. (b) Inverter implementation. From top to bottom: phase *a* S1 turn-ON delay, phase *a* S2 turn-ON delay, dc-link voltage, ac capacitor voltage, phase *a* current bands, and switching frequency.

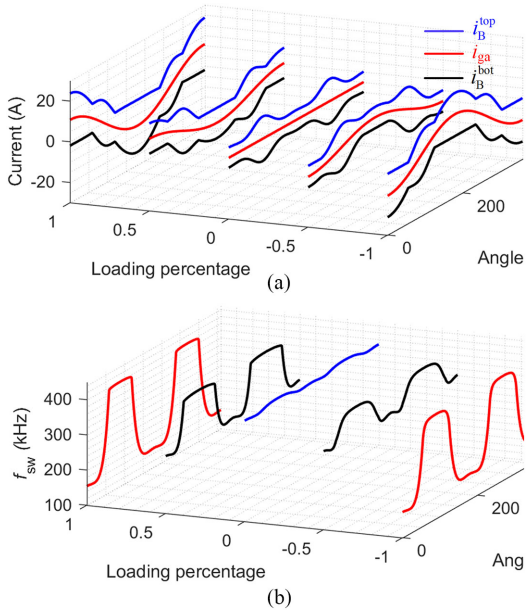

Fig. 10. (a) Current band at different loading percentages in one line-cycle. (b) Switching frequency variation at different loading percentages in one line-cycle (unity power factor).

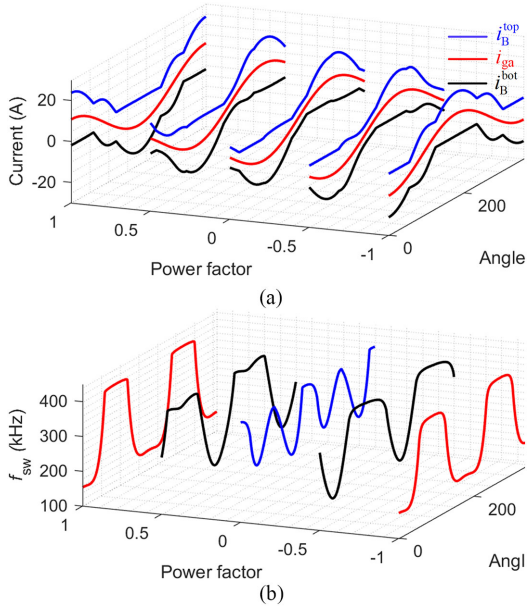

Fig. 11. (a) Current band at different power factors in one line-cycle. (b) Switching frequency variation at different power factors in one line-cycle (ac-side current magnitude remains constant).

The proposed ZVS modulation approach is applicable for various loading conditions. Fig. 10(a) and (b) demonstrates the current band design and the switching frequency variation in one line-cycle at loading percentage of 100%, 50%, 0%, –50%, and –100% while the power factor remains to be 1. The larger the loading percentage the wider the switching frequency variation range. Fig. 11(a) and (b) demonstrates the current band design and the switching frequency variation at power factor of 1, 0.5, 0, –0.5, –1 while the ac-side current and voltage magnitude remain the same.

Fig. 12 presents a switching frequency variation comparison between Topologies 1 and 3 under inverter mode operation as an example. For Topology 1, the control approach documented in [9], [10], and [12] is used and a constant "bias current" of 0.5 A is adopted for the whole line-cycle. The resulted maximum switching frequency of Topology 1 is around 220 kHz and for a fair comparison, this frequency is set as the allowed maximum switching frequency for Topology 3 as discussed in Section II-C. Comparing the bottom figure in Fig. 12(a) and (b), the two topologies share a quite similar switching frequency range, but with different changing periods. Topology 3 shows a period of 180° and Topology 1 shows a period of 60°. The top figures in Fig. 12(a) and (b) demonstrate the different ways of zero-sequence voltage injection for these two topologies. Meanwhile, in the bottom figure of Fig. 12(a), the switching frequency without frequency limitation and zero-sequence voltage injection is presented in the dashed line. The green arrow shows the switching frequency reduction contributed by allowing a

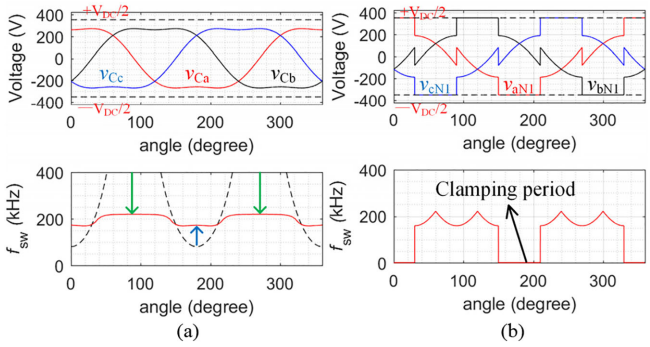

Fig. 12. Switching frequency variation comparison. (a) Topology 3 with the proposed control. (b) Topology 1 with the control approach documented in [9], [10], and [12]. From top to bottom: Line to the dc midpoint voltage and the switching frequency of phase *a*.

TABLE IV
CURRENT SENSOR COMPARISONS

	Shunt + iso. op-amp	Open-loop hall sensor	Closed-loop hall sensor	Current transformer
Accuracy	High	Low	High	Low
Size	Medium	Medium	Large	Large
Bandwidth	High, (< 1 MHz)	Medium (~ 100 kHz)	Medium (100 kHz – 300kHz)	High (> 100 kHz)
Aux. supply	Primary and secondary side	Secondary side	Secondary side	No need

larger ripple current at the high switching frequency range and the blue arrow shows the switching frequency increase because of the zero-sequence voltage injection. In together, the switching frequency variation range can be effectively narrowed.

V. HARDWARE DESIGN AND IMPLEMENTATION

A. Current Sensor Design

Since the proposed approach includes current band comparisons, the design of the current sensor is critical. It requires the current sensor to be with high bandwidth (>1 MHz) and high accuracy. In order to achieve this, Amirahmadi *et al.* [8] combined a high-frequency shunt current sensor and a low-frequency Hall sensor to realize the high frequency and average current control, respectively. However, the separated current sensing increases the system complexity. In this article, an integrated high-performance current sensor design is proposed.

In order to directly measure the inductor current, the current sensor needs to be in series with the inductor L_t. Since there is no common point for three-phase inductors, the current sensing should be isolated. Table IV compares several isolated current sensing solutions.

The second column shows the solution using a shunt resistor combined an isolated (iso.) operational amplifier (op-amp). The bandwidth of this solution is mainly determined by the isolated linear op-amp. A bandwidth of higher than 1 MHz can be achieved but the isolated amplifier circuit with this high bandwidth is difficult to design and expensive. In addition, the shunt resistors will introduce additional loss and the auxiliary power

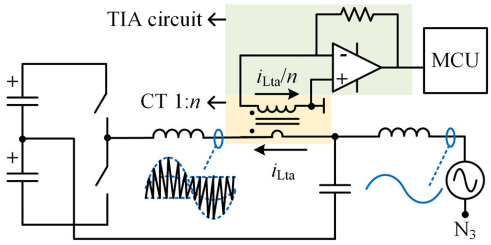

Fig. 13. Current sensor design. The CT and the TIA circuits are marked in yellow and green, respectively.

supplies need to be applied at both the primary and the secondary sides, which results in a larger volume. The Hall-effect-based sensors are demonstrated in the third and fourth columns. However, they cannot meet the bandwidth requirement. The last column shows the current transformer (CT) method. It can achieve a high bandwidth, but the size of the CT is determined by the low-frequency components in the measured current due to the saturation concern [26]. Since there are both line-frequency and high-frequency current components on inductor L_t, the size of the CT will be large. Meanwhile, normally a resistor is applied in parallel with the CT secondary winding and the created voltage drop represents the measured current. Since the resistor current is affected by the impedance match between the CT mutual inductance and the resistance, the accuracy is compromised.

In this article, a CT plus transimpedance (TIA) circuit approach [27] is used for the inductor current sensing. Fig. 13 shows the schematic design of the current sensor. The primary side of a 1:n CT is placed between inductor L_t and the ac capacitor tank. At the secondary side, an op-amp circuit is applied, which virtually short circuits the secondary winding. The short-circuit effect brings two major benefits. First, the voltage applied on the secondary side becomes very small (only small voltage drop on the winding resistor), therefore there will be no saturation even a small magnetic core is used. Second, the excitation current becomes very small; therefore, the current ratio between the primary side and secondary side current is very close to 1:n, which improves the accuracy.

B. Digital and Analog Control Implementation

As demonstrated in Fig. 8, there are both digital and analog parts in the control system. In order to achieve a better electromagnetic compatibility (EMC) and reduce cost, a single microcontroller unit (MCU) implementation is proposed without using any external comparators or DAC circuits, as shown in Fig. 14. In this article, a low-cost microcontroller TMS32028379D is used. Based on the sampled voltages and currents, the band and turn-ON delay calculations are executed in the CPU. The digital to analog band conversion and current comparisons are realized by the comparator peripherals in the MCU. The PWM module is used to implement the SR flip–flop logic and the dynamic turn-ON delay. The measured delay period t_d is about 100 ns, which includes all the delays coming from the current sensing, comparator, SR logic, and gate drivers. This

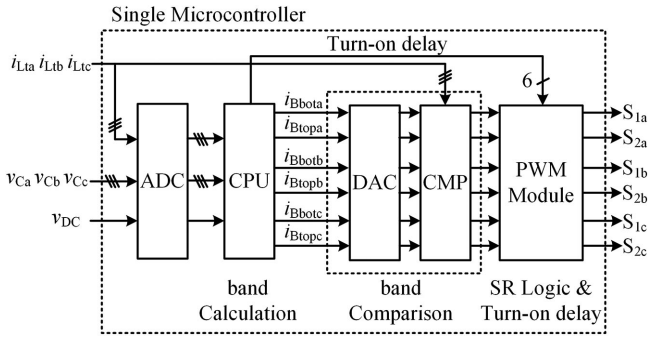

Fig. 14. Single microcontroller implementation for the proposed approach.

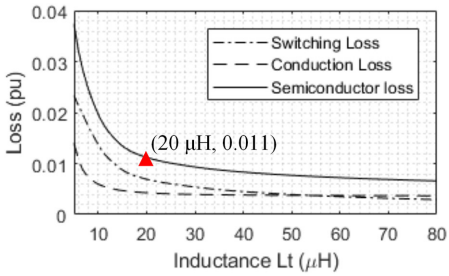

Fig. 15. Semiconductor loss change versus inductance change, per-unit (p.u.) value, base power 5 kW.

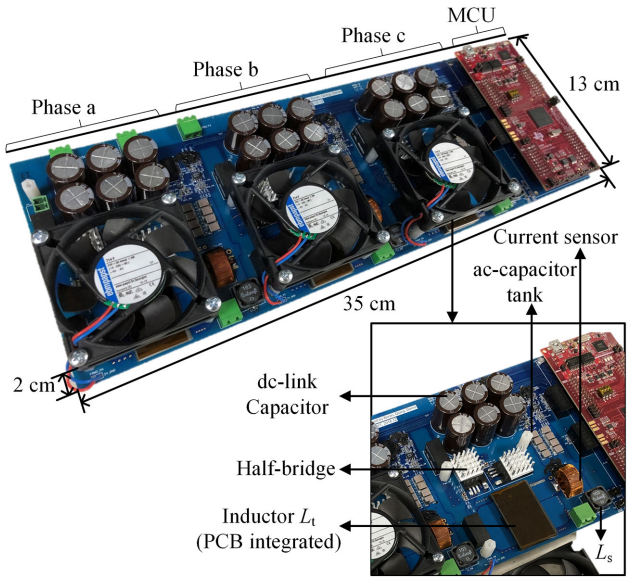

Fig. 16. Hardware integration of an SiC-implemented 5-kW 380-V three-phase ZVS converter prototype.

delay time will be used for the current band compensation as discussed in Section II-D.

C. LCL *Filter Design*

In the three-phase ZVS converter, there is an *LCL* filter formed by L_t, C and L_s. The design of the *LCL* filter will heavily affect the system performance like efficiency, THD, and power density. A following *LCL* filter design approach is proposed.

First the L_t inductance value design is based on the system efficiency requirement. A small L_t is preferred from power density point of view. However, according to (8) and (2), a small L_t leads to a higher switching frequency and larger current band. Using a 1000-V 65-mΩ SiC MOSFET as an example, Fig. 15 shows the switching/conduction loss respective to the inductance value change. In this article, the inductance value L_t is selected as 20 μH to realize a close to 1% loss on the semiconductor stage. Second, once the L_t is selected, the minimum switching frequency can be calculated according to (8) and the capacitance C is selected to make sure the corner frequency of the *LC* filter (L_t and C) ten times lower than the minimum switching frequency. It ensures a small capacitor voltage ripple and the THD performance on the ac side.

Finally, the selection of L_s depends on the application; in motor drive application, L_s is the motor leakage inductance and in AFE applications, L_s is the grid-side inductor or the grid-side line impedance. Due to the band current control, inductor L_t can be treated as a current source, which feeds the paralleled inductor L_s and capacitor C. The impedance of L_s is selected to be five times larger than the impedance of C at the possible minimum switching frequency. Normally, the motor leakage inductance or the line impedance would be enough for this requirement and no additional L_s is required. It is worth mentioning that for conventional CCM three-phase converters, an *L* filter can be used instead of an *LCL* filter at the ac side despite a filter size increase. However, in CRM operation, the *LCL* filter is always necessary because switching patterns are designed based on the inductance of L_t and without the ac capacitor tank, which serves as a decoupling stage between L_t and ac-side line impedance L_s, the ZVS conditions are not guaranteed. In addition, as shown in Fig. 1, the current on the inductor L_t exhibits a triangular shape with large ripple. It is not preferred to feed this current directly to the ac side.

VI. Experiment Results

A. *Hardware Integration*

Fig. 16 shows the designed SiC-based 5-kW three-phase ZVS converter prototype. The design parameters are summarized in Table III. The power density is 5.5 kW/L, which includes all the semiconductor devices, passive filters, MCU, heatsink, and cooling fan. Three phase-legs and the MCU are marked in the top figure. The bottom figure shows the phase-leg design, which includes the dc-link capacitor, SiC half-bridge, ac capacitor tank, current sensor, and the inductor L_t. The current sensor was customized according to the analysis in Section V-A with a bandwidth higher than 1 MHz. To simplify the manufacturing process in the mass production and make the inductor design more repeatable and predictable, 12-layer printed circuit board (PCB) integrated inductors L_t were implemented instead of the conventional discrete inductors.

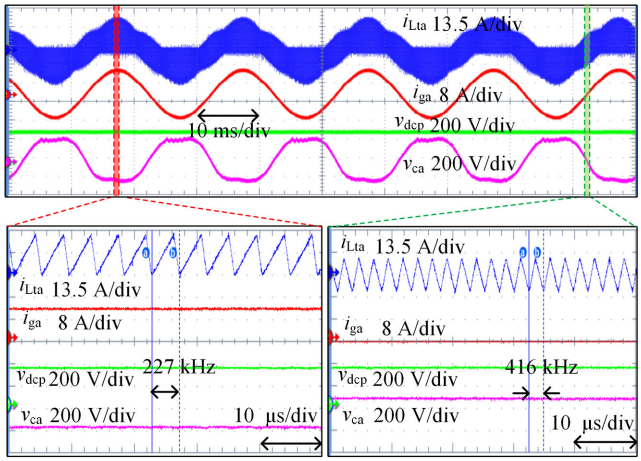

Fig. 17. 5-kW 380 Vac–700 Vdc unity power factor testing results (phase *a*). In each waveform, from top to bottom: inductor current, ac-side current, half dc-link voltage, and ac capacitor voltage.

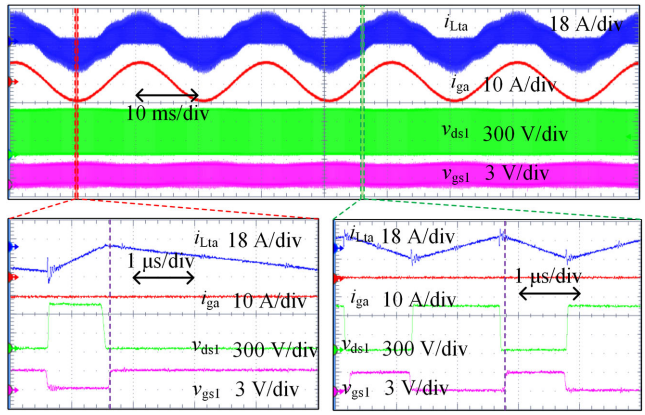

Fig. 18. 5-kW ZVS condition verifications for unity power factor testing (phase *a*). In each waveform, from top to bottom: inductor current, ac-side current, top device drain–source voltage, and gate signal.

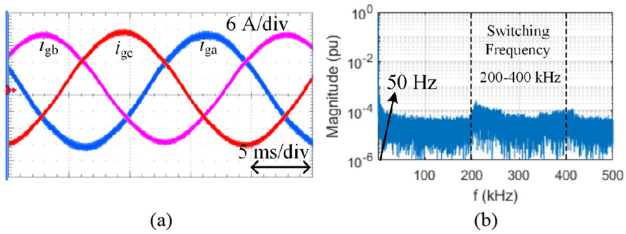

Fig. 19. Three-phase currents. (a) Measured currents. (b) Current spectrum analysis, p.u. value over the 50-Hz fundamental magnitude, THD 1.52%.

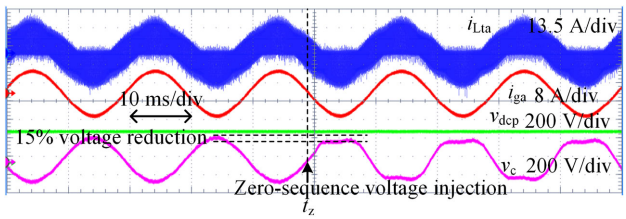

Fig. 20. 5-kW voltage gain compensation verification (phase *a*). From top to bottom: inductor current, ac-side current, half dc-link voltage, and ac capacitor voltage.

B. Unity Power Factor Testing Result

Fig. 17 shows the 5-kW 380 Vac to 700 Vdc testing results under unity power factor condition. Critical system parameters are shown in Table III and a three-phase resistor load is used at the ac side. In each waveform, from top to bottom, the measurements are the L_t inductor current, ac-side current, positive half dc-link $v_{\mathrm{dc}p}$ voltage, and ac capacitor voltage in phase *a*. The measured envelope of the inductor current corresponds to the calculated top and bottom current band, as shown in Fig. 9. The measured ac-side current is very sinusoidal with a THD of 1.52%.

As discussed in Section III, a third-harmonic zero-sequence voltage is injected on the ac capacitor and the voltage magnitude of the ac capacitor is reduced. The bottom two waveforms in Fig. 17 are the zoom-in results of the top waveform. Clear triangular-shape currents are measured on the inductor L_t. The switching frequency is ranging from about 200 to 400 kHz and the measured converter efficiency is 98.5%, which includes both the device and the inductor loss. Fig. 18 shows the 5-kW ZVS condition verification under unity power factor. The testing condition is the same as in Fig. 17. In each waveform, from top to bottom, the measurements are the L_t inductor current, ac-side current, top device drain–source voltage and top device gate signal in phase *a*. The gate signal is measured from the MCU output. The bottom two waveforms in Fig. 18 are the zoom-in results of the top waveform. The device turns ON after the drain–source voltage reduced to zero, so the zero-voltage turn-ON is realized.

Fig. 19(a) shows the measured ac-side three-phase currents. The currents are sinusoidal and balanced. Fig. 19(b) shows the current spectrum analysis. The *x*-axis is the frequency and the *y*-axis is the p.u. current magnitude (magnitudes over the 50 Hz fundamental frequency magnitude) in log scale. Due to the nature of variable switching frequency operation, there are no significant spikes in the harmonics. In the switching frequency range of around 200–400 kHz, switching harmonics are evenly distributed, which is beneficial for passing the electromagnetic interference standards.

Fig. 20 presented a dynamic verification of the voltage gain compensation. At the t_z moment, the voltage gain compensation in Section III is applied. The peak voltage across ac capacitor is reduced by around 15%.

C. Reactive Power Testing Results

Figs. 21 and 22 show the 5-kVA 380 Vac–700 Vdc testing results with 2.25 kvar reactive power. Critical system parameters are shown in Table III and a three-phase *RL* load is used at the ac side.

In Fig. 21, from top to bottom, the measurements are the L_t inductor current, ac-side current, positive half dc-link voltage, and ac capacitor voltage in phase *a*. The inductor current envelope

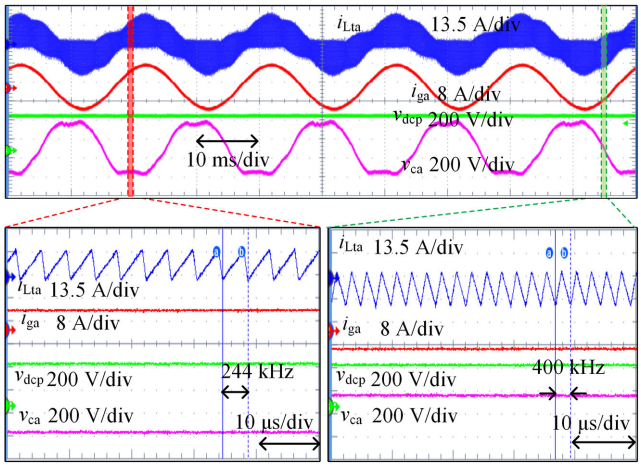

Fig. 21. 5-kVA 380 Vac–700 Vdc testing results with 2.25 kvar reactive power (phase a). In each waveform, from top to bottom: inductor current, ac-side current, half dc-link voltage, and ac capacitor voltage.

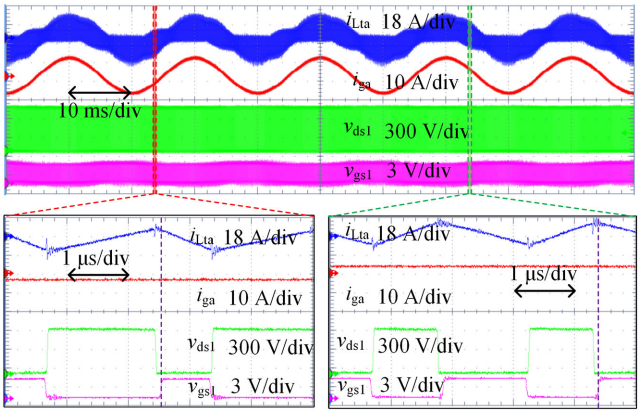

Fig. 22. 5-kVA ZVS condition verifications with 2.25 kvar reactive power (phase a). In each waveform, from top to bottom: inductor current, ac-side current, top device drain–source voltage, and gate signal.

becomes unsymmetrical and corresponds to the current band analysis in Fig. 11. The measured ac-side current is sinusoidal with a THD of 1.5%. As discussed in Section III, a third-harmonic zero-sequence voltage is injected on the ac capacitor and the voltage magnitude of the ac capacitor is reduced. The bottom two waveforms in Fig. 21 are the zoom-in results of the top waveform. Clear triangular-shape currents are measured on the inductor L_t. The switching frequency is ranging from around 200 to 400 kHz. Fig. 22 shows the 5-kVA ZVS condition verification with 2.25 kvar reactive power. The testing condition is the same as in Fig. 21. In each waveform, from top to bottom, the measurements are the L_t inductor current, ac-side current, top device drain–source voltage and top device gate signal in phase a. The gate signal is measured from the MCU output. The bottom two waveforms in Fig. 22 are the zoom-in results of the top waveform. The device turns ON after the drain–source voltage reduced to zero so the zero voltage turn-ON is verified.

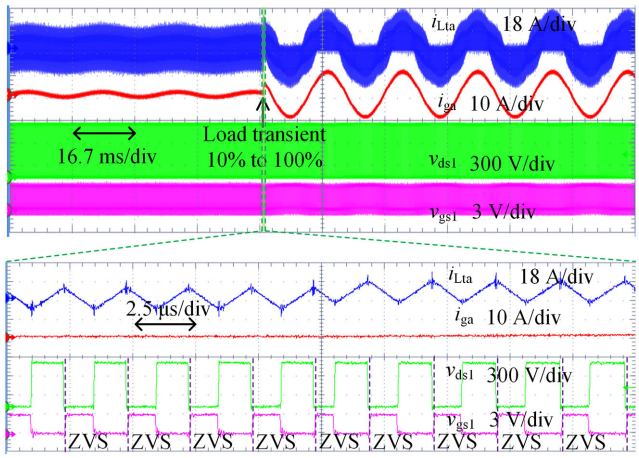

Fig. 23. Transmission power transient test results (phase a). In each waveform, from top to bottom: inductor current, ac-side current, top device drain–source voltage, and gate signal.

D. Transmission Power Transient Testing Results

Fig. 23 shows the transmission power transient test results where the delivered power jumped from 0.5 to 5 kW (10%–100%). In Fig. 23, from top to bottom, the measurements are the L_t inductor current, ac-side current, top device drain–source voltage, and top device gate signal in phase a. The bottom waveform is the zoom-in result in the transient period. The device turns ON after the drain–source voltage reduced to zero therefore the zero-voltage turn-ON is realized around the transient moment.

VII. Conclusion

This article proposed a systematic approach for the control of a three-phase bidirectional ZVS converter based on hysteresis-band current control. The soft-switching resonant period is carefully analyzed, and the current band is designed accordingly, which helps reducing the additional conduction loss. Since the current band and turn-ON delay are calculated online, the ZVS can be realized in full line-cycle at all loading conditions. A zero-sequence voltage injection control is introduced, which compensates the voltage gain by 15% and narrows down the switching frequency variation range.

The hardware design approach is also provided including the *LCL* filter design and a low-cost high-bandwidth high-accuracy current sensor design. A highly integrated 5-kW SiC-implemented three-phase ZVS converter prototype with PCB integrated inductors and customized current sensors is designed. All the analog and digital control is implemented in a single MCU, which achieves a high EMC. All the analysis and the proposed control approach are experimentally verified on the designed prototype.

Appendix
Derivation of ZVS Extension Current

The derivation of (2) is based on the state-plane plot. The detailed definition of the state-plane plot is presented in Figs. 2

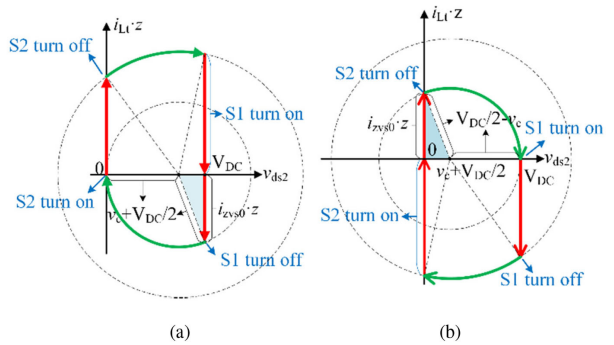

Fig. 24. Derivation of ZVS extension current. (a) Condition of $v_c > 0$. (b) Condition of $v_c < 0$.

and 3 for condition of $v_c > 0$ and $v_c < 0$, where the two states are selected as the bottom device drain–source voltage v_{ds2} and the inductor current i_{Lt}. As shown in Fig. 24(a), if $v_c > 0$, a negative current is essential to achieve the ZVS turn-ON of device S2. The minimum absolute value of this negative current can be calculated based on the marked triangle in Fig. 24(a), as presented in (23). Similarly if $v_c < 0$, a positive current is essential to achieve the ZVS turn-ON of device S1. The minimum value of this positive current can be calculated based on the marked triangle in Fig. 24(b), as presented in (24). Combining the above two conditions, the ZVS extension current is given by (2)

$$\left(V_{\rm DC}-\left(v_C+\tfrac{V_{\rm DC}}{2}\right)\right)^2+(i_{\rm zvs0}z)^2=(v_C+\tfrac{V_{\rm DC}}{2})^2, z=\sqrt{\frac{L_t}{C_{osseq}}}$$
$$\Rightarrow i_{\rm zvs0}=\sqrt{2C_{osseq}V_{\rm DC}v_C/L_t},\ v_C>0 \tag{23}$$

$$\left(v_C+\tfrac{V_{\rm DC}}{2}\right)^2+(i_{\rm zvs0}z)^2=\left(\tfrac{V_{\rm DC}}{2}-v_C\right)^2, z=\sqrt{\frac{L_t}{C_{osseq}}}$$
$$\Rightarrow i_{\rm zvs0}=\sqrt{-2C_{osseq}V_{\rm DC}v_C/L_t},\ v_C<0. \tag{24}$$

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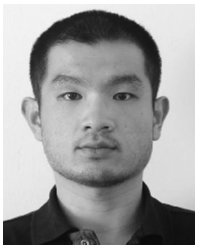

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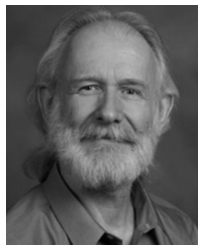

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