A Modified DPWM With Neutral Point Voltage Balance Capability for Three-Phase Vienna Rectifiers

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***Abstract*—Compared with continuous pulsewidth modulation (PWM), discontinuous PWM (DPWM) is a preferred solution in high-frequency Vienna-type rectifiers due to its inherent characteristics of less commutation number and higher efficiency. In this article, redundant clamping modes at the same subsector with opposite effects on the neutral point (NP) voltage are presented. Then, a modified DPWM (MDPWM) scheme is proposed to regulate the NP voltage by using redundant clamping modes. Thus, the NP voltage can be controlled in each switching period to lower the NP voltage fluctuation. The implementation of the proposed MDPWM is given with variable power factors analysis. Further, the switching loss comparison of conventional space vector PWM (SVPWM), hybrid DPWM (HDPWM), and proposed MDPWM is presented as well. A simulation model was built to verify the proposed NP voltage balance with different modulation indices and variable power factors. Finally, a 10-kW prototype is built to evaluate the proposed MDPWM scheme at conversion efficiency and current total harmonic distortion (THD). Experimental results and analysis show that comparing conventional SVPWM and HDPWM, the efficiency of MDPWM is the highest. The THD of DPWM is slightly higher than that of SVPWM, and it is only 2.5% at rated output power.**

***Index Terms*—Discontinuous pulsewidth modulation (DPWM), modulation scheme, neutral point (NP) voltage balance, Vienna-type rectifier.**

I. Introduction

COMPARED with the conventional three-level neutral-point-clamped (NPC) and T-type bidirectional ac/dc converters, Vienna-type rectifiers feature higher reliability and higher efficiency [1], [2]. Therefore, Vienna-type rectifiers, as shown in Fig. 1, are widely used in telecommunication power systems, wind energy applications, electric vehicle charging systems, and aircraft systems [3], [4]. As well known, the fundamental frequency of aircraft systems is much higher than that of the commercial utility grid [5]. To achieve an excellent total harmonic distortion (THD) performance, the switching frequency is expected to be as high as possible to make a wider control bandwidth [6], [7]. Moreover, increasing switching frequency also makes a significant contribution toward improving power density as well as reducing hardware cost [8], [9]. However, the switching loss of Si-MOSFET increases significantly when the switching frequency increases to hundreds of kilohertz. The switching losses can be reduced by using discontinuous PWM (DPWM) compared with space vector PWM (SVPWM) and carrier-based PWM (CBPWM) [10]–[13]. Thus, it is being considered as a candidate solution in high-switching frequency applications [14], [15].

The vector diagram of conventional DPWM is shown in Fig. 2. To maximize the switching loss reduction, it is preferred to keep the phase with the highest phase current unswitched. Switching state sequences at the big sector I are listed in Table I for analysis. The clamping mode (X–Y) represents that the bridge midpoint of each phase (X = A, B, and C) is connected to different output voltage levels (Y = P, O, and N). To avoid input alternating currents distortion, the utility grid voltage and

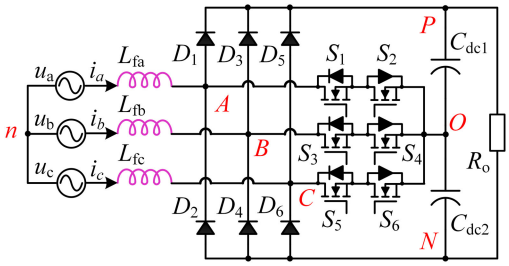

Fig. 1. Topology of the three-phase Vienna-type rectifier.

TABLE I
SWITCHING STATE SEQUENCE OF CONVENTIONAL DPWM

Subsector	Clamping Mode	Switching states sequence	Effect on NP voltage
1	A-O	OOO OON ONN OON OOO	Positive
2	C-O	OOO POO PPO POO OOO	Negative
3	A-P	PON POO PPO POO PON	Negative
4	C-N	PON OON ONN OON PON	Positive
5	A-P	POO PON PNN PON POO	Negative
6	C-N	PPN PON OON PON PPN	Positive

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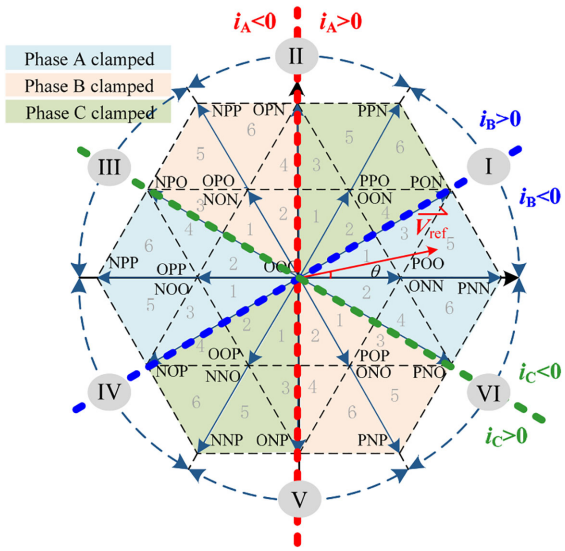

Fig. 2. Vector diagram of conventional DPWM for the Vienna-type rectifier.

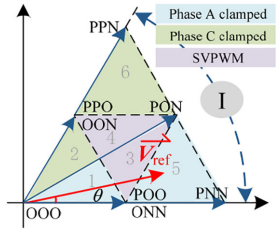

Fig. 3. Vector diagram at big sector I of hybrid DPWM proposed in [20].

the input alternating current of the Vienna-type rectifier usually have the same phase [15]. Thus, clamping modes of subsectors 3 and 4 are unavailable by employing the conventional DPWM, since they lead to the opposite direction of voltage and current near the zero-crossing point of phase-B. In [16], a carrier-based discontinuous space-vector modulation with varying clamped area was proposed to improve the performance of alternating current by clamping zero-crossing phase to neutral point (NP). In [17], a segmented component injection scheme was proposed not only to keep the alternating current with low-harmonic distortion but also to minimize the oscillation of dc-link voltage under balanced and unbalanced conditions. Unfortunately, efficiency optimization has not yet been discussed by both of them.

On the other hand, the three-level Vienna-type rectifier has the issue of unbalanced NP voltage, which causes increased voltage stress on switching devices and leads to a low-order harmonic current. In SVPWM, the NP voltage can be balanced by distributing the dwell time of redundant small vectors [18], but the effect of middle vectors on the NP voltage cannot be ignored. To overcome this issue, a virtual SVPWM (VSVPWM) was proposed in [19], which has an excellent control capability of the NP voltage balance with a wide range of modulation indices. A hybrid modulation scheme was proposed in [20], where VSVPWM is employed when the NP voltage is unbalanced otherwise, SVPWM is used. However, the VSVPWM causes higher switching losses because there are four switching actions in each switching period. Unfortunately, the conventional DPWM with lower switching losses lacks the ability to balance NP voltage, since redundant small vectors are unused in each switching period to maintain the certain bridge leg unswitched [21], [10]. Thus, the effect on the NP voltage of each subsector is fixed, as illustrated in Table I. As a result, the NP voltage cannot be regulated in accordance with the deviation of upper and lower capacitor voltages.

Several literature have addressed the NP voltage issue by using DPWM. A common method is to use hybrid continuous PWM and DPWM, and the continuous PWM is used to balance the NP voltage [21], [22], [25]. A hybrid DPWM (HDPWM) scheme was proposed to maintain the lower switching loss with the NP voltage controllability [21], and the vector diagram in the big sector I is depicted in Fig. 3. Since the SVPWM is used at subsectors 3 and 4, the NP voltage can be balanced by using redundant small vectors. In [22], a similar hybrid modulation scheme was proposed to regulate the unbalanced NP voltage with SVPWM. Another hybrid modulation scheme of SPWM and DPWM was proposed in [25]. However, the switching loss is increased by using continuous PWM. Other DPWM solutions to control the NP voltage were proposed in [10]–[28]. A DPWM method based on a circuit-level decoupling principle was proposed in [10], which can balance the NP voltage of NPC inverters without any feedback control. However, this modulation scheme has the problem of input alternating currents zero-crossing distortion. An extended DPWM modulation strategy based on the NPC inverter was investigated in [23], which can control the NP voltage with a wide range of modulation indices. However, zero vectors PPP and NNN are used in this modulation scheme, so it is not suitable for three-phase Vienna rectifiers. In [24], the NP voltage was regulated by injecting different zero-sequence voltages into the modulation wave. However, the switching loss cannot be minimized by clamping the bridge-leg voltage near the zero-crossing point. The NP voltage can also be controlled by adjusting the discontinuous width of positive and negative cycles [26]. This method maintains low switching losses and achieves the effective NP voltage balance. However, since the NP voltage is regulated in a fundamental period, the NP voltage fluctuation varies with the fundamental frequency. Thus, it may need a larger capacitance to limit the NP voltage fluctuation. In [27], a new DPWM was proposed to regulate NP voltage in 3L-NPC inverters by injecting positive and negative offset voltages. However, this method is not suitable for Vienna-type rectifiers, because it exists zero-crossing distortion in reference voltages by injecting these two offset voltages. A triangle carrier-based PWM was proposed in [28] to achieve NP voltage balance by employing redundant clamping modes, but both the minimum switching loss and variable power factors are not achieved.

In this article, a modified DPWM (MDPWM) scheme is proposed by regulating the NP voltage in each switching period. The article is organized as follows. In Section II, redundant clamping modes of subsectors are presented, and one of the bridge legs is also unswitched in each switching period. In Section III, the implementation of NP voltage balance control and variable power factors is given in detail. Moreover, the switching loss of the

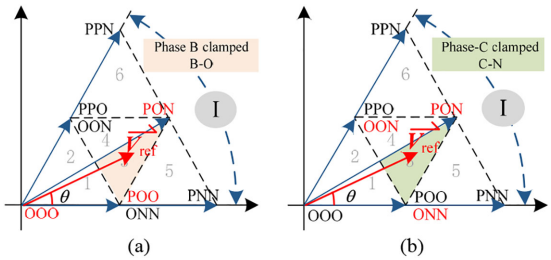

Fig. 4. Vector diagram of subsector 3. (a) Clamping mode B-O. (b) Clamping mode C-N.

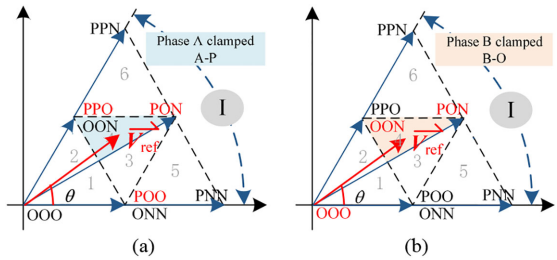

Fig. 5. Vector diagram of subsector 4. (a) Clamping mode A-P. (b) Clamping mode B-O.

TABLE II
REDUNDANT CLAMPING MODES AT SUBSECTORS 3 AND 4

Subsector	Clamping mode	Switching state sequence	Effect on NP voltage
3	B-O	PON POO OOO POO PON	Negative
	C-N	PON OON ONN OON PON	Positive
4	A-P	PON POO PPO POO PON	Negative
	B-O	PON OON OOO OON PON	Positive

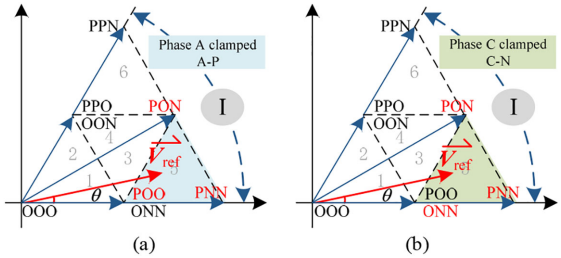

Fig. 6. Vector diagram of subsector 5. (a) Clamping mode A-P. (b) Clamping mode C-N.

proposed MDPWM, the HDPWM, and the conventional SVPWM is fairly compared. Then, the simulation results of the proposed MDPWM are also presented. In Section IV, experiments are carried out with efficiency, THD, and NP voltage balance capability measurement. Finally, Section V concludes the article.

II. REDUNDANT CLAMPING MODES

The big sector I is taken as an example for the analysis. As mentioned earlier, the utility-grid voltage and input alternating current of the Vienna-type rectifier should have the same phase. As shown in Fig. 2, it is clear that the grid voltage of phase-A is always positive in big sector I, and phase-A voltage can be clamped to $+U_{\rm dc}/2$ (P) or 0 (O). The grid voltage of phase-C is always negative in big sector I, and phase-C voltage can be clamped to $-U_{\rm dc}/2$ (N) or 0 (O). The grid voltage of phase-B is positive at subsectors 2, 4, and 6.

Contrarily, it is negative at subsectors 1, 3, and 5. As a result, the phase-B voltage cannot be clamped to $+U_{\rm dc}/2$ (P) at subsectors 1, 3, and 5, and it cannot be clamped to $-U_{\rm dc}/2$ (N) at subsectors 2, 4, and 6 either. In this article, the modulation index (MI) of the Vienna-type rectifier is defined as follows:

$$\mathrm{MI} = \frac{\sqrt{6}u_{\rm ac}}{U_{\rm dc}} \tag{1}$$

where $u_{\rm ac}$ represents the rms value of utility grid voltage and $U_{\rm dc}$ represents the output dc voltage.

A. Clamping Modes at Subsectors 3 and 4

The vector diagram of subsectors 3 is depicted in Fig. 4. Since the vector PPO is unavailable at subsector 3, there are two redundant clamping modes, B-O and C-N, as listed in Table II. The vector diagram of subsector 4 is depicted in Fig. 5. Since the vector ONN is unavailable at subsector 4, there are still two redundant clamping modes, A-P and B-O.

Switching state sequences of different clamping modes at subsectors 3 and 4 are listed in Table II. It can be seen that only one bridge leg voltage varies in each switching state transition. Further, the initial vector of each clamping mode is PON. Thus, the minimum switching action is achieved in each subsector transition.

For the three-level three-phase Vienna-type rectifier, it is well known that positive small vectors, such as POO and PPO, have a negative effect on the NP voltage. On the contrary, negative small vectors, such as OON and ONN, have a positive effect on the NP voltage. Therefore, different clamping modes, such as B-O and C-N, have opposite effects on the NP voltage at subsector 3. Similarly, different clamping modes, such as B-O and A-P, have opposite effects on the NP voltage at subsector 4 as well. As a result, it is possible to regulate the NP voltage in each switching period by employing the redundant clamping modes in accordance with the deviation of upper and lower capacitor voltages.

As a front-end converter, to lower the voltage stress on switching devices and dc capacitors, the output dc voltage of the Vienna-type rectifier is usually not very high. Thus, it leads to a high MI. Since the MI is high, the dwell time of the reference vector at subsectors 3 and 4 is shorter than that of subsectors 5 and 6. Thus, with a relatively high MI, the controllability of NP voltage balance is weak at subsectors 3 and 4.

B. Clamping Modes at Subsectors 5 and 6

The vector diagram of subsectors 5 is depicted in Fig. 6, since vectors PNN and PON should be used at subsector 5, there are two redundant clamping modes A-P and C-N, as listed in Table III. Similarly, since vectors PPN and PON should be used at subsector 6, there are two redundant clamping modes, A-P and C-N at subsector 6 as well, as shown in Fig. 7.

From Table III, initial vectors of redundant clamping modes at the same subsector are different. However, there is still only one bridge leg switched in each switching state transition. Further,

TABLE III
REDUNDANT CLAMPING MODES AT SUBSECTORS 5 AND 6

Subsector	Clamping mode	Switching state sequence	Effect on NP voltage
5	A-P	POO PON PNN PON POO	Negative
	C-N	PON PNN ONN PNN PON	Positive
6	A-P	PPO PPN PON PPN PPO	Negative
	C-N	PPN PON OON PON PPN	Positive

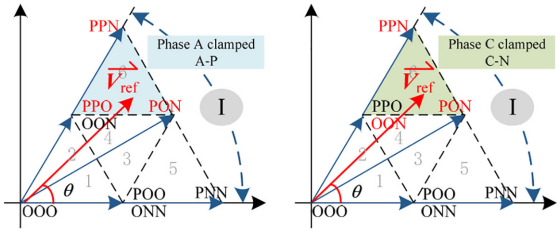

Fig. 7. Vector diagram of subsector 6. (a) Clamping mode A-P. (b) Clamping mode C-N.

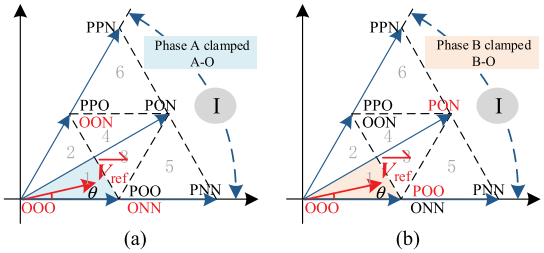

Fig. 8. Vector diagram of subsector 1. (a) Clamping mode A-O. (b) Clamping mode B-O.

different clamping modes, such as A-P and C-N, have opposite effects on the NP voltage at subsectors 5 and 6, respectively. As a result, the NP voltage can also be regulated in each switching period by employing redundant clamping modes at these subsectors.

C. Clamping Modes at Subsectors 1 and 2

When the MI is lower than 0.5, the reference vector is located at subsectors 1 and 2. Therefore, it is also necessary to analyze redundant clamping modes at these two subsectors.

As mentioned earlier, to avoid input alternating currents distortion, the vector OOO is the only available zero vector for the Vienna-type rectifier. Thus, three-phase bridge voltages can only be clamped to 0 (O) at subsectors 1 and 2. Since the small vector PPO is unavailable at subsector 1, there are two redundant clamping modes, A-O and B-O, as depicted in Fig. 8. Similarly, the small vector ONN is unavailable at subsector 2. Therefore, there are two redundant clamp modes, C-O and B-O as well, as depicted in Fig. 9. Switching states sequences of different clamping modes at subsectors 1 and 2 are listed in Table IV. The initial vector of each clamping mode is OOO; thus, the minimum switching action is achieved in each switching state transition. Further, different clamping modes have opposite effects on the NP voltage at subsectors 1 and 2. As a result, the NP voltage

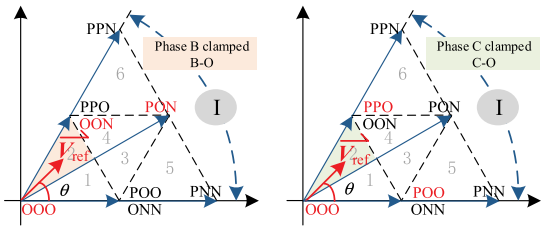

Fig. 9. Vector diagram of subsector 2. (a) Clamping mode B-O. (b) Clamping mode C-O.

TABLE IV
REDUNDANT CLAMPING MODES AT SUBSECTORS 1 AND 2

Subsector	Clamping mode	Switching state sequence	Effect on NP voltage
1	B-O	OOO POO PON POO OOO	Negative
	A-O	OOO OON ONN OON OOO	Positive
2	C-O	OOO POO PPO POO OOO	Negative
	B-O	OOO OON PON OON OOO	Positive

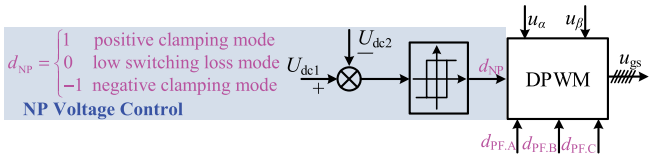

Fig. 10. NP voltage balance and power factor control diagram of the proposed MDPWM.

can also be regulated in each switching period by employing redundant clamping modes at subsectors 1 and 2.

Based on the earlier analysis, the NP voltage can be balanced in each switching period by using the proposed redundant clamping modes. Therefore, a MDPWM with NP voltage balance capability for three-phase Vienna rectifiers is realized.

III. NP VOLTAGE BALANCE CONTROL AND ANALYSIS

A. Implementation of NP Voltage Balance Control

The NP voltage control diagram of the proposed MDPWM is depicted in Fig. 10, where u_α and u_β represent the modulation signals of the α-axis and the β-axis. These modulation signals are generated by the outer dc voltage control and inner current control, so the conventional dual-loop control is not depicted in Fig. 10. $u_{\rm gs}$ represents the drive signals. $U_{\rm dc1}$ and $U_{\rm dc2}$ represent the upper and lower capacitor voltages, respectively. $\Delta u_{\rm dc}$ is the voltage difference between $U_{\rm dc1}$ and $U_{\rm dc2}$. $d_{\rm NP}$ represents the output signal of the NP voltage control. $d_{{\rm PF}.X}$ ($X = {\rm A, B, C}$) represents the directions of phase-X alternating current and voltage.

From Fig. 10, it can be seen that $d_{\rm NP}$ has three levels. The subsector 3 of the big sector I is taken as an example for the analysis. If $\Delta u_{\rm dc}$ reaches the upper limit, $d_{\rm NP}$ is set to 1. Then the clamping mode, C-N is used by the MDPWM scheme. If $\Delta u_{\rm dc}$ reaches its lower limit, $d_{\rm NP}$ is set to -1. Then the clamping mode, B-O is used by the MDPWM scheme. If $\Delta u_{\rm dc}$ is within the upper and lower limits, $d_{\rm NP}$ is set to 0. Then, the clamping mode with the minimum switching loss is used by the MDPWM

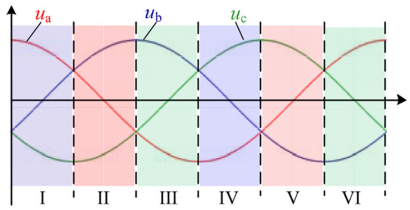

Fig. 11. Relationship of three-phase voltages and big sectors.

scheme. The switching loss of the redundant clamping modes depends on the amplitude of the clamping phase current at the same subsector. The relationship between three-phase voltages and big sectors is shown in Fig. 11.

As mentioned earlier, the utility grid voltage and input alternating current of the Vienna-type rectifier should be in phase. Therefore, the highest grid voltage represents the highest current. To minimize switching losses, it is preferred to keep the phase with the highest current unswitched. Thus, from Fig. 11, it is clear that phase-B current is the lowest one in big sector I. Therefore, if $d_{\rm NP}$ is set to 0, the clamping mode A-O will be used by the MDPWM scheme at subsector 1. Similarly, the clamping mode C-O is used by the MDPWM scheme at subsector 2. If $d_{\rm NP}$ is set to 0, the clamping mode C-N will be used by the MDPWM scheme at subsector 3. Similarly, the clamping mode A-P is used by the MDPWM scheme at subsector 4. Moreover, if $d_{\rm NP}$ is set to 0 at subsectors 5 and 6, the candidate clamping mode is dependent on the higher current of phase-A and phase-C.

It should be noted that the minimum switching loss cannot be maintained by using redundant clamping modes. Since there is a tradeoff between the low fluctuation of NP voltage and high switching times of redundant clamping modes, the upper and lower NP voltage limits should be carefully designed. In this article, the hysteresis voltage is set as 1% of the dc output voltage.

B. Analysis of Power Factor Variable Range

The Vienna-type rectifier has the ability of power factor compensation. In [24] and [29], both the carrier-based DPWM and continuous PWM for the Vienna-type rectifier operation with variable power factors were proposed. However, the NP voltage balance as well as the minimum switching loss has not yet been presented by the proposed MDPWM scheme.

Due to the uncontrollable switching devices, the applicable power factor of the Vienna-type rectifier is limited. The big section I is taken as an example for analysis, and the non-unity power factor is assumed. From Fig. 2, it is obvious that the direction of the phase-B alternating voltage and current may be opposite when θ is close to 30°. Thus, to solve this issue, the clamping mode B-O must be used near the phase-B zero-crossing point. Further, the applicable phase difference is determined by the angle region, where the clamping mode B-O can be used.

The applicable phase difference is depicted in Fig. 12. From Fig. 12, it can be seen that, when the MI is lower than 0.577, the reference vector is located at subsectors 1 and 2 or subsectors 1–4. Thus, the applicable phase difference is ±30°. When the MI is higher than 0.577, the angle region is dependent on the MI, which

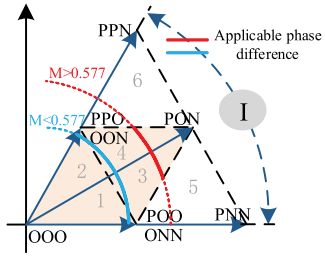

Fig. 12. Applicable phase difference in MDPWM.

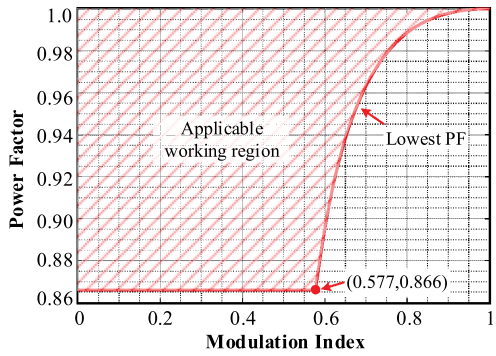

Fig. 13. Applicable power factors with different modulation indices by using MDPWM.

means that the higher MI leads to the smaller applicable phase difference. The allowed power factors with different modulation indices are depicted in Fig. 13, and it is almost the same as that of the carrier-based DPWM and continuous PWM proposed in [10] and [27].

Furthermore, as depicted in Fig. 10, a variable $d_{{\rm PF}.X}$ is introduced to represent the directions of phase-X alternating current and voltage, and could be represented as

$$d_{{\rm PF}.X} = \begin{cases} 1, & u_x i_x \le 0 \\ 0, & u_x i_x > 0. \end{cases} \quad (x = {\rm a}, {\rm b}, {\rm c}) \tag{2}$$

Taking phase-A as an example for analysis, when the directions of $u_{\rm a}$ and $i_{\rm a}$ are detected to be opposite, $d_{\rm PF.A}$ is set to one. Then, the phase-A voltage is clamped to A-O. As a result, when $d_{{\rm PF}.X}$ is set to one, the clamping mode is prior determined by the $d_{{\rm PF}.X}$. Thus, the NP voltage balance control is disabled at this time. However, because the applicable power factor of Vienna-type rectifiers is limited, it leads to a negligible effect on the NP voltage balance. Both the NP voltage balance and the power factor control could be well achieved by the proposed MDPWM.

C. Switching Loss Comparison

In order to illustrate the efficiency advantage of the proposed MDPWM, a switching process model of the Si-MOSFET is established, as depicted in Fig. 14, where $u_{\rm DS}$ is the drain-source voltage, and $i_{\rm D}$ represents the drain current [30].

One turn-ON process and one turn-OFF process are included in a switching period, and the following assumptions are considered in the model:

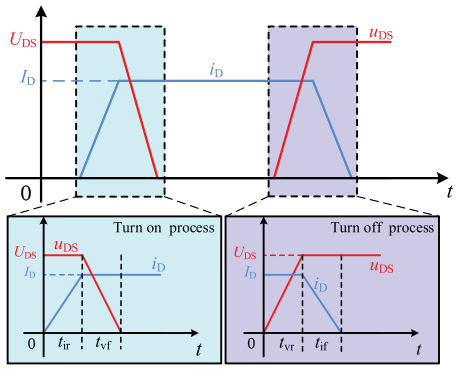

Fig. 14. Switching process of Si-MOSFET.

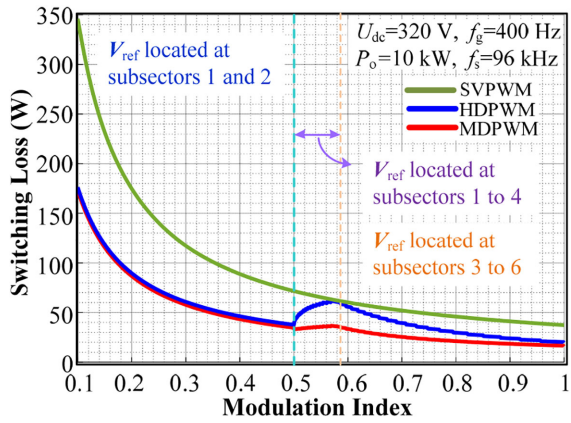

Fig. 15. Switching losses comparison of MDPWM, HDPWM, and SVPWM.

1) the system is already in a steady state;
2) the NP voltage is balanced;
3) the drain current can be considered as a constant in a switching period because of the high switching frequency.

Moreover, thanks to the SiC material, the switching loss of diodes is not included in this article.

Therefore, according to the switching model depicted in Fig. 14, when the bridge-leg voltage is not clamped, the switching loss of one Si-MOSFET in the kth switching period can be calculated by (3), where $t_{\rm ir}$ and $t_{\rm if}$ represent the rise and fall time of drain current, respectively. $t_{\rm vr}$ and $t_{\rm vf}$ represent the rise and fall time of drain-source voltage, respectively

$$P_{{\rm loss}.k} = \frac{1}{T_s}\int_0^{Ts} u_{\rm DS} i_{\rm D} dt = \frac{1}{2T_s} U_{{\rm DS}.k} I_{D.k} \left(t_{\rm ir} + t_{\rm if} + t_{\rm vr} + t_{\rm vf}\right). \quad (3)$$

When the bridge leg voltage is clamped, there is no switching loss, which means that $P_{{\rm loss}.k}$ is zero in the kth switching period.

The total switching times $M_{\rm f}$ in a fundamental period is calculated by (4), where $f_{\rm g}$ represents the fundamental frequency, and $f_{\rm s}$ is the switching frequency. Thus, the switching loss of the three-phase Vienna-type rectifier can be calculated by (5)

$$M_{\rm f} = \frac{f_{\rm s}}{f_{\rm g}} \quad (4)$$

$$P_{\rm loss} = 6 \times \sum_{k=1}^{M_{\rm f}} P_{{\rm loss}.k}. \quad (5)$$

The calculated switching loss of the three-phase Vienna-type rectifier with the proposed MDPWM, the HDPWM proposed in [19], and the conventional SVPWM is depicted in Fig. 15. The used specifications are listed in Table V. From Fig. 15, it can be seen that compared with the conventional SVPWM, the proposed MDPWM scheme can effectively reduce the switching loss with different modulation indices at rated power. When the MI is higher than 0.5, the switching loss of HDPWM increases rapidly due to SVPWM used at subsectors 3 and 4. When the MI is between 0.5 and 0.577, the clamping mode C-N and the clamping mode A-P are used at subsectors 3 and 4, respectively. Thus, the clamped bridge leg is not the phase with the highest current. As a result, the switching loss is increased, but it is still much lower than that of the HDPWM and SVPWM. Therefore, compared with the SVPWM and the HDPWM, the proposed MDPWM has the lowest switching loss over the whole MI.

Further, it is worth mentioning that since the dc output voltage is 320 V, the switching loss reduction is not significant. However, either higher output voltages or higher switching frequencies will lead to better efficiency superiorities of the proposed MDPWM scheme.

TABLE V
PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Parameter	Value
DC-link voltage	320 V
Input AC voltage	60 V - 115 V
Input AC frequency	400 Hz
Switching frequency	96 kHz
Filter inductor $L_{\rm f}$	68 uH
DC link capacitor $C_{\rm dc}$	660 uF
Si MOSFET (S_1 to S_6)	IPW60R041P6
SiC DIODE (D_1 to D_6)	C3D20060D
Cooling	Liquid Cooling

D. Simulation Results

To verify the effectiveness of NP voltage balance control and the feasibility of variable power factors operation, a MATLAB/Simulink model was built. The parameters are listed in Table V. Simulation results are shown in Fig. 16, where $u_{\rm a}$ and $i_{\rm a}$ represent the phase-A voltage and current. $\Delta u_{\rm dc}$ is the difference between upper and lower capacitor voltages. $d_{\rm NP}$ represents the output signal of the NP voltage control. $u_{\rm AO}$ is the differential mode (DM) voltage between the terminals A and O in Fig. 1. $d_{\rm PF.A}$ represents the directions of phase-A alternating current and voltage.

In Fig. 16(a), the MI is set at 0.48. It can be seen that there is no alternating current distortion after enabling the NP voltage balance control. The power factor can be regulated from 1 to 0.88, and the NP voltage is balanced as well. Further, when

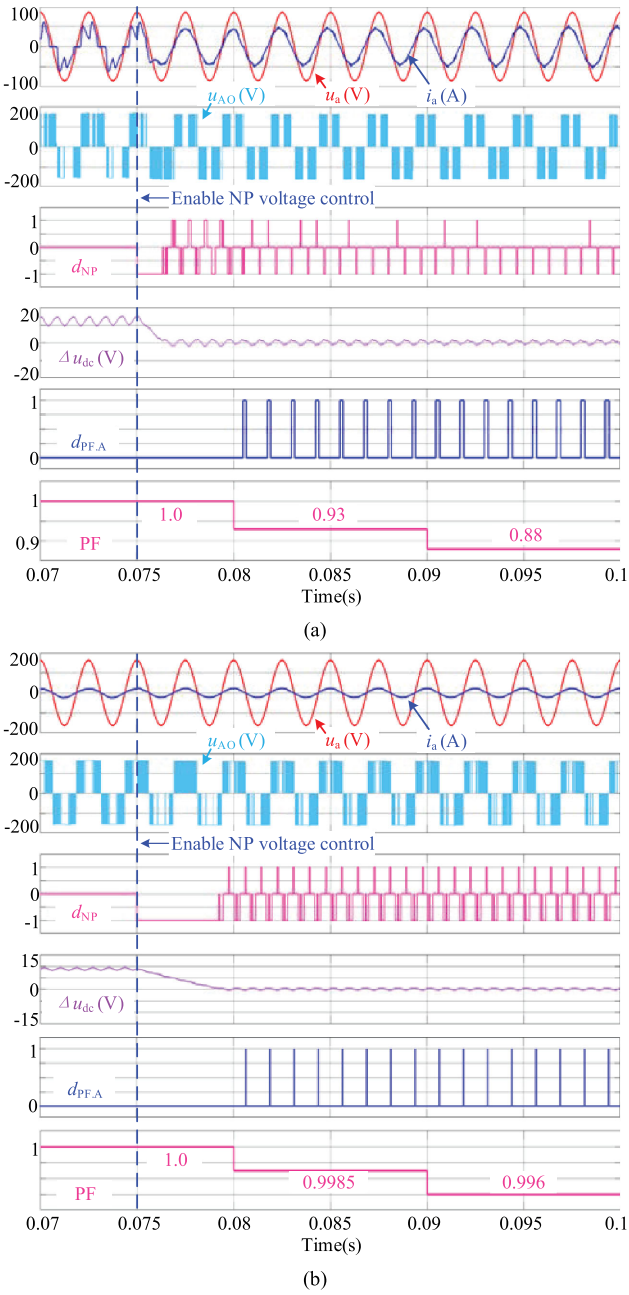

Fig. 16. Simulation results. (a) MI = 0.48. (b) MI = 0.88.

$d_{\mathrm{PF\_A}}$ is set to 1, u_{AO} is clamped to 0 (O). In Fig. 16(b), MI is set at 0.88, where the lowest applicable power factor is 0.996. When the power factor is decreased from 1 to 0.996, there is no alternating current distortion, and the NP voltage is balanced as well. Moreover, it is worth mentioning that by enabling the NP voltage control, the states of d_{NP} are changed between $-1, 0$, and 1, indicating that clamping modes are switched. However, d_{NP} is mainly kept in "0" state, which indicates that the NP voltage balance as well as the minimum switching loss is achieved with different modulation indices and power factors. This is the main advantage of the proposed MDPWM compared with the previous work.

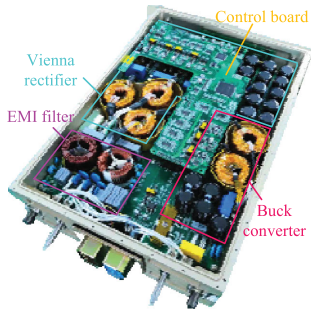

Fig. 17. Prototype of the three-phase Vienna-type rectifier.

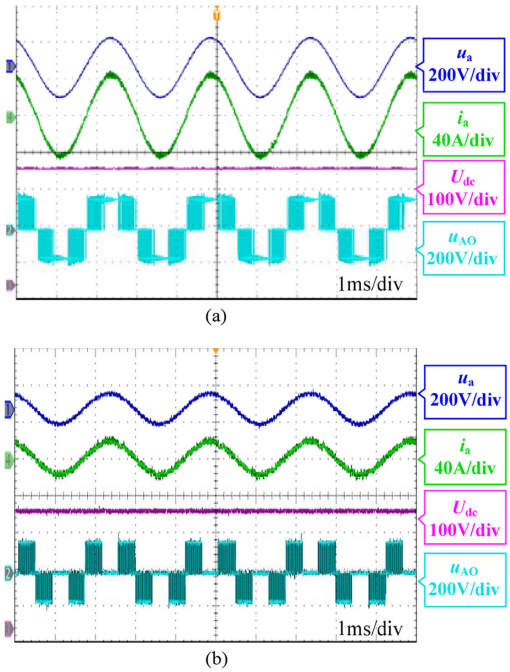

Fig. 18. Steady-state waveforms of the proposed MDPWM with different input alternating voltages. (a) $u_{\mathrm{ac}} = 115$ V. (b) $u_{\mathrm{ac}} = 60$ V.

IV. Experimental Results

A 10-kW Vienna-type rectifier prototype was built to verify the validity of the proposed MDPWM scheme. The specifications of the prototype are listed in Table V. The efficiencies and THD are measured by a power analyzer WT 1800. The rectifier is powered by a programmable ac source 61512 and connected to an electronic load 63206A-1200-240.

The modulation scheme is driven by a digital signal processor TMS320F28335 and a complex programmable logic device EPM570T100. Fig. 17 presents the photograph of the prototype.

The steady-state waveforms by using the proposed MDPWM scheme with different utility grid voltages are shown in Fig. 18, where u_{a} and i_{a} represent the phase-A voltage and current. U_{dc} represents the dc output voltage. u_{AO} is the DM voltage between the terminals A and O in Fig. 1. In Fig. 18(a), the utility grid voltage is 115 V, and the output power is 10 kW. It can be seen that the DM voltage of phase-A is clamped to $+U_{\mathrm{dc}}/2$ (P) around its peak current. It indicates that the bridge leg with the highest

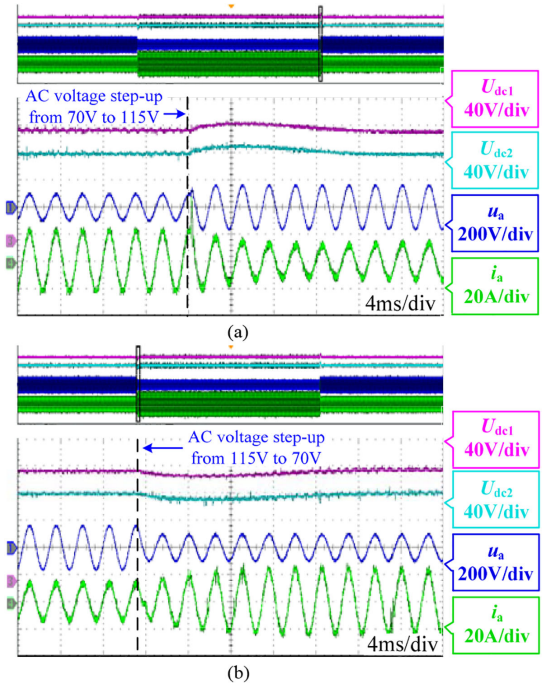

Fig. 19. Dynamic waveforms of the NP voltage under input alternating voltages step-up and step-down conditions. (a) Input ac voltages step-up from 70 to 115 V. (b) Input ac voltages step-down from 115 to 70 V.

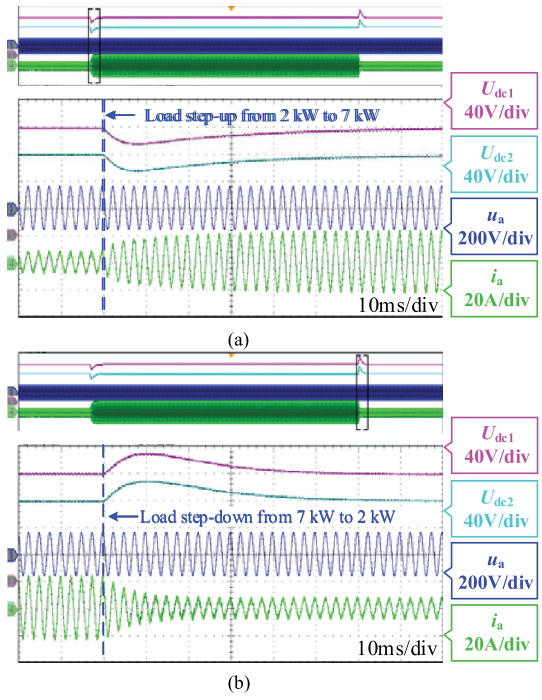

Fig. 20. Dynamic waveforms of the NP voltage under output power step-up and step-down conditions. (a) Output power step-up from 2 to 7 kW. (b) Output power step-down from 7 to 2 kW.

current is unswitched. In Fig. 18(b), the utility grid voltage is 60 V, and the output power is 4 kW. It can be seen that the DM voltage of phase-A can also be clamped to 0 (O) around its peak current. Further, in Fig. 18(a) and (b), there is no input alternating current distortion near the zero-crossing point of

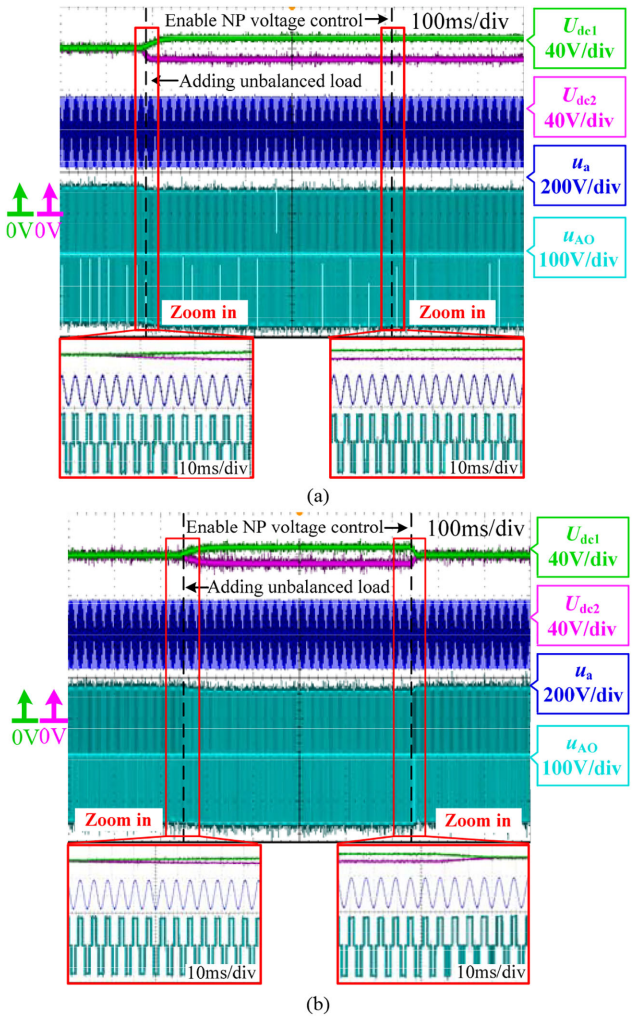

Fig. 21. Dynamic waveforms of different modulation schemes. (a) NP voltage balance control with HDPWM proposed in [19]. (b) NP voltage balance control with the proposed MDPWM.

phase-A, which indicates the correctness of the clamping mode selection. The experimental results are also consistent with the description shown in Fig. 2.

The dynamic waveforms by using the proposed MDPWM scheme with different input alternating voltages and output power are shown in Figs. 19 and 20, respectively, where $U_{\rm dc1}$ and $U_{\rm dc2}$ represent the upper and lower dc capacitor voltage, respectively.

In Fig. 19(a), the utility grid voltage is step-up from 70 to 115 V. Thus, the MI varies from 0.54 to 0.88. In Fig. 19(b), the utility grid voltage is step-down from 115 to 70 V. Thus, the MI varies from 0.88 to 0.54. It can be seen that the upper and lower capacitor voltages are balanced when the MI is abruptly changed. It indicates that the proposed MDPWM can balance the NP voltage with a wide range of modulation indices.

In Fig. 20(a), the output power is step-up from 2 to 7 kW. In Fig. 20(b), the output power is step-down from 7 to 2 kW. It can be seen that the upper and lower capacitor voltages are also well balanced by the proposed MDPWM scheme when the output power is abruptly changed.

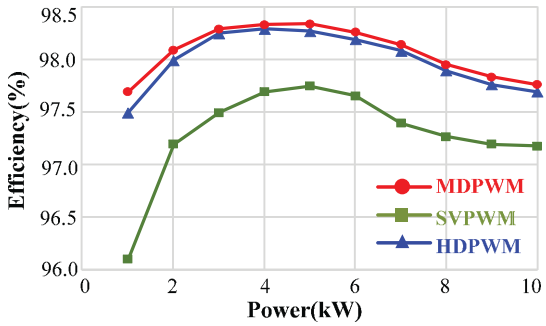

Fig. 22. Measured efficiencies of MDPWM, HDPWM, and SVPWM.

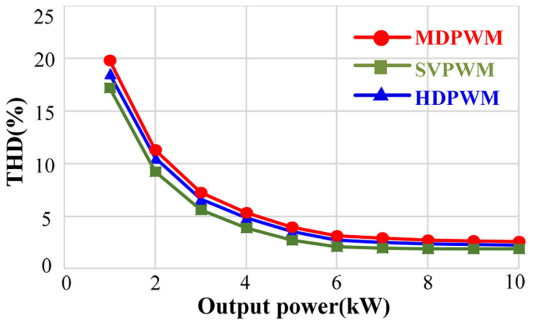

Fig. 23. Measured current THD of MDPWM, HDPWM, and SVPWM.

The waveforms of the NP voltage balance control by using HDPWM and MDPWM are shown in Fig. 21. To demonstrate the NP voltage balance control clearly, one of dc capacitors is connected with an additional resistor to achieve the unbalanced upper and lower capacitor voltages. The utility grid voltage is 115 V, and the dc output voltage is 320 V.

From Fig. 21, it can be seen that upper and lower capacitor voltages can be balanced by enabling the proposed MDPWM scheme even if the load of upper and lower capacitors is unbalanced. However, upper and lower capacitor voltages cannot be rebalanced by the HDPWM proposed in [19]. Since the MI is 0.84, the dwell time of the reference vector at subsectors 5 and 6 is much longer than that of subsectors 3 and 4. However, the NP voltage can only be balanced by the HDPWM at subsectors 3 and 4. Therefore, the proposed MDPWM shows the stronger NP voltage balance capability compared with the HDPWM.

The efficiency comparison among the SVPWM, the HDPWM, and the proposed MDPWM is depicted in Fig. 22. The utility grid voltage is 115 V, and the dc output voltage is 320 V. From Fig. 22, it is clear that the proposed MDPWM has the highest efficiency, and the peak efficiency of MDPWM is 98.35%.

The current THD comparison among the SVPWM, the HDPWM, and the proposed MDPWM is depicted in Fig. 23. It can be seen that the SVPWM has the best THD performance because the seven-segment switching sequence is employed in the conventional SVPWM. However, the five-segment switching sequences are used in MDPWM. Therefore, the THD of MDPWM is the highest. Fortunately, when the output power is higher than 5 kW, the THD of MDPWM is lower than 5%, which can also meet the THD requirement in aircraft systems. Moreover, the THD of MDPWM at rated output power is 2.5%.

V. Conclusion

In this article, a MDPWM is proposed to regulate the NP voltage by using the redundant clamping modes. Therefore, the NP voltage is regulated within the switching period. Analysis and experimental results demonstrate the following features of the proposed MDPWM scheme.

1) The NP voltage can be strongly balanced by using the proposed MDPWM scheme, and the capacitor voltage fluctuations are very small.
2) Compared with SVPWM and HDWPM, the efficiency of the proposed MDPWM is enhanced, and the THD performance of the proposed MDPWM is improved as well.
3) Since the switching loss is mainly reduced by the MDPWM, either higher output voltages or higher switching frequencies will lead to better efficiency superiorities of the proposed MDPWM scheme.

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