A Dual Active Clamp DC–DC Converter With High Voltage Gain

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***Abstract*—In this article, a novel dual active clamp converter with high voltage gain is proposed for dc–dc applications. The active clamps' switches turn ON and OFF under zero-current switching (ZCS). In addition, the main switch turns ON under ZCS condition, as well. Therefore, switching losses are significantly reduced. The converter is also capable of operating under quasi-resonance (QR) mode. In this mode, switching losses are reduced further by lowering the voltage and current, at which the main switch turns OFF. In comparison with the conventional interleaved converter, the voltage gain of the proposed converter is almost the same, but the number of semiconductors and switching loss are significantly reduced. The switching frequency of the active clamps' switches is half of the main switching frequency. The operation principles of the proposed converter are studied in both pulsewidth modulation and QR modes, and the advantages are investigated. A 200-W prototype is implemented to validate the desired functionality of the converter, and experimental results are compared in both modes.**

***Index Terms*—Active clamp circuit, dc–dc converter, double frequency, high step-up, soft switching.**

I. Introduction

RENEWABLE energy sources (RES) will have a significant role in supplying the required power in the near future. Therefore, improving the ways these sources are utilized is of high importance. Despite the variety in the characteristics of different types of RESs, some common problems exist in most of them. One can consider photovoltaic (PV) and fuel cell (FC) systems as two prominent candidates. Due to the intrinsic features, the output voltage of these systems is much lower than the desired value, suitable for being connected to the utility grid. Using power electronics converters is necessary to connect a RES to the grid or a load [1]–[4]. Hence, it seems reasonable to retrofit the converters to overcome the low-voltage problem of RESs. There are many methods, and topologies proposed to increase the voltage level. A simple boost convert is a basic solution which functions acceptably in low voltage gains. However, in most of the cases, a high voltage gain converter is needed. Increasing the duty cycle in a boost converter results in low efficiency, diode reverse recovery problem, and electromagnetic interference (EMI) [5], [6]. Cascaded/multilevel boost converters are proposed to overcome such limitations. These converters benefit from modularity feature that makes it possible to reach higher voltage gains. But using the increased number of elements causes higher costs, more complex control, and low power density [7]. DC–DC step-up converters based on a transformer or a coupled inductor are suggested as an alternative idea [8]–[14]. These converters provide galvanic isolation, and voltage gain can be obtained by adjusting the turn ratio of the magnetic elements. The application of the converters with high turn ratio transformers/coupled-inductors is limited due to some drawbacks. The design of transformers/inductors for high-voltage/power applications is difficult and costly. Also, the large size of these elements decreases the power density [15], [16]. The main defect is related to the leakage inductance, which limits the voltage gain. Moreover, in the converters with hard switching condition, it causes high voltage spikes across the switches that increases power loss, and decreases the lifespan of the switches [17]. In order to overcome these problems, interleaved dc–dc converters have been introduced. They are claimed to be a suitable solution to reach higher voltage/power levels [18]–[23]. In this type, two or more converters contribute to the voltage boosting process. These converters are connected in parallel at the input and series at the output side. Using magnetic elements provides electrical isolation as it brings soft-switching possibilities. Since in the interleaved structure, some partial scale transformers are utilized, the disadvantages related to high turn ratio transformers are relieved. Connecting many converters in parallel at the input side raises the capability to operate at higher power ranges. However, using an increased number of elements, especially semiconductors, is the most crucial challenge associated with interleaved dc–dc converters [10]. It can result in more weight, large size, and more importantly, increase in the cost. Hence, any effort to reduce the number of the components while preserving/improving the performance of the converter is significantly important.

In this article, a dual active clamp (DAC) converter with a reduced number of elements is proposed. This converter copes with most of the above-mentioned demands. By reducing the number of elements, in comparison with the interleaved converters, the cost is lowered as higher power density is achieved. The proposed converter is highly efficient because of full soft-switching operation (at both turn-ON and -OFF moments) of

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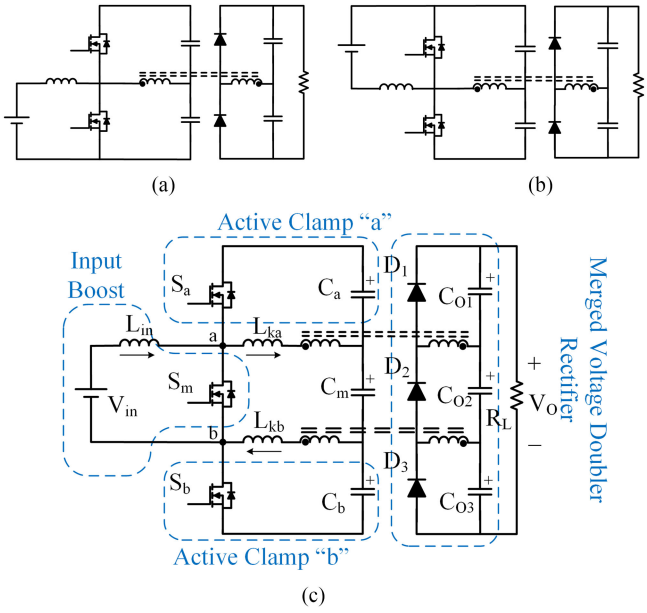

Fig. 1. (a) Conventional ISBC. (b) ISBC in reverse structure. (c) Proposed converter.

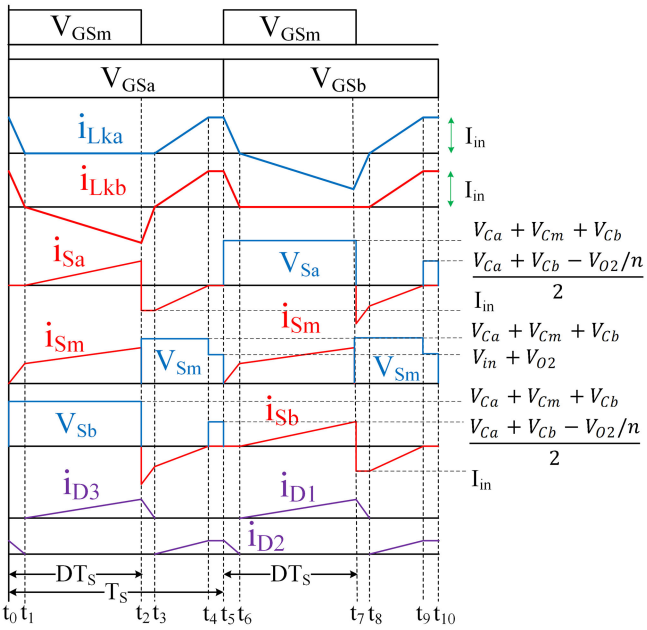

Fig. 2. Key waveforms of the proposed converter.

two auxiliary switches, and turn-ON ZCS operation of the main switch.

The process by which the topology of the proposed converter is derived is investigated as follows. A conventional isolated soft-switched boost converter (ISBC), suggested in [12] and [13], is presented in Fig. 1(a). Such a converter has a reasonable switching loss because of soft-switching operation. However, to achieve higher voltage gain, the interleaved ISBC (IISBC) is taken into account [22], [23]. The circuit shown in Fig. 1(b) presents the same functionality of the ISBC illustrated in Fig. 1(a). To obtain the proposed converter, the converters shown in Fig. 1(a) and (b) are merged together to achieve the converter depicted in Fig. 1(c) where, in comparison with an IISBC, two capacitors, one switch, and one diode are eliminated.

The operation of the proposed converter in the pulsewidth modulated (PWM) and quasi-resonant (QR) modes is investigated in two subsections in Section II. Voltage gain studies for two operation modes are presented in Section III and soft-switching condition is discussed in Section IV. Section V provides simulation results, where a comparison is carried out among the proposed converter and conventional interleaved converters in [22] and [23]. In Section VI, the experimental results are presented, and the operation of the converter in both modes is compared. Finally, a conclusion is provided in Section VII.

II. Operation Principles of the Proposed Converter

In this section, the operation of the proposed DAC converter at different intervals of a switching cycle is inspected for the PWM and the QR modes.

A. PWM Operation Mode

In this mode, the capacitors and the input inductance are assumed to be large enough to ensure constant voltages and input current, respectively. In addition, the switches are considered to be ideal, and the leakage inductances are supposed to have the same value, i.e., $L_{ka} = L_{kb} = L_k$. In the proposed converter, L_{in} is the input inductor and S_m is the main switch. Two active clamp circuits are realized by C_a, S_a and C_b, S_b. The operating frequency of S_a and S_b is half of the switching frequency of the main switch. Switches S_a and S_b operate complementary with duty cycles equal to 0.5. In the secondary side, D_1, D_2, D_3, C_{O1}, C_{O2}, and C_{O3} form a merged voltage doubler rectifier. The key waveforms are plotted in Fig. 2. Considering the waveforms, ten intervals can be specified in each switching cycle under steady-state condition. However, because of the symmetrical structure of the converter, the first five intervals are similar to the second five intervals, except for S_b and D_1, which operate instead of S_a and D_3, respectively. Therefore, just half of a switching period is discussed here. Fig. 3 provides the equivalent circuit of the first five intervals. The detailed study of each interval is as follows.

Interval 1 [t_0–t_1]*:* At t_0, gate-pulse of the switch S_b is removed, and turn-ON command is applied to S_m and S_a. Since S_m is connected to magnetic components, its current rises gently from zero, and it turns ON under ZCS condition. In this interval, only diode D_2 is conducting. Therefore, the secondary windings have equal current value, which implies the same current in the primary windings. Consequently, no current flows through S_a, despite its gate having been activated. This results in ZCS turn-ON for S_a at the beginning of the next interval. The input inductor L_{in} and the capacitor C_m are being charged in this interval. The amount of current variation in the leakage inductances can be calculated as

$$\Delta i_{Lka}(t_1-t_0)=\Delta i_{Lkb}(t_1-t_0)=\frac{(t_1-t_0)}{2L_k}\left(V_{\text{in}}+\frac{V_{O1}}{n}\right)=I_{\text{in}} \quad (1)$$

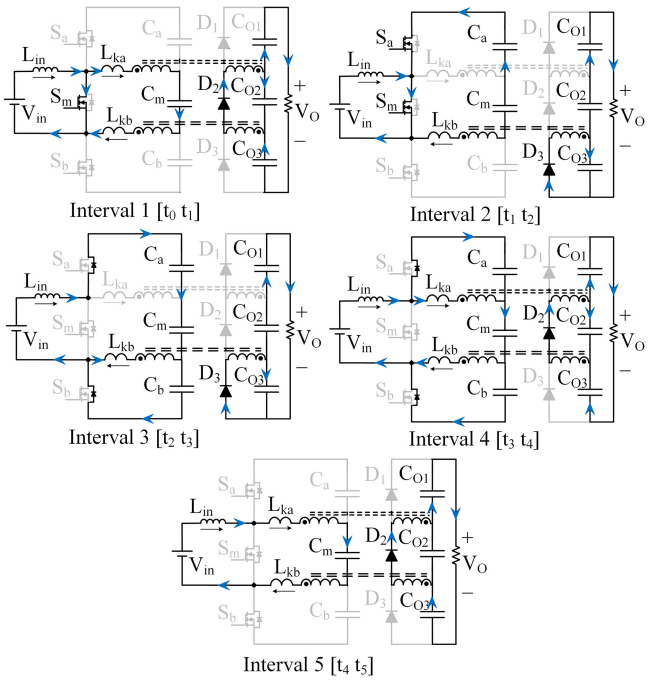

Fig. 3. Equivalent circuit of the proposed converter in each interval.

where V_{in} and I_{in} are the input voltage and current, respectively. V_{O1} is the voltage across C_{O1}, and n is the turn ratio of the transformers ($n = N_2/N_1$). As the current through D_2 descends to zero, it turns OFF under ZCS condition and interval 1 ends.

Interval 2 [t_1–t_2]*:* At the moment t_1, the diode D_3 turns ON. The current through L_{kb} changes its direction, but i_{Lka} remains zero. This inequality between i_{Lka} and i_{Lkb} causes S_a to start conduction. Since S_m is also conducting, the input inductance continues its charging. The value of i_{Lkb} at the end of this interval is given by

$$\Delta i_{Lkb}\,(t_2 - t_1) = \frac{(t_2 - t_1)}{2L_k}\left(V_{\text{in}} + V_{Ca} - \frac{V_{O3}}{n}\right). \tag{2}$$

In (2), V_{Ca} and V_{O3} are the voltages across the capacitors C_a and C_{O3}, respectively. The circuit operates in this condition until S_m turns OFF.

Interval 3 [t_2–t_3]*:* As S_m turns OFF, the input current flows through the body diode of S_a. Therefore, at t_2, i_{Sa} is reversed immediately and becomes negative. In this condition, the voltage across S_a is zero, while its gate-pulse is still high. Also, the body diode of S_b conducts $I_{\text{in}} + i_{Lkb}$. Among the output diodes, only D_3 is conducting and this interval ends when i_{D3} settles down to zero. The variation of current passing through L_{kb} can be obtained by

$$\Delta i_{Lkb}\,(t_3 - t_2) = \frac{(t_3 - t_2)}{2L_k}\left(V_{Cb} + \frac{V_{O3}}{n}\right) \tag{3}$$

where V_{Cb} is the voltage of capacitor C_b.

Interval 4 [t_3–t_4]*:* At the moment t_3, the current through L_{kb} changes its direction, and D_3 turns OFF, while D_2 is turned ON. Similar to the first interval, the conduction of D_2 implies equal current values in L_{ka} and L_{kb}. In this interval, as shown in Fig. 3, the input current value is more than the current flowing through the leakage inductances. Hence, the body diodes of S_a and S_b conduct the excessive current. Capacitors C_a, C_m, and C_b continue getting charged and the current through leakage inductances increases up to I_{in}. At the end of this interval, the currents passing through S_a and S_b become zero, and their antiparallel diodes turn OFF under ZCS condition. The current change value in the leakage inductances during interval 4 is obtained by

$$\begin{aligned}\Delta i_{Lka}(t_4 - t_3) &= \Delta i_{Lkb}(t_4 - t_3)\\ &= \frac{(t_4 - t_3)}{2L_k}\left(V_{Ca} + V_{C_b} - \frac{V_{O2}}{n}\right) = I_{\text{in}}\end{aligned} \tag{4}$$

where V_{O2} is the voltage of capacitor C_{O2}.

Interval 5 [t_4–t_5]*:* During this interval, as indicated in Fig. 3, none of the three switches are carrying current. The constant input current, passing through the leakage inductances, charges the capacitor C_m, while at the output side, only D_2 is conducting. The switch S_m is turned ON at t_5 and interval 5 ends.

B. QR Operation Mode

Minimizing switching loss is vital to increase the efficiency of a converter. Since in a switching converter, switching loss is a considerable portion of the total power loss, the QR operation is employed in this converter. It is an effective technique to reduce the switching loss. The switches S_a and S_b both turn ON and OFF under soft-switching condition, and so is the turn-ON of the switch S_m. So, considering that all diodes turn OFF under ZCS condition, the only switching loss occurs at the turn-OFF moment of switch S_m.

Reducing the value of the capacitor C_m expands the resonance frequency between C_m and the leakage inductances.

As a result of the resonant operation, S_m turns OFF at lower current and voltage, leading to lower switching loss. To achieve QR mode, the conduction duration of S_m should be more than half of the resonant period, so

$$DT_S \geq \frac{T_r}{2} = \pi\sqrt{L_k C_m} \tag{5}$$

$$C_m \leq \frac{D^2 T_S^2}{\pi^2 L_k} \tag{6}$$

where T_r is the resonant period. It is helpful to analyze each interval separately, to make the converter's operation clear in resonance mode and obtain the principal equations. The key waveforms and the equivalent circuit of the converter in different intervals are presented in Figs. 4 and 5, respectively.

Interval 1 [t_0–t_1]*:* In this interval, the operation of the converter is similar to the first interval in the previous section. the amount of current variation in L_{ka} and L_{kb} is determined by

$$\begin{aligned}\Delta i_{Lka}\,(t_1 - t_0) &= \Delta i_{Lkb}\,(t_1 - t_0)\\ &= \frac{(t_1 - t_0)}{2L_k}\left(V_{\text{in}} + \frac{\Delta V_{Cm}}{2} + \frac{V_{O2}}{n}\right) = I_{in}\end{aligned} \tag{7}$$

where ΔV_{Cm} is the voltage variation of capacitor C_m (shown in Fig. 4).

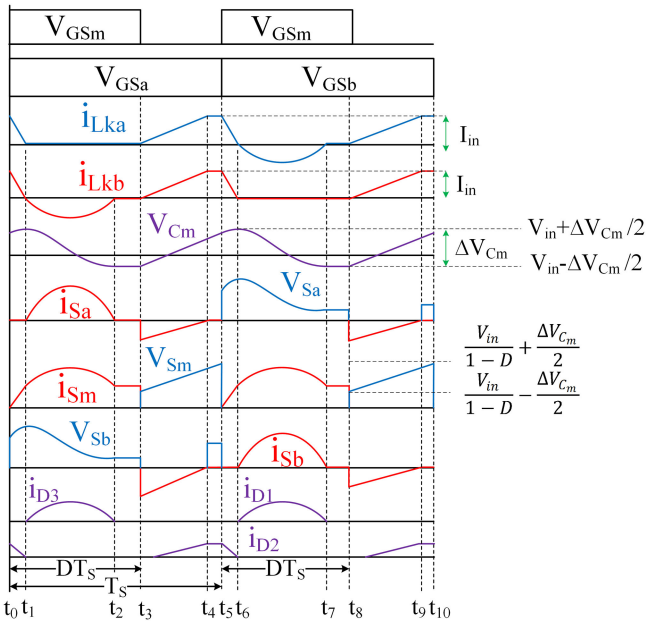

Fig. 4. Key waveforms of the proposed converter in resonance mode operation.

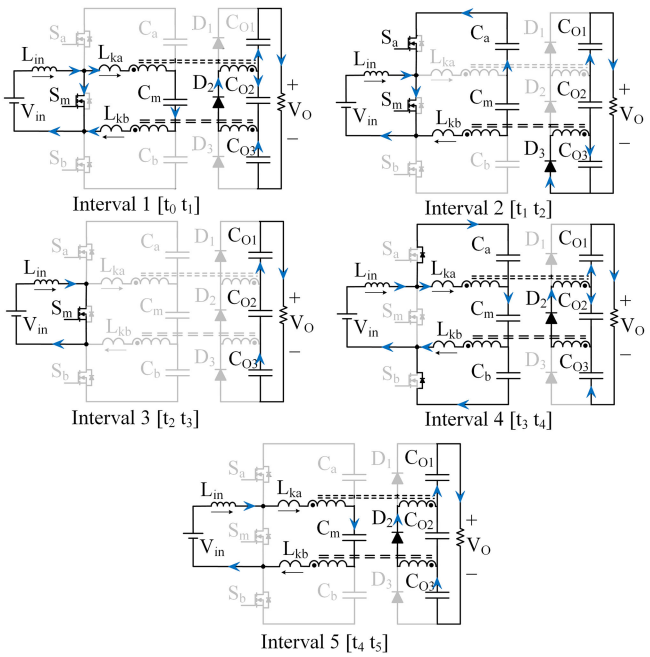

Fig. 5. Equivalent circuit of the proposed converter in each interval for resonance mode operation.

Interval 2 [t_1–t_2]*:* The operation of the converter in this interval is similar to the second interval in the previous section, but as shown in Fig. 4, in this mode, C_m and L_{kb} form a resonant circuit. The resonant current is

$$i_{Lkb}(t_2-t)=\frac{\left(V_{in}+\frac{\Delta V_{Cm}}{2}+V_{Ca}-\frac{V_{O3}}{n}\right)}{\sqrt{L_k/C_m}}\sin\left(\omega_r\left(t_2-t\right)\right) \tag{8}$$

where ω_r is the angular resonant frequency ($\omega_r=1/\sqrt{L_kC_m}$). As the current passing through the leakage inductance reaches zero, this interval ends.

Interval 3 [t_2–t_3]*:* In this interval, only S_m conducts, and the converter enters into discontinuous conduction mode (DCM). As a result, when S_m is turned OFF, this interval ends.

Interval 4 [t_3–t_4]*:* At the moment t_3, the converter operates just like the fourth interval in the previous section, but in this mode, C_m is charged from $V_{\rm in}-\Delta V_{Cm}/2$ to $V_{\rm in}+\Delta V_{Cm}/2$. Therefore, the blocking voltage across S_m increases from $V_{\rm in}/(1-D)-\Delta V_{Cm}/2$ to $V_{\rm in}/(1-D)+\Delta V_{Cm}/2$ (as shown in Fig. 4). This introduces an additional improvement in switching loss reduction, because the voltage and the current at which S_m is turned OFF are declined (more discussion is presented in later sections). At the end of this interval, the leakage inductances' current reaches the input current value as calculated in the following:

$$\begin{aligned}\Delta i_{Lka}(t_4-t_3)&=\Delta i_{Lkb}(t_4-t_3)\\&=\frac{(t_4-t_3)}{2L_k}\left(V_{Ca}+V_{Cb}-\frac{V_{O2}}{n}\right)=I_{\rm in}.\end{aligned} \tag{9}$$

Interval 5 [t_4–t_5]*:* In this interval, the converter operates as in the fifth interval of the previous section. A similar analysis is valid for the next five intervals. For the corresponding intervals, the waveforms of i_{Lka}, i_{Lkb}, i_{Sb}, i_{sa}, i_{D1}, and i_{D3} are just like those of i_{Lkb}, i_{Lka}, i_{Sa}, i_{sb}, i_{D3}, and i_{D1} in the former five intervals.

III. Voltage Gain Studies

A. PWM Operation Mode

In this section, the voltage gain of the proposed converter in the PWM mode is discussed. Under steady-state condition, the average voltage across each inductor, in a switching cycle, has to be zero. Applying this fact on the input inductor $L_{\rm in}$ yields

$$DV_{\rm in}=(1-D)\left(V_{C_a}+V_{C_b}\right) \tag{10}$$

where D is the duty cycle of S_m. Interval 5 is negligible due to its short duration compared to the other intervals. Because of the symmetrical topology of the converter, it can be claimed that $V_{Ca}=V_{Cb}$. Hence, the following can be derived from (10):

$$V_{C_a}=V_{C_b}=\frac{DV_{\rm in}}{2(1-D)}. \tag{11}$$

On the other hand, since the average current passing through a capacitor has to be zero in each cycle, it can be concluded that the output current is equal to the average current of D_2 during T_S or the average current of D_1 or D_3 during $2T_S$. Since the diodes' currents are formed by leakage inductances' current, the output current (I_O) can be presented as

$$I_O=\frac{1}{T_s}\int_{t_3}^{t_6}\frac{1}{n}i_{Lk}(t)\,.dt=\frac{1}{2T_s}\int_{t_1}^{t_3}\frac{1}{n}i_{Lk}(t)\,.dt. \tag{12}$$

The following equation can be derived using (2), (4), and (12) where the first, third, and fifth intervals are neglected because

of short durations:

$$(1-D)^2\left(\frac{DV_{\text{in}}}{1-D}-\frac{V_{O_2}}{n}\right)=D^2\left(\frac{(2-D)\,V_{\text{in}}}{2\,(1-D)}-\frac{V_{O_3}}{n}\right). \tag{13}$$

Simplifying (13) results in

$$(1-D)^2V_{O_2}-D^2V_{O_3}=\left(\frac{D\left(2-6D+3D^2\right)}{2\,(1-D)}\right)nV_{\text{in}}. \tag{14}$$

The symmetry of the converter suggests that $V_{O1}=V_{O3}$. As a result, applying KVL at the output loop yields

$$V_{O_2}+2V_{O_3}=V_O. \tag{15}$$

V_{O2} and V_{O3} can be calculated as (16) and (17), respectively, in the following, by combining (12) and (13):

$$V_{O_2}=\frac{D^2V_O}{2-4D+3D^2}+\frac{D\left(2-6D+3D^2\right)nV_{\text{in}}}{(1-D)\,(2-4D+3D^2)} \tag{16}$$

$$V_{O_3}=\frac{(1-D)^2V_O}{2-4D+3D^2}-\frac{D\left(2-6D+3D^2\right)nV_{\text{in}}}{2\,(1-D)\,(2-4D+3D^2)}. \tag{17}$$

As mentioned before, the output current is the average current passing through D_1 within $2T_S$. In other words, according to (2) one can state that

$$I_O=\frac{V_O}{R_L}=\frac{DT_s}{2nL_k}\left(V_{\text{in}}+V_{C_a}-\frac{V_{O_3}}{n}\right). \tag{18}$$

Finally using (11), (17), and (18), the voltage gain is obtained as

$$\frac{V_O}{V_{\text{in}}}=\frac{2n}{\left(1+\frac{4n^2L_k(2-4D+3D^2)}{(1-D)^2D^2R_LT_s}\right)(1-D)}. \tag{19}$$

B. QR Operation Mode

In the QR mode, during interval 2, capacitor C_m is discharged by the current passing through the leakage inductance L_{kb}. According to Fig. 4, the value of maximum ripple in V_{Cm} can be calculated as

$$\begin{aligned}\Delta V_{C_m}&=\frac{1}{C_m}\int_{t_1}^{t_2}i_L\,(t)\,.dt\\&=\frac{\left(V_{in}+\frac{\Delta V_{C_m}}{2}+V_{C_a}-\frac{V_{O_3}}{n}\right)}{\sqrt{C_m.L_k}}\int_{t_1}^{t_2}\sin\,(\omega_r t)\,.dt.\end{aligned} \tag{20}$$

Since the duration of interval 2 equals half the resonance period, i.e., $t_2-t_1=\frac{T_r}{2}=\pi\sqrt{C_m.L_k}$, (20) is rewritten as

$$\Delta V_{C_m}=\frac{2\sqrt{C_m.L_k}}{C_m\sqrt{\frac{L_k}{C_m}}}\left(\frac{(2-D)\,V_{\text{in}}}{2\,(1-D)}+\frac{\Delta V_{C_m}}{2}-\frac{V_{O_3}}{n}\right). \tag{21}$$

As a result, V_{O3} is calculated as

$$V_{O_3}=\frac{n\,(2-D)\,V_{\text{in}}}{2\,(1-D)}. \tag{22}$$

As mentioned before, the output current is equal to the average current of D_2 within T_S. Neglecting interval 1 because of its short duration, the following equation is derived using (7):

$$I_O=\frac{V_O}{R_L}=\frac{(1-D)\,T_S}{2nL_k}\left(V_{C_a}+V_{C_b}-\frac{V_{O_2}}{n}\right). \tag{23}$$

Equation (23) is rewritten as follows, using (11), (15), and (22):

$$\frac{V_O}{R_L}=\frac{(1-D)^2T_S}{4L_k}\left(\frac{2V_{\text{in}}}{1-D}-\frac{V_O}{n}\right). \tag{24}$$

Eventually, voltage gain for the resonance condition is calculated as

$$\frac{V_O}{V_{\text{in}}}=\frac{2n}{\left(1+\frac{4n^2L_k}{(1-D)^2R_LT_s}\right)(1-D)}. \tag{25}$$

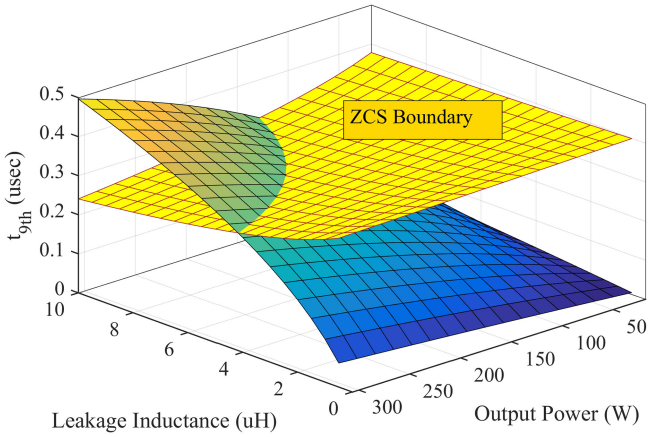

Fig. 6. ZCS condition for the main switch.

IV. Soft-Switching Analysis

Since soft-switching plays a crucial role in efficiency enhancement, in this section, soft-switching condition of the switches is analyzed.

A KCL on node "a" reveals

$$i_{Sm}=I_{\text{in}}-i_{Lka}+i_{Sa}. \tag{26}$$

At the beginning of the first interval, i_{Sa} is zero. Hence, to guarantee ZCS for S_m, i_{Lka} in the previous intervals (ninth and tenth intervals) should reach I_{in}. Therefore, the forth (and the ninth) interval duration has to be less than $(1-D)T_S$, so that i_{Lka} has enough time to rise from zero to I_{in}. So, based on (4) (and (9))

$$t_{9th}=t_4-t_3=\frac{2L_kI_{\text{in}}}{\left(V_{Ca}+V_{Cb}-\frac{V_{O2}}{n}\right)}. \tag{27}$$

Also, ZCS constraint for S_m is

$$t_{9th}<(1-D)\,T_S \tag{28}$$

where $t_{9\text{th}}$ is the time duration of the ninth interval. As far as (28) is true, S_m turns ON under ZCS condition. This condition is valid for both PWM and QR modes. Fig. 6 compares the two sides of (28) at $V_O=400\,\text{V}$, $V_{\text{in}}=16\,\text{V}$, and $n=5$, for different values of P_O and L_k. It can be seen that for L_k less

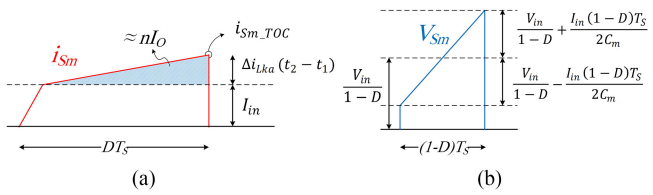

Fig. 7. Detailed waveform of (a) i_{Sm} in the PWM mode and (b) V_{Sm} in the QR mode.

than 4 μH, ZCS condition is obtained for the whole range of output power. Fig. 6 shows that at low output power, I_{in} is small. Consequently, i_{Lka} can reach I_{in} faster, and ZCS condition improves. Furthermore, when L_k decreases, i_{Lka} rises more rapidly and $t_{9\text{th}}$ shortens. This condition is desirable for the ZCS condition in (27). Consequently, in contrast to the ZVS condition, the ZCS condition improves at light loads and in small values of leakage inductance.

Based on Figs. 2 and 4, S_a and S_b start conduction after S_m turns ON. Thus, when S_m turns ON under ZCS condition, the condition is surely achieved for S_a and S_b as well, in both operational modes.

V. Simulation Results and Comparison

Using soft-switching techniques and reducing voltage and current amplitudes of the main switch at turn-OFF moment have resulted in reduced switching losses. In this section, the power loss is calculated for the proposed converter, and finally, an analogy is drawn among this converter and the basic interleaved converters of this type, introduced in [22] and [23].

The switching loss in a switching cycle is generally calculated as [13]

$$P_{\text{switching}}=\frac{t_{\text{on}}}{2T_S}\left(I_{\text{turn-on}}V_{\text{turn-on}}\right)+\frac{t_{\text{off}}}{2T_S}\left(I_{\text{turn-off}}V_{\text{turn-off}}\right) \tag{29}$$

where the first and the second terms stand for the turn-ON and the turn-OFF losses, respectively. In (29) t_{on} and t_{off} are the time duration of getting ON and OFF. Also, $I_{\text{turn-on}}$, $V_{\text{turn-on}}$, $I_{\text{turn-off}}$, and $V_{\text{turn-off}}$ are the current and voltage of a switch at turn-ON and turn-OFF moments, respectively. At first, the PWM mode is being discussed, and then, the QR mode. In the PWM mode, the switches S_a and S_b are turned ON and OFF under the ZCS condition. Hence, switching losses for S_a and S_b are zero. As shown in Fig. 2, in the first interval S_m is turned ON under the ZCS condition. Interval 2 has to be investigated, as shown in Fig. 7(a), to calculate the power loss of turn-OFF process. According to (29), the value of current at which S_m turns OFF, indicated by i_{Sm_TOC} in Fig. 7(a), is needed. i_{Sm_TOC} is obtained as

$$i_{Sm\_\text{TOC}}=I_{\text{in}}+\Delta i_{Lka}\left(t_2-t_1\right). \tag{30}$$

Within $[t_1-t_2]$, the diode D_3 is conducting a current which is equal to $i_{Lka}(t_2-t_1)/n$. So

$$I_O=\frac{1}{2T_S}\frac{1}{2}\frac{\Delta i_{Lka}\left(t_2-t_1\right).DT_S}{n}. \tag{31}$$

The first interval has been neglected in (31). Substituting (31) in (30) yields

$$i_{Sm\_\text{TOC}}=I_{\text{in}}+\frac{4nI_O}{D}. \tag{32}$$

The voltage across S_m at turn-OFF, shown by V_{Sm_TOV}, is obtained by applying KVL and is provided as

$$V_{Sm\_\text{TOV}}=V_{C_a}+V_{Cm}+V_{C_b}=\frac{V_{\text{in}}}{1-D}. \tag{33}$$

Using (26), (29), and (30), the switching loss of S_m in the PWM mode can be calculated.

For the QR condition, i_{Sm_TOC} has lower value, i.e., it is equal to the input current I_{in}. It is necessary to calculate the voltage across C_m at t_3 ($V_{Cm}(t_3)$) to obtain V_{Sm_TOV}. It is shown in Fig. 7(b) in detail. Applying KVL at the input side of the circuit indicates that the average value of C_m voltage V_{Cm} equals V_{in}. At t_3, the voltage across C_m is $V_{CM}(t_3)=V_{\text{in}}-\Delta V_{Cm}/2$ where ΔV_{Cm} is peak-to-peak voltage variation of C_m. In order to calculate ΔV_{Cm}, one should consider intervals 4 and 5 in Fig. 4, where the input current flows through C_m and charges it. From t_3 to t_5, V_{Cm} is increased by ΔV_{Cm}. Hence, ΔV_{Cm} can be obtained using

$$\Delta V_{C_m}=\frac{I_{\text{in}}\left(1-D\right)T_S}{C_m}. \tag{34}$$

Now, $V_{Sm_}$TOV can be calculated as

$$V_{Sm\_\text{TOV}}=\frac{V_{\text{in}}}{1-D}-\frac{I_{\text{in}}\left(1-D\right)T_S}{2C_m}. \tag{35}$$

Having V_{Sm_TOV} and i_{Sm_TOC} in the QR mode, one can calculate the switching loss of S_m when turning OFF. To clarify the improvements achieved by using the proposed converter, some features of this converter and the basic interleaved converters suggested in [22] and [23] are compared in Table I. The voltage and current of switches at turn-OFF moment, which affect the switching loss, are presented in this table. Fig. 8(a) presents the switching loss curves versus the output power for $V_{\text{in}}=16\,\text{V}$, $V_O=400\,\text{V}$, $n=5$, $L_k=2\,\mu\text{H}$, $t_{\text{off}}=65\,\text{ns}$, $T_S=10\,\mu\text{s}$, $C_m=10\,\mu\text{F}$ for the PWM mode, and for the QR mode, C_m obtained from (6), which is $1\,\mu\text{F}$. As shown in Fig. 8(a), the switching loss of the converters increases linearly with the output power, except for the proposed QRDAC. Although the QR interleaved converter in [23] has lower switching loss than the PWM one in [22], the proposed DAC has reduced the loss even further. However, the proposed QRDAC presents a superior condition in which the switching loss is considerably diminished. In contrast with the other converters, switching loss in the QRDAC does not increase significantly according to the output power. Because, based on the data in Table I, although its turn-OFF current increases along with the output power, its turn-OFF voltage decreases dramatically. Consequently, switching loss remains almost constant at high output powers.

The main impetus to introduce the proposed converter is to reduce the number of semiconductors, as well as achieve lower power loss. However, the voltage gain should be considered too. Table I also provides the voltage gain equations of the proposed converter and the basic interleaved converters suggested in [22]

TABLE I
SWITCHING LOSSES OF THE PROPOSED CONVERTER AND INTERLEAVED CONVERTERS PROPOSED IN [22] AND [23]

	Turn-off current		Turn-off voltage	Voltage gain	Number of	
					switches	diodes
QR	I_{in}		$\frac{V_{in}}{(1-D)} - \frac{I_{in}(1-D)T_s}{2C_m}$	$\frac{2n}{(1-D)\left(1+\frac{4L_k n^2}{(1-D)^2 T_S R_L}\right)}$	3	3
PWM	$I_{in} + \frac{nI_o}{D}$		$\frac{V_{in}}{(1-D)}$	$\frac{2n}{(1-D)\left(1+\frac{4n^2 L_k (2-4D+3D^2)}{(1-D)^2 D^2 R_L T_S}\right)}$	3	3
PWM-Interleaved [22]	S_1&S_3	$2\times[\frac{I_{in}}{2}+\frac{nI_o}{D}]$	$\frac{V_{in}}{(1-D)}$	$\frac{2n}{(1-D)\left(1+\frac{4L_k n^2}{(1-D)^2 D T_S R_L}\right)}$	4	4
	S_2&S_4	$2\times[\frac{nI_o}{(1-D)}]$	$\frac{V_{in}}{(1-D)}$			
QR-Interleaved [23]	S_1&S_3	$2\times\frac{I_{in}}{2}$	$2\times\left[\frac{V_{in}}{(1-D)} - \frac{I_{in}(1-D)T_s}{4C_m}\right]$	$\frac{2n}{(1-D)\left(1+\frac{4L_k n^2}{(1-D)^2 D T_S R_L}\right)}$	4	4
	S_2&S_4	$2\times\frac{I_{in}}{2}$	$2\times\left[\frac{V_{in}}{(1-D)} + \frac{I_{in}(1-D)T_s}{4C_m}\right]$			

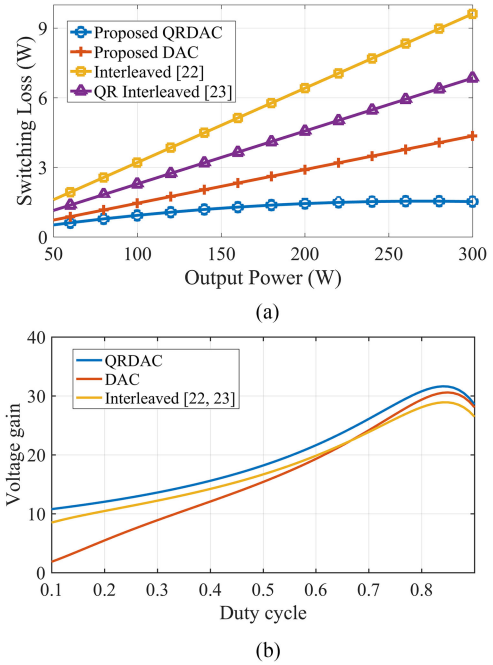

Fig. 8. Comparison between the proposed converter and interleaved converters introduced in [22] and [23]. (a) Switching loss versus output power. (b) Voltage gain against duty cycle.

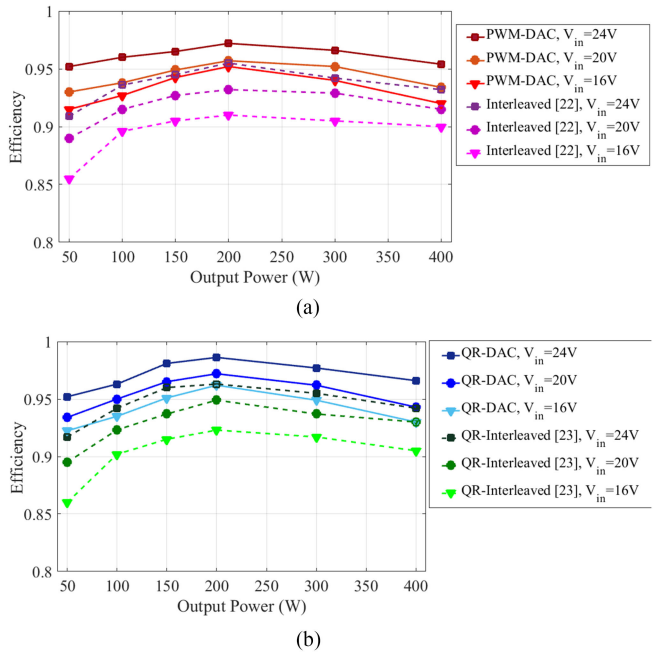

Fig. 9. Efficiency comparison for three voltage conversion ratios between (a) DAC-PWM and interleaved converter in [22] and (b) DAC-QR and the QR-interleaved converter in [23].

and [23] in two modes of operation. The voltage gain plots are presented in Fig. 8(b), in order to make it possible to compare the functionality of each converter in boosting the input voltage. As can be seen, for high values of the duty cycle, the proposed converter excels the interleaved converter. However, at low duty cycles, despite the other advantages, the proposed converter has less voltage gain. Nevertheless, its operation in QR mode has resulted in a superior behavior and higher voltage gain in the entire range of duty cycle.

The efficiency of the converters is compared in Fig. 9. The converters in [22] and [23] are designed in different conditions from this study, for example, using lower switching frequency, higher input voltage, etc., which can significantly affect the efficiency. Hence, for an accurate comparison, all the converters are simulated in the same condition with the same components as presented in Table II.

Fig. 9(a) shows the efficiency of the proposed DAC for different output power values in the range of 50 to 400 W in the PWM operation mode. Simulations are done for three input voltages, i.e., $V_{\text{in}} = 16$, 20, and 24 V, to examine the effect of voltage ratios on the efficiency. Similar simulations are conducted for the interleaved converter proposed in [22] and the results are shown in the same plot. It can be seen that for equal conversion ratios, the proposed converter brings higher efficiencies. For both

TABLE II
DESIGN SPECIFICATIONS OF THE PROTOTYPE

Components	Value	Description
V_{in}	16V	-
V_O	400V	-
R_L	800Ω	-
f_S	100kHz	-
n	5	-
L_{ka}& L_{kb}	2uH	ETD39, $R_{primary}$=1 mΩ, $R_{secondary}$=15 mΩ
L_{in}	200uH	T150-26, R=11 mΩ
C_a, C_b, C_m	100uF	nichicon UPM
C_m (QR mode)	1uF	Vishay MKT1822
C_{O1}-C_{O3}	470uF	nichicon UPM
D_1-D_3	600V/9A	CREE C3D06060A,
S_a, S_b, and S_m	150V/43A,	Infineon IPA075N15N3,

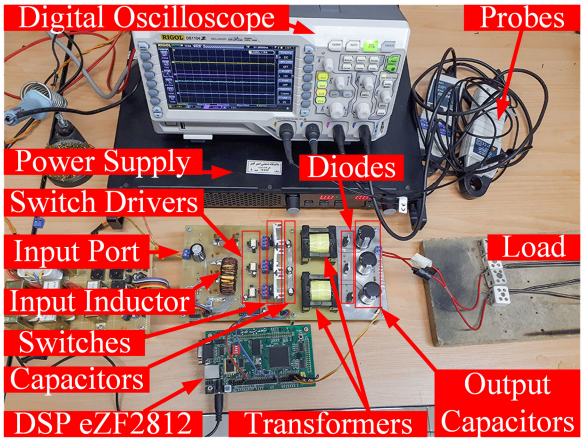

Fig. 10. Photograph of the experimental hardware.

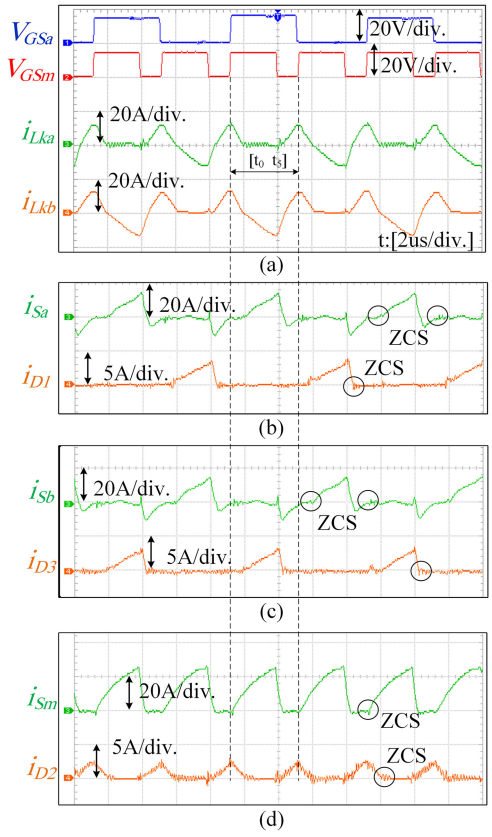

Fig. 11. Experimental results for the proposed DAC converter: (a) i_{Lka}, i_{Lkb}, (b) i_{Sa}, i_{D1}, (c) i_{Sb}, i_{D3}, and (d) i_{Sm}, i_{D2}, in accordance with V_{GSa}.

converters, the efficiency increases as more power is delivered, until they reach about 200 W output power where the maximum efficiency occurs. After that, increasing the output power reduces the efficiency. As for the effect of voltage conversion ratio, the simulations show that for the same output power, more efficiency is achieved for the lowest conversion ratio. This was expected, since current decreases as voltage increases in the same output power and the power loss will be diminished. Simulation results in the QR mode for the proposed converter and the interleaved converter introduced in [23] are shown in Fig. 9(b). Similar inferences can be drawn for this mode too. Comparing Fig. 9(a) and (b) reveal that, at the same condition, QRDAC is more efficient than the others.

VI. EXPERIMENTAL RESULTS

A prototype has been implemented and tested based on the specifications given in Table II. The experimental hardware is shown in Fig. 10 with the devices' description. Fig. 11 shows the experimental results of the converter in the PWM mode. The waveforms are plotted in accordance with the gate-pulses of S_m and S_a. As it is seen, the switching frequency of S_a is half that of S_m. In Fig. 11(a), i_{Lka} and i_{Lkb} are shown, which are similar to each other with a half-cycle phase shift. Fig. 11(b) and (c) shows i_{Sa}, i_{D1} and i_{Sb}, i_{D3}, respectively. The time duration t_0–t_5 is indicated in these figures. It can be seen that the current of the switch S_a rises from zero after t_0, and then, before t_5, returns to zero again. This condition results in ZCS at turn-ON and turn-OFF moments for S_a. The same analyses are valid for S_b. In addition, both diodes are turned OFF under the ZCS condition. In these figures, the maximum current of the switches and diodes are 14 and 3 A, respectively. Fig. 11(d) shows i_{Sm} and i_{D2}, where the switch turns ON and the diode turns OFF under the ZCS condition. The switch turns OFF at 26 A, and the maximum current of D_2 is 2.5 A. The waveforms shown in Fig. 11 are analogous to those in Fig. 2 and justify the theoretical analysis. Fig. 12 shows the experimental results of the proposed converter in the QR mode, in the same form as those in Fig. 11. In Fig. 12(a), i_{Lka} and i_{Lkb} are shown, which are a half-cycle phase shifted. The resonant behavior of the converter can be observed in these waveforms. Fig. 12(b) and (c) shows i_{Sa}, i_{D1} and i_{Sb}, i_{D3}, respectively. Similar to the PWM mode, the time duration t_0–t_5 is specified in these figures. It is seen that the current of S_a rises from zero after t_0, and descends to zero again before t_5. This condition results in ZCS at turn-ON and turn-OFF moments for S_a. The same condition is true for S_b. In addition, both diodes turn OFF under ZCS. In these figures, the maximum current of the switches and diodes are 18 and 3.5 A, respectively. Fig. 12(d) shows i_{Sm} and i_{D2}, where the switch turns ON and the diode turns OFF under ZCS condition. The maximum current of D_2 is 2.5 A. The switch turns OFF at 13 A, which is much lower than that in the PWM mode.

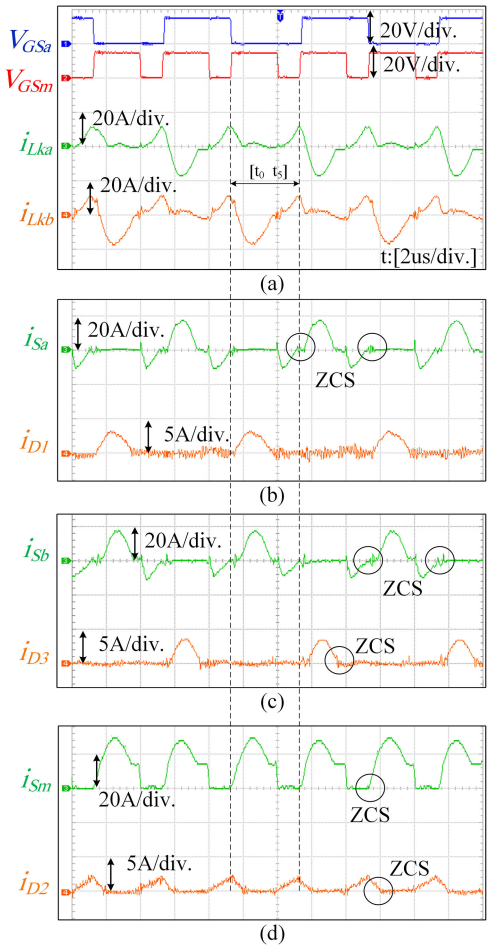

Fig. 12. Experimental results for the proposed DAC converter in the QR mode: (a) i_{Lka}, i_{Lkb}, (b) i_{Sa}, i_{D1}, (c) i_{Sb}, i_{D3}, and (d) i_{Sm}, i_{D2}, in accordance with V_{GSa}.

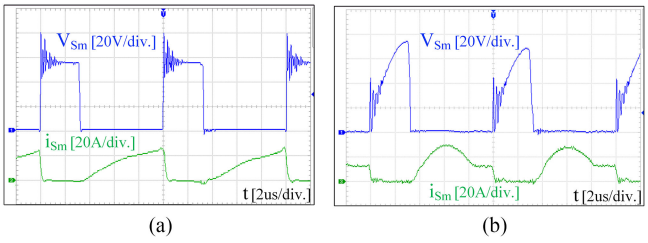

Fig. 13. Voltage and current waveforms of S_m in the (a) PWM mode and (b) QR mode.

In Fig. 13(a) and (b), voltage and current waveforms of the main switch in both PWM and QR modes are presented, respectively. It can be seen that the turn-OFF voltage of the switch in the PWM mode is 65 V, while in the QR mode, it is about 20 V. Moreover, the turn-OFF current of the switch in the PWM mode is almost 26 A, but in the QR mode, it is limited to 13 A. A comparison between these waveforms reveals that turn-OFF current and voltage of S_m are considerably reduced in QRDAC. Consequently, the switching loss in QRDAC is supposed to be improved significantly.

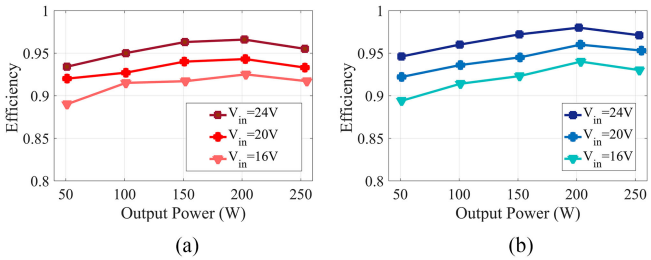

Fig. 14. Experimental efficiency values, measured in the (a) PWM mode and (b) QR mode, for various input voltage values.

In order to verify the simulation results, the 50–250 W power range and the same voltage conversion ratios shown in Fig. 9 are chosen. Because of converter component rating and design considerations, experimental efficiency measurement was not possible for more than 125% of nominal loads ($P_O = 250$ W). Fig. 14(a) and (b) shows the measured efficiency values of the proposed converter in the PWM and the QR modes. As shown in Fig. 14, for both operational modes, efficiency increases as the output power expands until $P_O = 200$ W. Moreover, considering Figs. 9 and 14 reveal that the simulation results have appropriately predicted the efficiency behavior of the proposed converter through the whole output power range, although there is a difference in values. This difference can be caused by the characteristic of the components which exist in practical cases but are not possible to be included in the simulations, for example, proximity effect of the windings and parasitic elements of the components which cause stray losses.

In addition, comparing the efficiency values between the PWM and the QR modes under the same operating conditions shows that the proposed DAC operates with higher efficiency in the QR mode.

VII. Conclusion

An interleaved converter is a desirable choice for high-power/voltage applications as in this case, literally, at least two converters participate in power conversion. Nevertheless, the main drawback of this kind of converter is the high number of components, especially semiconductors. This results in a costly and relatively low-efficiency converter. In order to eliminate these problems as far as possible, a DAC converter is proposed in this article. In the proposed converter, the number of semiconductors is reduced, while its voltage gain is improved in comparison with the conventional interleaved converter. In this converter, all diodes turn OFF under the ZCS condition. Moreover, active clamps' switches preserve soft-switching at both turn ON and OFF moments. Thus, switching loss for these switches is zero. In addition, the main switch turns ON under the ZCS condition. Accordingly, not only is the number of semiconductors reduced, but also the switching loss occurs only at the turn-OFF moment of the main switch. Therefore, the proposed converter has basically reduced losses compared to interleaved converters. Furthermore, the QR technique is employed to reduce the switching loss further and enhance the voltage gain. For the proposed converter, it is preferred to operate in the QR mode, since, as a consequence

of reducing the switching loss of the main switch, the efficiency of the converter in the QR mode, in comparison with the PWM mode, is enhanced from 96.6% to 98% at $V_{\rm in} = 24\,{\rm V}$. The provided experimental results approve the functionality of the proposed converter.

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