A Direct Current Control Scheme With Compensation Operation and Circuit-Parameter Estimation for Full-Bridge DC–DC Converter

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***Abstract*—To boost the dynamic performance of the full-bridge (FB) dc–dc converter, some model-based controls have been recently proposed in the literature. However, in terms of dynamic performance, these methods have failed to reveal the potential of this converter since the inherent relationship among the duty ratio, the input voltage, the output voltage, and the load resistor is not adopted in the controller, and the dynamic performances are still relayed on the fuzzy adjustment based on the disturbances of output voltage as the single-voltage-loop control method. In this article, based on this inherent characteristic of the FB dc–dc converter, an accurate transferred current modulation method is presented first. Based on this modulation method, a simple direct current control (DCC) scheme is proposed for a fast dynamic response with the feedback values of input voltage and load current. Moreover, the model uncertainties such as the power losses and control delay may influence the control performance. Therefore, a compensation operation is also presented to reduce the impact caused by these uncertainties to ensure the dynamic performance of the proposed strategy. In addition, since the circuit parameters including the leakage inductance and the output capacitor should be employed to implement the proposed DCC strategy with compensation operation, inaccurate circuit parameters may influence the performance of these proposed strategies. Therefore, the circuit-parameter estimation methods for these two circuit parameters are also proposed to ensure the dynamic performance of the FB dc–dc converter. Finally, the simulation and experiment results have verified the correctness and effectiveness of the proposed DCC strategy.**

***Index Terms*—Circuit-parameter estimations, direct current control (DCC), dynamic performance, full-bridge (FB) dc–dc converter.**

I. Introduction

With the high-power application and the electric isolation requirement, the isolated dc–dc converter has been extensively studied in the unidirectional power flowing systems, such as photovoltaic system [1]–[3] and fuel cell system [4]–[6]. Among these unidirectional dc–dc converters, the full-bridge (FB) dc–dc converter can be regarded as the original topology, which can be shown in Fig. 1, and it is very attractive because of its zero-voltage switching, low component stresses, and electrical isolation [7]–[8].

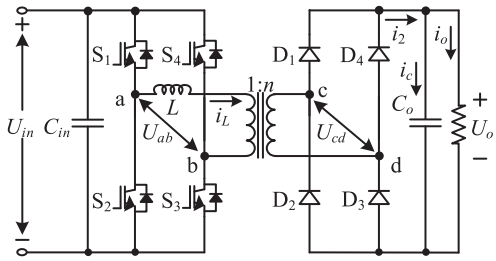

Fig. 1. Topology of FB dc–dc converter.

To face the disturbances of input voltage and load resistor in the actual application, the fast-dynamic response and the stable output voltage are the crucial requirements for the control design of the isolated dc–dc converter [9]–[10]. Traditionally, the single voltage-loop control [11], [12] and the double current-voltage-loop control [13] are the common choices to maintain the output voltage for these converters. However, these two methods are more dependent on the rough regulating function of the PI controller, which can only reduce the error between the desired output voltage and the actual output voltage slowly. Therefore, this adjusting function cannot deal with the various disturbances of input voltage and load resistor with a fast transient performance for FB dc–dc converter.

Generally, the model-based control method becomes as a promising candidate to boost the dynamic performance of the dc–dc converters [14]–[16]. Based on the analysis of the first-order circuit model for the FB dc–dc converter, a nonlinear observer has been proposed to estimate the transformer primary current and the input/output current of the FB dc–dc converter [17]. This observer-based method can be employed to implement the fast-dynamic response of different desired transferred power with two dc sources system, which may not be suitable for maintaining the output voltage actively for the FB dc–dc converter. Moreover, an implicit model predictive control scheme is proposed to boost the dynamic performance of the FB dc–dc converter under the disturbances of the load resistor [18]. However, the more efficient relationship among the transferred power, the output power, and the duty ratio are not adopted, and the accurate modulation method is not obtained, so the response time under disturbances of load resistor is still

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long. Similarly, the linear MPC and nonlinear MPC strategies of FB dc-dc converter are proposed [19], but the setting time under disturbances of load resistor is still obvious, and the overshoot of the output voltage can also be noticed. Although the MPC concept has been introduced to the FB dc–dc converter for over a decade, the inner-loop controls for connecting the outer-loop output value and the phase-shift ratio are inaccurate in those methods. Therefore, the full potential of the fast-dynamic performance of the FB dc–dc converter cannot be achieved in these strategies, and the dynamic behavior of these existing strategies is similar to the single-voltage-loop control (SVLC) method, where the dynamic performance is mainly relying on the amplification of the output-voltage error.

In this article, based on the analysis of the discontinuous conduction mode (DCM) and the continuous conduction mode (CCM) of the inductance current, the accurate transferred current (ATC) modulation method is presented for the FB dc–dc converter, and a direct current control (DCC) scheme is further proposed for boosting the dynamic performance of this converter under the variation of the input voltage and the load resistor. Moreover, when the input voltage and the load resistor are changed, the efficiency of the FB dc–dc converter may be changed with the power loss. Therefore, there will be a little difference between the theoretical control model and the actual converter, which will damage the dynamic performance of the proposed method. Thus, a compensation operation is also developed to ensure the dynamic performance of the proposed DCC strategy. In addition, since the circuit parameters including the leakage inductance and the output capacitor should be employed to implement the proposed DCC strategy and the proposed compensation operation, the estimating methods for these two circuit parameters are also proposed to ensure the dynamic performance of the FB dc–dc converter.

The rest of the article is organized as follows. In Section II, the DCM and CCM of the inductance current are analyzed, and then, the ATC modulation method is presented for the FB dc–dc converter. Then, the DCC strategy is proposed for the fast-dynamic response in Section III. Moreover, considering the power losses, the expected converter behaviors are discussed, which will affect the performance of the proposed DCC scheme. Thus, the corresponding compensation method is also presented in this section. Then, the estimating methods for the leakage inductance and the output capacitor are also proposed to ensure the dynamic performance of the proposed DCC strategy with compensation operation for the FB dc–dc converter. In addition, simulation results and experimental results are both provided to validate the effectiveness of the presented DCC scheme with the compensation operation in Section IV. Finally, Section V concludes thew article.

II. Accurate Transferred-Current Modulation Method for FB DC–DC Converter

As shown in Fig. 1, the FB dc–dc converter is constructed by one H bridge with switches (HBS) and one H bridge with diode (HBD). The HBS can implement the positive control of its output voltage, and the diodes of HBD are turned ON by the

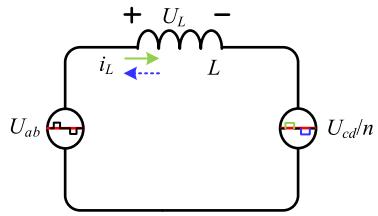

Fig. 2. Equivalent circuit of the FB dc–dc converter.

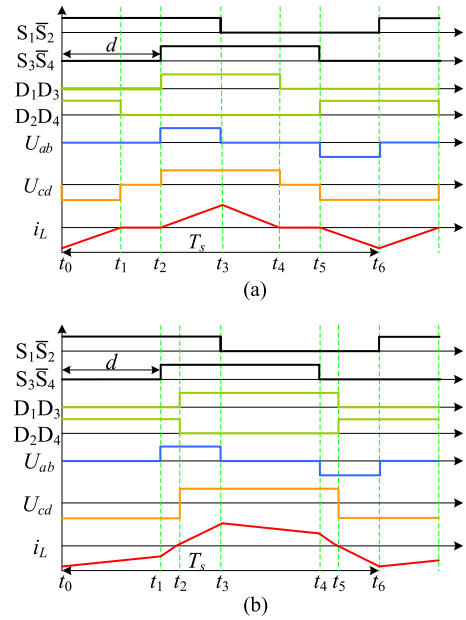

Fig. 3. Phase-shift modulation method for the FB dc–dc converter. (a) Main waveform under DCM. (b) Main waveform under CCM.

inductance current forcedly. Then, the equivalent circuit of the FB dc–dc converter can be illustrated in Fig. 2, where U_{ab} is the output voltage of the HBS, U_{cd} is the output voltage of the HBD, i_L is the inductance current, U_L is the inductance voltage, and n is the transformer turn ratio.

To realize the power transmission and avoid the magnetic saturation of the transformer, the phase-shift modulation method becomes the most suitable modulation method to regulate the output voltage of the HBS and implement the control of transferred power for the FB dc–dc converter [17]–[19]. According to the inductance–current condition, there are two modes for FB dc–dc converter as the DCM and CCM, which can be shown in Fig. 3, where T_s is the switching period, and d is the phase-shift ratio. The transferred power of the FB dc–dc converter can be regulated by adjusting the value of d, and d can be configured from 0 to 1. S_1–$_4$ are square-wave gate driving signals with a 50% duty ratio for the corresponding switches and conducting states of D_1–D_4 are determined by the inductance current i_L. When i_L is positive, D_1 and D_3 are turned ON and D_2 and D_4 are turned OFF, and when i_L is negative, D_1 and D_3 are turned OFF and D_2 and D_4 are turned ON. Moreover, when i_L is equivalent to zero, the whole diodes are turned OFF. Therefore, the values of U_{ab} and U_{cd} of the FB dc–dc converter can be shown in Table I.

TABLE I
VALUES OF U_{ab} AND U_{cd}

Switch condition	U_{ab}	i_L condition	U_{cd}
S_1S_3 are turned on	U_{in}	i_L>0	U_o/n
S_2S_4 are turned on	-U_{in}	i_L<0	-U_o/n
S_1S_4 or S_2S_3 are turned on	0	i_L=0	0

Combining Fig. 3(a) and Table I, the boundary values of the inductance current under DCM can be expressed as

$$\begin{cases} i_L(t_0) = \frac{(1-d)(nU_{\rm in}-U_o)T_s}{2nL} \\ i_L(t_1) = 0 \\ i_L(t_2) = 0 \\ i_L(t_3) = -\frac{(1-d)(nU_{\rm in}-U_o)T_s}{2nL} \\ i_L(t_4) = 0 \\ i_L(t_5) = 0. \end{cases} \tag{1}$$

Similarly, the boundary values of the inductance current under CCM can be calculated as

$$\begin{cases} i_L(t_0) = -\frac{[(n^2-n^2d)U_{\rm in}^2+ndU_oU_{\rm in}-U_o^2]T_s}{4n^2LU_{\rm in}} \\ i_L(t_1) = -\frac{[(n^2-n^2d)U_{\rm in}^2-ndU_oU_{\rm in}-U_o^2]T_s}{4n^2LU_{\rm in}} \\ i_L(t_2) = 0 \\ i_L(t_3) = \frac{[(n^2-n^2d)U_{\rm in}^2+ndU_oU_{\rm in}-U_o^2]T_s}{4n^2LU_{\rm in}} \\ i_L(t_4) = \frac{[(n^2-n^2d)U_{\rm in}^2-ndU_oU_{\rm in}-U_o^2]T_s}{4n^2LU_{\rm in}} \\ i_L(t_5) = 0. \end{cases} \tag{2}$$

Moreover, combining Fig. 3(a) and (b), the boundary condition between DCM and CCM by using volt–second balance can be expressed as

$$\frac{(1-d_b)U_{\rm in}T_s}{2} = \frac{U_oT_s}{2n} \tag{3}$$

where d_b is the boundary phase-shift ratio. Assuming $k = nU_{in}/U_o$, k should be bigger than 1 based on (3), and d_b can be calculated as

$$d_b = \frac{k-1}{k}. \tag{4}$$

According to (4), when d is smaller than d_b, the FB dc–dc converter is in CCM, and when d is bigger than d_b, the FB dc–dc converter is in DCM. In addition, since the stored energy of inductance in the steady stage of FB dc–dc converter is unchanged at the end of each switching period, the transferred power from the input side to the output side of this converter can be directly expressed as the integral of U_{ab} and i_L by combining (1), (2), and Table I, which can be calculated as [17]

$$P = \begin{cases} \frac{(k-1)U_{\rm in}U_o(1-d)^2T_s}{4nL} & \left(\frac{k-1}{k} < d \le 1\right) \\ \frac{U_{\rm in}U_o(1-d^2)T_s}{8nL} - \frac{U_o^3T_s}{8n^3U_{\rm in}L} & \left(0 \le d \le \frac{k-1}{k}\right). \end{cases} \tag{5}$$

According to (5), the transferred power of the FB dc–dc converter can be calculated by the phase-shift ratio d, the input voltage $U_{\rm in}$, the output voltage U_o, and the circuit parameter $L\&n$ of the FB dc–dc converter. Moreover, ignoring the power losses and assuming the whole transferred power can be transmitted to the output side, the transferred current I_T of the FB dc–dc converter can be expressed as

$$I_T = \frac{P}{U_o} = \begin{cases} \frac{(k-1)U_{\rm in}(1-d)^2T_s}{4nL} & \left(\frac{k-1}{k} < d \le 1\right) \\ \frac{U_{\rm in}(1-d^2)T_s}{8nL} - \frac{U_o^2T_s}{8n^3U_{\rm in}L} & \left(0 \le d \le \frac{k-1}{k}\right). \end{cases} \tag{6}$$

Then, the simplified transferred current I_{TS} can be expressed as

$$I_{TS} = \frac{I_T}{\frac{U_{in}T_s}{4nL}} = \begin{cases} (k-1)(1-d)^2 & \left(\frac{k-1}{k} < d \le 1\right) \\ \frac{(1-d^2)}{2} - \frac{1}{2k^2} & \left(0 \le d \le \frac{k-1}{k}\right). \end{cases} \tag{7}$$

According to (7), the waveform of the simplified transferred current I_{TS} with the variation of the variations of duty ratio d and voltage turn ratio k can be shown in Fig. 4. It is clear that the simplified transferred current is monotone decreasing along with the increase of the duty ratio, and when the input voltage is the same, the transferred current is increasing along with the increasing of the voltage turn ratio k that means the output voltage U_o is decreasing.

Reversely, according to (6), the transferred current I_T of FB dc–dc converter can be calculated by the phase-shift ratio d, the input voltage $U_{\rm in}$, the output voltage U_o, and the circuit parameter $L\&n$ of the FB dc–dc converter. In reverse, when the required transferred current I_T^* is determined, the phase-shift ratio d can be calculated by this transferred current I_T^* as

$$d = \begin{cases} 1 - \sqrt{\frac{4nLI_T}{(k-1)U_{\rm in}T_s}} & \left(0 \le I_T \le \frac{(k-1)U_o^2T_s}{4n^3LU_{\rm in}}\right) \\ \sqrt{1 - \frac{8nLI_T}{U_{\rm in}T_s} - \frac{U_o^2}{n^2U_{\rm in}^2}} & \left(\frac{(k-1)U_o^2T_s}{4n^3LU_{\rm in}} < I_T \le \frac{(n^2U_{\rm in}^2-U_o^2)U_oTs}{8n^3LU_{\rm in}^2}\right). \end{cases} \tag{8}$$

Combining (6) and (8), it is clear that each transferred current I_T can be related to a particular phase-shift ratio d, and it is possible for the FB dc-dc converter to implement the accurate control of the transferred current. Therefore, the ATC modulation method is presented in this article and shown in Fig. 5.

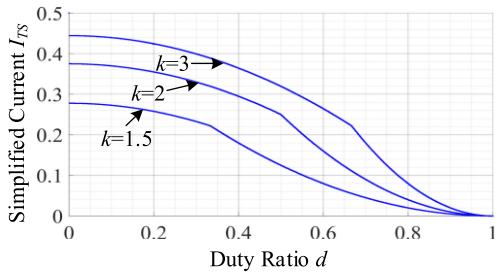

Fig. 4. Waveform of the simplified transferred current I_{TS} with the variations of duty ratio d and voltage turn ratio k.

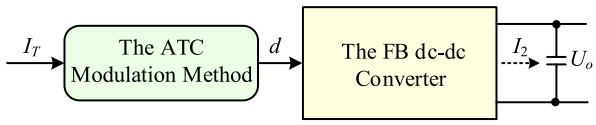

Fig. 5. ATC modulation method for the FB dc–dc converter.

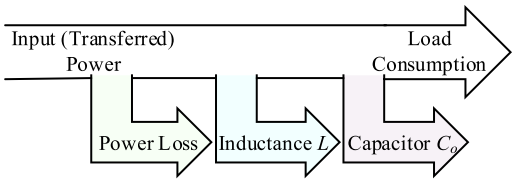

Fig. 6. Power flowing condition of the FB dc–dc converter.

As shown in Fig. 4, when the required transferred current I_T is obtained, the desired phase-shift ratio d can be calculated by using (8) for the FB dc–dc converter. Then, ignoring the power loss, the equivalent output current I_2 of the FB dc–dc converter can be very close to the transferred current as

$$I_2 \approx I_T. \tag{9}$$

Therefore, combining (8) and (9), the ATC modulation method can be implemented for the FB dc–dc converter, and when the desired transferred current I_T is equivalent to the required load current i_o, the desired output voltage will be obtained quickly even when the input voltage and the load resistor of the FB dc–dc converter are suddenly changed. Based on this characteristic, the ultra-fast dynamic performance can be provided for the FB dc–dc converter.

III. Proposed DCC Strategy With Compensation Operation and Circuit-Parameter Estimation for the FB DC–DC Converter

The existing advanced strategies for boosting dynamic performance are mainly based on the first-order model of the FB DC–DC converter [17]–[19]. However, this converter should be regarded as a two-stage power conversion converter including the dc–ac stage and the ac–dc stage, which is very similar to another converter named as the dual-active-bridge (DAB) dc–dc converter [20], [21]. To boost the dynamic performance of the DAB dc–dc converter, the transferred power- or current-based schemes may be the most suitable control methods [21], [22]. Therefore, the power flowing condition of the FB dc–dc converter is analyzed at first, and then, the DCC strategy is proposed for improving the dynamic performance of this converter in this section. Moreover, a compensation operation is also presented to compensate the difference between the ideal converter model and the actual converter and ensure the dynamic performance of the proposed DCC scheme. In addition, the estimating methods for the leakage inductance and the output capacitor are also proposed for ensuring the dynamic performance of the FB dc–dc converter.

A. Power Flowing Analysis of the FB DC–DC Converter

For accurately analyzing the power flowing condition of the power converter, the power loss and the passive circuit components including the inductance and the capacitor should be considered. Then, assuming that the transferred power is equivalent to the input power of the FB dc–dc converter, the complete power flowing diagram can be illustrated as Fig. 6.

In Fig. 6, the total transferred power P of the FB dc–dc converter can be divided into four parts including the power loss $P_{\rm loss}$, the stored power in inductance P_L, the stored power in output capacitor $P_{\rm Co}$, and the load consuming power P_o. When the output voltage U_o is equivalent to the desired value U_o^*, the required power for the output capacitor $P_{\rm Co}$ can be equivalent to zero, and the more difference between the actual output voltage and the desired output voltage, the more regulation of transferred power P will be demanded for the FB dc–dc converter. Therefore, it is better to decrease the initial change of output voltage during transient process. Moreover, when the inductance current is changed between different steady-state conditions, the extra energy from the inductance will be transferred two the output side, and the disturbance of output voltage may emerge.

Therefore, the inductance behavior between during transient process should be analyzed for the FB dc–dc converter. Moreover, since the power loss in the actual converter is very difficult to determine under different conditions accurately, the PI controller should be selected to act as the outer-loop control to make sure that the desired output voltage can be obtained for the FB dc–dc converter.

B. Proposed DCC Strategy for the FB DC–DC Converter

As the analysis in Section II, when the power loss is ignored, the transferred current I_T will be equivalent to the output current I_2, and the ATC modulation method can be implemented easily for the FB dc–dc converter. Then, to maintain the output voltage, the core work of the control strategy should be regulating the transferred current I_T to meet the demand of the load current i_o quickly, and then, the dynamic performance of the FB dc–dc converter can be improved.

According to (6), the transferred current I_T of the FB dc–dc converter is monotone decreasing along with the increasing of the phase-shift ratio d. To design the control system simply, a middle variable φ can be employed to replace the phase-shift d as

$$d = 1 - \varphi. \tag{10}$$

Then, the positive correlation between φ and I_T can be calculated as

$$I_T = \begin{cases} \frac{(k-1)U_{\rm in}\varphi^2 T_s}{4nL} & \left(0 \le \varphi \le \frac{1}{k}\right) \\ \frac{U_{\rm in}\varphi(2-\varphi)T_s}{8nL} - \frac{U_o^2 T_s}{8n^3 U_{\rm in} L} & \left(\frac{1}{k} < \varphi \le 1\right). \end{cases} \tag{11}$$

With the positive relationship between the transferred current and the control value, it is better to realize the current-based control method. According to (11), the middle variable φ can be calculated by the transferred current I_T as

$$\varphi = \begin{cases} \sqrt{\frac{4nLI_T}{(k-1)U_{\rm in}T_s}} & \left(0 \le I_T \le \frac{(k-1)U_o^2 T_s}{4n^3 L U_{\rm in}}\right) \\ 1 - \sqrt{1 - \frac{8nLI_T}{U_{\rm in}T_s} - \frac{U_o^2}{n^2 U_{\rm in}^2}} & \left(\frac{(k-1)U_o^2 T_s}{4n^3 L U_{\rm in}} < I_T \le \frac{(n^2 U_{\rm in}^2 - U_o^2)U_o Ts}{8n^3 L U_{\rm in}^2}\right). \end{cases} \tag{12}$$

According to (12), when the required transferred current I_T is obtained, the intermediate variable φ can be calculated easily.

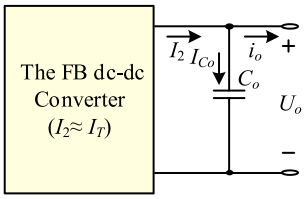

Fig. 7. Equivalent circuit of the output side of the FB dc–dc converter.

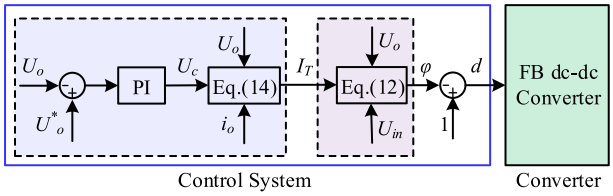

Fig. 8. Control block of the DCC strategy for the FB dc–dc converter.

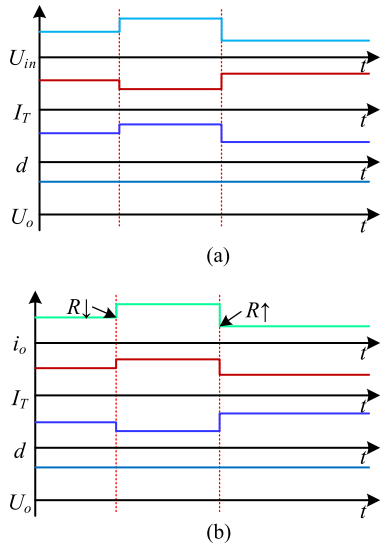

Fig. 9. Expected dynamic behavior of the FB dc–dc converter under the DCC strategy. (a) Schematic diagram under disturbance of input voltage. (b) Schematic diagram under disturbance of load resistor.

In addition, since the output side of the FB dc–dc converter is the output capacitor, the simplified equivalent circuit of the FB dc–dc converter can also be shown in Fig. 7.

As shown in Fig. 7, in order to meet the demand of the load current immediately when the input voltage or the load resistor are changed, the output current I_2 of the FB dc–dc converter should be equivalent to the load current i_o quickly. Then, the output current I_2 should be equivalent to the load current i_o as

$$I_2 = i_o. \tag{13}$$

Furthermore, as shown in (9), in order to compensate the difference between the transferred current I_T and the output current I_2, a PI controller is employed to compensate the power loss of the FB dc–dc converter. When the required transferred current I_T can be further expressed as

$$I_T = \frac{i_o U_c}{U_o} \approx i_o. \tag{14}$$

According to (14), when the desired output voltage U_o^* of the FB dc–dc converter is acquired, the compensated output voltage U_c should be closed to the desired output voltage, and the difference between the compensated output voltage U_c and the output voltage U_o should be caused by the power loss of the FB dc–dc converter. Then, combining (10), (12), and (14), the control block of the proposed DCC scheme can be shown in Fig. 8.

As shown in Fig. 8, the DCC strategy for the FB dc–dc converter and the procedures of this strategy is very simple. At the beginning of each switching period, the input voltage $U_{\rm in}$, the output voltage U_o, and the load current i_o can be measured for the FB dc–dc converter. Then, combining the desired output voltage U_o^* and the measured output voltage U_o, the compensated output voltage U_c can be obtained by using the outer PI controller. Moreover, combining the measured load current i_o, the measured output voltage U_o, and the compensated output voltage U_c, the required transferred current I_T can be calculated by using (14). Furthermore, combining the required transferred current I_T, the measured output voltage U_o, and the measured input voltage $U_{\rm in}$, the middle variable φ can be acquired by using (12). Finally, according to (10), the required phase-shift ratio d can be obtained for controlling the FB dc–dc converter.

Importantly, the PI controller in the proposed DCC scheme is used to reduce the difference between the actual output voltage and the desired output voltage caused by the power loss. Moreover, with the feedback values of the input voltage $U_{\rm in}$ and the load current i_o, the phase-shift ratio can be regulated quickly when the input voltage or the load resistor is changed. Therefore, the fast-dynamic performance can be provided for the FB dc–dc converter by using this proposed DCC strategy.

C. Dynamic Behaviors Analysis for the DCC Strategy With the Power Loss

Based on the proposed DCC strategy, the dynamic behavior of the FB dc–dc converter without power loss under the disturbances of the input voltage $U_{\rm in}$ and the load resistor R can be predicted as Fig. 9.

As shown in Fig. 9, when the input voltage $U_{\rm in}$ is changed, the corresponding phase-shift ratio φ can be determined by using (12) quickly. Moreover, when the load resistor R is changed, the load current i_o is changed immediately. Then, according to (14), the desired transferred current I_T can be obtained, and the corresponding phase-shift ratio φ can also be obtained quickly. Therefore, the output voltage U_o of the FB dc–dc converter can remain stable, and the excellent dynamic performance can be provided.

However, although the PI controller of the proposed DCC strategy can be used to compensate the error between the ideal converter model and the actual converter caused, the dynamic performance of the FB dc–dc converter may also be affected by the efficiency difference between different conditions caused by the power loss. Because a new compensated output voltage U_c' should be achieved for the new steady state, and the regulating

function of the PI controller has to be used. Therefore, the dynamic response of the FB dc–dc converter will be a little affected. In order to reduce the impact of the efficiency difference between different working conditions, a compensation operation should be presented for the FB dc–dc converter. In steady-state condition, the relationship among the transferred current I_T, the output current I_2, and the load current i_o can be shown as

$$\frac{U_o}{U_c} I_T = i_o. \tag{15}$$

Assuming that the load resistor is changed to k times, the load current should be changed to i_o/k immediately since the output voltage can remain stable in the previous switch periods with the output capacitor C_o. Then, based on the proposed DCC strategy, the required transferred current I_T is also changed to I_T/k. However, when the efficiencies of these two conditions are different, the new transferred current I_T/k cannot meet the demand of the new load condition as

$$\frac{U_o}{U_c}\frac{I_T}{k} \neq \frac{i_o}{k}. \tag{16}$$

Then, a new compensated output voltage U_c' should be regulated to meet the demand of the new load resistor and reach the desired output voltage again by using the PI controller, and the relationship between the load current i_o/k and the new transferred current I_T' can be expressed as

$$\frac{U_o}{U_c'}\frac{I_T'}{k} = \frac{i_o}{k}. \tag{17}$$

Thus, the dynamic performance of the FB dc–dc converter under the DCC strategy will be affected by the efficiency difference. Moreover, when the input voltage is changed, the required phase-shift ratio φ under the DCC strategy will be obtained immediately by using (12) to meeting the demand of the new input voltage. However, when the efficiencies of these two conditions are different, a new transferred current I_T' may be provided for the FB dc–dc converter as

$$\frac{U_o}{U_c} I_T' \neq i_o. \tag{18}$$

Similarly, a new compensated output voltage U_c' should be regulated to meet the demand of the load current i_o and reach the desired output voltage U_o^* again by using the PI controller, and the relationship between the load current i_o and the new transferred current I_T' can be expressed as

$$\frac{U_o}{U_c'} I_T' = i_o. \tag{19}$$

Then, the dynamic performance of the FB dc–dc converter under the DCC strategy will be a little affected by the efficiency difference between different steady-state conditions caused by the power loss.

Moreover, as analyzed in Section III-A, the status change of the inductance current may also influence the stability of the output voltage. Based on the proposed DCC strategy, the transient process when the load current is changed can be shown in Fig. 10.

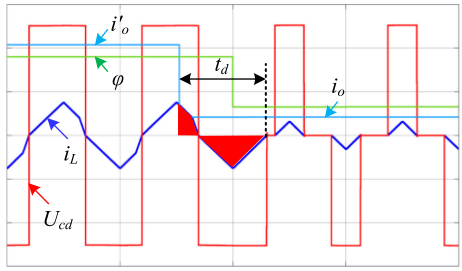

Fig. 10. Transient waveforms under the proposed DCC scheme when the load resistor is changed.

As shown in Fig. 10, there is always a control delay between the disturbance of load resistor and new duty ratio under the proposed DCC scheme. Then, the relationship between the output-voltage disturbance and the load current can be shown as

$$\frac{1}{2}C_o[(\Delta U_o + U_o)^2 - U_o^2] \approx \left[\left(U_o + \frac{\Delta U_o}{2}\right) i_o - U_o i_o'\right] t_d \approx U_o(i_o - i_o')t_d = U_o \Delta i_o t_d \tag{20}$$

where ΔU_o is the disturbance of output voltage, i_o' is the load current in a previous steady-state condition, i_o is the load current when load resistor is changed, and t_d is the delay time between the change of load current and the update of duty ratio. According to (20), the output-voltage disturbance ΔU_o can be expressed as

$$\Delta U_o = \sqrt{\frac{2U_o \Delta i_o t_d}{C_o} + U_o^2} - U_o = U_o\left[\sqrt{\frac{2\Delta i_o t_d}{C_o U_o} + 1} - 1\right] \leq U_o\left[\sqrt{\frac{2\Delta i_o T_s}{C_o U_o} + 1} - 1\right]. \tag{21}$$

As shown in Fig. 4, the transferred current of the FB dc–dc converter always has a limitation. According to (6) and (11), when d is equivalent to 0 or φ is equivalent to 1, the maximum transferred current $I_{T\max}$ of the FB dc–dc converter will be obtained. Then, (21) can be simplified as

$$\Delta U_o \leq U_o\left[\sqrt{\frac{2I_{T\max} T_s}{C_o U_o} + 1} - 1\right]. \tag{22}$$

Therefore, the power loss of the converter and the delay of the control system will bring the output-voltage disturbance under the DCC strategy for the FB dc–dc converter. Therefore, a compensation operation should be illustrated for reducing these impacts caused by the power loss and control delay and ensuring the dynamic performance of the proposed DCC strategy.

D. Compensation Operation for the Efficiency Difference Caused by the Power Loss and Control Delay.

As shown in Fig. 7, the relationship among the output current I_2, the capacitor charging current I_{Co}, and the load current i_o can always be expressed as

$$I_{Co} = I_2 - i_o. \tag{23}$$

Moreover, with the output capacitor C_o, the output voltage of the FB dc–dc converter can still close to its desired voltage in the previous switching periods after the variation of the input voltage or the load resistor. Therefore, when the capacitor charging current I_{Co} is not equivalent to zero, the output current I_2 should make up for this capacitor current I_{Co}, which also means that the transferred current I_T of the FB dc–dc converter should compensate this capacitor current I_{Co} since the total output current is close to the required load current. Then, the transferred current I_T can be expressed as

$$I_T = \frac{i_o U_c}{U_o} - I_{Co} = \frac{i_o U_c}{U_o} - \frac{C_o}{T_s}(U_o - U_o') \tag{24}$$

where U_o' is the measured output voltage in the last switching period. Based on (14), the new compensated output voltage U_c' for the FB dc–dc converter can be expressed as

$$U_c' = \frac{U_o}{i_o}\left[\frac{i_o U_c}{U_o} - \frac{C_o}{T_s}(U_o - U_o')\right]. \tag{25}$$

Therefore, when the load current i_o or the input voltage U_{in} is changed, (25) can be used to calculate the required compensated output voltage U_c' for dealing with the efficiency difference under different conditions for the FB dc–dc converter. Moreover, as shown in Fig. 10, the current status of the inductance will change when the load current is changed, and according to (20), the additional power from the inductance is transferred to the output side. Then, (24) will become inaccurate, and the expected transferred current of the FB dc–dc converter will also become inaccurate. Therefore, the compensation operation should be used after several switching periods until the peak value of the inductance current become stable. In addition, in the actual converter system, the measurement noise is unavoidable for the FB dc–dc converter. In order to make the calculation of the capacitor charging current I_{Co} more accurate, (25) should be further expressed as

$$U_c' = \frac{U_o}{i_o}\left[\frac{i_o U_c}{U_o} - \frac{\sum_{j=1}^{m} \frac{C_o}{T_s}(U_{oj} - U_{oj}')}{m}\right]. \tag{26}$$

E. Circuit-Parameter Estimation Methods for the Leakage Inductance and the Output Capacitor

According to (12) and (26), the leakage inductance *L* and the output capacitor C_o are used to implement the proposed DCC strategy and the compensation operation, respectively. Then, when these circuit parameters are inaccurate, the control performances of these two schemes will usually be affected. Therefore, the corresponding estimating method should be presented for ensuring the dynamic performance of these proposed strategies.

Because the relationship among the input voltage, the output voltage, the load current, and the duty ratio of the FB dc–dc converter is strictly determined, and the approximate inductance *L* and the approximate output capacitor can be easily estimated. The leakage inductance *L* can be obtained based on the information on the steady-state condition, and then, the output capacitor *C* should be calculated based on disturbances of output voltage when the load resistor or input voltage are changed. When the steady-state condition is obtained, the approximate inductance value *L* can be obtained as

$$L = \begin{cases} \frac{(k-1)U_{\text{in}}\varphi^2 T_s}{4nI_T} & (0 \le \varphi \le \frac{1}{k}) \\ \frac{U_{\text{in}}\varphi(2-\varphi)T_s}{8nI_T} - \frac{U_o^2 T_s}{8n^3 U_{\text{in}} I_T} & (\frac{1}{k} < \varphi \le 1). \end{cases} \tag{27}$$

After the approximate inductance is obtained, the output capacitor of the FB dc–dc converter can be estimated. In order to estimate the output capacitor, the relatively big disturbance of the output voltage should emerge when the input voltage or load resistor is changed. Therefore, the SVLC method can be selected. Based on the energy law, when the output voltage is changed under input-voltage or load-resistor variations, the relationship among the load current i_o, the capacitor charging current I_C, and the transferred current I_T can be shown as

$$I_T = I_C + i_o = \frac{C\Delta U_o}{T_s} + i_o. \tag{28}$$

When the load current or input voltage is changed, the sum operation is beginning, and when the biggest disturbance of output voltage is reached, the sum operation should be stopped. Then, the capacitor *C* can be calculated as

$$C = \frac{(\sum I_T - \sum i_o)T_s}{\sum \Delta U_o}. \tag{29}$$

TABLE II
CIRCUIT PARAMETERS OF FB DC–DC CONVERTER

Switches	SCT3080
L	50μH
n	2
f_s	10kHz
U^*_o	50V
C_o	1mF
R	12Ω or 40Ω
k_p, k_i in SVLC method	0.12, 0.012
k_p, k_i in DCC strategy	2.5, 0.25

IV. SIMULATION AND EXPERIMENTAL RESULTS

In order to verify the effectiveness of the proposed DCC strategy with the compensation method and circuit-parameter estimation method for the FB dc–dc converter, both the simulation result and the experimental result are provided. The main circuit parameters of the FB dc–dc converter are shown in Table II.

A. Simulation Result

In this section, since the power loss can be set in the simulation model, the necessity of the proposed compensation operation is verified for the FB dc–dc converter.

In order to realize a relatively fair comparison between the SVLC and the proposed DCC strategy, the PI parameters in these two schemes are tuned until the disturbances of phase-shift ratio φ in the steady-state condition is close when the load resistor *R* is equivalent to 12 Ω. Then, amplifications of the output-voltage error are semblable, and the PI parameters in these two methods are shown in Table II. The corresponding simulation results can be shown in Fig. 11.

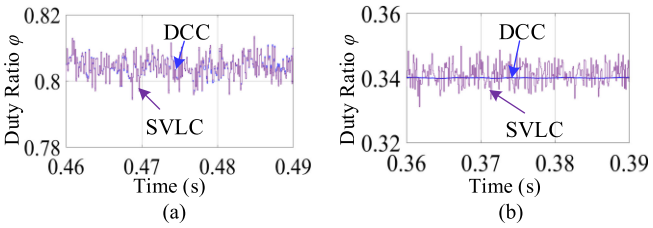

Fig. 11. Simulation results of the zoom-in waveform of the duty ratio φ. (a) $R = 12\ \Omega$. (b) $R = 40$.

As shown in Fig. 11(a), when the load resistor is equivalent to 12 Ω, the disturbances of duty ratio under the DCC strategy and the SVLC method are similar to each other in steady-state condition, which means that the amplifications of the measurement noise and the output-voltage error are semblable. With constant PI parameters, the disturbances of duty ratio under the proposed DCC strategy can be reduced when the load resistor is equivalent to 40 Ω, compared with the SVLC method [see Fig. 11(b)]. Then, the robustness should be stronger under the proposed DCC strategy. When the FB dc-dc converter is at light-load condition, the inductance current is always in DCM, and then, the relationship between the measurement noise ΔU_{om} and the disturbances of duty ratio $\Delta\varphi_{\mathrm{DCC}}$ under the proposed method can be shown as

$$\Delta\varphi_{DCC} \approx \sqrt{\frac{4nLI_T}{(k-1)U_{in}T_s}} - \sqrt{\frac{4nLI'_T}{(k-1)U_{in}T_s}} \approx \sqrt{i_o}\sqrt{\frac{4nL}{(k-1)U_{in}T_s}}\left[\sqrt{\frac{U_c + k_p\Delta U_{om}}{U_o}}\sqrt{\frac{U_c}{U_o}}\right] \tag{30}$$

where I_T is the calculated transferred current in the current switching period, and I'_T is the calculated transferred current in the last switching period. According to (30), the duty ratio disturbance and the square root of load current are proportional, and when the load current is smaller, the duty ratio disturbance is smaller. Moreover, when the input voltage is set to 50 V, the simulation results under the proposed DCC strategy without power loss can be shown in Fig. 12, where the power loss is close to zero.

As shown in Fig. 12, when the load resistor is changed between 12 and 40 Ω, the compensated output voltage U_c is changed a little, and the disturbance of output voltage is smaller than 0.2 V. Therefore, the excellent dynamic performance can be provided for the FB dc–dc converter. However, in the practice condition, the power loss is unavoidable. Thus, in the Simulink model, the internal resistor of switching is equivalent to 0.1 Ω and the forward voltage is equivalent to 1 V, the power loss of the FB dc–dc converter is simulated. Then, based on the DCC strategy, the simulation results can be shown in Fig. 13. As shown in Fig. 13(a), the compensated voltage is changed a lot, which has to depend on the adjusting function of the PI controller in the DCC strategy. Therefore, output-voltage disturbances are close

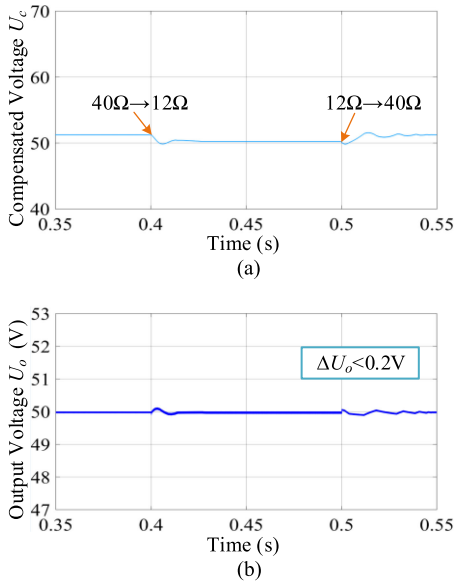

Fig. 12. Simulation results under the proposed DCC strategy without power loss. (a) Compensated output voltage. (b) Output voltage.

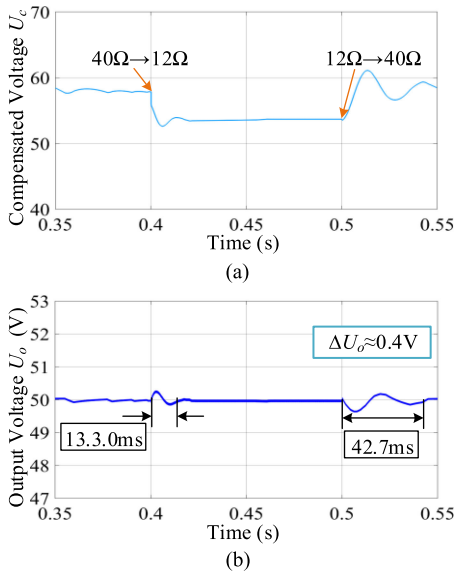

Fig. 13. Simulation results under the proposed DCC strategy without power loss. (a) Compensated output voltage. (b) Output voltage.

to 0.4 V, and the setting time for obtaining the desired output voltage again cannot be omitted.

Therefore, the compensation operation should be employed to ensure the dynamic performance of the DCC strategy, and the simulation results under the proposed DCC strategy with compensation operation and the SVLC method can be shown in Fig. 14.

Compared with Figs. 13(a) and 14(a), it is clear that the compensated output voltage U_c based on the compensation operation can reach its required value quickly when the load resistor is changed. Then, the output-voltage disturbance can be reduced to 0.2 V by using the DCC strategy with the compensation

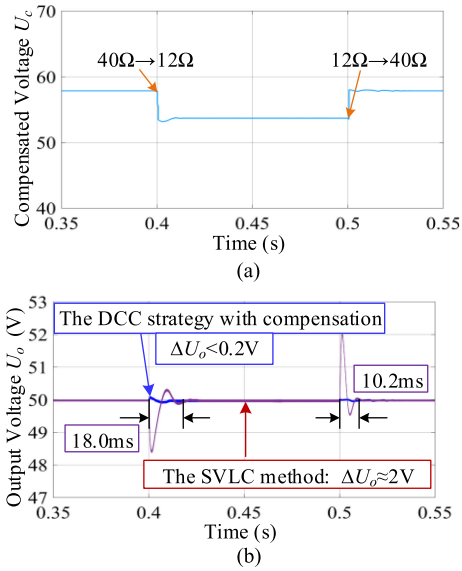

Fig. 14. Simulation results under the proposed DCC strategy without power loss. (a) Compensated output voltage. (b) Output voltage.

method. In addition, the output-voltage disturbances under the SVLC method is close to 2 V, and the setting time is bigger than 10 ms when the load resistor is changed between 12 and 40 Ω. Therefore, the DCC strategy can provide excellent dynamic performance for the FB dc-dc converter, and the proposed compensation method can ensure the dynamic performance of the DCC strategy.

Moreover, a simulation model for the FB dc-dc converter with 100 kHz switching frequency is established, and the corresponding inductance is changed to 5 μH. The simulation results when the load resistor is changed between 12 and 200 Ω can be shown in Fig. 15. As shown in Fig. 15(a), when the resistor is changed between 12 and 200 Ω (90% and 5% of the maximum output capacity), the disturbance of output voltage is very tiny based on the proposed direct-current control strategy with delay compensation [see Fig. 15(b)]. Moreover, as shown in Fig. 15(c) and (d), the inductance current is changed between CCM and DCM.

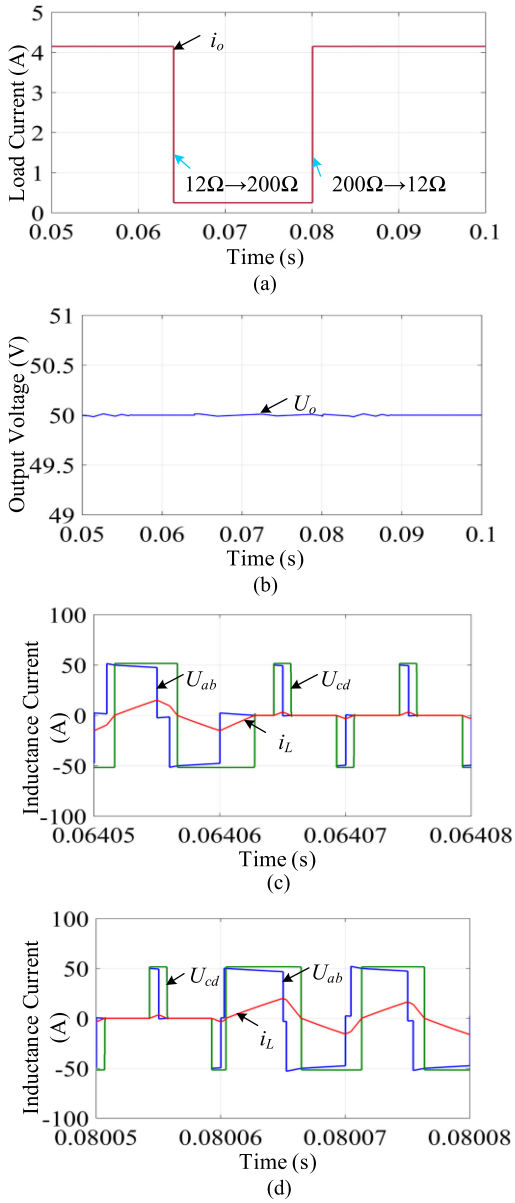

Fig. 15. Simulation results when the load resistor is changed between 12 and 200 Ω under 100-kHz switching frequency. (a) Load inductance. (b) Output voltage. (c) Inductance current #1. (d) Inductance current #2.

B. Experimental Results When Input Voltage or Load Resistor Are Changed

In order to verify the effectiveness of the proposed hybrid control scheme, a dSPACE MicroLabBox DS1202 is adopted to implement the digital control, and the experimental system can be shown in Fig. 16, and the control and circuit parameters can be shown in Table II.

When the load resistor is selected as 40 Ω, the experiment results under the SVLC method, the DCC strategy, and the DCC strategy with compensation operation when the input voltage $U_{\rm in}$ is changed from 60 to 40 V can be shown in Fig. 17, and when the input voltage $U_{\rm in}$ is changed from 40 to 60 V, the experiment results can be shown in Fig. 18, where $U_{o\rm ac}$ is the ac component of output voltage U_o during the transient process.

As shown in Figs. 17(a) and 18(a), when the input voltage is changed, the setting time under the SVLC method for obtaining the desired output voltage again is close to 30 and 20 ms, respectively, and the output-voltage disturbances are over 1 V. Moreover, as shown in Figs. 17(b) and 18(b), the setting time under the DCC strategy is about 21 and 12 ms, respectively, and the output voltage disturbances are close to 0.5 V. Therefore, compared with the SVLC method, the DCC strategy can provide better dynamic performance for the FB dc–dc converter. Furthermore, as shown in Figs. 17(c) and 18(c), based on the proposed DCC strategy with compensation operation, the disturbances of output voltage when the load resistor R is changed can be neglectful, and the excellent dynamic performance can be provided for the FB dc–dc converter.

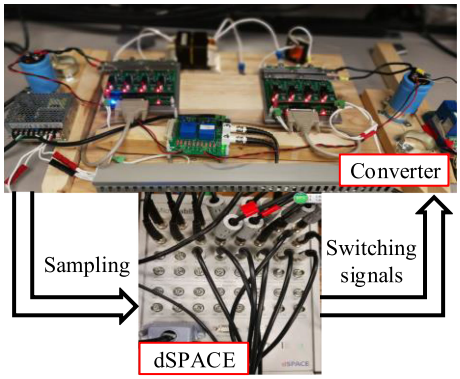

Fig. 16. Experimental system of the FB dc–dc converter with dsPACE MicroLabBox.

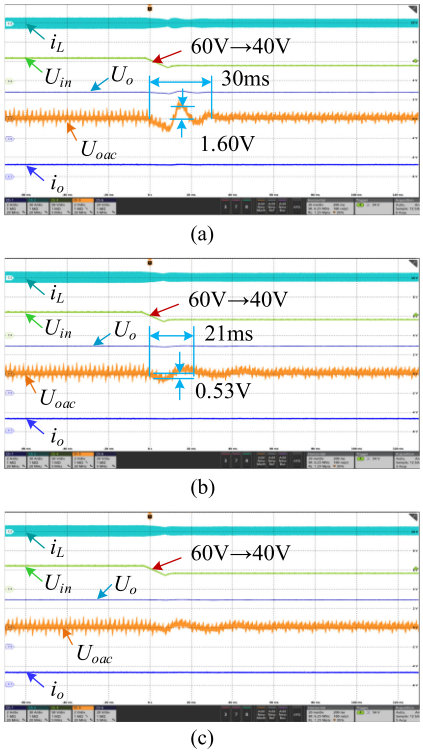

Fig. 17. Experiment results when the input voltage is changed from 60 to 40 V. ($U_{\rm in}$: 50 V/div; i_L: 30 A/div; U_o: 20 V/div; U_{oac}: 2 V/div; i_o: 2 A; t: 20 ms/div). (a) SVLC scheme. (b) DCC strategy without compensation. (c) DCC strategy with compensation.

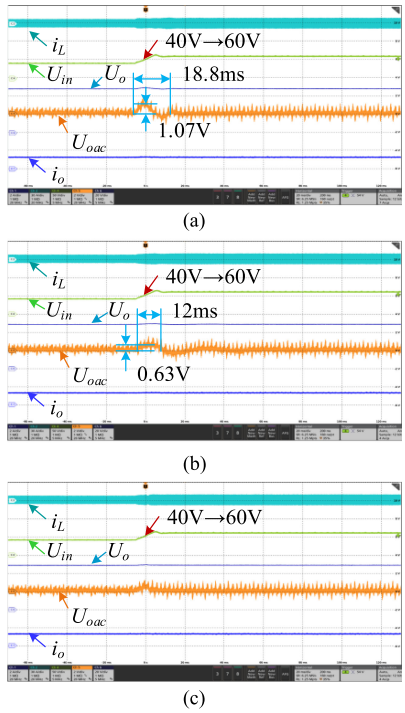

Fig. 18. Experiment results when the input voltage is changed from 40 to 60 V. ($U_{\rm in}$: 50 V/div; i_L: 30 A/div; U_o: 20 V/div; U_{oac}: 2 V/div; i_o: 2 A; t: 20 ms/div). (a) SVLC scheme. (b) DCC strategy without compensation. (c) DCC strategy with compensation.

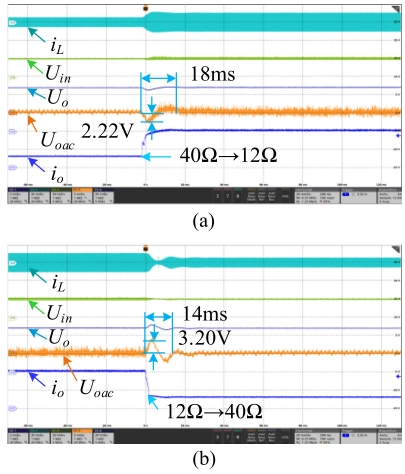

Fig. 19. Experiment results under SVLC method when load resistor is changed. ($U_{\rm in}$: 50 V/div; i_L: 30 A/div; U_o: 20 V/div; U_{oac}: 5 V/div; i_o: 2 A; t: 20 ms/div). (a) R is changed from 40 to 12 Ω. (b) R is changed from 12 to 40 Ω.

In addition, when the input voltage $U_{\rm in}$ is set to 50 V and the load resistor is changed between 12 and 40 Ω, Figs. 19, 20, and 21 show the experimental results under the SVLC method, the DCC strategy, and the DCC strategy with compensation operation, respectively.

As shown in Fig. 19, when the load resistor is changed, the setting time under the SVLC method is close to 15 ms, and the output-voltage disturbances are bigger than 2 V. Moreover, as shown in Fig. 20(a), when the load is changed from 40 to 12 Ω, the setting time under the proposed DCC strategy is 5 ms, and the output-voltage disturbance is 0.87 V. Thus, the DCC strategy can provide better dynamic performance for the FB dc–dc converter. In addition, when the load resistor is changed from 12 to 40 Ω, the output disturbance under the DCC strategy as 0.87 V is smaller than that of the SVLC method as 14 ms, but the setting time as 28 ms is bigger, which is the same as the simulation results. The main reason should be that the amplification of the output-voltage error under the DCC strategy is smaller than that under the SVLC method when the load

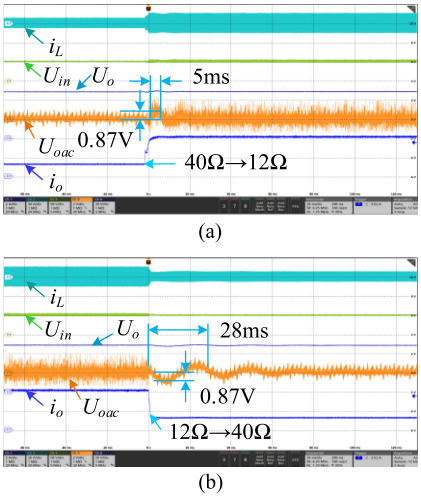

Fig. 20. Experiment results under DCC strategy without compensation when load resistor is changed. ($U_{\rm in}$: 50 V/div; i_L: 30 A/div; U_o: 20 V/div; $U_{\rm oac}$: 2 V/div; i_o: 2 A; t: 20 ms/div). (a) R is changed from 40 to 12 Ω. (b) R is changed from 12 to 40 Ω.

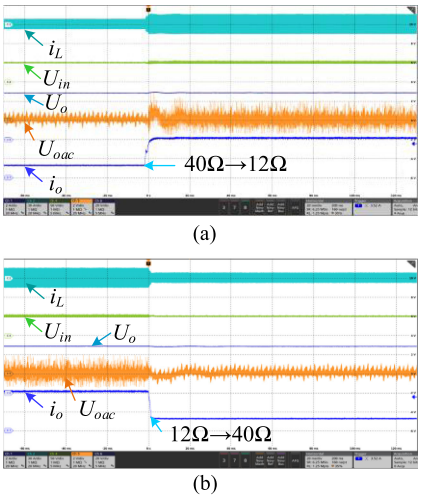

Fig. 21. Experiment results under DCC strategy with compensation when load resistor is changed. ($U_{\rm in}$: 50 V/div; i_L: 30 A/div; U_o: 20 V/div; $U_{\rm oac}$: 2 V/div; i_o: 2 A; t: 20 ms/div). (a) R is changed from 40 to 12 Ω. (b) R is changed from 12 to 40 Ω.

resistor is equivalent to 40 Ω. Furthermore, when the proposed DCC strategy with compensation operation is employed for the FB dc–dc converter, the setting time and the output-voltage disturbance can be omitted when the load resistor is changed between 12 and 40 Ω, as shown in Fig. 21. Thus, based on the proposed DCC strategy with compensation operation, the excellent dynamic performance can be acquired to the FB dc–dc converter.

C. Experimental Results of the Circuit-Parameter Estimation Methods for the Leakage Inductance and the Output Capacitor

Based on (27), the experiment results of the estimated leakage inductance under different steady-state conditions can be shown

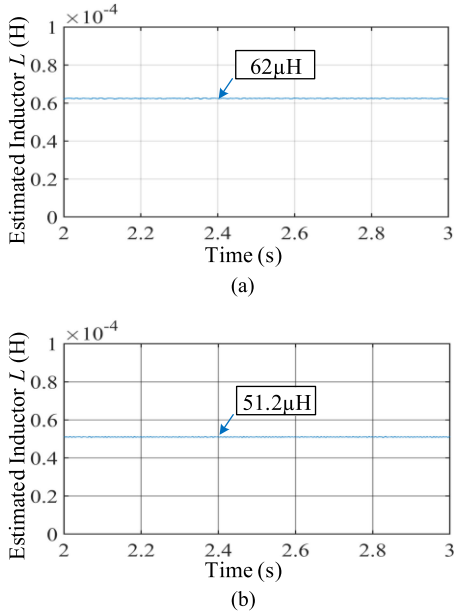

Fig. 22. Estimated inductance under different steady-state conditions. (a) Estimated inductance when R=40 Ω. (b) Estimated inductance when R=12 Ω.

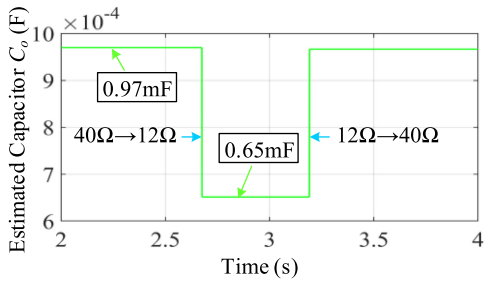

Fig. 23. Estimated output capacitor C_o when the load resistor is changed between 12 and 40 Ω.

in Fig. 22. When the load resistor R is 40 Ω, the estimated leakage inductance is about 62 μH, and when the load resistor is 12 Ω, the estimated leakage inductance is around 51.2 μH. Therefore, it is better to estimate the leakage inductance at heavy load condition, where the efficiency of the FB dc–dc converter is relatively high, and the mathematic model of this converter is more accurate.

Moreover, based on the SVLC method, which can provide big disturbances of output voltage under load changes, the estimated output capacitor C_o can be shown in Fig. 23. When the load resistor is changed from 40 to 12 Ω, the estimated output capacitor C_o is 0.65 mF, and when the load resistor is changed from 12 to 40 Ω, the estimated output capacitor C_o is 0.97 mF. Therefore, compared with Fig. 18(a) and (b), it is better to estimate the output capacitor C_o with a big disturbance of output voltage, and the estimated capacitor will be close to its actual value.

In addition, as shown in Figs. 22 and 23, although the proposed circuit-parameter estimation methods can be employed to estimate the leakage inductance and the output capacitor, the estimated errors are unavoidable. In order to further test

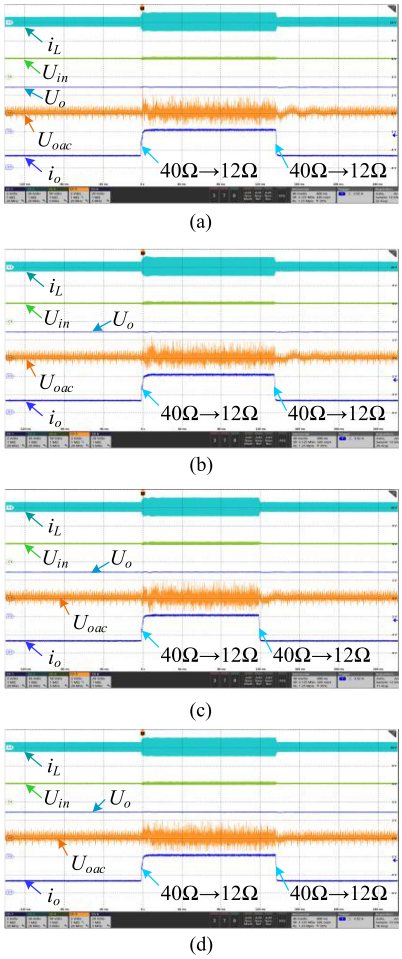

Fig. 24. Experiment results when the circuit parameters are inaccurate. ($U_{\rm in}$: 50 V/div; i_L: 30 A/div; U_o: 20 V/div; $U_{\rm oac}$: 2 V/div; i_o: 2 A; t: 40 ms/div). (a) $C'o = 0.5$ C, $L' = L$. (b) $C'o = 1.5$ C, $L' = L$. (c) $C'o = C$, $L' = L$. (d) $C'o = 1.5$ C, $L' = 60$ μH.

the dynamic performances of the proposed DCC strategy with compensation operation, the simulation results when the circuit parameters are inaccurate are also illustrated as shown in Fig. 24, where C'_o and L' are the adopted circuit parameters in the controller system. As shown in Fig. 24, even when the output capacitor and the leakage inductance are inaccurate, the good dynamic performance can also be provided for the FB dc–dc converter.

IV. Conclusion

In order to boost the dynamic performance of the full-bridge dc–dc converter, a direct-current control strategy is proposed based on the inherent average current transferred characteristic of this dc–dc converter. Ideally, the excellent dynamic performance under the proposed direct-current control strategy can be obtained However, there is always a difference between the ideal converter model and the actual converter system caused by the power loss, the measurement noise, and the inaccurate circuit parameters. Therefore, the corresponding compensation method and the circuit-parameter estimation method are also proposed in this article for ensuring the excellent dynamic performance of the proposed direct-current control scheme. With simulation and experiment verifications, the conducted studies in this article can lead to the following conclusions.

1) Without power loss, the excellent dynamic performance can be obtained by using the proposed direct-current control strategy for the FB dc–dc converter. Thus, with higher efficiency performance, the better dynamic performance can be provided by only using this direct-current control.
2) The power loss can influence on the dynamic performance of the direct-current control scheme, and combing the proposed compensation operation, the excellent dynamic performance can also be provided for the FB dc–dc converter.
3) Based on the circuit-parameter estimation methods for the leakage inductance and the output capacitor, the approximate inductance value and output capacitor value can be obtained, which can be employed to ensuring the dynamic performance of the direct-current control strategy with compensation operation in case the inductance and capacitor are not know.
4) Even when the adopted circuit parameters including the leakage inductance and the output capacitor are a few differences from their actual values, the excellent dynamic performance can also be provided for the FB dc–dc converter.

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