A Delay-Line DPWM Architecture With Compensation Module and Delay-Adjustable Unit Based on DLL

Daying Sun, Jiayi Hu, Chong Wang, Xiong Cheng, and Wenhua Gu

***Abstract*—Due to the increasing resolution, the duty cycle in digital pulsewidth modulation (DPWM) is affected by the variation of external clock frequency or temperature, and the time error becomes larger and larger, even reaches a few nanoseconds. The increment of the duty cycle will affect the regulation performance of the converter and the output of DPWM. In this article, a delay-line DPWM architecture with a compensation module and a delay-adjustable unit based on delay-locked loop is proposed. The delay-adjustable unit is realized by using a multiplexer and some delay paths with different delay times, which effectively reduces the influence of temperature or the frequency changes from the input clock. Furthermore, a time compensation method is used to reduce the error generated by the critical path delays. A 10-bit DPWM with 781-kHz switching frequency is achieved on A-7 (xc7a100tfgg484) Xilinx FPGA, and the time error of the architecture decreases to around 500 ps. The duty cycle range is from 1.63% to 98.44%.**

***Index Terms*—Digital pulsewidth modulation (DPWM), delay-adjustable unit, error compensation, field-programmable gate array (FPGA).**

I. Introduction

DUE to the rapid development of semiconductor technology, the digital switching converter has obtained more attentions and become the research hotspot of major companies and scientific research institutions [1]–[3]. An analog-to-digital converter (ADC), a digital compensator, and a digital pulsewidth modulation (DPWM) module are necessary in the digital control loop of switching converter. To improve the performance, an ADC with high accuracy and high resolution is often required. Meanwhile, higher resolution is necessary for DPWM to avoid the undesired limited cycling [4]–[7]. Thus, as the high-performance ADC exists, high-performance DPWM with high resolution and stability is required.

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The authors are with the School of Electronic and Optical Engineering, Nanjing University of Science and Technology, Nanjing 210094, China (e-mail: hasdysun@126.com; 418029834@qq.com; 1040623911@qq.com; njust_iccheng@foxmail.com; guwenhua@njust.edu.cn).

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In order to improve the resolution and the stability of DPWM, hybrid digital-analog systems are proposed in many literature works [8]–[11]. Most of them add analog circuit designs or use analog techniques to optimize the traditional DPWM structure. The stability of the system and the utilization of resources are improved via the aforementioned solutions, but the complexity and the cost of the design are inevitably increased. For example, Lukic *et al*. [8] demonstrate a flexible four-phase digital PWM controller. The new proposed multiphase DPWM (MDPWM) utilizes a programmable counter, a delay line, and a digital logic circuit. The time of the transient response is reduced by the MDPWM architecture, which means that the delay time of the circuit is reduced, thereby the resolution is increased. However, the resolution and the delay time of DPWM are still affected by the process, voltage, and temperature (PVT) of the circuits.

Considering the high programmability and outstanding performance of field-programmable gate array (FPGA), many DPWM architectures based on FPGA have been proposed to improve the DPWM resolution and reduce the design complexity [12]–[17]. Architectures composed of the coarse-tuning module and the fine-tuning module are often used, where the coarse-tuning module uses the counter-comparator method and the fine-tuning module uses the different control methods. In [13], the DPWM architecture is based on the counter-comparator method with a digital clock manager (DCM). The inherited phase shifting characteristics of DCM simplify the generation of the duty cycle and improve the regulation accuracy of the converter. To implement the regulation of the delay line, the architecture of the carry chain logic path is realized and simplified in [14] and [15], respectively. However, a large amount of manual works are required while designing the above DPWM modules, which needs nonmonotonic operation and long designing time to avoid time errors. The digital dithering technology is used in [16] and [17], but the slow response in multicycle adjustment cannot be avoided. In the above DPWM architectures, the time error of the output signal is large. As their fine-tuning module is consisted of the delay-unadjustable units, the time error of the output duty cycle caused by the effect of the PVT or other factors cannot be reduced.

In order to reduce the time error, considering the variation of the temperature or the input clock frequency, a delay-line DPWM architecture based on delay-locked loop (DLL) is proposed to automatically regulate the total delay time of the delay line. However, the critical path delays of the architecture make

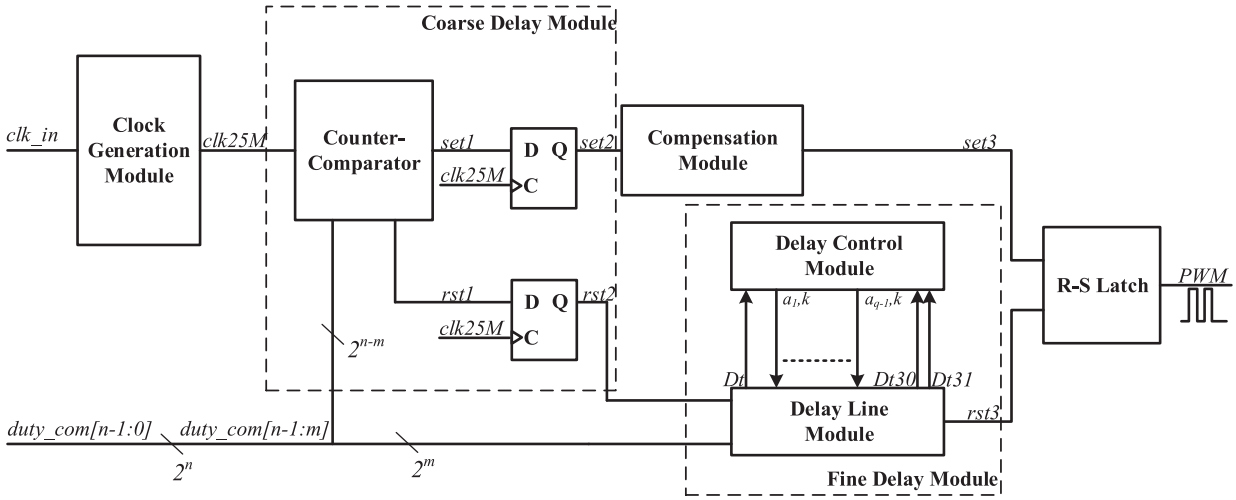

Fig. 1. Top-level of a delay line DPWM architecture with the compensation module and the delay-adjustable unit based on DLL.

the high-level duration of the output duty cycle larger than the theoretical value. To compensate the critical path delays, a compensation module is used. In summary, a delay-line

DPWM architecture with the compensation module and the delay-adjustable unit based on DLL is proposed in this article. It is verified on FPGA.

The rest of this article is organized as follows. The delay-line DPWM architecture with the compensation module and the delay-adjustable unit based on DLL is analyzed in Section II. Then, the whole architecture of DPWM and experimental results are committed in Sections III. Finally, Section IV concludes the article.

II. Analysis of the Proposed DPWM Architecture

The top-level of the proposed DPWM architecture is shown in Fig. 1. It consists of a clock generation module, a coarse delay module, a fine delay module, a compensation module, and an R-S latch.

The clock generation module is used to synchronize the input clock signal. The counter-comparator module is used to implement the coarse-tuning of the output digital pulse signal. The delay line module and the delay control module are used to implement the fine-tuning of the output digital pulse signal. The compensation module is adopted to compensate the unavoidable delay time of the critical path. Furthermore, several D flip-flops are used to remove the glitch of the signal. clk_in is the external clock signal of DPWM, and duty_com[n-1:0] is the duty command, where *n* is the resolution of DPWM. When the output of the counter equals "0," the counter-comparator module outputs a high-level signal set1. set1 is sent to a D flip-flop to remove the glitch. The output set2 is sent to the compensation module to generate set3 which changes the R-S latch output signal PWM into a high-level signal. When the output of the counter equals the most significant bits duty_com[n-1:m], the counter-comparator module outputs a high-level signal rst1. rst1 is sent to a D flip-flop to remove the glitch. The output rst2 is sent to the delay line module to generate rst3 which changes the R-S latch output signal PWM into a low-level signal. Thereby, the required output duty cycle PWM is obtained. Detailed analysis of the operation will be explained in the following part.

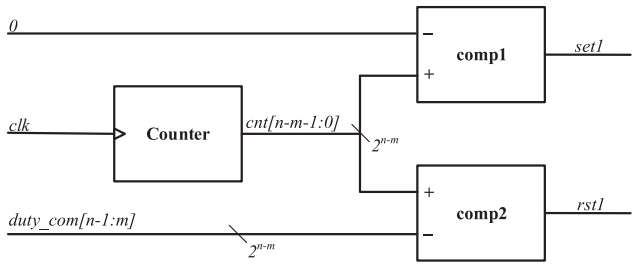

Fig. 2. Proposed counter-comparator module.

A. Coarse Delay Module Based on Counter-Comparator Module

Coarse delay function is realized by the proposed counter-comparator module, as shown in Fig. 2. The timing diagram of the counter-comparator module is shown in Fig. 3. It contains a counter and two comparators (comp1 and comp2). The counter counts at the rising edge of clock signal clk25M, which is generated by the clock generation module. The output cnt[n-m-1:0] increases from "0" to "2^{n-m-1}" by an increment of "1" in a single switching cycle. cnt[n-m-1:0] is compared with "0" in comp1, and the comparison result is *set1*. When cnt[n-m-1:0] equals "0", set1 turns high. Otherwise, set1 keeps low. cnt[n-m-1:0] is compared with the most significant bits duty_com[n-1:m] in comp2, and the comparison result is rst1. To compensate for one cycle delay introduced by the D flip-flop, the output of the counter is compared with duty_com[n-1:m]-1 instead of duty_com[n-1:m], as shown in Fig. 4. Thus, when cnt[n-m-1:0] equals duty_com[n-1:m]-1, rst1 turns high. Otherwise, rst1 keeps low. set1 and rst1 are sent to D flip-flop to remove the glitch.

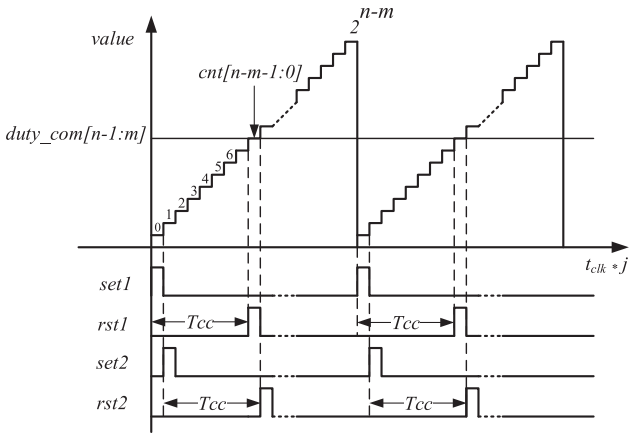

Fig. 3. Timing diagram of the counter-comparator module.

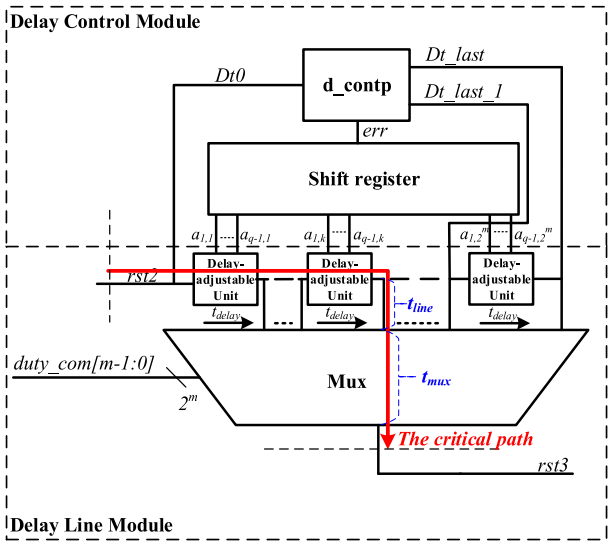

Fig. 4. Fine delay module architecture.

This coarse delay module generates a delay time and satisfies the following relationship:

$$T_{\rm cc} = j \times t_{\rm clk}\left(0 \le j \le 2^{n-m}-1\right) \tag{1}$$

where j is the corresponding decimal number of duty_com[n-1:m], $T_{\rm cc}$ is an integer multiple of the clock cycle, and $t_{\rm clk}$ is the period time of clock signal clk25M.

B. Fine Delay Module Based on DLL

The architecture of the fine delay module is shown in Fig. 5. Fine-tuning is realized by a multiplexer and a number of 2^m delay-adjustable units. The delay time of the delay-adjustable unit is detected by the d_contp module and modified by the shift register module.

1) Delay Line Module: Reset signal rst2 is first passed into the delay line module with 2^m delay-adjustable units that are connected sequentially, and each output of the units is connected to a multiplexer. Assuming that the transportation time of a delay-adjustable unit is $t_{\rm delay}$, this delay time must satisfy (2). m is the bit width of the least significant bits of the duty command duty_com[m-1:0], and the total delay time of all the serially connected delay-adjustable units is equal to the input clock cycle $t_{\rm clk}$. The transportation time of kth output of the delay-adjustable unit $T_{dl}(k)$ can be expressed in (3). Thus, selecting different input signals by the least significant bits of duty command duty_com[m-1:0], fine-tuning can be realized

$$t_{\rm clk} = 2^m \times t_{\rm delay} \tag{2}$$

$$T_{dl}\left(k\right) = k \times t_{\rm delay} = k \times \frac{t_{\rm clk}}{2^m}\left(1 \le k \le 2^m\right). \tag{3}$$

The output signal of the multiplexer rst3 is sent to the R-S latch to pull down the output signal.

Owing to the variation of the input clock frequency or the temperature, the input clock cycle $t_{\rm clk}$ and the delay time of the delay unit will change, respectively. If the delay time of the delay unit is unadjustable, the average delay time of delay line module is not equal to the theoretical value when the $t_{\rm clk}$ or the delay time of delay unit is changed, and the larger the change value, the larger the error value. Thus, the delay units are realized by the delay-adjustable units. Considering (2), the delay time of each delay-adjustable unit $t_{\rm delay}$ needs to be modified accordingly. The architecture of the kth delay-adjustable unit is shown in Fig. 6. A number of 2 ($q-1$) NOT gates are serially connected, and the delay paths with different number of NOT gates are selected by the control words "$a_{1,k}$~$a_{q\text{-}1,k}$". When the pth path is selected, "$a_{1,k}$~$a_{q\text{-}1,k}$" makes the OR gate Sp outputs "0" and the other OR gates such as $S1$, $S2$, …, $Sp-1$, $Sp+1$, …,Sq output "1." The value of each control word satisfies the following relationship:

$$a_{i,k} = \begin{cases} 0 & i < p \\ 1 & i \ge p. \end{cases} \quad (1 \le p \le q) \tag{4}$$

The specific procedure is as follows: when the delay signal $i_{k\text{-}1}$ enters the kth delay-adjustable unit, it first passes through a series of NOT gates. Then, the outputs of the delay path with $2(p-1)$ NOT gates and the OR gate Sp are sent to a dual-input NOR

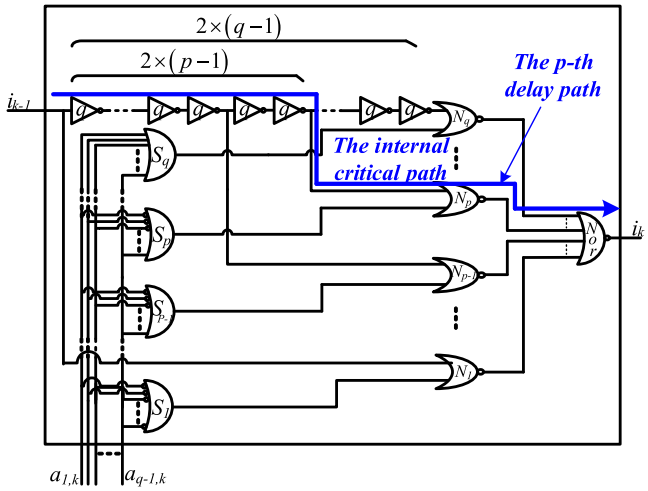

Fig. 5. Architecture of the delay-adjustable unit.

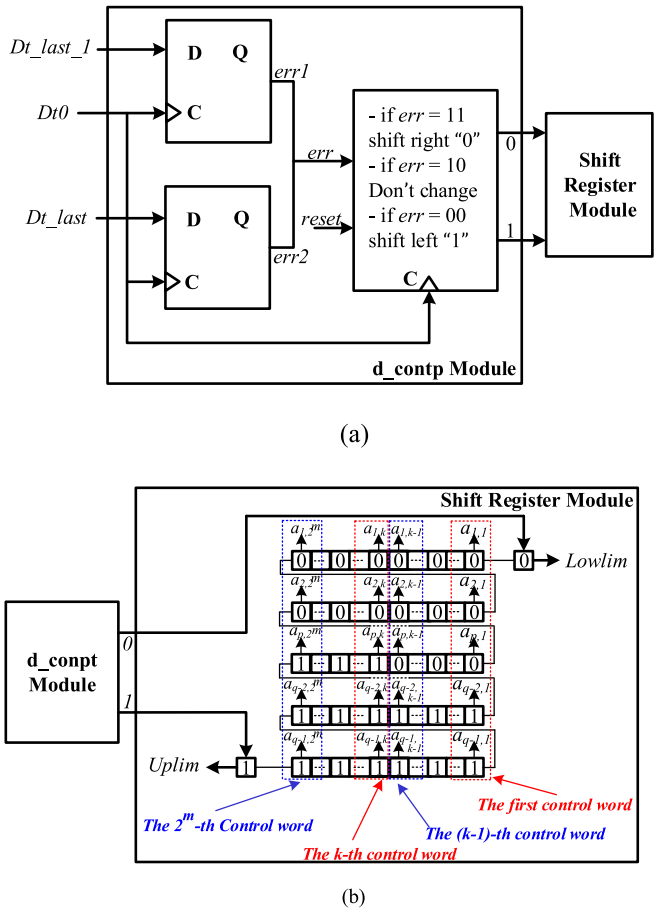

Fig. 6. Architecture of the delay control module. (a) d_conpt module. (b) Shift register module.

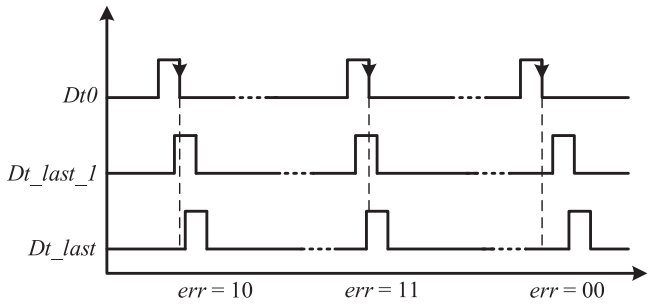

Fig. 7. Information detected by the signal Dt0.

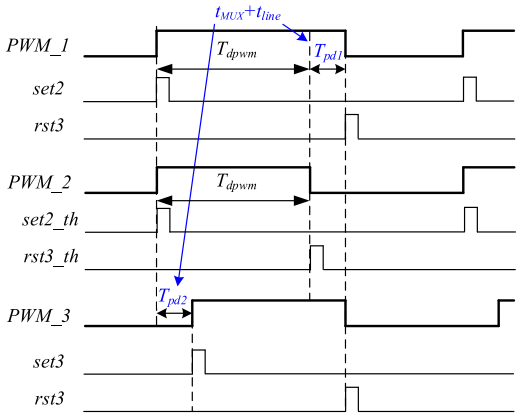

Fig. 8. Duty-cycle increment phenomenon and its solution.

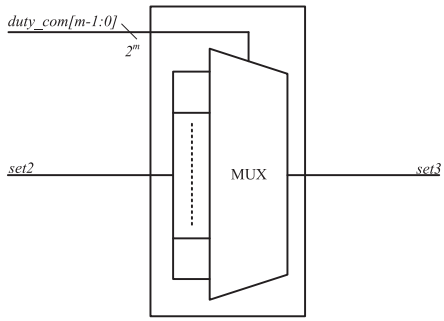

Fig. 9. Architecture of the compensation module.

gate *Np*. When the *Sp* outputs "0," other OR gates output "1," which means that the other delay paths are turn-OFF. The output of *Np* is the same as its input signal and the other dual-input NOR gates output "0." Finally, all of the dual-input NOR gates are connected to the multi-input NOR gate Nor to make the level of i_k keep consistent with i_{k-1}.

In the *p*th path, there are a number of 2 $(p-1)$ NOT gates, a NOR gate, and a multi-input NOR gate. There is no NOT gate on the path with the lowest delay time. The delay time of the signal t_{delay} in the fine delay module satisfies

$$t_{\mathrm{delay}} = 2\,(p-1) \times t_{\mathrm{NOT}} + t_{\mathrm{nor}} + t_{\mathrm{mnor}}\,(0 \le p \le q-1) \tag{5}$$

where t_{nor} is the delay time of the dual-input NOR gate and t_{mnor} is the delay time of the multi-input NOR gate.

2) Delay Control Module: As aforementioned, the delay time of the delay-adjustable unit should be adjustable by the delay control module, which can be achieved via the basic operation principle of DLL. The architecture of the delay control module is shown in Fig. 7. In this article, a delay line module with 2^m delay units is used.

In order to generate a signal that controls and adjusts the delay time of the delay-adjustable units, shift registers are serially connected. The delay time of each individual delay-adjustable unit is controlled by its corresponding shift register. The number of shift registers in one delay-adjustable unit is equal to the bit number of the control words. The *k*th delay-adjustable unit control words are represented by "$a_{1,k}a_{2,k}\ldots a_{q-2,k}a_{q-1,k}$."

The inputs of the delay control module are signal *Dt0*, *Dt_last_1*, and *Dt_last*, and these three signals are the outputs of the first, the last but one [the (2^m-1)th] and the last [the (2^m)th] delay-adjustable units, respectively. Ideally, the total delay time of the 2^m delay units should be equal to a single clock cycle t_{clk}. Therefore, the falling edge of the signal *Dt0* should be aligned with the rising edge of the signal *Dt_last*. The rising and falling edges are checked by the edge trigger of the delay control module

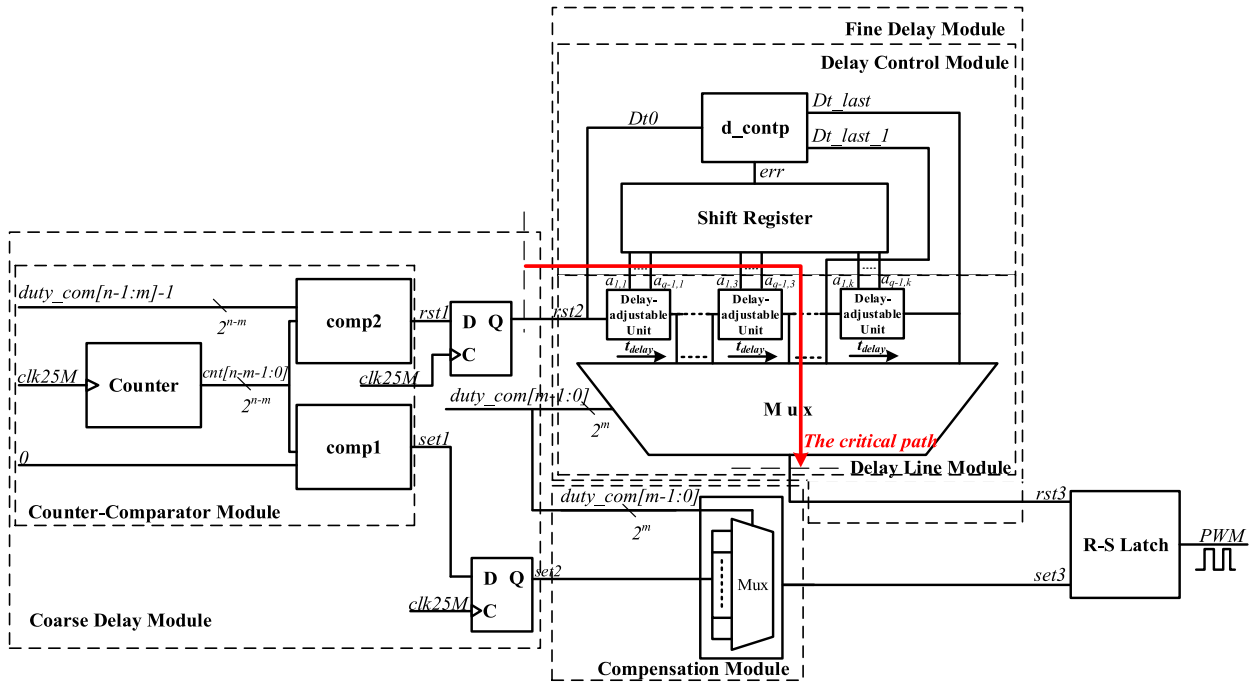

Fig. 10. A delay-line DPWM architecture with the compensation module and the delay-adjustable unit based on DLL.

as in Fig. 8. Since jitter of the output of DPWM exists, the falling edge of the signal *Dt0* is often compared with the rising edges which are considered to be be-tween the rising edges of signal *Dt_last_1* and *Dt_last* in steady state, the detection result *err* is assigned with "10" in this condition, the control words keep unchanged. Assuming that the control is stable, all the control words are serially connected as in Fig. 7. The *p*th delay path is selected inside from the first delay-adjustable unit to the $(k-1)$th delay-adjustable unit, while the $(p-1)$th delay path is selected inside from the *k*th delay-adjustable unit to the 2^mth delay-adjustable unit.

The average delay time ofthe delay line module almost reaches the theoretical value via the automatic regulation of 2^m delay-adjustable units.

If the falling edge of *Dt0* is before the rising edge of *Dt_last*_1, the delay time of delay-adjustable unit needs to be reduced and the detection result *err* changes to "00." If *p* is larger than zero, "$a_{p\text{-}1,k}$" turns high and the $(p-1)$th delay path in the *k*th delay-adjustable unit will replace the *p*th delay path. Otherwise, the delay-adjustable unit has reached the minimum delay time and the warning signal Lowlim turns high.

If the falling edge of *Dt0* is after the rising edge of *Dt_last*, the delay time of delay-adjustable unit needs to be increased and the detection result *err* changes to "11." If *p* is smaller than $(q-1)$, "$a_{p\text{-}1,k}$" turns low and the $(p+1)$th delay path in the *k*th delay-adjustable unit will replace the *p*th delay path. Otherwise, the delay-adjustable unit has reached the maximum delay time and the warning signal Uplim turns low.

When Lowlim goes high or Uplim goes low, the delay control module cannot satisfy the requirement that the falling edge of the signal *Dt0* aligns the partial alignment between the rising edges of the signals *Dt_last*_1 and *Dt_last*.

C. Proposed Compensation Module

When a DPWM architecture works with higher switching frequency and the resolution becomes smaller, the critical path delays including logic elements and interconnects are close to the same magnitude level as the switching period. Meanwhile, the difference between two adjacent duty cycle values becomes smaller, which means the critical path delays on the output signal PWM becomes larger, so it is more necessary to optimize and compensate the critical path [18].

Fig. 9 shows that the output duty cycle PWM_1 is obtained by the signals set2 and rst3, the theoretical output duty cycle PWM_2 is obtained by the theoretical signals set2_th and rst3_th. Since the path delay of the critical path T_{pd1} exists, the high-level duration of PWM_1 is longer than PWM_2. T_{pd1} satisfies the following relationship:

$$T_{\mathrm{pd1}} = t_{\mathrm{MUX}} + t_{\mathrm{line}}. \tag{6}$$

As shown in Fig. 5, t_{MUX} is the delay time of the multiplexer inside the delay line module, t_{line} is the delay time of interconnects. The rising edges of PWM_1 and PWM_2 arrive at the same time during one switching cycle. However, the falling edge of PWM_1 is after PWM_2 because of T_{pd1}, and the difference of high-level duration between PWM_1 and PWM_2 exactly equals T_{pd1}. Furthermore, when the signal enters the multiplexer, the delay time from the different input ports to the output port is different. To mitigate the impact in this situation, a multiplexer is used in the compensation module, as shown in Fig. 10, the output PWM_3 is turned ON by set3 and turned OFF by rst3.

The output of the multiplexer set3 in the compensation module is after set2, and the difference of rising edges between set2

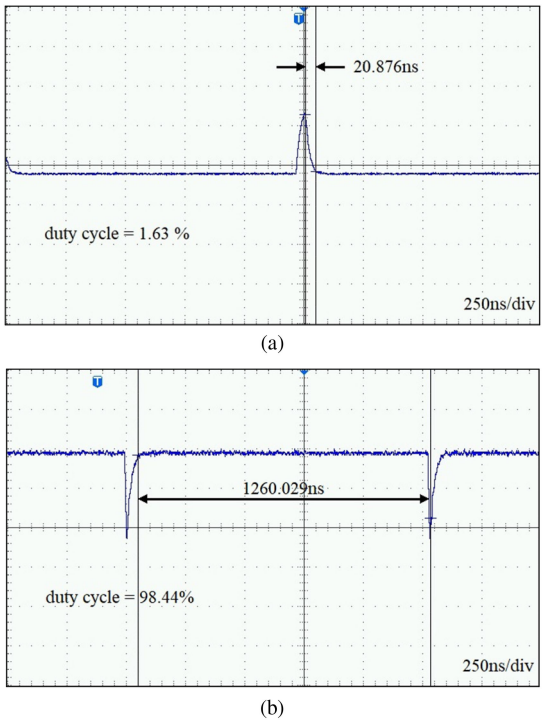

Fig. 11. Duty cycle range of the proposed DPWM. (a) Minimum duty cycle. (b) Maximum duty cycle.

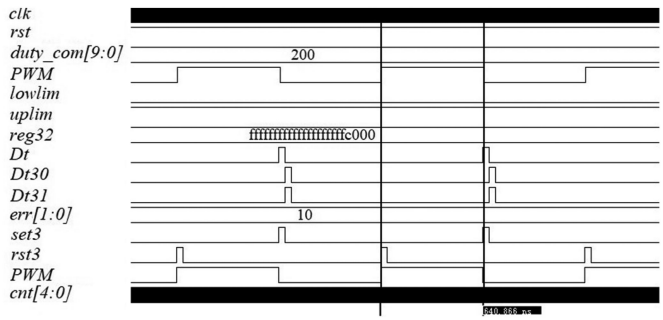

Fig. 12. Timing diagram of the proposed DPWM architecture in 25-MHz clock frequency.

and set3 equals T_{pd2}. Compared to t_{MUX}, t_{line} is too short, it is not considered in the design of T_{pd2}. Therefore, to guarantee that T_{pd2} equals T_{pd1}, the type of multiplexer in the compensation module is the same as the one which is used in the delay line module, so this multiplexer also has a number of 2^m input ports. In addition, when the multiplexer inside the delay line module selects the output of *k*th delay-adjustable unit by duty_com[m-1:0], the multiplexer inside the compensation module also selects the input signal of *k*th port by duty_com[m-1:0], and the connection mode of the two multiplexers is same; so T_{pd2} satisfies the following relationship:

$$T_{\mathrm{pd2}} \approx T_{\mathrm{pd1}}. \tag{7}$$

As aforementioned, the high-level duration of the output is equal to the total delay time T_{total} of the coarse delay module,

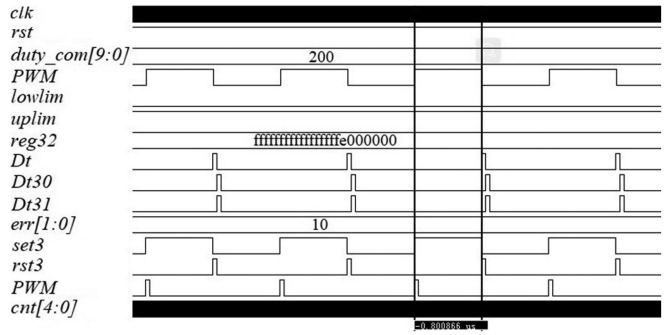

Fig. 13. Timing diagram after clock frequency is changed from 25 to 20 MHz.

the fine delay module, and T_{pd1}. Thus, the duty cycle satisfies the following relationship:

$$\begin{aligned}\mathrm{dutycycle} &= \frac{T_{\mathrm{total}}}{2^{n-m} \times t_{clk}} \\ &= \frac{T_{cc} + T_{dl}(k) + T_{\mathrm{pd1}}}{2^{n-m} \times t_{clk}} \\ &= \frac{j \times t_{clk} + k \times t_{\mathrm{delay}} + T_{\mathrm{pd1}}}{2^{n-m} \times t_{clk}}.\end{aligned} \tag{8}$$

III. Experimental Results

The proposed DPWM is implemented in Vivado 2017.4 and the implementation is built on the Xilinx Artix-7 FPGA development board. The global working frequency is 25 MHz, and the switching frequency is 781 kHz. The five most significant bits of duty command duty_com[9:5] are used in the counter-comparator module. Meanwhile, the five least significant bits of duty command duty_com[4:0] are used in the delay line module with 32 delay-adjustable units. There are 12 NOT gates in each delay unit which is divided into four delay paths, and the delay time of each NOT gate is approximately equal to 0.5 ns. The maximum delay time of delay-adjustable unit equals 6.5 ns and the minimum delay time of delay-adjustable unit equals 0.9 ns, which means that the theoretical switching frequency range is from 150 kHz to 1.1 MHz.

A. Duty Cycle Range of Proposed DPWM

When the input clock frequency is 25 MHz, the duty cycle range can be adjusted from 1.63% to 98. 44% as in Fig. 11, and the duty command are, respectively, set to 10'd16 and 10'd1008. The duty cycle range is larger after using the proposed DPWM architecture.

B. Stability of Proposed DPWM

As aforementioned, because the delay time in the delay unit is unadjustable, errors of the final outputs are greatly increased in prior DPWM architecture when the input clock frequency changes. Thus, the product of 2^m and t_{delay} is not equal to t_{clk}, where t_{clk}' is the actual input clock cycle. Due to the effects of

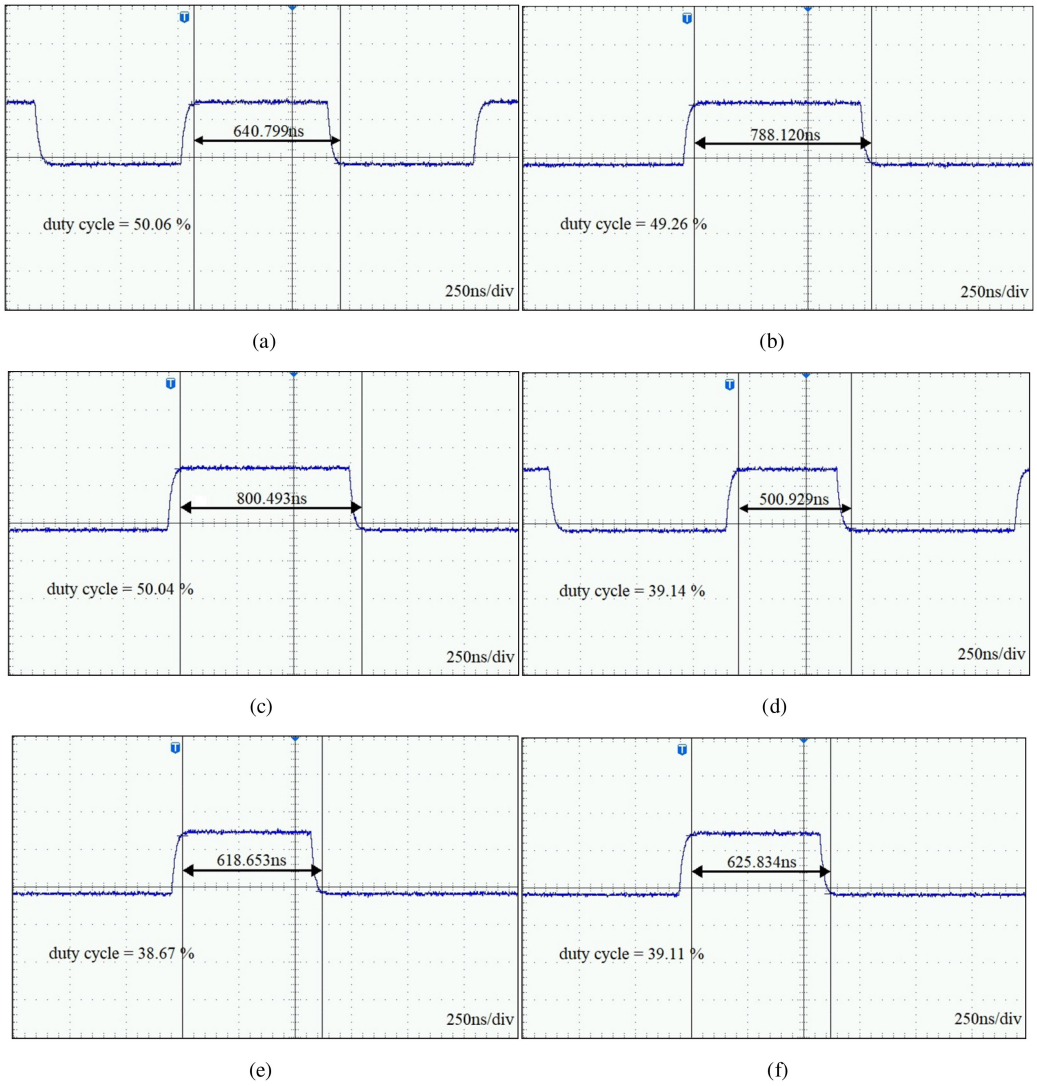

Fig. 14. Comparison of the duty cycle of the DPWM with and without the delay-adjustable unit when the input clock frequency change from 25 to 20 MHz. (a) Delay-adjustable unit, 25 MHz, duty_com[9:0] = 10'd511. (b) Delay-unadjustable unit, 20 MHz, duty_com[9:0] = 10'd511. (c) Delay-adjustable unit, 20 MHz, duty_com[9:0] = 10'd511. (d) Delay-adjustable unit, 25 MHz, duty_com[9:0] = 10'd400. (e) Delay-unadjustable unit, 20 MHz, duty_com[9:0] = 10'd400. (f) Delay-adjustable unit, 20MHz, duty_com[9:0] = 10'd400.

the PVT or other factors, the deviation from the theoretical input clock always exists for the actual input clock.

However, the effect of input clock frequency variation on the output duty cycle is reduced via the delay line with the delay-adjustable unit, which is proposed in this article. In order to analyze the stability of DPWM, the input clock frequency is changed from 25 to 20 MHz, and the duty command is set as 10'h200. Considering the changes in temperature or the input clock frequency, the delay time of delay unit should be automatically modified to adapt the variation. In order to reduce the set-up time, the best initial state of the delay units is obtained by extensive experiments and it is as follows. Half of the delay units are set to the maximum delay time, and the others are set to the minimum delay time, then they are adjusted by the d_contp module. The control signal of the shift register reg32 changes from 96'hffffffff_ffffffff_ffffc000 to 96'hffffffff_ffffffff_fe000000 as shown in Figs. 12 and 13, which means that the delay time of the delay line module is automatically adjusted as needed. reg32 is adjusted based on the previously stable value, which will reduce its modification period [19]. In addition, the theoretical value of the high-level duration and the duty cycle are 801.563 ns and 50.10%, respectively. The simulation result is shown in Fig. 13, it can be seen that the high-level equals 800.866 ns, and the duty cycle equals 50.04%. The output duty cycle of proposed DPWM architecture is stable when the input frequency is changed.

In order to verify the stability of the proposed DPWM architecture, the results are shown in Fig. 14. When the designed input frequency is 25 MHz, the control words are 96'hffff-ffff_ffffffff_fffffe00. When the duty cycle command *duty_com[9:0]* is 10'd511, the output of the DPWM with the delay-adjustable unit is shown in Fig. 14(a). The duty cycle is 50.06% and the high-level duration is 640.799 ns. Compared to the theoretical duty cycle 50% and the theoretical high-level duration 640.000 ns, the duty cycle error is 0.06%, and the

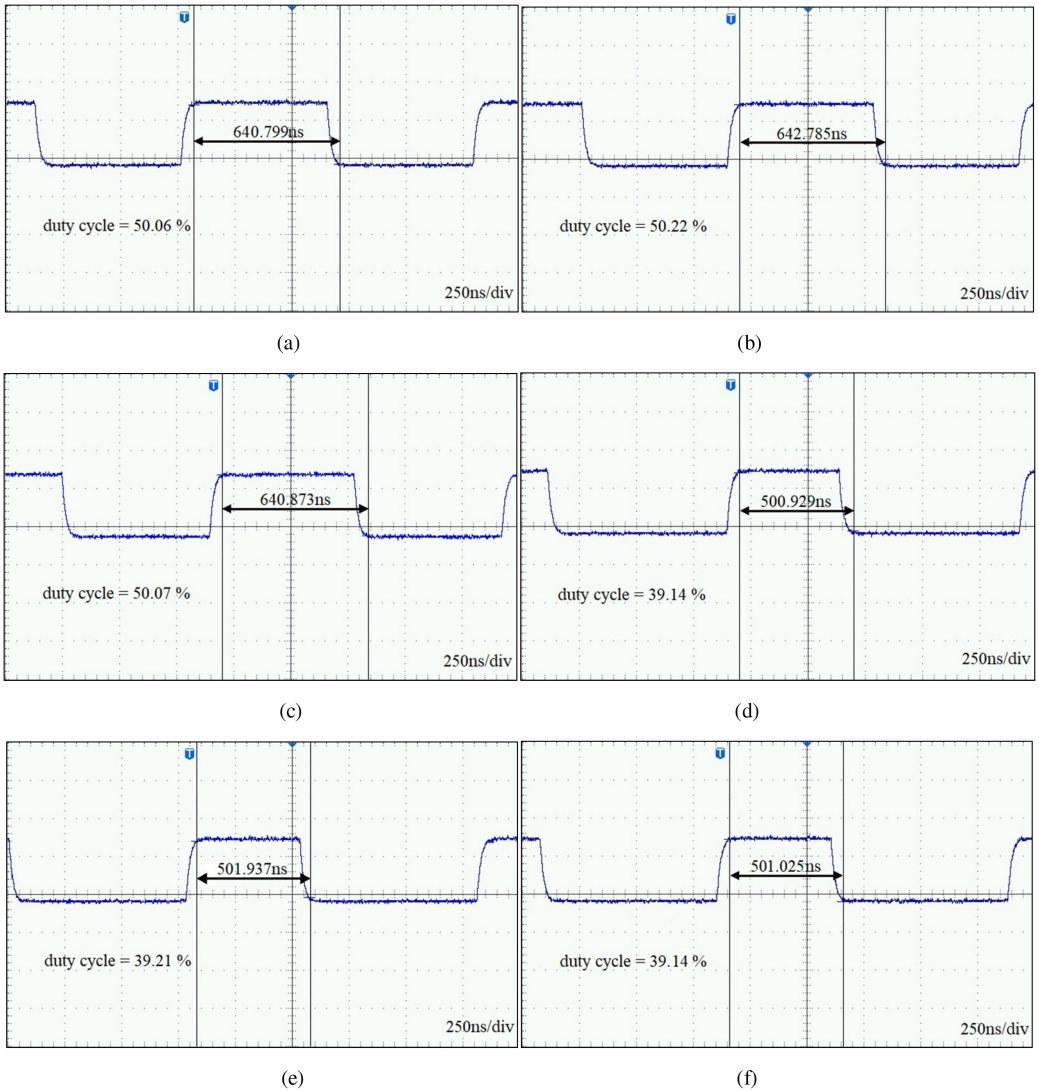

Fig. 15. Comparison of the duty cycle when the temperature changes from 20 to 60 °C. (a) Delay-adjustable unit, 20 °C, duty_com[9:0] = 10'd511. (b) Delay-unadjustable unit, 60 °C, duty_com[9:0] = 10'd511. (c) Delay-adjustable unit, 60 °C, duty_com[9:0] = 10'd511. (d) Delay-adjustable unit, 20 °C, duty_com[9:0] = 10'd400. (e) Delay-unadjustable unit, 60 °C, duty_com[9:0] = 10'd400. (f) Delay-adjustable unit, 60 °C, duty_com[9:0] = 10'd400.

high-level duration error is 0.799 ns. When the input frequency changes to 20 MHz and the control words are unchanged, the duty cycle waveform is shown in Fig. 14(b). The duty cycle is 49.26% and the high-level duration is 788.120 ns. The duty cycle error is 0.74%. The time error of output duty cycle increases when the input frequency varies. When the delay-adjustable unit is used, the duty cycle waveform is shown in Fig. 14(c). The control words change to 96'hffffffff_ffffffff_f-0000000. The duty cycle is 50.04%, and the high-level duration is 800.493 ns. The duty cycle error is 0.04% and the high-level duration error is 0.493 ns. Compared to the DPWM with the delay-unadjustable unit, the duty cycle error is greatly reduced. Similarly, when the duty cycle command duty_com[9:0] is 10'd400 and the input frequency changes to 20 MHz, compared to the duty cycle error of traditional DPWM, the duty cycle error of the proposed DPWM with the delay-adjustable unit is reduced from 0.49% to 0.05%.

When the temperature changes, the delay time of the component varies. The delay time of the delay-adjustable unit will change to make the output duty cycle of DPWM stable. Fig. 15 shows the comparison of the output duty cycle of the DPWM with and without the delay-adjustable unit when the temperature changes from 20 to 60 °C.

When the temperature is 20 °C and duty_com[9:0] equals 10'd511, the duty cycle of the DPWM equals 50.06%, as shown in Fig. 15(a). The control words in this condition are 96'hffffffff_ffffffff_ffffe000. The duty cycle error is 0.06% compared to the theoretical value, which is 50%. When the temperature changes from 20 to 60 °C and the control words keep unchanged, the duty cycle of the DPWM with the delay-unadjustable unit equals 50.22%, as shown in Fig. 15(b). The duty cycle error is 0.22% and it is increased in this condition. When temperature changes to 60 °C, the duty cycle of the

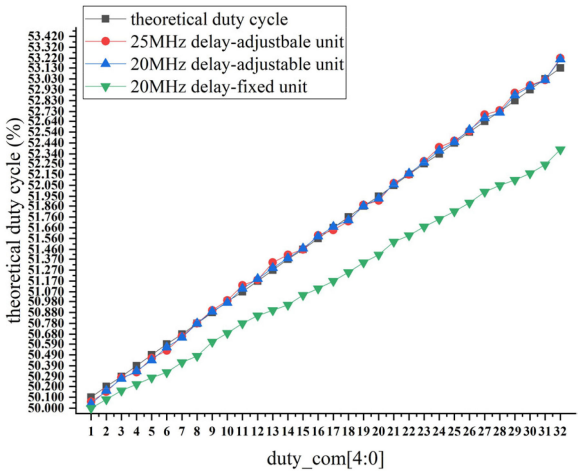

Fig. 16. The comparison between curves of the duty cycle of the DPWM with and without the delay-adjustable unit when the input clock frequency increases from 10'd512 to 10'd543.

DPWM with the delay-adjustable unit equals 50.07%, as shown in Fig. 15(c). The duty cycle error is reduced to 0.07%.

The control words change to 96'hffffffff_ffffffff_fffff800. Similarly, as in Fig. 15(d)–(f), when duty_com[9:0] equals 10'd400, we have made the same comparison among the different outputs. When the temperature is 60 °C, the duty cycle error is reduced from 0.05% to 0.02% after the delay-adjustable unit is applied.

To further verify the validity of the delay-adjustable unit and the stability of the proposed DPWM, the total comparison between the DPWMs with and without the delay-adjustable unit is made, as shown in Fig. 16. Assuming that the theoretical input clock frequency is 25 MHz, the theoretical duty cycle increases linearly when duty_com[9:0] increases from 10'd512 to 10'd543. For the DPWM with the delay-adjustable unit, when the input frequency of DPWM is 25 MHz, the time error of the duty cycle is rather small, and the largest error of duty cycle is 0.09%. When the input frequency of the above traditional DPWM changes to 20 MHz, the time error of the duty cycle gets larger when the five least significant bits duty_com[4:0] gets larger. The largest duty cycle error is 0.25%. When the DPWM with the delay-adjustable unit is applied, the input frequency changes to 20 MHz. The time error of the duty cycle is still small and is within 0.08%. Thus, when the input clock frequency changes, the delay time of the delay-adjustable unit is automatically modified and the time error of the duty cycle is reduced.

C. Compensation Module of Proposed DPWM

In order to verify the function of the compensation module, the proposed DPWM architectures with and without the compensation module are compared to observe the effect of the critical path delay on the output duty cycle. The parameters of the proposed DPWM architecture without the compensation module are shown in Fig. 17. It can be seen that when the input frequency is 25 MHz, the high-level duration is 637.983 ns, and the

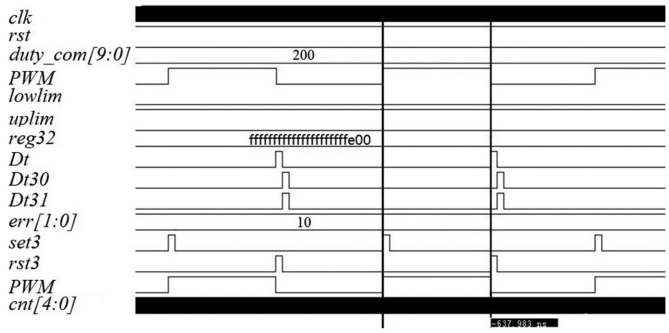

Fig. 17. Timing diagram of the architecture without the compensation module.

TABLE I
EXPERIMENTAL DUTY CYCLE FOR DIFFERENT DUTY COMMANDS

Duty command	Uncompensated (ns)	Error value(ns)	Compensated (ns)	Error value(ns)
10000_00000	642.017	0.767	641.295	0.045
10000_00010	645.343	1.593	642.301	-0.199
10000_00101	649.748	2.248	646.321	0.071
10000_01100	658.496	2.246	656.363	0.113
10000_10010	665.882	2.132	663.829	0.079
10000_11111	683.438	3.438	681.180	1.180

signal *reg32* changes from 96'hffffffff_ffff0000_00-000000 to 96'hffffffff_ffffffff_fffffe00. The duty command equals 10'h200, and the theoretical high-level duration equals 641.250 ns. Thus, the time error is reduced when the compensation module is used, as shown in Fig. 14.

In order to further demonstrate the validity of the compensation module, the DPWM architectures with and without compensation module are implemented on FPGA, and the duty command is changed to increase the universality of the result. Fig. 18 clearly shows the merits of the compensation module. When duty_com*[*9:0*]* equals 10'd511 and the input clock frequency is 25 MHz, the ideal duty cycle equals 50.00% and the ideal high-level duration equals 640.000 ns. As in Fig. 18(a), the results of the case without the compensation module are 50.24% and 643.038 ns, respectively. As in Fig. 18(b), the duty cycle of the DPWM with the compensation module is 50.06% and the high-level duration is 640.799 ns. Comparing with the theoretical value, the time error of the DPWM with the compensation module is smaller. Similarly, when duty_com[9:0] changes from 10'd511 to 10'd80, the ideal duty cycle equals 7.91% and the ideal high-level duration equals 101.250 ns. As in Fig. 18(c), the duty cycle of the DPWM without the compensation module is 8.12% and the high-level duration is 103.996 ns. As in Fig. 18(d), the duty cycle of the DPWM with the compensation module is 7.88% and the high-level duration is 100.918 ns. The duty cycle error is reduced from 0.21% to 0.03%. Therefore, the compensation module can reduce the time error of the output duty cycle.

Several additional results are presented in Table I to further verify the compensation method. It can be seen that the error value of DPWM with the compensation module is obviously less than the case without the compensation module. The maximum

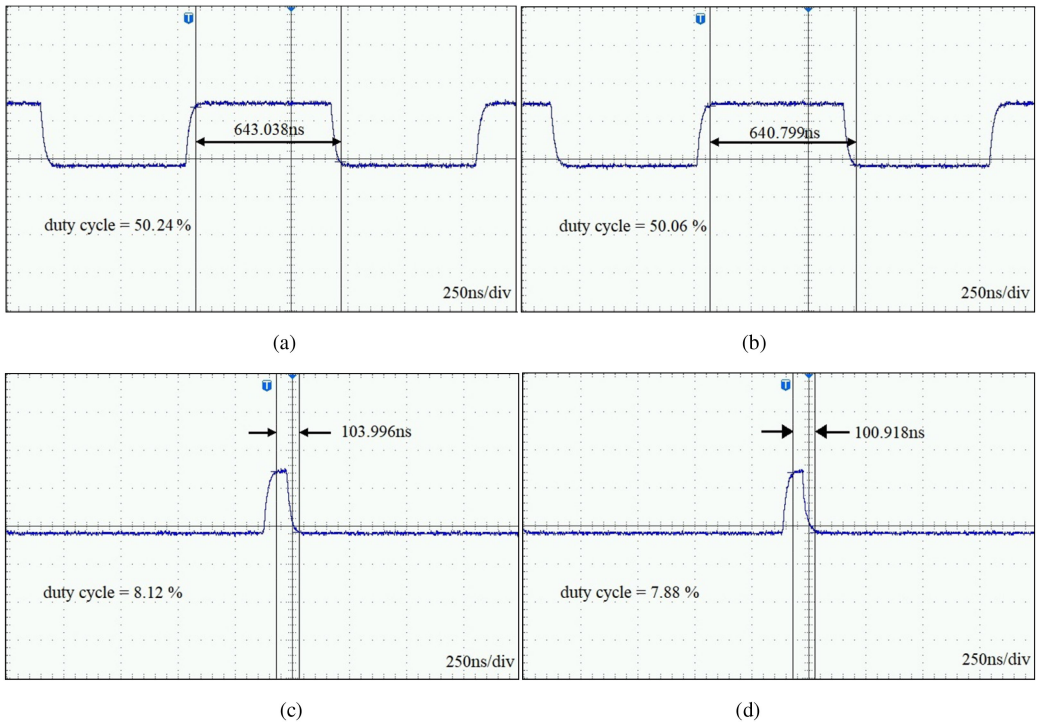

Fig. 18. Comparison of the duty cycle that the DPWM architecture with and without the compensation module. (a) Without a compensation module when duty_com[9:0] = 10'd511. (b) With a compensation module when duty_com[9:0] = 10'd511. (c) Without a compensation module when duty_com[9:0] = 10'd80. (d) With a compensation module when duty_com[9:0] = 10'd80.

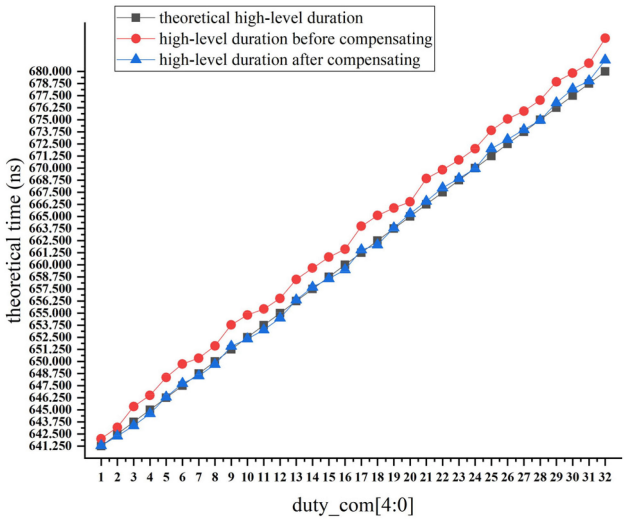

Fig. 19. High-level duration of the duty cycle from 10'd512 to 10'd543.

error values are 1.180 and 3.438 ns, respectively. High-level duration of the duty cycle with and without the compensation module has been investigated in Fig. 19. Assuming that the theoretical input clock frequency is 25 MHz, the theoretical duty cycle increases linearly when duty_com[9:0] increases from 10'd512 to 10'd543. The minimum time error of the duty cycle between actual time and theoretical time is 0.044 ns, while the maximum time error is 1.180 ns, and the range of the rest of time errors is from 0 to 500 ps. The curve of actual time overlaps the curve of theoretical time, indicating that the proposed DPWM has excellent linearity means that the high about 1.25 ns which can be concluded that the high mono resolution and monotonicity can be obtained. Furthermore, the difference between the neighboring duty command units is tonicity, and resolution is achieved via the architecture of the proposed DPWM.

D. Comparison With Prior DPWM Architectures

Table II provides a summary index of the proposed DPWM and a comparison with the prior DPWM architectures. All architectures use delay-unadjustable units, without considering the effect of changes in temperature or changes in input clock frequency and the effect of duty cycle increment caused by the critical path delays. The resolution of the proposed DPWM is lower than the resolution of the DPWMs in Table II. However, the stability of the proposed DPWM is relatively high compared with other works in Table II when the input frequency or temperature varies after working. And this wide range of the input clock frequency and the working temperature means that the proposed DPWM has high compatibility and stability. In addition, the proposed DPWM can compensate the critical path delays to decrease the time error of the output duty cycle, which means that the precision of the DPWM output is improved.

TABLE II
EXPERIMENTAL DUTY CYCLE FOR DIFFERENT DUTY COMMANDS

Ref.	Architecture	Switching Frequency	Time Resolution	Input frequency range	Compensation for Path	Bit	Adjustable Delay
[14]	Carry flag delay time	1 MHz	90 ps	50 MHz	No	12	No
[15]	Carry chain	1 MHz	90 ps	50 MHz	No	11	No
[16]	Dual clock	5 MHz	30 ps	100 MHz	No	12	No
[20]	DCM and LUT	781 kHz	625 ps	200 MHz	No	11	No
[21]	DCM	781 kHz	625 ps	200 MHz	No	11	No
This paper	DLL and delay-adjustable unit	781 kHz	1.25 ns	20-25 MHz	Yes	10	Yes

IV. CONCLUSION

This article introduces a delay line DPWM architecture with a delay-adjustable unit and compensation module based on DLL. The DPWM has a clock generation module, a 5-bit coarse delay module, a 5-bit fine delay module, a compensation module, and an R-S latch. When the input clock frequency varies or the delay time of the component is changed by the temperature variation, the required total delay time of the delay line module needs to be changed. Otherwise, the total delay time of the delay line module is not equal to the clock cycle, and the time error of the output duty cycle will increase. The proposed DPWM architecture can solve these problems by automatically adjusting the delay time of the delay-adjustable unit in the delay line module. The delay time of delay-adjusta- ble units is adjusted by the 96-bit shift registers and the signal detector. Furthermore, as the critical path delays of the delay line module lead to a larger high-level duration than the theoretical value, a compensation module is proposed to compensate the critical path delays in this article. The compensation module consists of a multiplexer, which is controlled by the least significant bits of duty command duty_com[m-1:0]. It has been implemented through a 10-bit DPWM with 781-kHz switching frequency, and it can achieve a wide duty range from 1.63% to 98.44% and the resolution is within 1.25 ns. The future work will focus on the verification of the proposed control method through experiments when the input frequency is higher.

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Daying Sun received the M.S. and Ph.D. degrees in integrated electronic engineering from Southeast University, Nanjing, China, in 2011 and 2015, respectively.

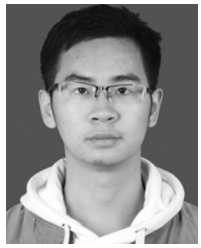
In 2015, he joined the School of Electronic and Optical Engineering, Nanjing University of Science and Technology, Nanjing, China, where he is currently an Associate Professor. His research interests include mixed-signal integrated circuits and deep learning.

Jiayi Hu received the B.S. degree in 2017 from the School of Electronics and Optoelectronics Engineering, Nanjing University of Science and Technology, Nanjing, China, where he is currently working toward the M.S. degree.

His research interests include digital pulse width modulation and single-inductor dual-output.

Chong Wang received the B.S., M.S., and Ph.D. degrees in electronic engineering from Southeast University, Nanjing, China, in 2012, 2015, and 2018, respectively.

In 2018, he joined the School of Electronic and Optical Engineering, Nanjing University of Science and Technology, Nanjing, China, where he is currently a Lecturer. His research interests include digital circuit design and low-power design.



Xiong Cheng received the B.S. degree in microelectronic science and engineering, in 2017, from the Nanjing University of Science and Technology, Nanjing, China, where he is currently working toward the Ph.D. degree.

His research interests include deep learning accelerator and low-power design.

Wenhua Gu received the B.S. degree in physical electronics and optoelectronics from Tsinghua University, Beijing, China, in 1999, the M.S. degree in optoelectronics from National University of Singapore, Singapore, in 2001, and the M.S. and Ph.D. degrees in electronic engineering from the University of Illinois at Urbana–Champaign, Chicago, IL, USA, in 2005 and 2008, respectively.

From 2008 to 2012, he was a Staff Engineer with the Infinera Corporation, Silicon Valley, USA. Since 2012, he is a Professor with the School of Electronic and Optical Engineering, Nanjing University of Science and Technology, Nanjing, China. His research interests include flexible electronic devices, mixed-signal integrated circuits.

Mr. Gu was the recipient of the Core Member of the High-Level “Innovation and Entrepreneurship” Education Team in Jiangsu Province, Jiangsu Province high-level "Innovation and Entrepreneurship" Key Discipline Talents Introduction Program, Nanjing University of Science and Technology “Zijin Star” Outstanding Talent and Henry Ford II Award in the University of Illinois at Urbana–Champaign.