A Composite Selective Harmonic Elimination Model Predictive Control for Seven-Level Hybrid-Clamped Inverters With Optimal Switching Patterns

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***Abstract*—A composite strategy that combines selective harmonic elimination pulsewidth modulation (SHE-PWM) and model predictive control (MPC) for seven-level hybrid-clamped (7L-HC) inverters is presented in this article. By introducing the unified SHE formulation, all seven-level switching patterns and corresponding switching angles can be obtained simultaneously. Therefore, the optimal switching pattern with the designed optimization goal of each modulation index can be evaluated, and the best expected output performance is achieved. For the voltage balancing issue of 7L-HC, MPC is adopted to control the dc-link and flying capacitors. After receiving the output voltage level signal from the SHE-PWM modulator, the optimal switching state that belongs to the received output voltage level that minimizes the cost function is selected by the MPC module, where the cost function is designed to simultaneously balance capacitor voltages and reduce the switching frequency. Dynamic weighting factors with variable band limits are also proposed to further improve the system performance. The potential industrial application of high-power motor drive is used as an example in designing the key parameters for both SHE and MPC parts. Simulation and experimental results confirmed the validity of this composite SHE-MPC strategy in reducing the switching frequency and improving harmonic performances while keeping capacitor voltages well balanced.**

***Index Terms*—Model predictive control (MPC), multilevel inverter, selective harmonic elimination (SHE), voltage balancing.**

I. Introduction

MULTILEVEL converters are widely implemented in high-power medium-voltage (MV) applications [1]–[3]. Generally, multilevel topologies reduce the blocking voltage of power semiconductors without connecting them in series, making it possible to build MV converters with low cost and high reliability. Besides the commercialized topologies, such as three-level neutral-point clamped (3L-NPC), five-level active neutral-point clamped, cascaded H-bridge (CHB), and modular multilevel converters, new topologies are being developed continuously to satisfy various requirements of industrial applications. Among the newly developed topologies, hybrid-clamped (HC) converters, i.e., 4L-HC [4] and 5L-HC [5], are attractive due to their relatively low number of switches and strong capacitor balancing capabilities.

Recently, a novel seven-level HC (7L-HC) converter was presented in [6]. Compared with the 5L-HC converter, only two switches are added in each phase to increase the output voltage level from five to seven while still keeping the overall advantages of the 4L-HC and 5L-HC, which makes it suitable in building a high power density, low-cost MV drive. The circuit topology of a three-phase 7L-HC converter is shown in Fig. 1. Compared with the existing seven-level topologies [7]–[10], this structure has the smallest device number and is free from the problem of series connection of switches. Besides, this 7L-HC does not need any isolated dc sources required by the CHB [11]. It uses only two switches and two flying capacitors (FC) for clamping in each phase and has 22 redundant switching states, giving more control freedom to the 7L-HC.

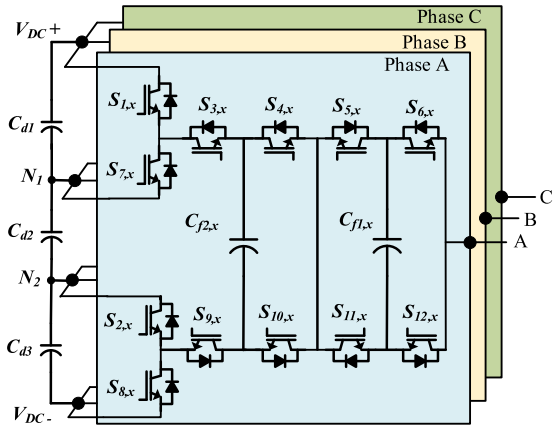

Fig. 1. Circuit topology of the three-phase 7L-HC inverter.

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For a given switching frequency, selective harmonic elimination pulsewidth modulation (SHE-PWM) offers the potential for improved waveform quality compared with the existing modulation techniques [12], [13]. This potential becomes advantageous for applications where low switching frequency is required, such as high-power MV applications. In order to fully exploit the advantages of SHE-PWM, it is not sufficient to apply one switching pattern over the whole modulation index range. Instead, all valid switching patterns that contain solutions, including some uncommonly used ones, should be evaluated and analyzed, since sometimes these uncommon switching patterns might have better performance over specific modulation index range. This approach is called unified SHE formulation, which has been extensively studied in [14]–[18]. This article further implements this unified SHE formulation to 7L-HC by selecting the optimal seven-level SHE switching pattern with the designed optimization goal for each modulation index, in order to achieve the best overall performance of the 7L-HC under SHE-PWM.

One of the most critical issues of the SHE-PWM operated 7L-HC is that all capacitor voltages have to be controlled to their reference values to ensure high-quality output waveforms and device safety. For clamped multilevel converters under SHE-PWM, the commonly used voltage balancing methods include angle modifications [19], [20], space voltage vector adjustments [21], [22], and redundant switching states [23], [24]. However, for 7L-HC that has three dc-link capacitors and two FC per phase, only the redundant switching states among them can be used to control the capacitor voltages. That method has already been presented in [25] for voltage balancing issue under level-shifted PWM (LS-PWM). As shown in [25], the logic of selecting proper redundant states for 7L-HC is very complex and might somehow limit its industrial practicality.

To ensure capacitor voltage balancing, model predictive control (MPC) can be adopted [26]. Due to its advantages of multiobjective control and fast dynamic response, the voltage balancing issues for clamped multilevel converters can be well addressed by MPC. In [27]–[31], the MPC has been investigated extensively for the voltage balancing control of the dc-link and/or FC of various clamped multilevel topologies, including 3L-NPC [27], 4L-NPC [28], four-level nested NPC (4L-NNPC) [29], 4L-HC [30], and 5L-NNPC converters [31]. Based on similar methods, the balancing problem of 7L-HC can also be addressed by MPC.

Despite the advantages that MPC offers in principles, some problems still exist, e.g., the spread voltage and current spectrum caused by the finite control set MPC (FCS-MPC) [30]. To solve this problem, a novel MPC strategy that combines FCS-MPC and SHE-PWM in its formulation is developed recently to control multilevel converters [32]–[34], which is able to track the converter output current reference in transits while preserving the SHE voltage pattern in steady state, keeping both advantages of FCS-MPC and SHE-PWM. However, for 7L-HC that has 22 redundant switching states per phase, the number of three-phase redundant states (voltage vectors) becomes 10 648 (22^3), which makes it extremely challenging to directly apply this type of SHE-MPC to 7L-HC.

Another major challenge faced by most MPC applications is the selection of weighting factors [26]. Since the weighting factors allocate the importance of each control objective, they have significant effects on the response of the whole system. However, the weighting factors are usually determined empirically. In [35], some guidelines for weighting factor adjustment that are based on algorithmic empirics are presented. However, if large dynamics occur, the predefined weighting factors might not perform well and somehow reduce the overall advantages of MPC. In order to solve this problem, the optimal weighting factors for various situations are stored in a look-up table [28]. Recently, some real-time/online weighting factor adjustment methods have been introduced in [36]–[38]. Although they avoid the need for additional look-up tables, the computational burden of MPC increases significantly, limiting their practicality in real industrial applications.

In this article, a composite strategy that combines SHE-PWM and MPC is proposed for 7L-HC, which uses the SHE-PWM in the modulation part for generating the real-time output voltage level and implements MPC for capacitor voltage balancing and switching frequency control. The unified SHE-PWM is adopted in the SHE-PWM formulation that is able to select the optimal switching pattern for each modulation index with the designed optimization goal, achieving the best system performance with SHE-PWM. After receiving the output voltage level signal from the SHE-PWM module, the prediction of dc-link capacitor voltages, FC voltages, and switching frequency increase, as well as the cost function minimization, are made on MPC part by only involving the redundant switching states of the selected output voltage level per phase. In this way, the proposed control method reduces the calculation time dramatically, i.e., the number of maximum prediction times are reduced from 10 648 to 18 in one control period without limiting the advantages of multiobjective control and fast response with MPC. Dynamic weighting factor with variable band limits is also discussed in details, which is able to avoid the high computational burden of online weighting factor calculation while still keeping the advantage of good dynamic performance. Simulation and experimental results for both steady-state and dynamic situations are obtained to validate the feasibility of this composite SHE-MPC strategy.

II. Operation Principle and Mathematical Model of the 7L-HC Inverter

In Fig. 1, the complementary switch pairs of the 7L-HC converters are as follows: $(S_{1,x}-S_{7,x})$, $(S_{2,x}-S_{8,x})$, $(S_{3,x}-S_{9,x})$, $(S_{4,x}-S_{10,x})$, $(S_{5,x}-S_{11,x})$, and $(S_{6,x}-S_{12,x})$, where switches $S_{1,x}$ and $S_{2,x}$ require the same switching signals, and *x* refers to the phase (a, b, or c). The 22 switching states are listed in Table I, where i_{ox} denotes the output current. If the dc-link voltage $V_{\rm dc}$ is 3*E*, the voltage of each dc-link capacitor and the FC C_{f2} should be maintained at *E*, whereas the voltage of the FC C_{f1} should be regulated at *E*/2.

For FC $C_{f1,x}$, the current flows out of it when $S_{6,x}$ and $S_{11,x}$ are switched ON and into it when $S_{5,x}$ and $S_{12,x}$ are ON. Thus, the FC current $i_{f1,x}$ can be written as

$$i_{f1,x} = (S_{5,x} - S_{6,x})i_{ox}. \tag{1}$$

TABLE I
SWITCHING STATES OF THE 7L-HC INVERTER

$S_{1,x}$ - $S_{6,x}$	u_{ox}	i_{N1}	i_{N2}	i_{cf1}	i_{cf2}	State No.
000000	0	0	0	0	0	$\mathbf{V_0}$
001010	E	i_o	0	i_o	i_o	$\mathbf{V_1}$
000110	E	0	0	i_o	$-i_o$	$\mathbf{V_2}$
110010	E	0	i_o	i_o	0	$\mathbf{V_3}$
000001	E	0	0	$-i_o$	0	$\mathbf{V_4}$
110000	$2E$	0	i_o	0	0	$\mathbf{V_5}$
001000	$2E$	i_o	0	0	i_o	$\mathbf{V_6}$
000111	$2E$	0	0	0	$-i_o$	$\mathbf{V_7}$
111010	$3E$	0	0	i_o	i_o	$\mathbf{V_8}$
110110	$3E$	0	i_o	i_o	$-i_o$	$\mathbf{V_9}$
001110	$3E$	i_o	0	i_o	0	$\mathbf{V_{10}}$
110001	$3E$	0	i_o	$-i_o$	0	$\mathbf{V_{11}}$
000101	$3E$	0	0	$-i_o$	$-i_o$	$\mathbf{V_{12}}$
001001	$3E$	i_o	0	$-i_o$	i_o	$\mathbf{V_{13}}$
001111	$4E$	i_o	0	0	0	$\mathbf{V_{14}}$
110111	$4E$	0	i_o	0	$-i_o$	$\mathbf{V_{15}}$
111000	$4E$	0	0	0	i_o	$\mathbf{V_{16}}$
111001	$5E$	0	0	$-i_o$	i_o	$\mathbf{V_{17}}$
110101	$5E$	0	i_o	$-i_o$	$-i_o$	$\mathbf{V_{18}}$
111110	$5E$	0	0	i_o	0	$\mathbf{V_{19}}$
001101	$5E$	i_o	0	$-i_o$	0	$\mathbf{V_{20}}$
111111	$6E$	0	0	0	0	$\mathbf{V_{21}}$

Similarly, the FC current $i_{f2,x}$ can be written as

$$i_{f2,x} = (S_{3,x} - S_{4,x})i_{ox}. \tag{2}$$

For the neutral points (N_1, N_2), the current flows out of N_1 when $S_{1,x}$ and $S_{3,x}$ are switched ON and out of N_2 when $S_{2,x}$ and $S_{9,x}$ are switched ON. Therefore, the neutral-point currents ($i_{N1,x}$, $i_{N2,x}$) can be written as

$$\begin{cases} i_{\mathrm{N1},x} = S_{3,x}(1 - S_{2,x})i_{ox} \\ i_{\mathrm{N2},x} = S_{2,x}(1 - S_{3,x})i_{ox}. \end{cases} \tag{3}$$

Then, the middle capacitor current is given as

$$i_{m,x} = i_{\mathrm{N2,x}} - i_{\mathrm{N1,x}} = (S_{2,x} - S_{3,x})i_{ox}. \tag{4}$$

Combing (3) and (4), the upper and lower dc-link capacitor currents, i.e., $i_{u,x}$ and $i_{l,x}$, can be obtained as

$$\begin{cases} i_{\mathrm{u,x}} = i_{m,x} + i_{\mathrm{N1,x}} = S_{2,x}(1 - S_{3,x})i_{ox} \\ i_{\mathrm{l,x}} = i_{m,x} - i_{\mathrm{N2,x}} = -S_{3,x}(1 - S_{2,x})i_{ox}. \end{cases} \tag{5}$$

According to the capacitor currents i_{cap} shown in (1)–(5), the general form of the predictive voltages of dc-link capacitor and FC V_{cap} at the (k+1)th instant can be expressed as

$$V_{\mathrm{cap}}(k+1) = V_{\mathrm{cap}}(k) + \frac{T_s \cdot i_{\mathrm{cap}}}{C_{\mathrm{cap}}}. \tag{6}$$

III. SEVEN-LEVEL UNIFIED SHE-PWM AND OPTIMAL SWITCHING PATTERN SELECTIONS

The SHE-PWM waveform is usually defined quarter-wave symmetric. The equations used to compute the amplitude of harmonics are listed as (7), with the constraints of (8)

$$b_n = \frac{4E}{n\pi}\left[\pm\sum_{i=1}^{N}\cos(n\alpha_i)\right] \tag{7}$$

$$0 < \alpha_1 < \alpha_2 < \ldots.. < \alpha_N < \frac{\pi}{2} \tag{8}$$

where b_n is the amplitude of the nth harmonics, and N is the number of switching angles α_i. The "$\pm$" sign in front of $\cos(n\alpha_i)$ in (7) depends on the transition states, i.e., rising or falling edges, of switching angles α_i.

A. Seven-Level Switching Patterns and Unified SHE Equations for 7L-HC With Seven Switching Angles

Among the various 7-level SHE-PWM switching patterns with seven switching angles, only 13 of them contain valid solutions for certain modulation index (m_a) range, which share the same SHE equations as (9).

According to unified SHE-PWM, the intervals where the solutions of (9) locate in depend on their transition states, i.e., the rising edge for the angles in (0, π/2) and the falling edge for those in (π/2, π). For those located in (π/2, π), the actual switching angles could be obtained by calculating their supplementary angles, but not considered as invalid solutions as usual. As a result, solving (9) is enough for obtaining all switching patterns and the corresponding switching angles. Based on the solving algorithm and switching pattern searching process discussed in [14] and [16], the half-period waveforms of these 13 valid switching patterns are shown in Fig. 2

$$\begin{cases} f_1(\alpha) = \sum_{i=1}^{7}\cos\alpha_i = \frac{\pi V_1}{4E} \\ f_2(\alpha) = \sum_{i=1}^{7}\cos(5\alpha_i) = 0 \\ \qquad\qquad \ldots \\ f_7(\alpha) = \sum_{i=1}^{7}\cos(19\alpha_i) = 0. \end{cases} \tag{9}$$

B. Optimal Switching Pattern Selections

Different switching patterns usually lead to different system performances, such as total harmonic distortion (THD), harmonic distortion factor (HDF), and harmonic loss factor, which can be utilized to compare and select the optimal switching pattern with the lowest optimization goal. In this article, high-power motor drive application is used as an example in designing the optimization objective. Due to the inductive nature of the motor, better filtering ability will be achieved for high-order harmonics, and thus it is important to suppress the low-order noneliminated harmonics as much as possible while maintaining a good overall performance of the output waveforms. As a result, both the THD and HDF are considered in the optimization goal for high-power motor drive applications, as shown in (10), with equal weighting factors k_1 and k_2 that are set to 0.5, respectively.

The minimum value of the designed optimization goal associated with the optimal switching pattern over the whole modulation index range is depicted in Fig. 3, from which it can be observed that the value of the optimization goal with THD and HDF reduces progressively, except for particular slight

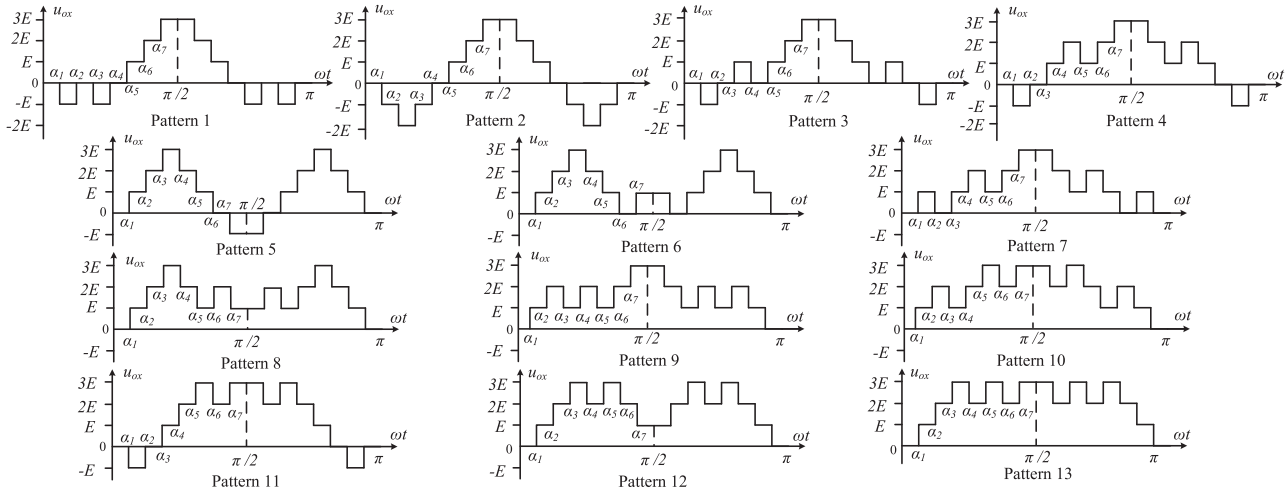

Fig. 2. Thirteen seven-level SHE switching patterns with seven switching angles.

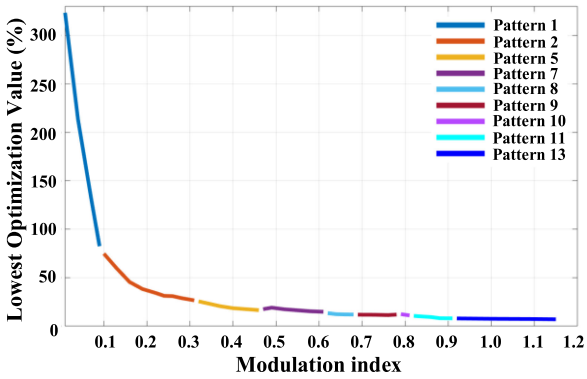

Fig. 3. Optimal pulse patterns with the lowest optimization value.

increments, when m_a is increased

$$\text{obj.} \quad \min \quad (k_1\text{THD} + k_2\text{HDF}) \tag{10}$$

In industrial applications, the components and weighting factors in the optimization goal (10) should be flexibly adjusted according to the specific type and aim of the application [14]. For example, with the same goal as (10), the k_2 with HDF should be set larger, i.e., 0.7, for better suppressions of the 23th and 25th harmonics in some grid-connected converter systems with *LCL* filters, to reduce the inductor size and avoid resonance with the *LCL* filter.

IV. Voltage Balancing Method With MPC

This section describes how the composite SHE-MPC is implemented for balancing capacitor voltages while regulating the switching frequency, after receiving the output voltage level signal from the optimal unified SHE-PWM module.

A. Cost Function Formulation

In order to balance the capacitor voltages while regulating the switching frequency of the 7L-HC, the cost function of the MPC part can be constructed as

$$\begin{aligned} g(k) = {} & \lambda_{cf1,x}|V^*_{cf1,x}(k+1) - V_{cf1,x}(k+1)|^2 \\ & + \lambda_{cf2,x}|V^*_{cf2,x}(k+1) - V_{cf2,x}(k+1)|^2 \\ & + \lambda_{u,x}|V^*_{u,x}(k+1) - V_{u,x}(k+1)|^2 \\ & + \lambda_{m,x}|V^*_{m,x}(k+1) - V_{m,x}(k+1)|^2 \\ & + \lambda_{l,x}|V^*_{l,x}(k+1) - V_{l,x}(k+1)|^2 + \lambda_{sf}N_{sf} \end{aligned} \tag{11}$$

where λ_{cf1}, λ_{cf2}, λ_u, λ_m, λ_l, and λ_{sf} are the weighting factors of the FC balancing of C_{f1} and C_{f2}, three dc-link capacitor balancing, and switching frequency regulation, respectively. A large value of certain λ implies greater priority to that objective. N_{sf} denotes the number of switch commutations to get to the next switching state.

The FC and dc-link capacitor voltage references $V^*_{cf1}(k+1)$, $V^*_{cf2}(k+1)$, and $V^*_{u,m,l}(k+1)$ are given as

$$\begin{cases} V^*_{cf1,x}(k+1) = \frac{V_{\text{dc}}}{6} \\ V^*_{cf2,x}(k+1) = V^*_{u,x}(k+1) = V^*_{m,x}(k+1) \\ \qquad\qquad = V^*_{l,x}(k+1) = \frac{V_{\text{dc}}}{3}. \end{cases} \tag{12}$$

The expression of N_{sf} is given as

$$N_{sf} = \sum_{i=1}^{6} |S_i - S_i^*| \tag{13}$$

where S_i represents the predicted gating signals of the switches $S_{1,x}$–$S_{6,x}$, and S_i^* denotes the optimal gating signals of switches $S_{1,x}$–$S_{6,x}$ in the previous sampling period. When λ_{sf} is greater than zero, switching frequency reduction can be achieved.

B. Dynamic Weighting Factor Adjustment

As shown in (11), the cost function of this composite SHE-MPC regulates both the capacitor voltages and switching frequency, which are variables of differing natures and do not contribute equally to the cost function value. Therefore, the job

of the weighting factors λ_{fc1}, λ_{fc2}, λ_u, λ_m, λ_l, and λ_{sf} in (11) is to compensate the differences in nature of the variables.

Instead of using static weighting factors that reduce the system dynamic performance to some extent, the dynamic weighting factor adjustment is proposed in this section. The weighting factor selection for high-power motor drive application with different fundamental frequencies is used as an example to better illustrate this proposed method. The specific steps are as follows.

The first step is to determine the importance of these variables and their initial values. For high-power motor drive applications, although the capacitor voltage balancing is vital to the overall system performance and output waveform quality, the switching frequency regulation is also very important, and the feature of low switching losses is indispensable for high-power SHE-PWM. Thus, the switching frequency regulation should be judged as critical as voltage balancing for capacitors, which is different than the previous studies, such as [28] and [29]. As a result, the initial values of all weighting factors are chosen as 1, which will be adjusted later.

The second step is to determine the rule of dynamically adjusting the weighting factors. In most cases, the capacitor voltages only need to be in the vicinity of their reference voltages, and a perfect tracking of them normally is not necessary and undesirable [39]. Therefore, certain deviation, called the normal band limit V_{band}, should be set for capacitor balancing to prevent excessive switching transitions, which is based on the idea similar to ones presented in [23]–[25]. However, in this article, a safe limit V_{safe} is further added, which denotes the maximum allowed voltage deviation to avoid overvoltage or damage to the hardware system.

For high-power motor drive system operated with normal fundamental frequency (i.e., 50 Hz), V_{safe} is usually set to 5% of the capacitor reference voltage E for maintaining both features of low switching frequency and desirable output waveform quality. However, in very low fundamental frequencies (i.e., 1 Hz), where larger dc-link capacitor ripples often appear due to the nature of NPC/HC topologies [40], [41], V_{safe} should be enlarged to $10\%E$ to avoid frequent switching transitions for capacitor balancing issue, and thus the feature of low switching frequency can still be maintained. As for V_{band}, instead of using a constant value as most studies did, a variable V_{band} that is related to the output current is proposed. Since low output current is often not advantageous for capacitor balancing, a tight V_{band} is required to better control the voltage ripples. The expression of the V_{band} based on its base value $V_{\text{band},b}$ is given in (14), where $V_{\text{band},b}$ is set to 60% of V_{safe} to ensure a high control flexibility between capacitor balancing effects and switching frequency regulations

$$V_{\text{band}} = V_{\text{band},b} \times \left(\frac{i_{ox}}{i_{o,\text{rated}}} \right). \tag{14}$$

Based on the aforementioned discussions, the following dynamic weighting factor adjustment rule for capacitors is proposed

$$\lambda_x = \begin{cases} 0 & 0 \le |V_x - V_x^*| < V_{\text{band}} \\ 1 + 10 \left| \frac{V_x - V_x^*}{V_x^*} \right| & V_{\text{band}} \le |V_x - V_x^*| < V_{\text{safe}} \\ 10\,000 & |V_x - V_x^*| \ge V_{\text{safe}}. \end{cases} \tag{15}$$

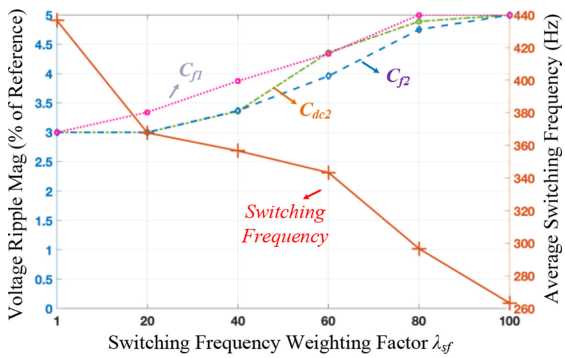

Fig. 4. Relationship between the capacitor ripple and switching frequency.

This dynamic weighting factor adjustment rule ensures that all capacitor voltages will never cross the safe limit, and thus the problem of intermittent large ripple voltage occurrences in both steady-state and dynamics situations is addressed. Besides, the voltage fluctuations are controllable and can be adjusted flexibly with different band limits according to various application requirements. Moreover, the selection of the weighting factors for capacitor voltage regulation cost terms become considerably less critical, and the high requirement for weighting factor selections in normal FCS-MPC can be released correspondingly.

The last step lies in the selection of λ_{sf} to search for the minimum switching frequency with the expected capacitor voltage balancing effects. The branch and bound algorithm is used to simply the searching process [33]. The starting point is $\lambda_{sf} = 1$, as discussed in step 1. Part of the searching process is shown in Fig. 4, where the $V_{\text{band},b}$ and V_{safe} are set to 3% and 5% of the reference voltages, respectively, considering the high-power motor drive with normal fundamental frequency. As shown in Fig. 4, the tradeoff between the capacitor ripple increase and switching frequency drop is very clear, i.e., larger capacitor voltage ripples with lower switching frequency and vice versa. For most cases, the capacitor voltages can be regulated between $V_{\text{band},b}$ and V_{safe}, but when λ_{sf} approaches 100, all capacitors keep the constant voltage deviations equal to V_{safe}. Considering the high-power situation assumed, λ_{sf} is supposed to be selected between 20 and 60 to keep the switching frequency low while controlling capacitor voltages within the V_{safe}. In Fig. 5, relationships of switching frequencies of $S_{3,x}$ and $S_{5,x}$ with different values of $V_{\text{band},b}$ and m_a are presented, where the switching frequency has a negative relationship with $V_{\text{band},b}$. However, the relationship of m_a and switching frequency is not that clear, i.e., sometimes a lower m_a induces higher switching frequency, such as the case with $m_a = 0.7$, $m_a = 0.5$, and $V_{\text{band},b} = 5\%E$. In conclusion, the selection of the λ_{sf}, $V_{\text{band},b}$, and V_{safe} should be treated carefully and is related to system parameters and aimed industrial applications.

C. Proposed Composite SHE-MPC

The overall control diagram of the proposed composite SHE-MPC is shown in Fig. 6, which can be generally divided into two parts: SHE-PWM part, and MPC part. For the SHE-PWM part, with the input m_a signal, the optimal switching pattern

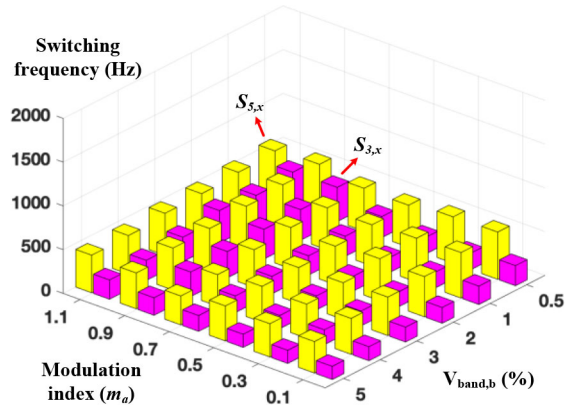

Fig. 5. Relationship of the switching frequencies of $S_{3,x}$ and $S_{5,x}$ with different values of $V_{\mathrm{band},b}$ and modulation index.

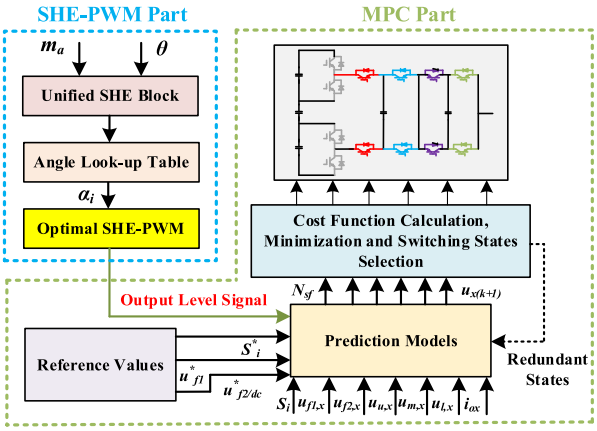

Fig. 6. Overall control diagram of the proposed composite SHE-MPC.

is selected according to the unified SHE approach presented in Section III. The selection rule in this article is based on Fig. 3, with the optimization goal as (10). Based on the selected pattern with the unified SHE block, the angle look-up table is updated accordingly. Then, based on the switching angles and the input phase angle θ of the SHE pattern, which will repeatedly increase from 0 to 2π at system fundamental frequency, the optimal SHE-PWM output level signal is obtained and delivered to the MPC part. Since this output signal is the link between these two parts, the linking line is marked in red in Fig. 6 for better presentation effects.

For the MPC part, after receiving the sensor signals, the reference values, and the output level signal from the SHE-PWM part, the predictive model and the cost function are calculated for each redundant switching state of the output level. For example, if the output level received is 5*E*, the MPC algorithm needs to run only four times with the states V_{17} –V_{20} according to Table II. Finally, the state that minimizes the cost function is selected and implemented to the corresponding phase of 7L-HC.

Different from traditional FCS-MPC, this composite SHE-MPC is performed for each phase, which means the optimal switching states are independently selected for each phase by minimizing phase-dependent cost functions. As a result, the maximum prediction cases for 7L-HC are reduced from 10 648 to 18 in one control period. In this case, the method achieves the advantages of multiobjective control and fast dynamic response of MPC while preserving the low switching frequencies and good harmonic performances of SHE-PWM.

TABLE II
PARAMETERS OF THE 7L-HC SIMULATION AND EXPERIMENT MODELS

Parameters	Simulation		Experiment	
	SI	p.u.	SI	p.u.
Rated power (VA)	500	1.0	500	1.0
Rated AC voltage (V)	104	1.0	104	1.0
DC-link voltage (V)	150	/	150	/
DC-link capacitor (μF)	2700	0.06	2700	0.06
Flying capacitor (μF)	1000	0.15	1000	0.15
Load resistance (Ω)	40	1.85	40	1.85
Load inductance (mH)	30	0.45	30	0.45
Sampling frequency (kHz)	10	200	10	200
Base frequency (Hz)	50	1.0	50	1.0
Switch type (IGBT)	/		NGTB20N120	

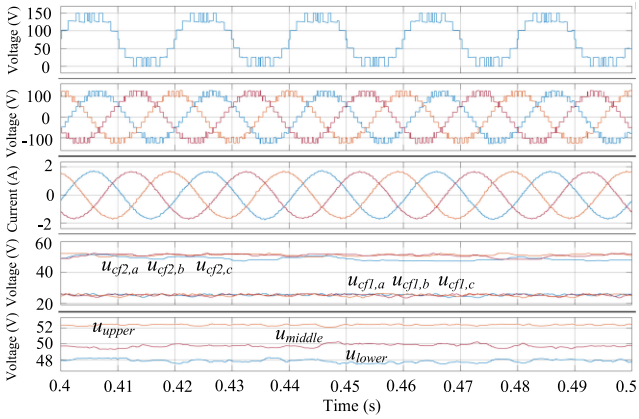

Fig. 7. Simulation results of case 1—steady states with $m_a = 1.0$.

V. SIMULATION AND EXPERIMENTAL RESULTS

To verify the validity of the proposed composite SHE-MPC, a range of simulations and experiments have been carried out by MATLAB/Simulink and a low-power 7L-HC platform. The circuit parameters used for simulation and experiment are summarized in Table II.

A. Simulation Results

In order to show the effectiveness of the proposed composite SHE-MPC, three cases are shown in both steady-state and dynamic situations. The rated values of three dc-link capacitors and FC C_{f2} are 50 V, whereas for FC C_{f1}, it is 25 V. The normal band limit for capacitors is 3% of the reference voltage, whereas the safe band limit is 5%.

Case 1: The steady-state simulation results with $m_a = 1.0$ are shown in Fig. 7, and the fast Fourier transform (FFT) analysis results of phase voltage, line voltage, and output current are shown in Fig. 8. In Figs. 7 and 8, the harmonic elimination effect of the SHE-PWM is demonstrated, and the tight control

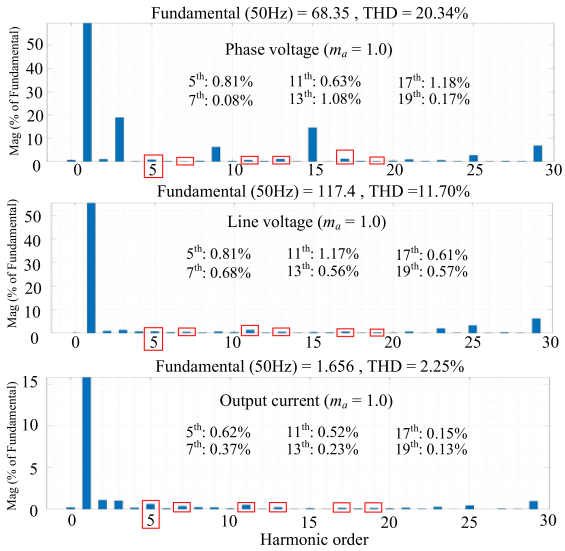

Fig. 8. FFT analysis results of phase voltage, line voltage, and output current.

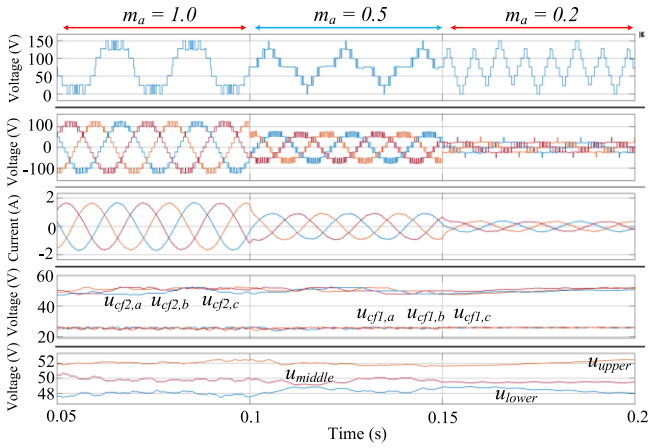

Fig. 9. Simulation results of case 2—Dynamic situation with changing the modulation index.

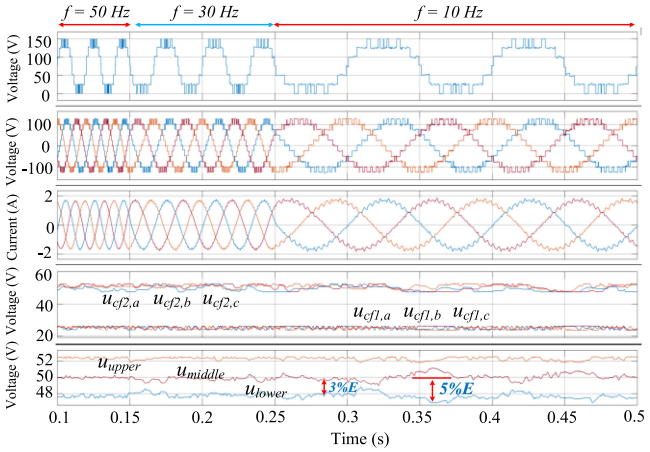

Fig. 10. Simulation results of case 3—Dynamic situation with changing the fundamental frequency.

of capacitors within the expected band limits is also presented to show the balancing effects of the MPC part.

As shown in Fig. 7, the FC and middle dc-link capacitor are well balanced around their reference values, with maximum voltage deviation of about 3% of the reference voltage, which is the defined normal band limit. However, the upper and lower dc-link capacitors are balanced and maintained with constant deviations, due to the dynamic weighting factor adopted in reducing the switching frequency, as well as the nature of the NPC/HC topologies [40], [41]. Besides, it can be observed that the upper and lower dc-link capacitors are balanced within the safe band limit instead of the normal band limit, since a large λ_{sf} is adopted here, which regulates the average switching frequency as low. If a tighter dc-link capacitor voltage is required, either the λ_{sf} or the band limit can be reduced accordingly in order to achieve such effect.

From the FFT analysis result, neither the low-order harmonic amplitudes nor THDs are affected by such band selections, which verifies the effectiveness of this method in capacitors voltage balancing while keeping a very low switching frequency and good system performances.

Case 2: In this situation, the dynamic simulation result is shown in Fig. 9, with m_a changing from 1.0 to 0.5 to 0.2. It can be observed that all capacitors are balanced perfectly around the expected band limits and do not shift over the safe limit in this dynamic situation. Besides, it should be noted that based on the optimal switching patterns presented in Fig. 3, the phase voltage waveform that represents the optimal switching pattern changes between those three m_a.

Case 3: In this case, the dynamic simulation result with the fundamental frequency changed from 50 Hz to 30 Hz to 10 Hz is carried out in Fig. 10. It can be observed that all capacitors are balanced perfectly around the expected band limits and do not exceed the safe limit regardless of the shifted frequency.

As shown in Fig. 10, a slightly larger voltage ripple occurs for dc-link capacitors in low fundamental frequencies, which is also caused by the innate characteristic of the NPC/HC topologies [40], [41], i.e., a longer constant charging or discharging time duration appears to the upper and lower dc-link capacitors due to the lower fundamental frequency. However, the maximum voltage deviation could still be well controlled as expected by the proposed dynamic weighting factors, which demonstrates the effectiveness of this method in low fundamental frequencies.

B. Experimental Results

In order to further demonstrate the effectiveness of the proposed composite SHE-MPC, four experimental cases are presented in both steady-state and dynamic situations. The rated value of three dc-link capacitors and FC C_{f2} is 50 V, whereas for FC C_{f1}, it is 25 V, which are the same as the simulations.

Case 1: For steady-state conditions, the phase voltage with the optimal switching pattern, output current, two FC voltages of phase A, and the upper and lower dc-link capacitor voltages are obtained for modulation index 1.0 and 0.2, as shown in Figs. 11 and 12, respectively. The corresponding FFT analysis results of the phase voltage and output current with $m_a = 1.0$, as well

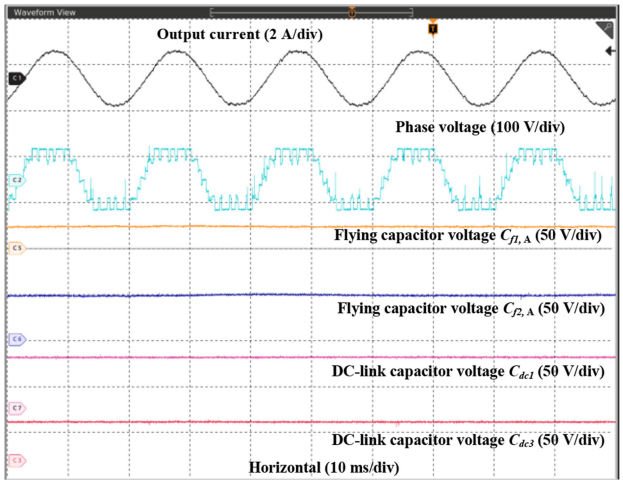

Fig. 11. Steady-state experimental results of $m_a = 1.0$.

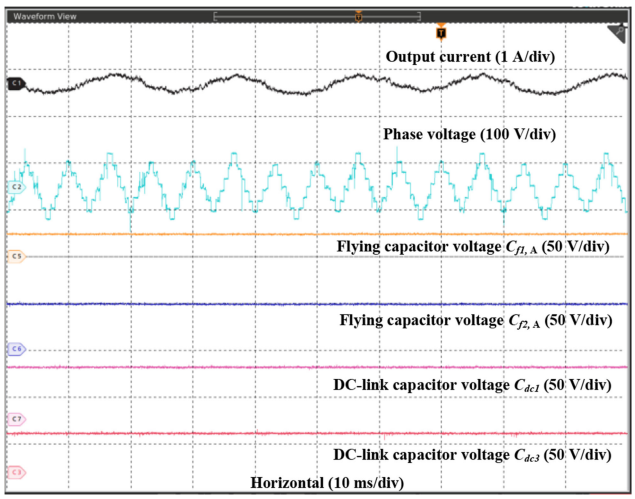

Fig. 12. Steady-state experimental results of $m_a = 0.2$.

as the one of output currents with $m_a = 0.2$, are presented in Fig. 13.

As shown in Figs. 11 and 12, all capacitors are well-balanced with the expected band limits, which correspond well with the simulation case 1. In Fig. 13, it can be observed that the amplitude of all selected harmonics is suppressed lower than 3%, with most of them under 1%, which demonstrates the effectiveness of the unified SHE approach introduced. From Fig. 13, the THD value of the output current with $m_a = 0.2$ is a bit higher, i.e., 8.08%, and such small distortion is due to the low modulation index adopted. However, the capacitor balancing ability and low-order harmonic elimination abilities are not affected, which shows the effectiveness of the proposed method in low-modulation-index situations.

It should be noted that a commonly adopted alternative in low modulation indexes (i.e., $m_a < 0.5$) would be using three-level or five-level switching pattern [13], as the traditional SPWM does. However, the results of this article demonstrate that such operation is also possible under the unified seven-level SHE approach with optimal switching patterns.

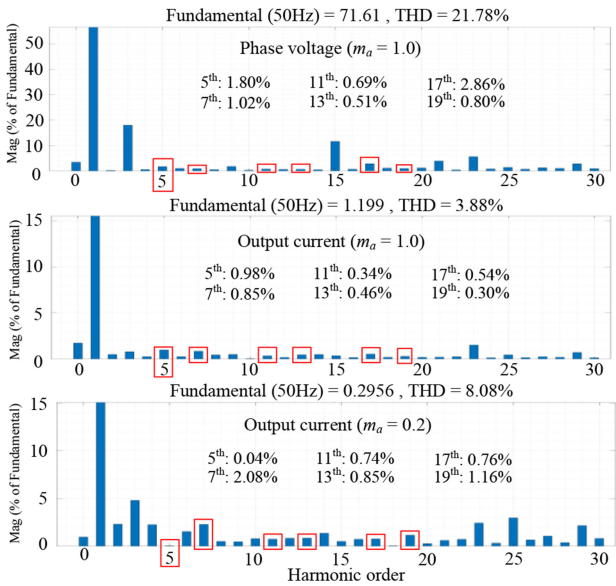

Fig. 13. FFT analysis results of steady-state experimental results.

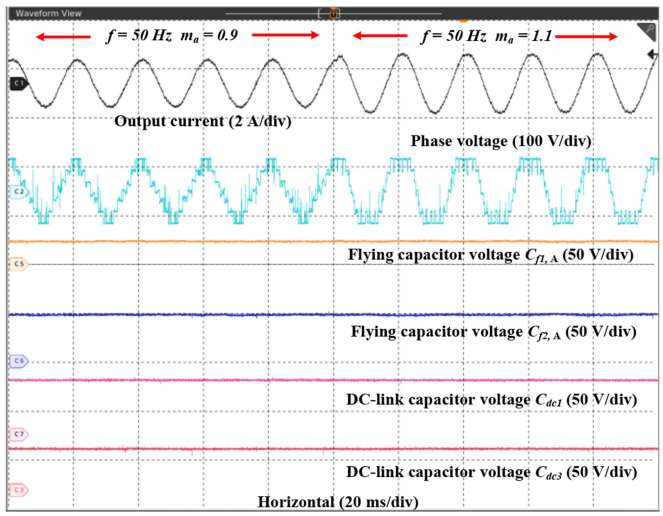

Fig. 14. Dynamic experimental results of changing m_a from 0.9 to 1.1.

Case 2: For dynamic situations, the same sets of signals are measured for m_a changing from 0.9 to 1.1 and from 0.3 to 0.9, as shown in Figs. 14 and 15, respectively. It should be noted that the fundamental frequency in Fig. 14 is set to 50 Hz, whereas in Fig. 15, it is set to 25 Hz, in order to be consistent with actual situations in industrial applications. From Figs. 14 and 15, the capacitor voltage balancing effects are not influenced by the changing modulation index, which demonstrate the effectiveness of this method in dynamic modulation index situations and corresponds well with simulation case 2.

As shown in Fig. 15, some distortions happen on the phase voltages. The main reasons behind such distortions lie on the processing speed of the DSP that could not guarantee precise switching actions on the precalculated switching angles, and sometimes even result in wrong actions when two switching angles are close to each other. Another reason of such distortions is the lower fundamental frequency adopted (25 Hz), which

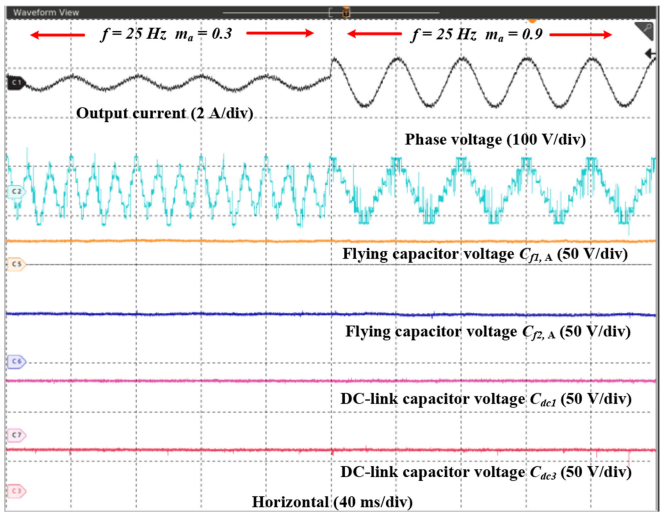

Fig. 15. Dynamic experimental results of changing m_a from 0.3 to 0.9.

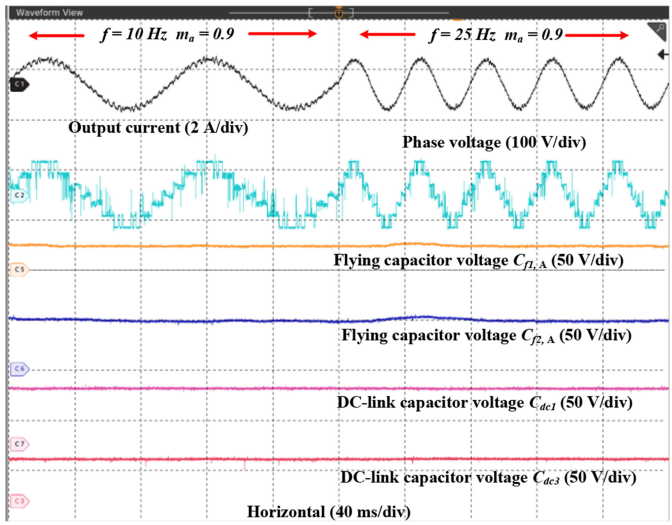

Fig. 17. Dynamic experimental results of changing f from 10 to 25 Hz.

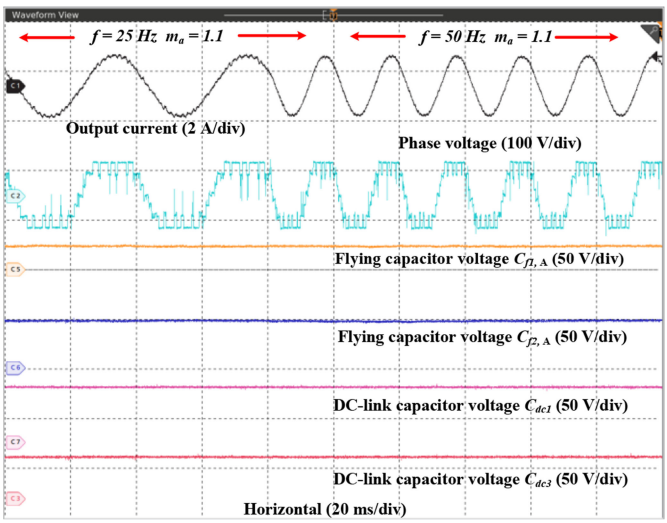

Fig. 16. Dynamic experimental results of changing f from 25 to 50 Hz.

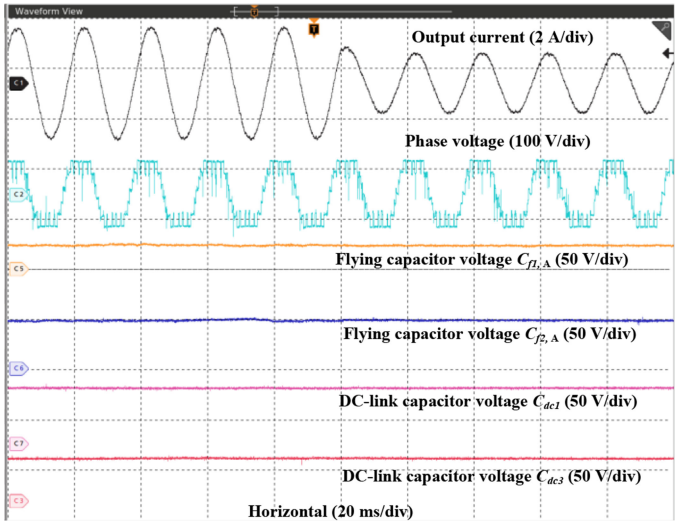

Fig. 18. Dynamic experimental results of changing R from 20 to 40 Ω.

affects the output quality to some extent, as discussed previously in simulation case 3 and experiment case 1.

Case 3: In Figs. 16 and 17, the dynamic experimental results of changing the fundamental frequency from 25 to 50 Hz and from 10 to 25 Hz are presented, respectively. Similarly, the modulation index in Fig. 16 is set to 1.1, whereas the modulation index in Fig. 17 is set to 0.9. From Figs. 16 and 17, we can observe that both the output waveform qualities and the capacitor voltage balancing effects are not influenced by changing the fundamental frequency, which demonstrate the effectiveness of this method in variable and low-frequency region and align well with simulation case 3.

Case 4: In Fig. 18, the dynamic experimental result of changing load resistance from 20 to 40 Ω, with $m_a = 1.1$ and fundamental frequency equals 50 Hz, is presented. Neither the voltage balancing effect nor waveform quality is affected, which shows the capacitor balancing ability of this method in transit.

VI. Conclusion

This article proposes a composite SHE-MPC strategy that keeps the overall advantages of SHE-PWM with optimal switching patterns and can also balance the capacitor voltages effectively with MPC. Simulation results and experimental testing are presented to validate the effectiveness of the proposed method. The major advantages of the proposed composite SHE-MPC are summarized as follows.

1) *Low switching frequency with good harmonic performance*. Compared with other PWM methods, the unified approach introduced in this article can select the optimal seven-level switching patterns in whole modulation index range, which has good performance under very low switching frequency.
2) *Reduced computational burden*. Compared with the traditional FCS-MPC or SHE-MPC, the computation burden of this composite SHE-MPC has been reduced significantly without the need to consider the huge

number of redundant three-phase voltage vectors, but by simply selecting the single-phase redundant states based on the received SHE-PWM voltage level signals.

3) *High flexibility and good voltage balancing ability*. Compared with most studies on MPC, which use static or online calculations of weighting factors, the dynamic weighting factors presented in this article not only have the ability of fast dynamic response, but also avoid the need to constantly calculate the weighting factors or add extra storage resources based on various situations. With the dynamic weighting factors, the composite SHE-MPC has strong voltage balancing ability in both steady-state and dynamic situations, which have been demonstrated in Section V.
4) *Good expandability*. This composite SHE-MPC can not only be implemented in three-phase multilevel converters, as shown in this article, but can also be used for single-phase situations. Besides, the MPC part with dynamic weighting factors in this article can be implemented not only with the presented optimal SHE-PWM, but can also be adjusted and combined with other PWMs, i.e., phase-shifted PWM or LS-PWM, to cope with different applications for the best system performance. Moreover, more control objective other than switching frequency regulation can be incorporated into the cost function, such as common-mode voltage reduction, while balancing the capacitor voltages at the same time.

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