Novel High-Efficiency Frequency-Variable Buck–Boost AC–AC Converter With Safe-Commutation and Continuous Current

Liangzong He, *Member, IEEE*, and Xinyong Xu

***Abstract*—In this article, a novel high-efficiency single-phase frequency-variable buck–boost ac–ac converter is proposed. AC input voltage can be bucked and boosted with step-changed frequency operation. In the topology, only six switches and total ten semiconductors are utilized, which is at the lowest level among existing works. Only two of the switches are operating at high frequency and only one switch is switched ON and OFF in each switching period, Therefore, the proposed converter has less power loss and features high efficiency. With simple and flexible control strategy, the converter is immune of commutation problem and thus no additional safe-commutation strategy or snubber circuit is needed. Power density of proposed converter is high considering the volume metric of the energy storage components. Moreover, the input current of proposed ac–ac converter is continuous. Therefore bulky input filter required by other existing works is totally removed, which further improve the power density. Operation principles and circuit analysis is provided. To verify the performance, a 200-W laboratory prototype is constructed and experiments are conducted in operation of buck and boost mode at step-changed output frequency of 30, 60, and 120 Hz.**

***Index Terms*—AC–AC conversion, buck–boost mode, high power density, step-changed frequency, safe-commutation.**

I. Introduction

THREE typical ways are commonly utilized to realize ac–ac power conversion: direct ac–ac converters [1]–[6], ac–dc–ac converters [7]–[12], and single-phase matrix converters (SPMCs) [13]–[18]. Direct ac–ac converters have the ability to change the amplitude of input voltage but without the ability to change the output frequency. For applications where only voltage regulation is required, direct ac–ac converters are a more practical choice in terms of superiority in cost and size. Indirect ac–ac converter, namely ac–dc–ac converters can be utilized when variable frequency is required since they can provide arbitrary ac voltages. The disadvantages of ac–dc–ac converters lay on requirement of bulky short-life dc-link capacitors and large source filter inductors, leading to low power density, low efficiency, low reliability, and high cost [19]. The SPMCs utilize a single-stage power conversion to achieve both regulated voltage and step-changed frequency. The bulky dc capacitor is also eliminated. However, it should be pointed out that pure sinusoidal output voltage waveforms cannot be generated by the SPMCs with step-changed frequency. Therefore, for applications that require variable voltage and frequency but not sensitive to the quality of waveforms, the SPMCs are preferred candidates. Such kind of applications include induction heating [20], [21] and motor driver systems [22], medium-frequency transformer-isolation for traction [23] and wind turbine power converters [24], audio power amplification [25], dynamic voltage restoring [26], and so on.

The first SPMC, proposed by Zuckerberger *et al.* in [27] has the capability of voltage amplitude step-down and frequency step-up operation. Thereafter, some more studies have been proposed on the modeling, control scheme improvement and application exploration of SPMCs [28], [29]. However, the conventional SPMCs only feature voltage buck operation and there exist commutation problems since the bidirectional switches of a phase leg cannot be turned ON or OFF at the same time. In [30] and [31], a safe-commutation strategy is developed which employs the bidirectional switch itself as the freewheeling paths with arranged switching sequences.

Afterward, more SPMCs have been proposed. A Z-source buck–boost matrix converter is proposed in [32]. A wide range of buck–boost voltage operation and step-changed frequency are realized. However, the commutation problem cannot be avoided in this topology and additional delicate control strategy is required, increasing the complexity of control. In addition, many passive components and semiconductors are employed, leading to low energy transmission efficiency. In [33], an isolated single-phase buck converter with high frequency transformer is proposed. It can provide step-changed frequency. Meanwhile, the switch count is reduced and the loss is reduced. The main drawback of the topology is that only buck operation is realized. In [34], a SPMC utilizing six unidirectional switches is proposed. Buck–boost voltage regulation and step-changed frequency is realized. High-speed power MOSFETs can be used as their body diodes never conduct, avoiding the poor reverse

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The authors are with the Department of Instrumental and Electrical Engineering, Xiamen University, Xiamen 361005, China (e-mail: hlz190213@163.com; xuxinyongwo@qq.com).

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recovery problem. This also helps the converter be equipped with inherent commutation capability and immune of safe-commutation problem. However, total high number of semiconductors which increase the conduction and switching loss is the main defect of the topology. Sharifi *et al.* [35] propose a novel generalized configuration of single-phase ac–ac converter. Based on the configuration and originated from idea of a single-phase inverting buck–boost ac–ac converter in [36] and a buck–boost ac–ac converter implemented with a series-connected freewheeling diode and MOSFET pair in [37], a highly efficient buck–boost variable frequency ac–ac converter is proposed in [38]. In the topology of [38], buck–boost voltage regulation and step-changed frequency operation are both realized. Switch count and number of semiconductors are reduced and transfer efficiency is improved. Inherent safe-commutation is realized with a simple control scheme. The main drawback of the topology is that the input current is quasi-continuous and input filter is still required.

In this article, a novel buck–boost single-phase ac–ac converter topology is proposed, which is suitable for the applications requiring regulated ac voltage and variable frequency but not sensitive to the quality of voltage waveform such as induction heating and induction motor drives. Main characteristics of proposed ac–ac converter are listed below.

1) The proposed converter can be operated at buck and boost modes with a wide range of voltage regulation. The output can be in-phase or out-of-phase with the input voltage and thus step-changed frequency can be achieved.
2) The switch count of the proposed converter is only six and total number of semiconductor is ten, which are both at the lowest level among the proposed ac–ac converters. Therefore, conduction loss is reduced. Additionally, only two of the switches operate at high frequency while the other four operate at line frequency. Furthermore, only one switch operates during a high-frequency switching period. Therefore, the switching loss is highly reduced and the efficiency is further improved.
3) The proposed converter embodies safe-commutation with a simple and flexible control scheme. Therefore, no voltage source short-through or extreme voltage spike appears and additional safe-commutation control strategy or snubber circuit is unneeded.
4) Although the number of inductors is increased in proposed converter, the power density metric of proposed converter evaluated by a quantitative calculating method proposed in [39] considering the passive components volume shows superiority among competitors. Additionally, with continuous and sinusoidal input current, bulky input inductor filter that are required by other converters is removed. The power density can be further improved.

The rest of this article is organized as follows. The topology description and operating mechanism is given in Section II. In Section III, the component design and topology analysis is carried out. In Section IV, a 200-W laboratory prototype is established and experiment is conducted to verify the performance of the proposed converter. The conclusion is drawn in Section V.

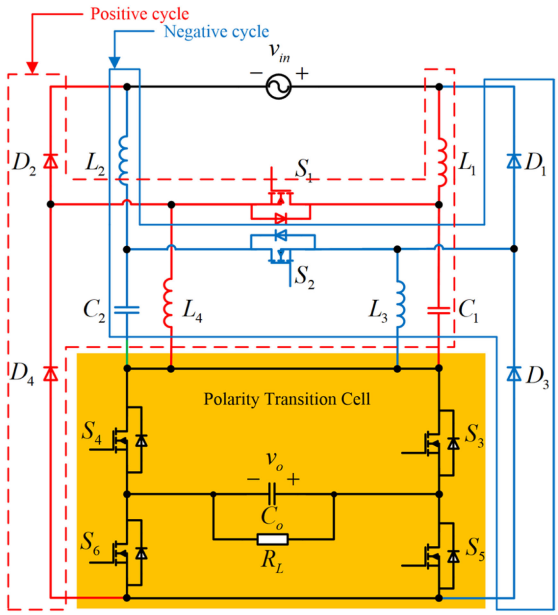

Fig. 1. Topology of the proposed single-phase buck–boost ac–ac converter.

II. Proposed Frequency-Variable Single-Phase Buck–Boost AC–AC Converter

A. Topology of the Proposed AC–AC Converter

The circuit topology of the proposed converter is shown in Fig. 1. It employs six active switches S_1–S_6 and four diodes D_1–D_4. Besides, two capacitors C_1–C_2 and four inductors L_1–L_4 are utilized for energy storage. The topology shows symmetry. As shown in Fig. 1, the set of components in dashed line frame mainly operates in the positive half cycle of input voltage while the set in solid line frame mainly works in the negative half cycle. Switches S_3–S_6 forms a polarity transition cell to generate inverting or noninverting output voltage, as shown in the shaded area. Except for storing energy, the capacitors are inserted to provide a freewheeling path for inductor currents. Therefore, safe-commutation is realized and no additional safe commutation control strategy or snubber circuit is required.

B. Control Strategy

The control scheme of proposed converter is depicted in Fig. 2, where switching diagram of three available output frequencies including 30, 60, and 120 Hz are shown. The input voltage frequency is 60 Hz. There are totally four circuit states in the converter operation, including state I: positive input with noninverting output, state II: negative input with inverting output, state III: positive input with inverting output, and state IV: negative input with noninverting output. With different permutation and combination of the four operation states, different output frequency is obtained. Arbitrary frequencies are attainable literally since the circuit state can be changed at any desired time. However, to maintain a good output voltage waveform, integer multiples and integer fractions of the input frequency are chosen in this article.

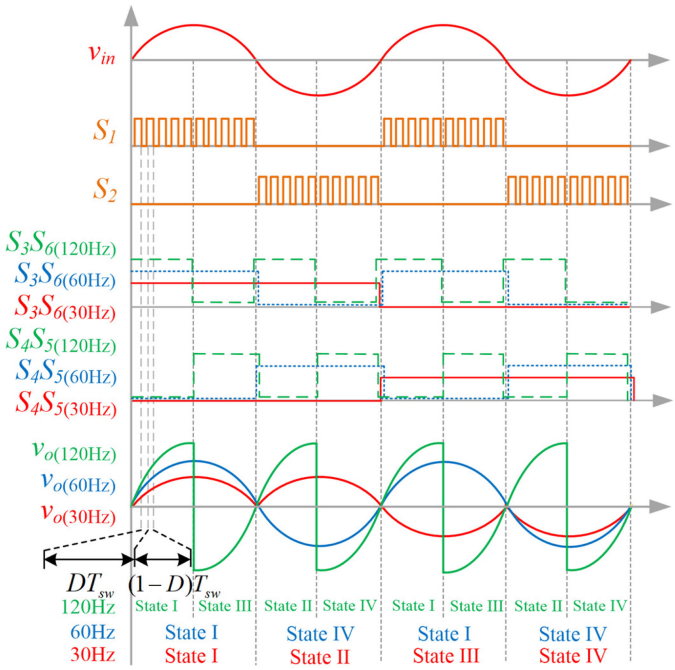

Fig. 2. Switching diagram of the proposed buck–boost ac–ac converter with 30-, 60-, and 120-Hz output frequency operation.

As shown in Fig. 2, S_1 and S_2 are controlled by high frequency PWM signals. S_1 functions to regulate the positive cycle of input voltage and S_2 regulates the negative cycle. S_3–S_6 constitutes a polarity transition cell, where S_3 and S_6 are simultaneously switched ON and OFF as the complementary of S_4 and S_5, both fed by low-frequency control signals. Switches S_3, S_6 are denoted as positive switch pair while S_4, S_5 are denoted as negative switch pair. During the positive cycle of input voltage, with the positive switch pair turned ON and negative switch pair turned OFF, the output voltage is in-phase with input voltage, otherwise it is out-of-phase. During the negative cycle of input voltage, with the positive switch pair turned ON and negative switch pair turned OFF, the output voltage is out-of-phase with input voltage and otherwise, it is in-phase.

Thirty-hertz output frequency case is taken as representative example to explain the operation principles. As shown in Fig. 2, 30-Hz operation case comprises total four typical circuit states.

1) State I. Positive Input With Noninverting Output: As shown in Fig. 2, 30-Hz frequency operation contains two 60-Hz input voltage line periods. The first circuit state of an output period is in the positive cycle of the first input line period. High-frequency switch S_1 is switched to form two operation modes for output voltage regulation. The positive switch pair is kept turned ON during this state, leading to noninverting operation.

a) Mode 1: S_1 is fed by a high frequency control signal with a dwell time $\mathrm{DT_{sw}}$. T_{sw} denotes the switching period. The equivalent circuit of this mode is depicted in Fig. 3(a). As seen from the figure, inductor L_1 is charged by the voltage source through S_1 and D_2, inductor L_4 is charged by capacitor C_1 through S_1. Another circuit path is the freewheeling current through inductor L_2, L_3, capacitor C_2, and parasitic diode of switch S_2. The output capacitor freely dissipates energy to the load. It should be noticed that the output current is natively blocked by diode D_4 in this mode. Current through S_3 and S_6 decreases to zero but the voltage over the switches still keeps zero. Therefore, the passive turning-OFF of switches in polarity transition cell does not contribute to the switching loss.

According to the equivalent circuit shown in Fig. 3(a), the voltage applied on the inductors in this duration can be summarized

$$\begin{cases} V_{L1} = V_{\mathrm{in}} \\ V_{L4} = V_{C1}. \end{cases} \tag{1}$$

b) Mode 2: S_1 is OFF during the time duration $(1-D)T_{\mathrm{sw}}$. As shown in Fig. 3(b), there are two charging paths. The first is shown with dashed line. In this path, capacitor C_1 and the output *RC* load is charged by the voltage source and inductor L_1 through S_3, S_6 and D_2, D_4. Another charging circuit is shown with solid line, where the output *RC* load is charged by inductor L_4 through S_3, S_6 and D_4. Inductor current freewheeling path involving inductor L_2, L_3, capacitor C_2 and parasitic diode of switch S_2 still exists.

According to the equivalent circuit of Fig. 3(b), the voltage applied on the inductors is summarized as below

$$\begin{cases} V_{L1} = V_{\mathrm{in}} - V_{\mathrm{o}} - V_{C1} \\ V_{L4} = -V_{\mathrm{o}}. \end{cases} \tag{2}$$

Applying the volt-second balance on inductor L_1 and L_4, respectively, the voltage on capacitor C_1 and input–output voltage gain M in this circuit state can be derived as

$$\begin{cases} V_{C1} = V_{\mathrm{in}} \\ M = \frac{V_{\mathrm{o}}}{V_{\mathrm{in}}} = \frac{D}{1-D}. \end{cases} \tag{3}$$

The voltage gain expression of the converter is the same as that of a conventional buck–boost converter. The voltage gain curve is depicted in Fig. 4 with the dashed line. Positive voltage gain value means the output voltage is noninverting and negative value means inverting output voltage. When $D < 0.5$, the converter operates as a buck converter; when $D > 0.5$, the converter operates as a boost converter.

Some circuit characteristics should be noticed: In state I, diode D_2 conducts in both operation modes. Therefore, D_2 conducts at the whole state and is passively switched at line frequency. Diode D_4 is forward biased in mode 1 and blocked in mode 2 and is operating at switching frequency. The body diode of S_2 keeps conducting during a whole switching period and is also switched at line period. To sum up, for all diodes of the converter, only D_3 and D_4 are switched at high frequency and should be considered the recovery problem when selecting practical devices. In state I, capacitor C_2 provides a circuit path for inductor current flowing. Capacitor C_1 functions for both energy storage and current freewheeling. Therefore, the capacitors C_1, C_2 are applied not only for energy transferring but also for providing freewheeling paths for inductor current to realize safe-commutation.

2) State II. Negative Input With Inverting Output: The second circuit state of an output period is in the negative half cycle of the first input line period. High frequency switch S_2 is switched

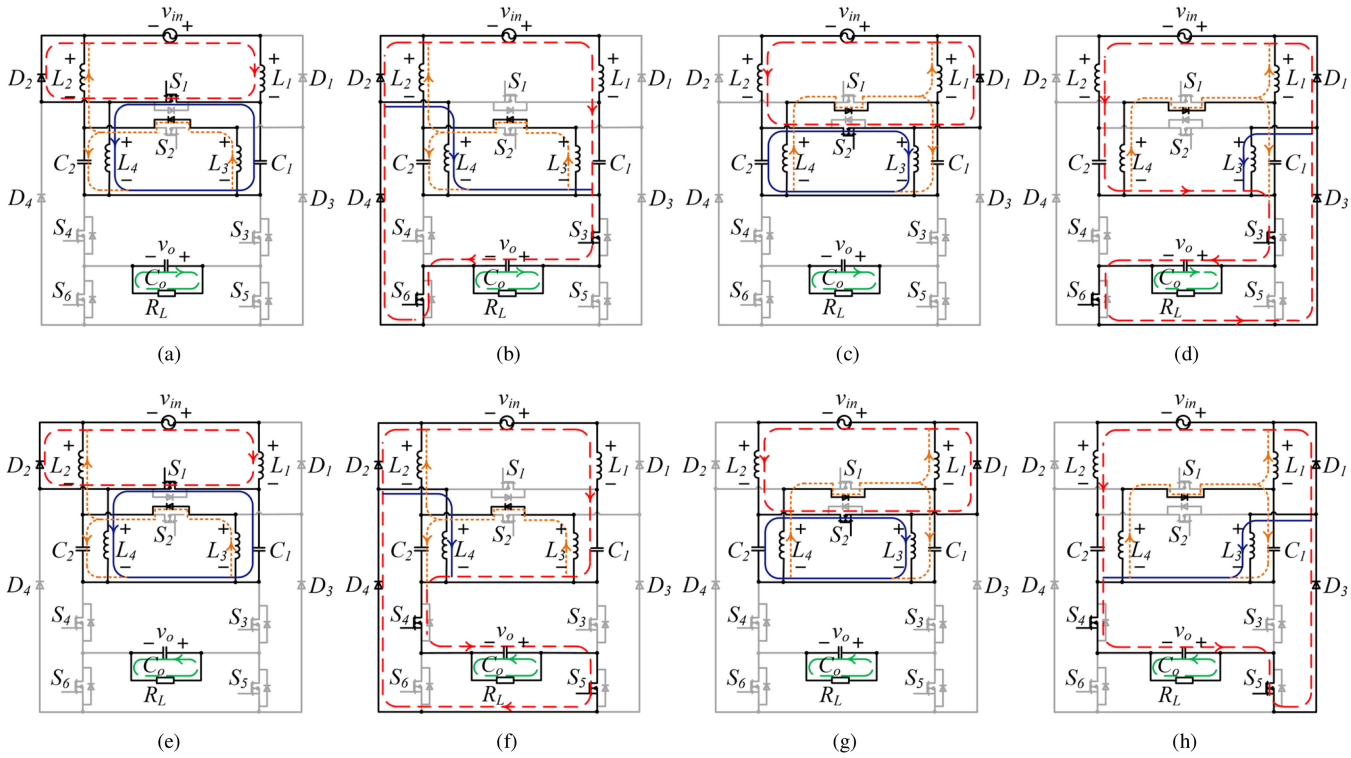

Fig. 3. Equivalent circuits of the proposed converter in 30-Hz output frequency operation during (a) Mode 1 and (b) Mode 2 in state I. (c) Mode 1 and (d) Mode 2 in state II. (e) Mode 1 and (f) Mode 2 in state III. (g) Mode 1 and (h) Mode 2 in state IV.

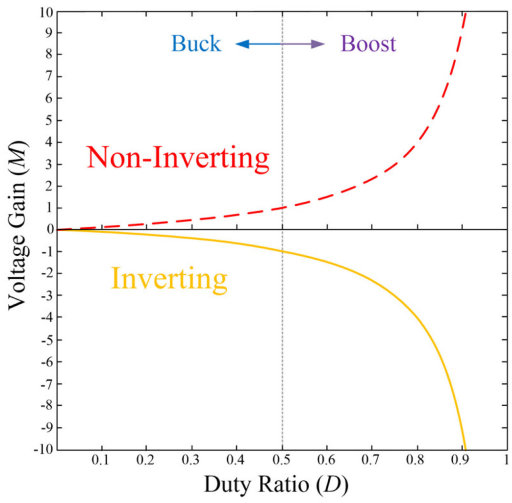

Fig. 4. Relationship between the voltage gain (M) and duty cycle (D).

for voltage regulation. The positive switch pair is turned ON during this time interval, leading to inverting operation capacitor C_2 through S_2. Another circuit path is the freewheeling current through inductor L_1, L_4, capacitor C_1 and parasitic diode of switch S_1. The output capacitor freely dissipates energy to the load.

a) Mode 1: S_2 is fed with a high frequency control signal with a dwell time DT_{sw}. The equivalent circuit of this mode is shown in Fig. 3(c). As seen from the figure, inductor L_2 is charged by the voltage source through S_2 and D_1, inductor L_3 is charged by capacitor C_2 through S_2. Another circuit path is the freewheeling current through inductor L_1, L_4, capacitor C_1 and parasitic diode of switch S_1. The output capacitor freely dissipates energy to the load.

According to Fig. 3(c), the voltage applied on the inductors in this duration is summarized

$$\begin{cases} V_{L2} = -V_{\mathrm{in}} \\ V_{L3} = V_{C2}. \end{cases} \tag{4}$$

Here, the actual direction of V_{in} is negative.

b) Mode 2: S_2 is OFF during the OFF-state time interval $(1-D)T_{\mathrm{sw}}$. As shown in Fig. 3(d), there are two charging paths. The first circuit path is shown with dashed line. In this circuit path, capacitor C_2 and the output RC load is charged by the voltage source and inductor L_2 through S_3, S_6 and D_1, D_3. Another charging path is shown with solid line, where the output RC load is charged by inductor L_3 through S_3, S_6 and D_3. Inductor current freewheeling path involving inductor L_1, L_4, capacitor C_1 and parasitic diode of switch S_1 still exists.

According to the equivalent circuit of Fig. 3(d), the voltage applied on the inductors in this duration can be summarized as

$$\begin{cases} V_{L2} = -V_{\mathrm{in}} - V_{\mathrm{o}} - V_{C2} \\ V_{L3} = -V_{\mathrm{o}}. \end{cases} \tag{5}$$

Applying the volt-second balance on inductor L_2 and L_3, respectively, the voltage on capacitor C_2 and input–output voltage

gain M in this state can be derived as

$$\begin{cases} V_{C2} = -V_{\text{in}} \\ M = \frac{V_o}{V_{\text{in}}} = -\frac{D}{1-D} V_{\text{in}}. \end{cases} \tag{6}$$

The voltage gain curve in this state is shown in Fig. 4 with the solid line. It is seen that the gain curves in the two states are symmetric with respect to the zero-axis. To obtain output voltage with stable amplitude, same duty cycle should be set for S_1 and S_2.

3) State III. Positive Input With Inverting Output: The third circuit state of the output voltage period is in the positive half cycle of the second input line period. The only difference of the control diagram in this state from state I is that the negative switch pair is turned ON instead, leading to inverting operation. The equivalent paths of two operation modes in this state are shown in Fig. 3(e) and (f) and the voltage gain is derived as

$$M = -\frac{D}{1-D}. \tag{7}$$

4) State IV. Negative Input With Noninverting Output: The fourth circuit state of the output voltage period is in the negative half cycle of the second input line period. The only difference of the control diagram in this state from state II is that the negative switch pair is turned ON in this time interval, leading to noninverting operation. The equivalent circuits of the two operation modes in this state are shown in Fig. 3(g) and (h) and the voltage gain is derived as

$$M = \frac{D}{1-D}. \tag{8}$$

With different permutation and combination of the four typical circuit states, other output frequency operation can be achieved. As seen in Fig. 2, when 60-Hz output frequency is desired which is identical with the input voltage, the output voltage keeps in phase with the input voltage during each half cycle. In other words, only states I and IV are utilized. To get step-up 120 Hz output frequency, as shown in Fig. 2, four circuit states are utilized in a single input period. In the first 1/4 input period time duration, state I operation is applied and in the 1/4–1/2 input period time duration, it changes to state III. In the third 1/4 input period time duration, state II operation is applied and in the last 1/4 input period time duration, state IV operation is utilized. For buck or boost operation, it depends on the duty ratio of the two high frequency switches S_1 and S_2. For buck mode, the duty ratio D is set to be lower than 0.5. For boost mode, it is higher than 0.5.

C. Safe Commutation

AC–AC converters usually suffer from commutation problems [40]. There inherently exists short dead-time or overlap between bidirectional switches of ac–ac converters, which may cause commutation problem of huge voltage spike or high current peak. Usually delicate control scheme is employed to avoid overlap and meanwhile provides flowing path for inductor current, which will increase the complexity of the control scheme. Snubber circuit can also be employed to absorb additional reactive power during dead-time for safe commutation.

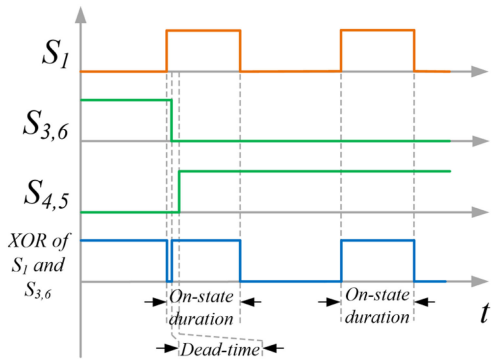

Fig. 5. Switching signals at the first state change moment of 30-Hz output frequency.

But, it highly increases the cost and complexity of the circuit and decrease the transfer efficiency.

For proposed ac–ac converter, a simple control scheme is conducted and it achieves safe-commutation. The control strategy has been presented in Part II. During positive half cycle of input voltage, only S_1 operates at high frequency and during negative half cycle of input voltage, only S_2 operates at high frequency. S_3–S_6 operate at line frequency as polarity transition cell to form inverting or noninverting output voltage. In the topology, the body diode of switch device is utilized to form safe flowing path for inductors. For example, as shown in Fig. 3(b), during the positive half cycle of input voltage, the body diode of S_2 conducts to provide current paths for inductor L_2 and L_3. One of the commutation paths consists of L_1, L_2, L_3, C_1 and body diode of S_2. The other commutation path includes L_3, C_2 and body diode of S_2. The body diode of S_1 plays the same role during negative half cycle of input voltage, as depicted in Fig. 3(d). The body diodes always conduct during each whole operation state. They are passively switched at line frequency and thus the poor recovery problem of them is not needed to be considered. Therefore, there exists no high-frequency commutation problem.

For 60- and 120-Hz output frequency operation, since the circuit state changes when the output voltage is zero, the overlap of low-frequency switching signals of S_3, S_6 and S_4, S_5 will not cause short through of output capacitor and there is no commutation problem. For 30-Hz output frequency operation, the output voltage is not zero and there cannot be overlap between the low-frequency switching signals. However, it can be found from the operation modes of the converter that when high-frequency switches are turned ON, the low-frequency switches S_3–S_6 are naturally blocked, as shown in Fig. 3(a), (c), (e), and (g). Therefore, switching the low-frequency switches at the ON-state modes of high-frequency switches will not affect the operation of the circuit. In this way, the switching of low-frequency switches can be arranged at the ON-state modes of high-frequency switches and a small dead time can be inserted to the low-frequency switching signals. As shown in Fig. 5, the first state change moment of 30-Hz output frequency is taken as an example. In this case, signal for allowing state changes is the low-level of XOR signal of S_1 and $S_{3,6}$. The dead time is set to tens of nanoseconds according to the turn-ON time and

turn-OFF time of MOSFET devices, which is much shorter than the ON-state duration of high-frequency switches. Therefore, the low-frequency safe commutation is easily achieved.

III. Components Design and Topology Analysis

A. Component Design

1) Passive Components Design: The passive components are designed considering their allowable maximum current ripples or voltage ripples. For proposed topology, passive components include four inductors L_1–L_4 and two energy storing capacitors C_1 and C_2.

For designing of L_1 and L_2, the peak current is given by

$$\sqrt{2}I_{L1(2)\_\mathrm{rms}} = \sqrt{2}I_{\mathrm{in\_rms}} = \sqrt{2}\frac{D}{1-D}I_{\mathrm{o\_rms}}. \tag{9}$$

Allowable current ripple is set to be $\alpha\%$ of peak inductor current

$$\Delta I_{L1(2)} = \alpha\%\sqrt{2}I_{L1(2)\_\mathrm{rms}}. \tag{10}$$

The requirement of L_1 and L_2 are obtained

$$L_1, L_2 \geq \frac{(1-D)V_{\mathrm{in\_rms}}T_{\mathrm{sw}}}{\alpha\%I_{\mathrm{o\_rms}}}. \tag{11}$$

For inductors L_3 and L_4, the peak current is given by

$$\sqrt{2}I_{L3(4)\_\mathrm{rms}} = \sqrt{2}I_{\mathrm{o\_rms}}. \tag{12}$$

Thus, the required inductance of L_3 and L_4 are

$$L_3, L_4 \geq \frac{DV_{\mathrm{in\_rms}}T_{\mathrm{sw}}}{\alpha\%I_{\mathrm{o\_rms}}}. \tag{13}$$

Analogous to sizing the inductors, the capacitance of C_1 and C_2 can be obtained from the capacitor voltage ripple constraint. Assuming the acceptable voltage ripple is $\beta\%$ of the peak voltage across them, the peak voltage and the required capacitance are

$$\sqrt{2}V_{C1(2)\_\mathrm{rms}} = \sqrt{2}V_{\mathrm{in\_rms}} \tag{14}$$

$$C_1, C_2 \geq \frac{DI_{\mathrm{o\_rms}}T_{\mathrm{sw}}}{\beta\%V_{\mathrm{in\_rms}}}. \tag{15}$$

Ripple of output voltage is decided by output capacitor C_{o}. To limit the output voltage ripple into $\gamma\%$ of peak value, the designed value of output capacitance is derived as

$$\sqrt{2}V_{C\mathrm{o,rms}} = \sqrt{2}\frac{D}{1-D}V_{\mathrm{in\_rms}} \tag{16}$$

$$C_{\mathrm{o}} \geq \frac{(1-D)I_{\mathrm{o\_rms}}T_{\mathrm{sw}}}{\gamma\%DV_{\mathrm{in\_rms}}}. \tag{17}$$

2) Active Components Design: The semiconductor devices are designed considering their voltage and current stress. The voltage and current stress of each switch and diode in proposed converter are listed below.

Voltage stress of each semiconductor device

$$\begin{cases} V_{S1\_\mathrm{peak}} = V_{S2\_\mathrm{peak}} = \sqrt{2}\frac{1}{1-D}V_{\mathrm{in\_rms}} \\ V_{S3\_\mathrm{peak}} \sim V_{S6\_\mathrm{peak}} = \sqrt{2}\frac{D}{1-D}V_{\mathrm{in\_rms}} \\ V_{D1\_\mathrm{peak}} = V_{D2\_\mathrm{peak}} = \sqrt{2}V_{\mathrm{in\_rms}} \\ V_{D3\_\mathrm{peak}} = V_{D4\_\mathrm{peak}} = \sqrt{2}V_{\mathrm{in\_rms}}. \end{cases} \tag{18}$$

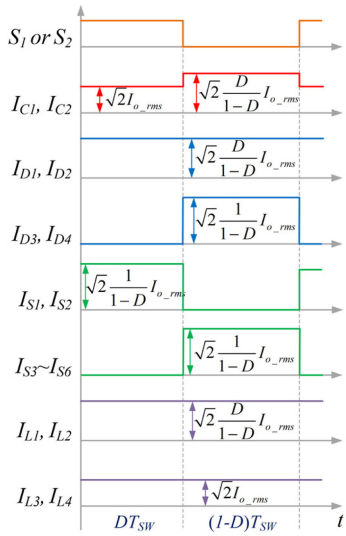

Fig. 6. Simplified current waveforms of each component during a switching period.

Current stress of each semiconductor device

$$\begin{cases} I_{S1\_\mathrm{peak}} = I_{S2\_\mathrm{peak}} = \sqrt{2}\frac{1}{1-D}I_{\mathrm{o\_rms}} \\ I_{S3\_\mathrm{peak}} \sim I_{S6\_\mathrm{peak}} = \sqrt{2}\frac{1}{1-D}I_{\mathrm{o\_rms}} \\ I_{D1\_\mathrm{peak}} = I_{D2\_\mathrm{peak}} = \sqrt{2}\frac{D}{1-D}I_{\mathrm{o\_rms}} \\ I_{D3\_\mathrm{peak}} = I_{D4\_\mathrm{peak}} = \sqrt{2}\frac{1}{1-D}I_{\mathrm{o\_rms}}. \end{cases} \tag{19}$$

B. Loss Analysis

Efficiency analysis for the proposed converter is conducted to further reveal the performance. Some assumptions are made for simplicity: components that work in the positive half cycle have the symmetric parameters with that work in the negative half cycle; the current ripples on the inductors and the voltage ripples on the capacitors are neglected; loss in auxiliary circuit is neglected. With the assumption, simplified operation current waveforms during a switching period on each component when input voltage is at peak value are depicted in Fig. 6.

The ON-state resistance of MOSFETs is represented by r_{on}, Forward voltage of diodes is denoted by V_{F}. r_L denotes the equivalent series resistance (ESR) of inductors and r_c represents the ESR of capacitors. The conduction loss of the proposed converter contains loss related to the MOSFETs, diodes, inductors, and capacitors.

Since each component only conducts during one half cycle of an input line period, the rms current of switches, inductors, and capacitors in a line period and average current of diodes in a line period yield

$$\begin{cases} I_{S1\_\mathrm{rms}} = I_{S2\_\mathrm{rms}} = \frac{1}{\sqrt{2}}\frac{\sqrt{D}}{1-D}I_{\mathrm{o\_rms}} \\ I_{S3\_\mathrm{rms}} \sim I_{S6\_\mathrm{rms}} = \sqrt{\frac{1}{2-2D}}I_{\mathrm{o\_rms}} \\ I_{L1\_\mathrm{rms}} = I_{L2\_\mathrm{rms}} = \frac{1}{\sqrt{2}}\frac{D}{1-D}I_{\mathrm{o\_rms}} \\ I_{L3\_\mathrm{rms}} = I_{L4\_\mathrm{rms}} = \frac{1}{\sqrt{2}}I_{\mathrm{o\_rms}} \\ I_{C1\_\mathrm{rms}} = I_{C2\_\mathrm{rms}} = \sqrt{\frac{D}{2-2D}}I_{\mathrm{o\_rms}} \\ I_{D1\_\mathrm{ave}} = I_{D2\_\mathrm{ave}} = \frac{\sqrt{2}D}{\pi(1-D)}I_{\mathrm{o\_rms}} \\ I_{D3\_\mathrm{ave}} = I_{D4\_\mathrm{ave}} = \frac{\sqrt{2}}{\pi}I_{\mathrm{o\_rms}}. \end{cases} \tag{20}$$

TABLE I
COMPARISON BETWEEN PROPOSED CONVERTER WITH OTHER FREQUENCY-VARIABLE SINGLE-PHASE AC–AC CONVERTERS

Items	Proposed Converter	Converter in [38]	Converter in [34]	Converter in [32]
Voltage gain	$\frac{D}{1-D}$	$\frac{D}{1-D}$	$\frac{D}{1-D}$	$\frac{1-D}{1-2D}$
Voltage regulation ability	Buck-Boost	Buck-Boost	Buck-Boost	Buck-Boost
Frequency variation ability	Yes	Yes	Yes	Yes
Number of MOSFETs	6	6	6	10
Number of diodes	4	4	6	0
Number of conducting devices in a switching period	Mode 1:3 Mode 2:5	Mode 1:4 Mode 2:4	Mode 1:6 Mode 2:6	Mode 1:5 Mode 2:3
Number of high-frequency switches in a switching period	1	1	4	4
Total semiconductor voltage stress, / $\sqrt{2}V_{in\_rms}$	$\frac{6}{1-D}$	$\frac{6+2D}{1-D}$	$\frac{8-4D}{1-D}$	$\frac{10}{1-2D}$
Total semiconductor current stress, / $\sqrt{2}I_{o\_rms}$	$\frac{8+2D}{1-D}$	$\frac{8-2D}{1-D}$	$\frac{12}{1-D}$	$\frac{20}{1-D}$
Number of inductors	4	2	1	2
Peak current of inductors, / $\sqrt{2}I_{o\_rms}$	$L_1L_2:\frac{D}{1-D}$ $L_3L_4:1$	$\frac{1}{1-D}$	1	$\frac{1-D}{1-2D}$
Number of magnetic cores	2	1	1	2
Number of energy storing capacitors	2	2	0	2
Peak voltage of energy storing capacitors, / $\sqrt{2}V_{o\_rms}$	$\frac{1-D}{D}$	$\frac{1}{D}$	/	1
Passive components volume, $/T_{sw}P_o$	$\frac{1}{\alpha\%\rho_{E,L}}+\frac{1-D}{\beta\%\rho_{E,C}}$	$\frac{1}{\alpha\%\rho_{E,L}}+\frac{1}{2\beta\%\rho_{E,C}}$	$\frac{1}{\alpha\%\rho_{E,L}}$	$\frac{D(1-D)}{(1-2D)\alpha\%\rho_{E,L}}+\frac{D(1-D)}{(1-2D)\alpha\%\rho_{E,C}}$
Continuity of input current	Continuous	Quasi-Continuous	Discontinuous	Discontinuous
Requirement of input filter	No need for input filter	Small input filter	Bulky input filter	Bulky input filter
Commutation Problem	No	No	No	Yes

With step-changed frequency operation, the calculation result remains the same. Therefore, the conduction power loss can be derived

$$\begin{aligned} P_{\text{loss\_con}} &= 2({I_{S1\_\text{rms}}}^2 + 2{I_{S3\_\text{rms}}}^2)r_{\text{on}} \\ &\quad + 2({I_{L1\_\text{rms}}}^2 + {I_{L3\_\text{rms}}}^2)r_L \\ &\quad + 2{I_{C1\_\text{rms}}}^2 r_C + 2(I_{D1\_\text{ave}} + I_{D3\_\text{ave}})V_F \end{aligned} \quad (21)$$

The switching loss involves high-frequency switches S_1 and S_2. With an instant input voltage V_{in}, the instantaneous switching loss can be derived as

$$\begin{cases} P_{\text{loss\_on\_ins}} = \frac{1}{6}\frac{f_{\text{sw}}D}{(1-D)^3}\frac{{V_{\text{in}}}^2}{R_L}t_{\text{on}} \\ P_{\text{loss\_off\_ins}} = \frac{1}{6}\frac{f_{\text{sw}}D}{(1-D)^3}\frac{{V_{\text{in}}}^2}{R_L}t_{\text{off}}. \end{cases} \quad (22)$$

$P_{\text{loss\_on\_ins}}$ and $P_{\text{loss\_off\_ins}}$ are the turn-ON loss and turn-OFF loss in this instant, respectively. t_{on} and t_{off} are the turn-ON time and turn-OFF time of the high-frequency switches, respectively. In a line period, the switching loss is integral of the instantaneous switching loss. Therefore, the switching loss of a high-frequency switch is derived as

$$\begin{cases} P_{\text{loss\_on}} = \frac{f_{\text{sw}}{DV^2}_{\text{in\_rms}}}{12(1-D)^3R_L}\cdot t_{\text{on}} \\ P_{\text{loss\_off}} = \frac{f_{\text{sw}}{DV^2}_{\text{in\_rms}}}{12(1-D)^3R_L}\cdot t_{\text{off}}. \end{cases} \quad (23)$$

The loss expressions of a switch also remain unchanged under step-changed output frequency operation. Thus, the total switching loss yields

$$P_{\text{loss\_sw}} = \frac{f_{\text{sw}}{DV^2}_{\text{in\_rms}}}{6(1-D)^3R_L}(t_{\text{on}} + t_{\text{off}}). \quad (24)$$

To sum up, the total power loss of the proposed converter yields

$$P_{\text{loss}} = P_{\text{loss\_con}} + P_{\text{loss\_sw}}. \quad (25)$$

Finally, the efficiency of the converter can be expressed as

$$\eta = \frac{P_{\text{o}}}{P_{\text{o}} + P_{\text{loss}}} \quad (26)$$

where, P_o represents the output power and $P_{\text{o}} = V_{\text{o\_rms}}I_{\text{o\_rms}}$.

C. Topology Analysis

An exhaustive comparison result between proposed converters with other single phase ac–ac converters proposed in [32], [34], and [38] is summarized in Table I.

Seen from Table I, the proposed converter features both buck and boost operation ability with frequency-variation ability. The switch count of the proposed converter is reduced to six. Number of semiconductors conduct in a high switching period is 3 and 5 in each mode, which is the same as that of converter in [32], same total number as converter in [38] but much reduced compared to converter in [34]. Only one switch is operated in each high switching period, much less than converters in [32] and [34], leading to highly reduced switching power loss. The proposed

converter achieves safe commutation, no additional safe commutation strategy or snubber circuit is required. Compared to converter in [38], total semiconductors current stress is increased but total voltage stress is reduced. Therefore, proposed converter is better candidate for occasions where there is high voltage and low current. Moreover, the inductors utilized in proposed converter suffer from lower current and capacitors suffer from lower voltage at the same duty ratio compared to converter in [38], which implies higher transfer efficiency.

Four independent inductors are employed in proposed topology. Taking the method of designing magnetic core in [38], two EE magnetic cores are utilized. L_1, L_2 share a same core and they are wound on the gapped side-limbs while the middle-limb is ungapped. L_3, L_4 are wound on another with the same idea.

When comparing the power density, assumption is usually made that volume of active devices and auxiliary circuits is neglected since volume of converter is dominated by capacitors and inductors in high power application. An analytical method to evaluate total volume metric for passive components of a converter is proposed in [39]. The volume of passive component is proportional to the energy it stored ($1/2LI^2$ for inductors and $1/2CV^2$ for capacitors), the minimum requirement of L and C considering the ripple constraint and rated current and voltage over the components is substituted to calculate the extreme small volume of converter. For proposed converter, the inductance and capacitance requirement and current, voltage rating of passive components are calculated before. The volume metric of an inductor is calculated by ratio of the energy it stored and the volumetric energy density of inductor $\rho_{E,L}$. The total inductor volume metric is the combination of four inductors

$$V_{\text{inductor}} = \frac{\sum E_{Li}}{\rho_{E,L}} = \frac{P_o}{\alpha\% f_{\text{sw}} \rho_{E,L}}. \tag{27}$$

Similarly, the volume metric of a capacitor is calculated by ratio of the energy it stored and the volumetric energy density of capacitor $\rho_{E,C}$. Total capacitor volume metric is the combination of two energy storing capacitors

$$V_{\text{capacitor}} = \frac{\sum E_{Ci}}{\rho_{E,C}} = \frac{(1-D)P_o}{\beta\% f_{\text{sw}} \rho_{E,C}} \tag{28}$$

where $\alpha\%$ and $\beta\%$ are current and voltage ripple tolerance coefficient to get least inductance and capacitance requirement, respectively. Total volume metric of converter is the combination of total inductor volume and capacitor volume

$$V_{\text{converter}} = \left(\frac{1}{\alpha\% \rho_{E,L}} + \frac{1-D}{\beta\% \rho_{E,C}} \right) \frac{P_{\text{o}}}{f_{\text{sw}}}. \tag{29}$$

The volume metric of other competitors are also calculated and listed in Table I. Here, the switching frequency, rated output power, and ripple tolerance coefficient for inductors and capacitors are kept identical for all converters. It can be seen that although more inductors are employed in proposed topology, the total requirement of inductor volume is the same as that of converter from [38] and [34]. For capacitor volume metric, the proposed converter shows its superiority in boost mode over converter in [38]. In both volume metric of inductor and capacitor, the first three topologies are better off against the converter in [32].

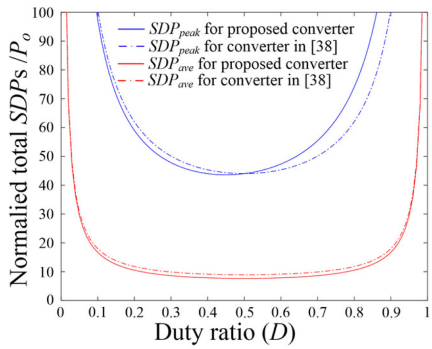

Fig. 7. Normalized total SDPs against duty ratio.

However, unlike the other converters, the input current of proposed converter is pure continuous and sinusoidal as it is the combination of the current of L_1 and L_2. Therefore, no additional input filter is needed for the converter. The input filter is not accounted in the calculation of converter volume metric but will actually decrease the power density. According to continuity of input current, small input filter is needed for converter in [38] and bulky input filter is needed for converters in [34] and [32]. Hence, the proposed topology can feature higher power density among the candidates in practical applications.

Furthermore, the index of total peak switching device powers (SDP_{peak}) and average switching device powers (SDP_{ave}), which have been introduced in [41], are calculated for proposed converter and converters in [38] to quantify and compare the voltage and current stress. The total SDPs are defined as the aggregate of product of voltage stress and current stress of all the switching devices used in the circuit to value the total cost of a converter design. A better topology tends to have lower total SDP_{peak} and SDP_{ave}. The calculation results of the proposed converter are:

$$\begin{cases} \text{SDP}_{\text{peak}} = \sum_{m=1}^{N} V_{\text{m\_peak}} I_{\text{m\_peak}} = \frac{8+8D-4D^2}{D(1-D)} P_{\text{o}} \\ \text{SDP}_{\text{ave}} = \sum_{m=1}^{N} V_{\text{m\_peak}} I_{\text{m\_ave}} = \frac{4+8D-8D^2}{\pi D(1-D)} P_{\text{o}} \end{cases} \tag{30}$$

where N is the total number of semiconductors, $V_{\text{m\_peak}}$ is voltage stress of each device, and $I_{\text{m\_peak}}$ and $I_{\text{m\_ave}}$ are the peak and average current stress, respectively.

The total SDP_{peak} and SDP_{ave} of converter in [38] is

$$\begin{cases} \text{SDP}_{\text{peak}} = \frac{8+12D-12D^2}{D(1-D)} P_{\text{o}} \\ \text{SDP}_{\text{ave}} = \frac{4+12D-12D^2}{\pi D(1-D)} P_{\text{o}}. \end{cases} \tag{31}$$

With same output power, the normalized total SDPs against duty ratio curves of each converter are shown in Fig. 7. The SDP_{peak} index of proposed converter is lower than that of converter in [38] when $D < 0.5$ and higher when $D > 0.5$.

For SDP_{ave} index, the proposed converter features lower one in the whole duty ratio region with comparison to converter in [38]. Therefore, superiority on the voltage and current stress of the proposed converter against the competitors is validated.

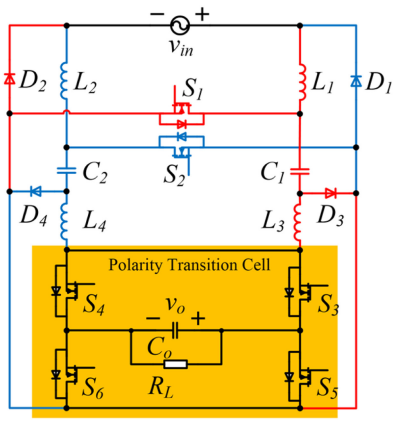

Fig. 8. Extended frequency-variable ac–ac topology.

TABLE II
COMPONENTS LIST AND SPECIFICATIONS OF THE PROTOTYPE

Component	Parameters
Switches S_1, S_2	IRFPS43N50KPBF/78mΩ
Switches S_3-S_6	IRFP4332PBF/29mΩ
Diodes D_1, D_2	MBR20200CT/0.89V
Diodes D_3, D_4	FX2000F/0.94V
Inductors L_1, L_2	450μH
Inductors L_3, L_4	300μH
Capacitors C_1, C_2	1.2μF
Output capacitor C_o	6.6μF
Switching frequency f_{sw}	50kHz
Input frequency f_{in}	60Hz
Output voltage $V_{o\ rms}$	71Vrms
Load R_L	25Ω
Output power P_o	200W

D. Extended Topology

The proposed converter is derived from SEPIC converter. According to the design idea of two-part with polarity unit configuration, more derivative frequency-variable ac–ac topologies can be designed. For example, a topology design based on Cuk converter is shown in Fig. 8. It also has buck–boost function. The input/output voltage ratio is $D/(1-D)$. The output voltage is regulated by switches S_1 and S_2, and the phase difference of input and output is adjusted by switches S_3–S_6. In this extended topology, the input and output current are both continuous.

IV. EXPERIMENTAL RESULTS

A 200-W laboratory prototype is built and experiments have been conducted to verify the performance of the proposed converter. Parameters of the components are listed in Table II. The block diagram of tested prototype is depicted in Fig. 9. A comparator circuit is constructed for detecting polarity of input ac voltage. The DSP generates control signals with corresponding time sequence as shown in Fig. 2 under three frequency operation conditions: 30 Hz (step-down frequency), 60 Hz (identical frequency), and 120 Hz (step-up frequency). Two operation modes under open-loop: buck ($D = 0.4$) and boost ($D = 0.6$) operation are performed for each frequency operation condition to validate the voltage gain expression. Output power maintains 200 W with

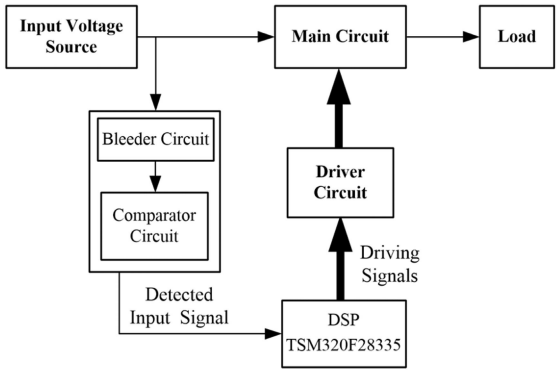

Fig. 9. Block diagram of the experimental prototype.

TABLE III
POWER FACTORS AND THD OF PROPOSED CONVERTER ON STEP-CHANGED FREQUENCY AND BUCK–BOOST OPERATION

Operation Mode	Buck			Boost		
Output Frequency	30Hz	60Hz	120Hz	30Hz	60Hz	120Hz
Power Factor	0.982	0.976	0.956	0.987	0.980	0.968
THD of V_o	60.5%	2.02%	56.0%	61.1%	2.84%	56.5%
THD of I_{in}	2.67%	3.13%	4.82%	2.91%	3.06%	4.66%

output voltage regulated to 71 Vrms and load fixed to 25 Ω. With buck or boost operation, the input voltage is correspondingly changed. The switching frequency is 50 kHz.

Fig. 10(a), (b), and (c) shows the proposed converter with 30-, 60-, and 120-Hz operation in buck mode, respectively. In each frequency operation condition, the waveforms of input voltage, output voltage, input current, output current, inductor current, capacitor voltage, voltage stress on high frequency switches and voltage stress on line frequency switches are depicted. Besides, zoom-in waveforms of inductor current, capacitor voltage and voltage stress on switches are represented. In buck mode, theoretical rms value of input voltage is 106.1 Vrms with comparison to the measured value of 107.8 Vrms. Fig. 11 depicts the proposed converter with three typical frequency operations in boost mode. In this case, output voltage increases to 71 Vrms when input voltage is 46.4 Vrms, with comparison to the calculated result of 47.1 Vrms. Seen from the zoom-in waveforms of inductor current, capacitor voltage, and stress voltage, it is verified that no short-through or voltage spike appears during the operation of proposed converter as in consistency with the analysis.

The power factor and total harmonic distortion (THD) value of input current and output voltage of the prototype under various conditions are listed in Table III. High power factor and good quality of waveforms are achieved. With lower output frequency under boost operation, the converter features higher power factor. From Figs. 10 and 11 and THD value of $I_{\rm in}$, it is validated that with proposed topology, pure continuous and sinusoidal input current is realized and therefore input filter is unneeded.

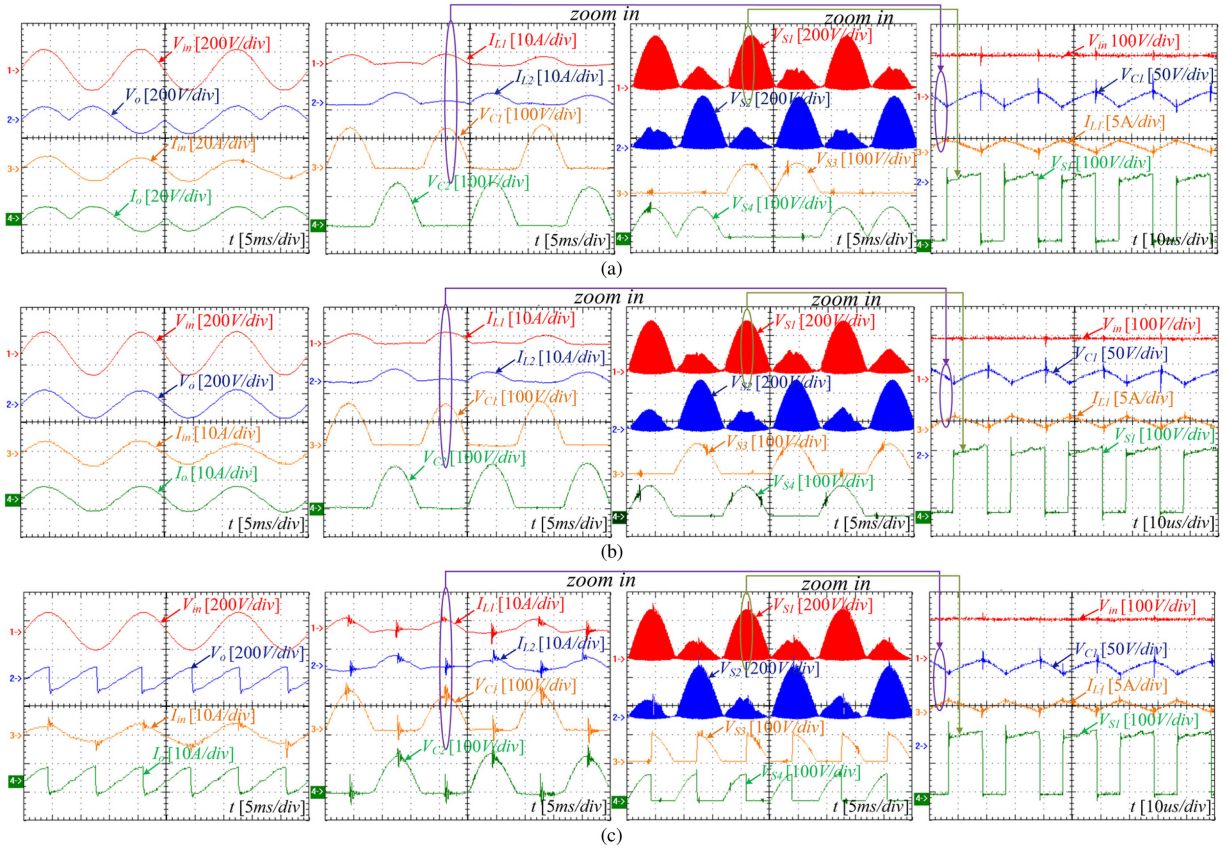

Fig. 10. Waveforms of the proposed converter in buck mode: input and output waveforms ($V_{\rm in}V_{\rm o}I_{\rm in}I_{\rm o}$), current and voltages waveforms on passive components ($I_{L1}I_{L2}V_{C1}V_{C2}$), stressed voltage on switches ($V_{S1}V_{S2}V_{S3}V_{S4}$) and zoomed-in waveforms of inductor current I_{L1}, capacitor voltage V_{C1} and blocked voltage V_{S1} under output frequency of (a) 30 Hz, (b) 60 Hz, and (c) 120 Hz.

Tests on the prototype with *RL* load ($R = 25\ \Omega$, $L = 3.8$ mH) and nonlinear load, which comprises full-bridge diode rectifier with *LC* filter ($L_f = 500\ \mu$H, $C_f = 470\ \mu$F) and 25-Ω resistor, have been implemented. The results are depicted in Figs. 12 and 13, respectively. With *RL* load, output voltage waveform oscillates at step-up frequency mode due to sudden circuit state change at nonzero output voltage. With nonlinear load, the output voltage is slightly distorted since the output impedance is nonzero. Dynamic experiment is also conducted where the load resistor steps from 25 to 12.5 Ω in buck mode and 30-Hz output frequency, as depicted in Fig. 14. Obviously, as the load transients, the proposed converter can also achieve safe commutation successfully, since no voltage spikes appear.

In Fig. 15, measured voltage gain curve as the duty ratio varying from 0.4 to 0.6 is shown in comparison with calculated voltage gain curve. Great agreement is achieved between the measured and calculated results.

The efficiency curves with the output power ranging of 50–200 W at buck ($D = 0.4$) and boost mode ($D = 0.6$) is shown in Fig. 16 comparing to the efficiency of converter in [38]. Here, the efficiency curves are measured at 60 Hz since the efficiency of proposed converter at 30 and 120 Hz would be the same as the efficiency at 60 Hz. The varying frequency operation only changes the direction of output voltage at certain times and direction change of output voltage means change of components set that is conducted, either positive set of components or negative set of components. With the ideally symmetrical circuit structure, the change of components set conducted literally will not influence the energy transfer efficiency.

With low total number of semiconductors utilized and lower switching power loss due to less high-frequency switches, the proposed converter has high efficiency, which is 93.5% in buck mode and 89.7% in boost mode at rated output power of 200 W. Boost mode converter has high efficiency at low duty ratio but buck mode converter at high duty ratio. With output power increasing, the input current (rms value) will increase correspondingly. The inductor loss dominates the total loss and the inductor loss is quadratic relationship with the inductor current. Hence, inductor loss increases more rapidly with the increasing of output power in boost mode. In buck mode, the proposed converter features a lower efficiency at small output power but higher one when the output power is over 170 W compared to converter in [38]. While in boost mode, the proposed converter keeps a higher efficiency at the whole output power range since the inductor current of converter in [38] rises more rapidly with the increase of duty ratio, as can be seen in Table I. More conduction loss is thus caused for converter in [38] than proposed converter.

In Fig. 17, the measured loss distribution of proposed converter in buck and boost mode with calculated results at rated

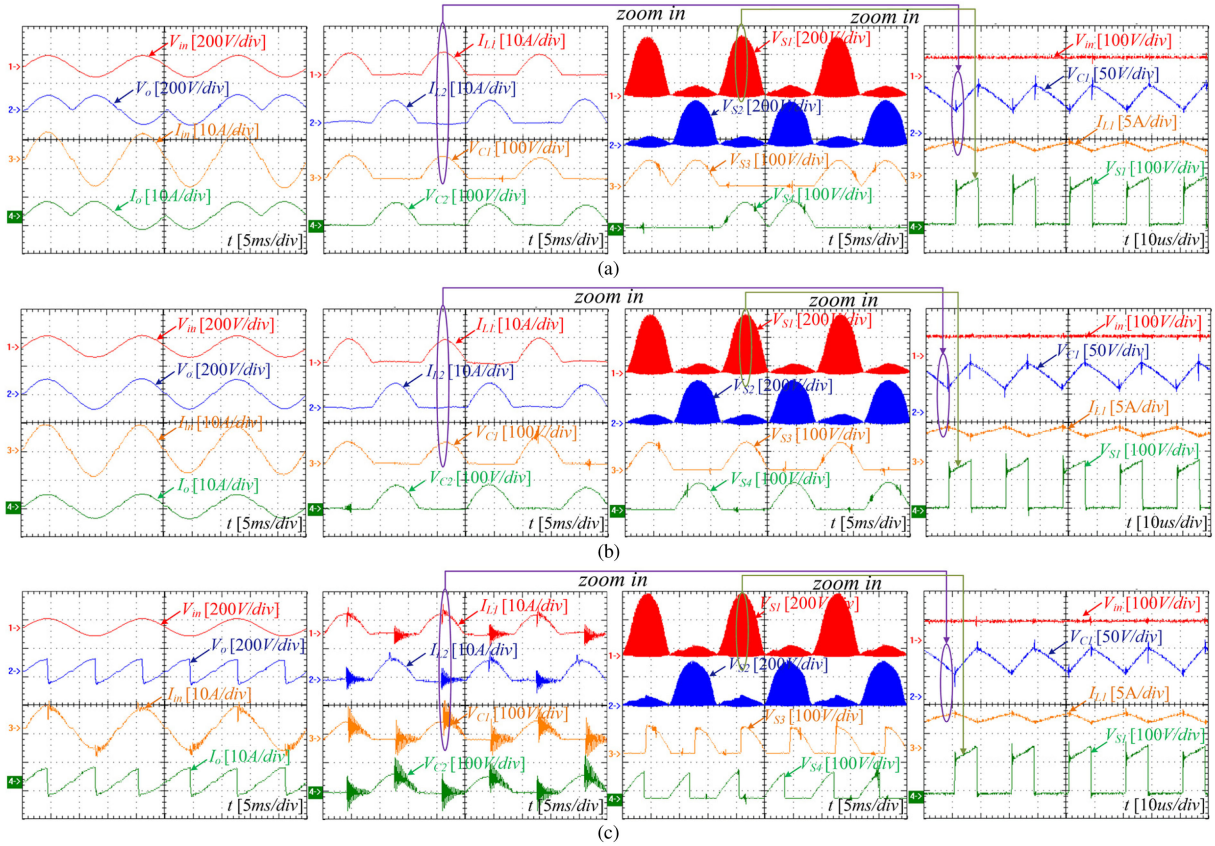

Fig. 11. Waveforms of the proposed converter in boost mode: input and output waveforms ($V_{\rm in}$ $V_{\rm o}$ $I_{\rm in}$ $I_{\rm o}$), current and voltages waveforms on passive components ($I_{L1}I_{L2}V_{C1}V_{C2}$), stressed voltage on switches ($V_{S1}V_{S2}V_{S3}V_{S4}$) and zoom-in waveforms of inductor current I_{L1}, capacitor voltage V_{C1} and blocked voltage V_{S1} under output frequency of (a) 30 Hz, (b) 60 Hz, and (c) 120 Hz.

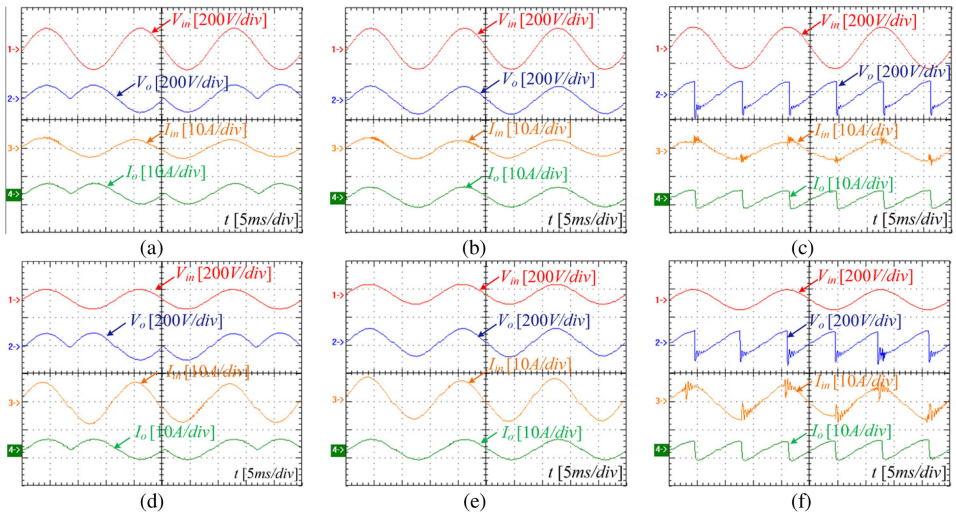

Fig. 12. Waveforms of the prototype with *RL* load in buck operation with output frequency of (a) 30 Hz, (b) 60 Hz, and (c) 120 Hz and in boost operation with output frequency of (d) 30 Hz, (e) 60 Hz, and (f) 120 Hz.

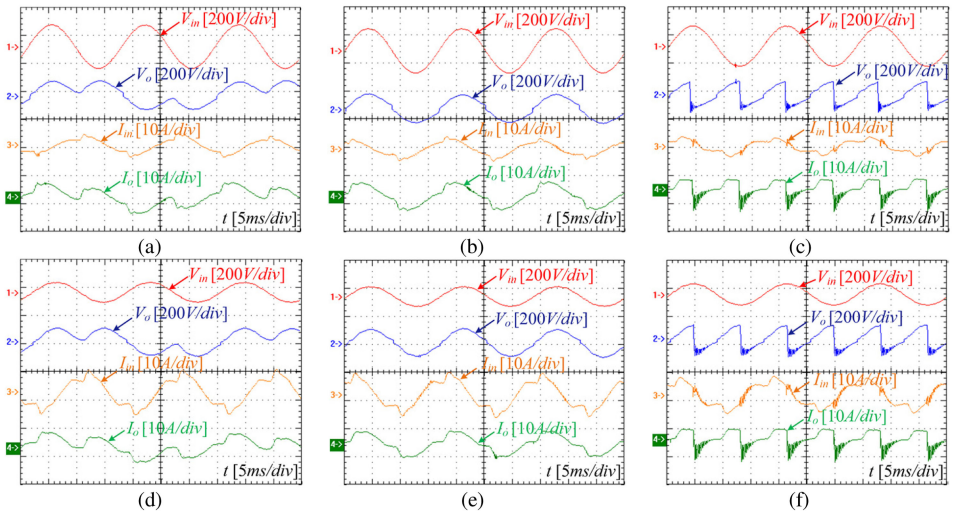

Fig. 13. Waveforms of the prototype with nonlinear load in buck operation with output frequency of (a) 30 Hz, (b) 60 Hz, and (c) 120 Hz and in boost operation with output frequency of (d) 30 Hz, (e) 60 Hz, and (f) 120 Hz.

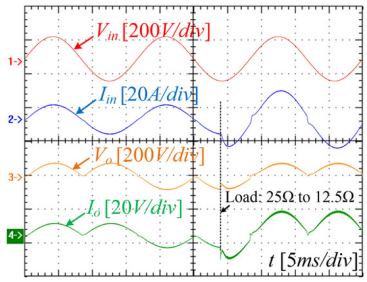

Fig. 14. Input and output waveforms when load steps from 25 to12.5 Ω in buck mode and 30-Hz output frequency.

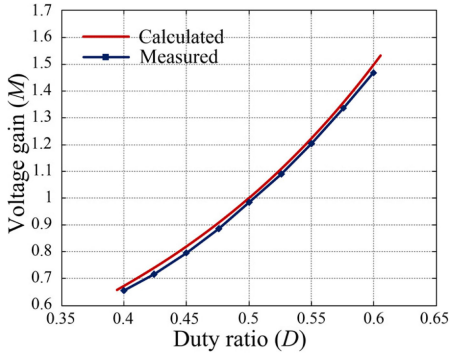

Fig. 15. Measured and calculated voltage gain of proposed converter.

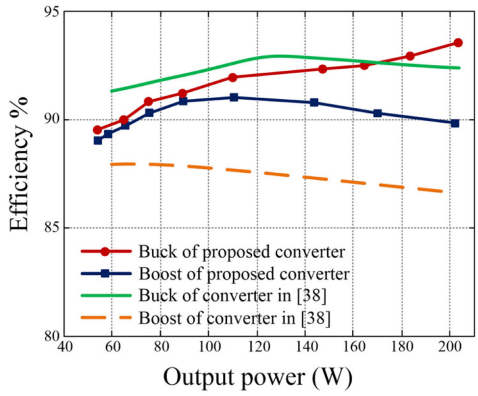

Fig. 16. Efficiency of the proposed converter and converter in [38] against output power.

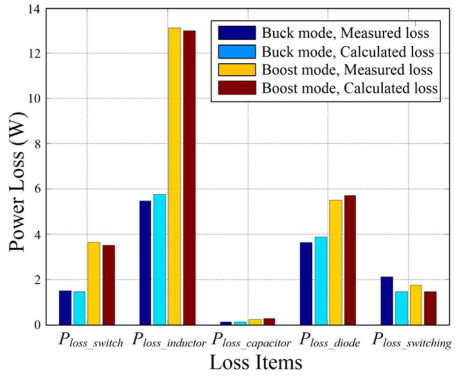

Fig. 17. Power loss distribution of the prototype at rated 200-W output power.

output power 200 W is depicted. Input current in buck mode is smaller than that in boost mode, leading to less amount of power loss. Therefore, in buck mode, the converter features a higher efficiency with a total power loss of 13.1 W while in boost mode, the total power loss is 23.5 W. In both modes, with fixed output power, the inductors contribute most to the conduction loss due to high equivalent series resistance r_L. Conduction loss caused by diodes places second on account of high constant ON-state voltage $V_{\rm F}$. Highest rms current flows through the switches but the conduction loss places only third since devices with low ON-state resistance $r_{\rm on}$ are selected for the prototype. The capacitor loss is low since the ESR of them is

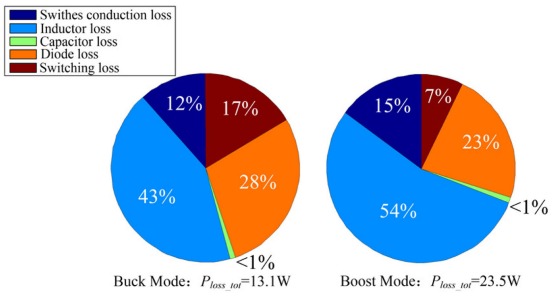

Fig. 18. Proportion of each kind of power loss at buck and boost mode.

very small. Switching loss of the prototype stays at a same level as the duty ratio varies. Proportion of each kind of power loss is further represented in Fig. 18. With low-level input current in buck mode, the diodes loss and switching loss takes very large proportion of total loss, accounting for 45%, as shown in the left pie chart of Fig. 18. In boost mode, the power loss caused by other components rises more rapidly with increased current and takes larger proportion of total power loss, as shown in the right pie chart of Fig. 18.

V. Conclusion

A novel high-efficiency frequency-variable single-phase buck–boost ac–ac converter is proposed in this article. The ac input voltage can be bucked or boosted through the converter with step-changed output frequency. Six switches and total ten semiconductors are employed in the topology, plus only one switch operates at each high-frequency switching period, conduction loss and switching loss can both be considerably decreased, leading to high energy transfer efficiency. The numbers of switches, semiconductors, and high-frequency switches are all at the lowest level among existing works. The control strategy for the proposed converter is simple. With permutation and combination of four typical circuit states, literally arbitrary step-changed output frequency can be realized. Operations of three representative output frequency 30, 60, and 120 Hz are analyzed. Safe-commutation is realized and no extra delicate control strategy or snubber circuit is needed. Proposed converter shows superiority in power density and high-voltage application scenario, especially when operating at boost mode. Moreover, continuous input current helps to remove the bulky input filter, which can further improve the power density. Besides, non-sinusoidal output voltage at varied-frequency mode limits the application of proposed converter and is suitable for applications such as induction heating and motor drivers. With tests on a 200-W prototype, the operation principle, safe commutation peculiarity, high efficiency, and continuous input current are confirmed.

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Liangzong He (Member, IEEE) was born in Hunan, China, in 1984. He received the B.Sc. degree from Jilin University, Changchun, China, in 2006, and the Ph.D. degree from the Huazhong University of Science and Technology, Wuhan, China, in 2012.

From November 2009 to August 2011, he was a Joint Ph.D. Education Student with Michigan State University, East Lansing, MI, USA. In September 2012, he joined Xiamen University, Xiamen, China, as an Assistant Professor, where he has been a Professor since August 2019. His research interests include dc–dc converters, switched-capacitor converters, Z-source converters, wireless power transmission, and microgrids.

Xinyong Xu was born in Zhejiang Province, China, in 1995. He received the B.Sc. degree, in 2017, from Xiamen University, Xiamen, China, where he is currently working toward the master's degree with the Department of Electrical Engineering.

His research interests include switched-capacitor dc–dc converters and renewable energy generation.