Nonlinear Compact Thermal Model of the IGBT Dedicated to SPICE

Krzysztof Górecki, *Senior Member, IEEE*, and Paweł Górecki, *Member, IEEE*

***Abstract*—In this article, the problem of modeling the thermal properties of the IGBT using a nonlinear compact thermal model is considered. This model has the form of an electrical network. In the proposed model, the influence of the internal temperature of this transistor on the efficiency of heat dissipation is taken into account. The elaborated model form is presented and the estimation method of this model parameters is described. The correctness of the new model is verified experimentally for different cooling conditions and different values of ambient temperature. Additionally, some results of calculations are compared to the results of calculations performed using selected models given in the literature.**

***Index Terms*—Insulated gate bipolar transistors, modeling, semiconductor device modeling, thermal management, thermal resistance.**

I. Introduction

INSULATED gate bipolar transistors (IGBTs) are very often used in modern power electronic circuits as electronic switches [1]–[5]. During the operation of these transistors, as in other such semiconductor devices, a self-heating phenomenon is observed. This phenomenon is caused by the conversion of power dissipated in the considered device into heat at non-ideal cooling conditions. As a result of self-heating an increase of internal temperature of these devices is observed [6]–[12], which may even exceed the maximum allowable value of this temperature given in the datasheet. Such a high value of the device internal temperature could cause changes in the course of characteristics of these devices [6], [7], [12]–[18] and shorten their life time [16], [19]–[21].

A very important step in designing electronic networks is a computer simulation. In such simulation, dedicated software for the analysis of electronic circuits, e.g., SPICE or PLECS, is commonly used [2], [3], [22]–[29]. On the other hand, in order to calculate the internal temperature of electronic devices their thermal model is indispensable. Such a kind of model makes it possible to calculate the value or the waveform of internal temperature of the considered semiconductor device at the well-known waveform of power dissipated in it [8], [13], [30]–[35].

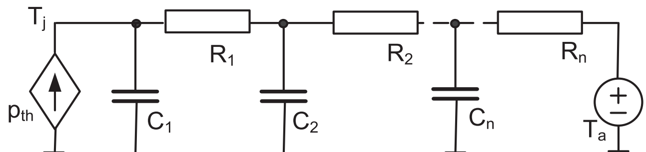

Fig. 1. Cauer structure of a compact thermal model.

Thermal models of electronic devices can be formulated in two forms. There are 2-D and 3-D models [35]–[38] or compact models [30], [34], [39], [40]. Two-dimensional and 3-D thermal models make it possible to calculate the time-spatial temperature distribution in semiconductor devices [41], [42], whereas in compact models uniform temperature distribution is assumed and only one value of the internal temperature of such devices is used [30], [34].

The 2-D and 3-D thermal models have complicated forms and they are formulated for a chip of semiconductor devices only. Therefore, they are typically used by designers of semiconductor devices, who require detailed information about the time-spatial temperature distribution of the device structure. In contrast, designers of electronic circuits typically use compact thermal models, which provide information about one internal temperature of the device structure in a relatively short time. In order to shorten time indispensable to obtain the results of calculations linear thermal models of electronic components, whose parameters have fixed values, are used [7], [9], [10], [15], [30]. These models can be expressed by analytical equations or they have the form of an electrical network, which uses an electro-thermal analogy. In this analogy, voltage corresponds to temperature, current—to electrical power and RC networks—to the transient thermal impedance of the modeled devices.

Compact thermal models of semiconductor devices [13], [30], [31], [43], [44] make it possible to calculate the internal temperature of such devices and they typically have the form of the RC Cauer network [3], [7], [8], [30], [39] shown in Fig. 1.

As it is visible, the RC elements used in the presented structure are linear, which means that they have a constant value.

In turn, as it is commonly known, the heat generated inside semiconductor devices can be removed to the surroundings using three mechanisms: conduction, convection, and radiation. As it is known, e.g., from [39], [43], [45], and [46], efficiency of all mechanisms nonlinearly depends on temperature [31], [39], [43], [47] and on the cooling system used [33], [43], [48]. For

Manuscript received February 3, 2020; revised April 1, 2020; accepted May 14, 2020. Date of publication May 17, 2020; date of current version July 31, 2020. This work was supported by the Polish Science Budget Resources under Program “Diamentowy Grant” and in part by the Ministry of Science and Higher Education Program “Regionalna Inicjatywa Doskonałości” under Project 006/RID/2018/19. Recommended for publication by Associate Editor D. G. Lamar. *(Corresponding author: Krzysztof Górecki.)*

Krzysztof Górecki is with the Department of Marine Electronics, Gdynia Maritime University 81-225, Gdynia, Poland (e-mail: gorecki@am.gdynia.pl).

Paweł Górecki is with the Gdynia Maritime University 81-225, Gdynia, Poland (e-mail: p.gorecki@we.umg.edu.pl).

Color versions of one or more of the figures in this article are available online at https://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2020.2995414

example, the efficiency of conduction decreases with an increase in the difference between the device internal temperature and temperature of its case. In turn, the efficiency of convection increases when the difference between the case temperature and ambient temperature increases. Finally, the efficiency of radiation increases with an increase in the case temperature [33], [39]. Also, in the articles [31]–[33], [47], [49], [50], it was shown that the device thermal resistance depends on power dissipated in this device.

In order to take into account the influence of the mentioned dependence, the use of a nonlinear thermal model is indispensable [31], [33], [50]. In such a kind of model dependence of efficiency of heat removal on dissipated power is taken into account. For example, in the article by Górecki and Zarębski [31], a nonlinear compact thermal model of semiconductor devices is proposed. In the considered model, based on the linear Cauer network, dependencies of thermal resistances and thermal capacitances of the heat transfer path elements depend on dissipated power [39]. Unfortunately, the description of these dependencies is very complex and it is a result of experimental results approximation with the sum of exponential functions.

In the article by Górecki and Zarębski [32], it was shown that in the nonlinear thermal model of the IGBT, thermal capacitances very weakly depend on dissipated power and neglecting this dependence does not result in worsening accuracy of the thermal model.

Nonlinear compact thermal models of semiconductor devices described in [31] and [32] take into account the only influence of dissipated power on the efficiency of heat removal generated in these devices. Meanwhile, the efficiency of physical phenomena deciding about heat removal depends not on dissipated power, but on the value of the device internal temperature and ambient temperature. Because of thermal inertia (caused by thermal capacitances) changes in the values of the device internal temperature cannot be so fast as changes in the values of dissipated power. Therefore, nonlinear compact thermal models using the dependence of thermal resistance on dissipated power can be used only in the situation, when the waveform of this power has the shape of the Heaviside step and ambient temperature has the fixed value, for which this model was formulated. For other shapes of the dissipated power waveform differences between the measured and calculated values of the device, the internal temperature can exceed even 20 K [32], [33].

It is visible that a very important problem is to formulate a nonlinear compact thermal model of the IGBT which takes into account the influence of changes of the device internal temperature and ambient temperature on the efficiency of the heat removal dissipated in this device.

In this article, which is an extended version of the conference paper [33], a new form of the nonlinear compact thermal model of the IGBT is proposed. This model takes into account the influence of the device internal temperature and ambient temperature on the efficiency of the device cooling. The new model characterizes the efficiency of heat transfer between the semiconductor chip and the surroundings taking into account all the mechanisms of heat transfer. The form of the elaborated model is presented with the adequate formulas, the method of model parameters estimation is described and the results of the model experimental verification for selected transistors are shown. This verification is performed for different cooling conditions of the tested transistor in a wide range of ambient temperature values and dissipated power values.

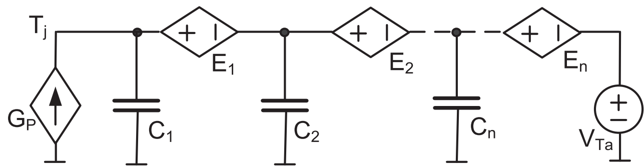

Fig. 2. Network form of the nonlinear thermal model of the IGBT.

II. Form of the Model

The proposed nonlinear compact thermal model of the IGBT has the form of an electrical network and it is dedicated to the SPICE software. In this model, all mechanisms and all paths of heat transfer between the semiconductor structure and the surroundings are taken into account. The dependence of thermal resistance of the heat flow path components on their temperature is proposed. The network form of this model is shown in Fig. 2.

The structure of the proposed model is based on the classical linear Cauer RC thermal model, but the influence of the internal device temperature and ambient temperature on thermal resistances existing in the heat flow path from the semiconductor structure to the surroundings is taken into account. This structure is an electrical analog of the heat transfer equation [30].

In this model, the device internal temperature is equal to voltage in node T_j, whereas ambient temperature T_a is modeled by voltage source V_{Ta}. The values of temperatures of particular components of the heat flow path (semiconductor chip, mounting base, case, heat-sink, PCB, etc.) are represented by voltages in particular nodes. The power dissipated in the device is described by the controlled current source GP, whereas temperature differences between each element of the heat flow path are represented by controlled voltage sources $E_1, E_2, \ldots, E_n$.

Equations describing values of the mentioned voltage sources present dependencies of thermal resistance between the considered components of the heat flow path on the device internal temperature. Thermal capacitances of these elements are represented by capacitors $C_1, C_2, \ldots C_n$.

The values of thermal capacitances of particular heat flow path components depend on density, specific heat, and volume of particular heat flow path components [39]. Such parameters slightly depend on temperature. Therefore, in the model constant values of thermal capacitances are used. These values for different types of the considered transistors depend on the volume of particular heat flow path components and on materials used to construct such components. In turn, the output value of each controlled voltage source E_i is described with the following equation:

$$E_i = d_i \cdot i_{Ei} \cdot \begin{pmatrix} R_{\mathrm{th1}} \cdot (1-a\cdot(T_a - T_0)) \cdot \exp\left(-(T_j - T_a)/T_z\right) \\ + R_{\mathrm{th0}} \cdot (1 - b\cdot(T_a - T_0)) \end{pmatrix}. \quad (1)$$

In (1), d_i is the quotient of thermal resistance of *i*th element of the heat flow path and the device thermal resistance $R_{\rm th}$, whereas i_{Ei} is current of source E_i. $R_{\rm th0}$ represents the minimum value of thermal resistance at an ambient temperature equal to reference temperature T_0. $R_{\rm th1}$ denotes the maximum change in the value of thermal resistance while changing the value of the device internal temperature and $T_a = T_0$. Coefficients *a* and *b* describe the influence of ambient temperature on thermal resistance, whereas T_z determines the slope of dependence $R_{\rm th}(T_j)$.

The presented form of (1) is formulated by the authors on the basis of the described in literature [45] dependencies of heat flux on the gradient of temperature (heat conduction), on differences between the temperature of the cooled surface and temperature of cooling fluid (heat convection) and on absolute temperature (heat radiation). The measured dependencies of thermal resistance of semiconductor devices on dissipated power presented in literature [31]–[34], [43], [46], [51] are also taken into account.

In comparison to the article [32], the influence of the device internal temperature T_j instead of dissipated power on the device thermal resistance is taken into account. In turn, in comparison to the article [33], the influence of ambient temperature on the device thermal resistance is additionally taken into account. The form of (1) is proposed by the authors basing on the results of many measurements of transient thermal impedance waveforms corresponding to different types of the IGBT operating at different cooling conditions and different values of the device internal temperature and ambient temperature.

Analyzing the form of (1), it is visible that thermal resistance decreases when the difference between the device internal temperature and ambient temperature increases. Such a character of the considered dependence correlates with the measurement results of semiconductor devices thermal resistance on dissipated power presented in the literature [32]–[34], [39], [43]. In the cited articles, it is shown that the difference between internal temperature and ambient temperature is proportional to dissipated power. It is also visible that an increase in ambient temperature causes an increase in the device thermal resistance. Additionally, it is well known that convection is a mechanism deciding about the efficiency of heat removal generated in these devices. The efficiency of convection is proportional to the difference between the device case temperature and ambient temperature [39]. The efficiency of heat radiation also increases with an increase in the device internal temperature [39].

III. Estimation of Model Parameters

In order to estimate values of parameters existing in the proposed model, waveforms of transient thermal impedance $Z_{\rm th}(t)$ measured at different values of power dissipated in the tested transistor and different values of ambient temperature are needed.

These measurements could be performed with the use of an indirect electrical method using a cooling curve [32], [52]. In literature, e.g., [53]–[56], the problem of selecting a proper thermally sensitive parameter of IGBTs is considered. In the article by Dupont *et al.* [55], it is shown that using such thermally sensitive parameters as gate-emitter voltage, collector-emitter voltage or saturation current, the same accuracy of measurements of the IGBT internal temperature as for the infrared method can be obtained. In the article by Dupont and Avenas [54], it is shown that using thermo-sensitive parameters internal temperature of the IGBT can be measured with the error not higher than 10 °C. Of course, typically this error is much smaller and does not exceed several Celsius degrees [51]. In the article by Górecki *et al.* [34], set-ups to measure the transient thermal impedance of the IGBT using gate-emitter voltage or forward voltage of the reverse diode as thermally sensitive parameters are discussed.

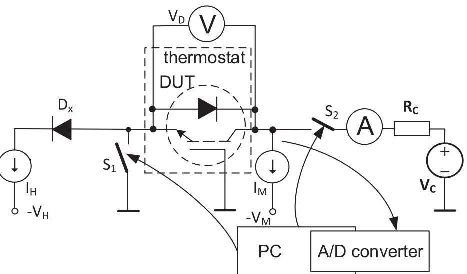

Fig. 3. Block diagram of the used measurement setup.

In the method used in this article, the forward voltage of the reverse diode is used as a thermally sensitive parameter [44], [51]. This method is realized in the measurement setup of the block diagram shown in Fig. 3.

In this measurement setup, the following components appear: the measured transistor (DUT) situated in the thermostat, two current sources I_H and I_M, voltage source V_C, resistor R_C, the ammeter, the voltmeter, switches S_1 and S_2, diode D_x, the analogue-to-digital (A/D) converter and the PC. Both the switches are made with the use of power MOSFETs. Diode D_x protects current source I_H against shortening when switch S_1 is closed. The used A/D converter contains a measurement amplifier that makes it possible to obtain a resolution of voltage drop measurements on the reverse diode equal to 0.2 mV. This resolution corresponds to the resolution of the measurement of device internal temperature equal to about 0.15 °C.

The considered measurements are performed in four steps. In the first step, thermometric characteristics $V_D(T)$ describing the dependence of the freewheeling diode (build-in in the tested transistor) forward voltage on temperature are measured at a fixed, small value of forward current I_M. The problem of selecting the proper value of this current is considered in the article by Zarębski and Górecki [57]. In this step, switch S_1 is closed and switch S_2 is opened. The thermostat makes it possible to regulate values of temperature *T*. After this step, the slope α_V of thermometric characteristic $V_D(T)$ is calculated.

In the second step, switch S_1 is opened and switch S_2 is closed. Power is dissipated in the tested device operating in the active range. This power is equal to the product of voltage $V_{\rm CE}$ between the collector and the emitter of the tested transistor and heating current I_H. The internal temperature of this transistor increases as a result of selfheating until the steady-state is obtained. Values of $V_{\rm CE}$ voltage are measured at the steady state.

The third step starts at time $t = 0$, when switch S_1 is closed and switch S_2 is opened. In this step, the tested transistor is cooled and the analogue-to-digital converter with the PC registered waveform of voltage $V_D(t)$ is registered until the steady-state is obtained. Finally, transient thermal impedance $Z_{\rm th}(t)$ is calculated according to the following formula [33]:

$$Z_{\rm th}\left(t\right) = \frac{V_D\left(t\right) - V_D\left(t = 0\right)}{\alpha_V \cdot I_H \cdot V_{\rm CE}}. \tag{2}$$

Due to the fact that in this method a cooling curve is used, it is possible to obtain the shape of dissipated power in the form of a step.

The measured waveform of $Z_{\rm th}(t)$ can be approximated by the following equation [13], [30], [31], [43]:

$$Z_{\rm th}\left(t\right) = R_{\rm th} \cdot \left(1 - \sum_{i=1}^{N} a_i \cdot \exp\left(-\frac{t}{\tau_{\rm thi}}\right)\right). \tag{3}$$

In (3), $R_{\rm th}$ denotes thermal resistance, N is the number of thermal time constants $\tau_{\rm thi}$, whereas a_i are coefficients of the sum equal to 1.

With the use of the measured waveforms of $Z_{\rm th}(t)$ obtained at different values of dissipated power and different values of ambient temperature fixed by the thermostat, values of parameters $R_{\rm th}$, N, a_i, and $\tau_{\rm thi}$ existing in (3) are estimated with the algorithm described in the article by Górecki *et al*. [39]. Next, values of thermal resistances R_i and thermal capacitances C_i existing in the Cauer network are calculated using the method described in the article by Górecki *et al*. [39] separately for each result of measurements.

Values of thermal capacitances C_i used in the thermal model are equal to the average values of the considered capacitances estimated at all the measured values of dissipated power and ambient temperature. Parameters d_i values are equal to the quotient of resistance R_i and thermal resistance corresponding to the highest values of power dissipated in the tested device.

The value of temperature T_j is calculated as the sum of ambient temperature and the product of the measured value thermal resistance and dissipated power, at which this value of $R_{\rm th}$ was measured. Then, coefficients R_{th1}, R_{th0}, d_i, and T_0, T_Z, a, b describing dependencies of each thermal resistance on the transistor internal temperature are estimated by matching the obtained dependencies $R_{\rm th}(T_j, T_a)$ with the following equation:

$$\begin{aligned} R_{\rm th} = {} & R_{\rm th1} \cdot \left(1 - a \cdot \left(T_a - T_0\right)\right) \cdot \exp\left(-\left(T_j - T_a\right)/T_z\right) \\ & + R_{\rm th0} \cdot \left(1 - b \cdot \left(T_a - T_0\right)\right). \end{aligned} \tag{4}$$

At first, using the measurements results obtained at $T_a = T_0$ the value of parameter R_{th0} is estimated as the minimum value of $R_{\rm th}$. Next, values of $R_{\rm th1}$ and T_z are estimated using the least-squares method for the dependence of the form

$$\ln\left(R_{\rm th} - R_{\rm th0}\right) = \ln\left(R_{\rm th1}\right) - \left(T_j - T_a\right)/T_z. \tag{5}$$

The value of parameter b is calculated using the lowest values of $R_{\rm th}$ obtained at two values of ambient temperature T_{a1} and T_{a2}. Finally, the value of parameter a is estimated using the previously estimated parameters and the measured values of $R_{\rm th}$ at two different values of ambient temperature.

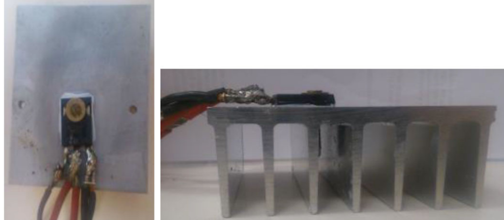

Fig. 4. View of the tested transistor mounted on the heat-sink.

TABLE I
PARAMETERS VALUES OF THE NONLINEAR THERMAL MODEL OF THE IRG4PC40UD TRANSISTOR

Parameters	Transistor situated on the heat-sink	Transistor operating without any heat-sink
C_1 [J/K]	0.25	0.05
C_2 [J/K]	240.2	3.21
C_3 [J/K]	553.75	27.745
d_1	0.09	0.19
d_2	0.488	0.488
d_3	0.422	0.322
a	5.6×10^{-3}	2.4×10^{-3}
b	-5.7×10^{-3}	2.4×10^{-3}
R_{th0} [K/W]	2.57	20.73
R_{th1} [K/W]	1.62	11.35
T_Z [K]	48	48
T_0 [K]	298	298

IV. INVESTIGATION RESULTS

Using the measurement method described in the previous section, waveforms of the transient thermal impedance of the IRG4PC40UD transistor by International Rectifier operating at different cooling conditions are measured for different values of dissipated power at different values of ambient temperature. The tested transistor is situated in the case TO-247 [58].

The considered transistor includes two semiconductor chips in the common case. The first is an IGBT and the other is a diode. The distance between these chips is very small. Therefore, the difference between temperatures of these structures is negligibly small and the measurement method described in Section III can be used. Of course, the values of the device internal temperature obtained with this method correspond to the internal temperature of the diode.

Two kinds of cooling conditions of this transistor are considered: operation without any heat-sink and operation with the heat-sink, on which this transistor is mounted. In Fig. 4, a view of the tested transistor mounted on the heat-sink is shown. As it is visible, the tested transistor is connected to the other parts of the measurement systems with the use of typical laboratory wires with the cross-section equal to 1.5 mm^2. It is the proper value of the mentioned parameter for the transistor of the maximum allowable collector current equal to 40 A [58].

Investigations were performed for the transistor situated in the thermostat of volume equal to 60 dm^3. On the basis of the performed measurements, the values of model parameters were obtained. In Table I, the values of model parameters corresponding to the transistor situated in the thermostat and operating at different cooling conditions are collected. These

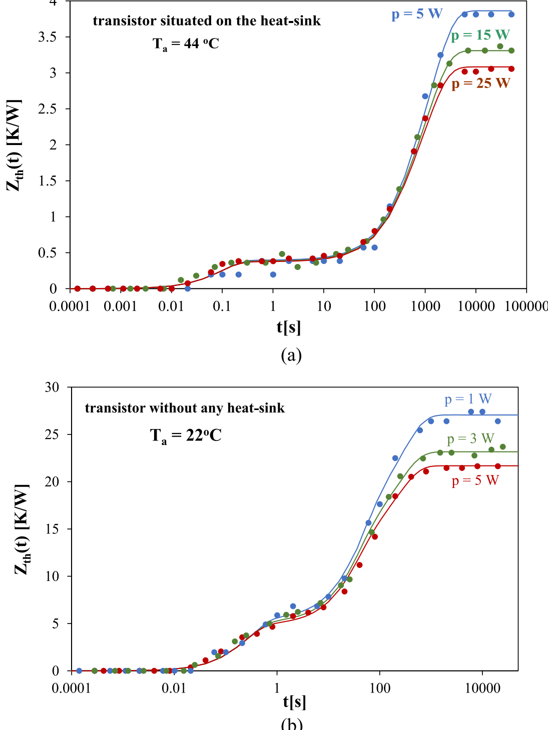

Fig. 5. Measured (points) and calculated (lines) waveforms of the transient thermal impedance of the IRG4PC40UD transistor: (a) situated on the heat-sink, (b) operating without any heat-sink at different values of dissipated power and the fixed value of ambient temperature.

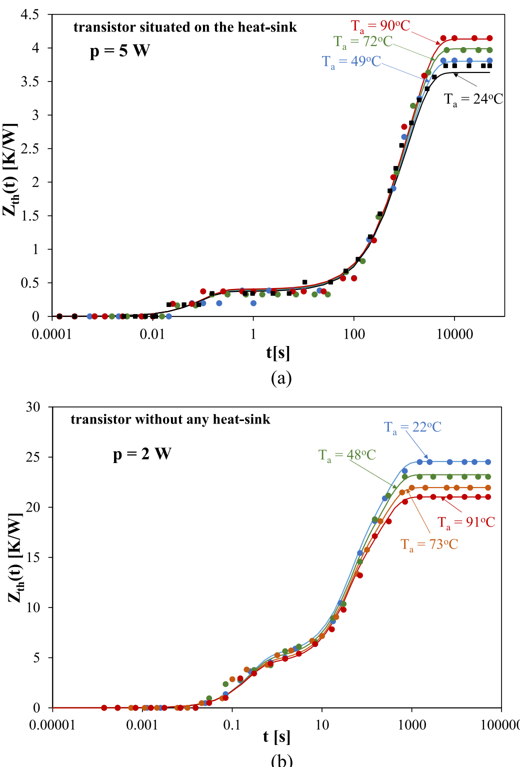

Fig. 6. Measured (points) and calculated (lines) waveforms of the transient thermal impedance of the IRG4PC40UD transistor: (a) situated on the heat-sink, (b) operating without any heat-sink at different values of ambient temperature and the fixed value of dissipated power.

values are obtained using the estimation method described in Section III.

Analyzing this table, it is easy to notice that parameter values that correspond to both kinds of the considered cooling conditions for the tested transistor considerably differ from each other. For example, the minimum value of thermal resistance $R_{\mathrm{th}1}$ in the transistor operating without any heat-sink is even seven times higher than the value of this parameter for the same transistor situated on the heat-sink. For both kinds of the considered cooling conditions, three capacitors C_i exist in the thermal model, but the biggest value of thermal capacitance used to describe the thermal properties of the transistor situated on the heat-sink is even over twenty times higher than for this transistor operating without any heat-sink. This is a result of a big difference between volumes of the used heat-sink and the case of the tested transistor.

It is also worth noticing that the coefficient d_1 is twice bigger for the transistor situated on the heat-sink than for the transistor operating without any heat-sink because in the second case the shortest thermal time constant plays a bigger role than in the first case.

In order to show the usefulness of the presented thermal model for accurate approximation of the measurement waveforms of the IGBT transient thermal impedances, the results of the calculation performed with the proposed model (lines) are compared to the measurements results (points) and shown in Figs. 5 and 6. Fig. 5 illustrates the influence of power dissipated in the tested device on waveforms of $Z_{\mathrm{th}}(t)$, whereas Fig. 6 illustrates the influence of ambient temperature on such waveforms. The results presented in Figs. 5(a) and 6(a) correspond to the transistor situated on the heat-sink, whereas the results presented in Figs. 5(b) and 6(b)—to the transistor operating without any heat-sink.

As shown in Fig. 5, the results of calculations and measurements obtained for all the considered values of dissipated power and ambient temperature at both kinds of the considered cooling conditions of the tested transistor differ very little between each other. This good agreement proves the correctness of the proposed model. Additionally, it is worth observing that it is possible to correctly model the influence of the device internal temperature on transient thermal impedance waveforms taking into account the only influence of this temperature on thermal resistance. Of course, the significant influence of the used cooling conditions on thermal capacitances existing in the proposed model is also visible.

Comparing the results presented in Fig. 5(a) and (b), it is worth observing that thermal resistance is a decreasing function of dissipated power. For the transistor operating without any heat sink, the thermal resistance value decreases by even 25% at an increase in the dissipated power value from 1 to 5 W, whereas for the transistor situated on the heat-sink this decrease is equal to about 25% at an increase in dissipated power from 5 to 25 W. The observed big changes in the thermal resistance value justify the use of the considered IGBT nonlinear thermal model.

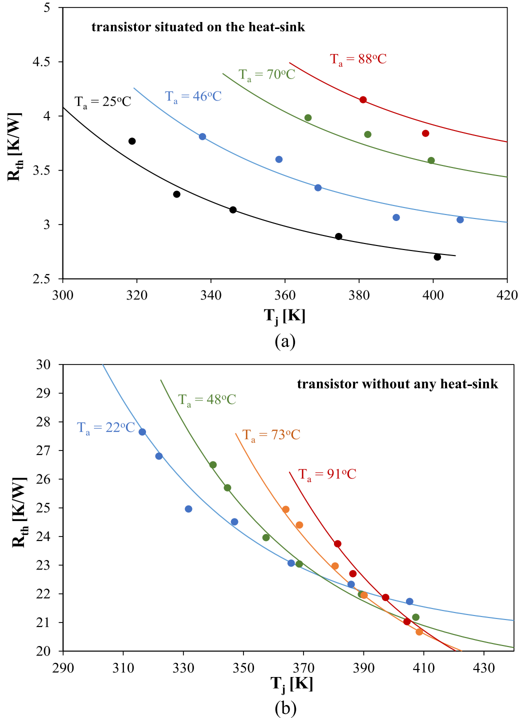

Fig. 7. Measured (points) and calculated (lines) dependencies of thermal resistance of the considered transistor situated on the heat-sink (a) or operating without any heat-sink (b) on the device internal temperature for selected values of ambient temperature.

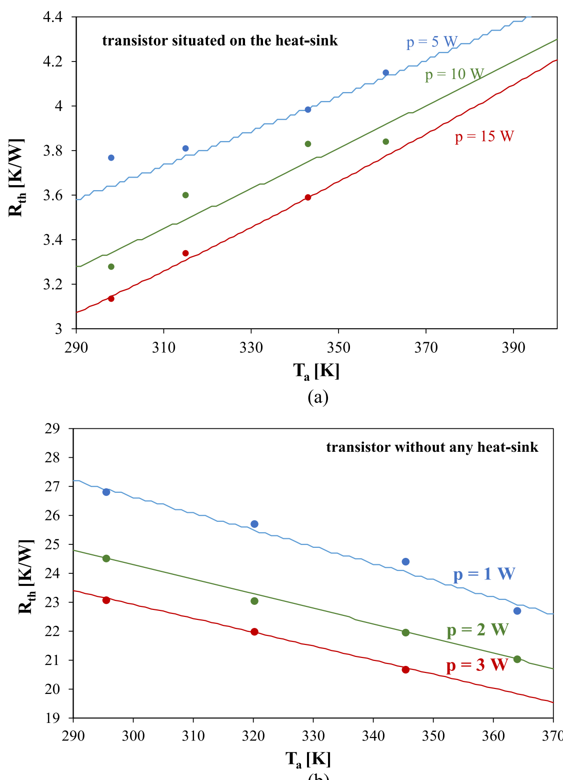

Fig. 8. Measured dependencies of the device thermal resistance on ambient temperature for selected values of dissipated power in the transistor situated on (a) the heat-sink and (b) operating without any heat-sink.

In Fig. 6, it is easy to observe that changes in the value of ambient temperature can visibly influence waveforms of $Z_{\mathrm{th}}(t)$. At the same value of dissipated power, an increase in the value of ambient temperature causes an increase in the value of $Z_{\mathrm{th}}(t)$ at the steady-state for the transistor situated on the heat-sink and a decrease in this value for the transistor operating without any heat-sink. In the considered range of ambient temperature changes and fixed values of dissipated power the value of $Z_{\mathrm{th}}(t)$ at the steady-state changes from about 10% for the transistor situated on the heat-sink to even 20% for the transistor operating without any heat-sink.

In Fig. 7, the measured (points) and calculated (lines) dependencies of the tested transistor thermal resistance on the device internal temperature for selected values of ambient temperature are shown. The results presented in Fig. 7(a) correspond to the transistor situated on the heat-sink, whereas the results presented in Fig. 7(b) correspond to the transistor operating without any heat-sink. The device internal temperature value is equal to the sum of ambient temperature T_a and the product of dissipated power and thermal resistance.

As can be seen, for both situations, the transistor situated on the heat-sink and the transistor operating without its dependence $R_{\mathrm{th}}(T_j)$ is a decreasing function. In the considered range of changes in the device internal temperature, the value of thermal resistance decreases even by 30% for the transistor operating without any heat-sink and even by 25% for the transistor situated on the heat-sink. It is worth noticing that the cooling conditions of the tested transistor improve when the device internal temperature increases. In this situation, smaller values of thermal resistance are obtained. Using the proposed in this article, an analytical description of the dependence $R_{\mathrm{th}}(T_j)$ good agreement between the results of measurements and calculations is obtained.

In turn, Fig. 8 illustrates the dependencies of the device thermal resistance on ambient temperature for fixed values of dissipated power p.

It is clearly visible that dependence $R_{\mathrm{th}}(T_a)$ is nearly linear and curves obtained for different values of dissipated power are practically parallel. This dependence slope is positive for the transistor situated on the heat-sink [see Fig. 8(a)] and negative for the transistor operating without any heat-sink [Fig. 8(b)]. This difference in the sign of the considered dependence slope is connected with a different mechanism of heat dissipation, which dominates in the considered cooling conditions. This is heat conduction—for the transistor situated on the heat-sink and convection—for the transistor operating without any heat-sink. It is worth noticing that for all the considered cooling conditions and all the used values of dissipated power and ambient temperature, good agreement between the measurement results and modeling is obtained. It proves the correctness of the proposed model. The observed in Fig. 8(a) differences in the measured and calculated values of thermal resistance for power $p = 10$ W differ from one other no more than 3%. It could be a result of the measurement error connected with fluctuations of ambient temperature during measurements.

In order to show the practical usefulness of the elaborated nonlinear thermal model, some calculations and measurements are performed. In Fig. 9, the measured and calculated waveforms

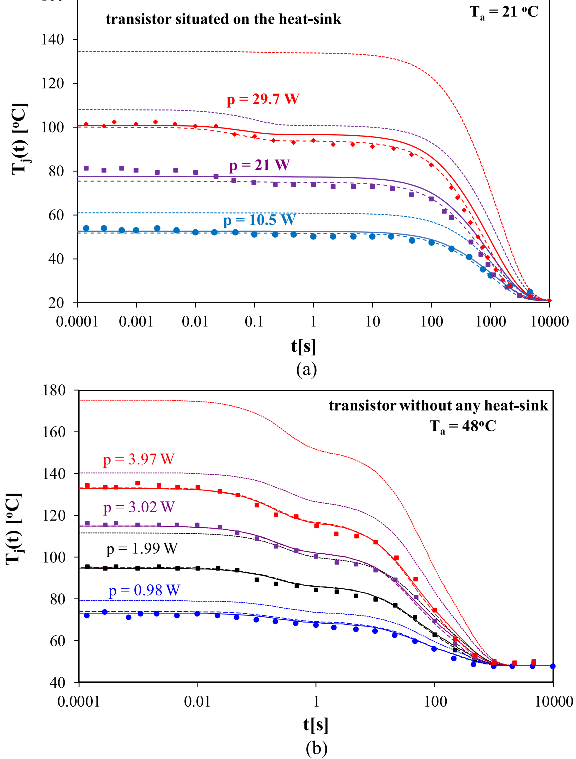

Fig. 9. Calculated (lines) and measured (points) waveforms of internal temperature of the IRG4PC40UD transistor when it is cooled for (a) the transistor operating without any heat-sink, and (b) the transistor situated on the heat-sink.

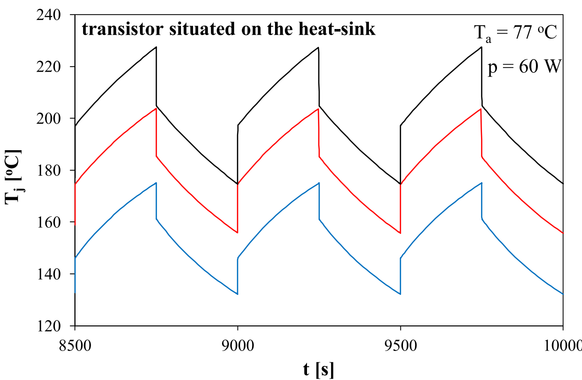

Fig. 10. Calculated waveforms of internal temperature of the IRG4PC40UD transistor stimulated by power of a rectangular pulses train for the transistor situated on the heat-sink.

of the internal temperature of the IRG4PC40UD transistor operating at different cooling conditions while being cooled are presented. These results correspond to different values of power dissipated in the considered transistor before starting the cooling process and to selected values of ambient temperature. In this figure, the results of calculations performed with the proposed nonlinear thermal model, as mentioned in this article, are marked with solid lines, whereas the results of measurements - with points. Additionally, dashed lines denote waveforms of the device internal temperature calculated with the model given in the article by Górecki and Górecki [32], whereas dotted lines—the results obtained with the classical linear thermal model. For the linear thermal model values of RC elements existing in the Cauer network are estimated for dissipated power equal to zero and the smallest value of ambient temperature (separately for the transistor situated on the heat-sink and for the transistor operating without any heat-sink).

As it is visible, both the considered nonlinear thermal models assure good agreement between the calculations and measurement results, while for the linear model the obtained results of calculations overstate the measurement results. For higher values of dissipated power, differences in the results of calculations and measurements are even over 40 °C. This justifies the use of a nonlinear thermal model of the IGBT.

The calculations results presented in Fig. 9 and obtained using both the considered versions of nonlinear thermal models are nearly the same. This is a result of the considered transistor stimulation by the power of the Heaviside step shape. In order to show the differences in the results of calculations of the IGBT internal temperature obtained using these models, in Fig. 10, the calculated waveforms of their internal temperature at the thermally steady state are shown. The tested transistor situated on the heat sink is stimulated by the power of the shape of a rectangular pulses train of frequency equal to 2 mHz and the duty cycle equal to 0.5. These conditions correspond to the tested transistor operation as a switch with a resistive load. The amplitude of these pulses is equal to 60 W. Calculations are performed at ambient temperature T_a equal to 77 °C. In this figure, red lines denote the results of calculations using the new nonlinear thermal model, blue lines—the results of calculations using the nonlinear thermal model described in [32], whereas black lines—the results of calculations using the linear thermal model.

As it can be observed, differences between the results of calculations obtained using both the nonlinear thermal models exceed even 30 °C. Using the nonlinear thermal model given in the article by Górecki and Górecki [32] the obtained results of the device internal temperature are underestimated. This could result in inappropriate design of the cooling system and short life time of the tested device. In turn, using the linear thermal model we could obtain overestimated values of the device internal temperature and have unjustifiably high costs of the cooling system.

For the considered transistor operating as a switch with resistive load at frequency typical for power electronic circuits, the shape of the waveform of the device internal temperature at the steady-state is nearly constant. Using the considered models, values of such temperature at the steady-state for the transistor situated on the heat-sink were calculated. For ambient temperature equal to 77 °C, frequency equal to 20 kHz, the duty cycle equal to 0.5, and amplitude of power equal to 60 W, we obtained the following values of the device internal temperature at the steady-state, for the new model this temperature was equal to 181 °C, for the model given in [32]—154.5 °C, whereas for the linear thermal model—202.5 °C. The observed differences between the obtained values of the considered temperature show that the use of the IGBT compact thermal model proposed in this article can make it possible to most accurately estimate this

temperature and consequently properties of the analyzed power electronic circuits.

Additionally, we performed measurements of thermal parameters of the tested transistor using gate-emitter voltage as a thermally sensitive parameter. These thermal parameters values correspond to the IGBT die. For the tested device differences between values of thermal resistance measured for the IGBT die, and for the diode die included in the common case are nearly constant and they belong to the range from 0.9 to 1.1 K/W. So, in order to determine the thermal resistance of the IGBT die only simple addition is needed. The constant equal to 0.9 K/W should be added to the value of thermal resistance measured with the use of the method shown in Section III. In this case, in the presented thermal model, the value of parameter R_{th0} should be increased by 0.9 K/W.

Similar investigations were performed also for different IGBTs types. For each tested device influence of the device, internal temperature on thermal resistance and transient thermal impedance had the same character as it was presented for the tested IGBT of the type IRG4PC40UD.

V. Conclusion

This article presents a new form of the IGBT nonlinear thermal model. This model has a simple form and it takes into account the influence of the device internal temperature and ambient temperature on the cooling process efficiency. The description of this model proposed by the authors takes into account physically observed slow changes of thermal parameters values with changes in the device internal temperature instead of fast changes in such parameters with changes of dissipated power used in the previously formulated thermal models. The model parameters values estimation is easy and it requires performing some measurements of the considered transistor transient thermal impedance and the measured dependence approximation of thermal resistance on the transistor internal temperature and ambient temperature with the function proposed in this article.

The presented calculations and measurement results prove that an increase in the device internal temperature can significantly improve the cooling process efficiency of the considered transistor (a decrease in thermal resistance). On the other hand, an increase in ambient temperature can improve this efficiency (a decrease in thermal resistance) for the transistor operating without any heat-sink (when a dominating mechanism of heat dissipation is convection) or it causes worsening (an increase in thermal resistance) of this efficiency for the transistor operating with the heat-sink (when a dominating mechanism of heat dissipation is conduction). The observed differences in thermal resistance values corresponding to different values of internal and ambient temperature can exceed even 25%. In contrast, the influence of these temperatures on thermal capacitances is negligibly small.

The correctness and usefulness of the proposed model are verified experimentally for the selected type of the IGBT operating at different cooling conditions and different ambient temperatures. On the basis of the obtained calculations and measurement results, superiority of this model over the selected model given in the literature is shown. The discrepancy between the calculations and measurement results can exceed even 20% when the classical linear model is used and it does not exceed 5% when the new nonlinear thermal model is used.

The presented calculation results show that the new form of the IGBT nonlinear thermal model makes it possible to take into account changes in efficiency of the cooling process with changes in the device internal temperature. The proposed compact nonlinear thermal model of the IGBT can also be used for other semiconductor devices. Of course, for these semiconductor devices, the different values of model parameters should be used. These values mainly depend on the type of a case, in which this device is mounted and on the construction of the used cooling system.

Of course, the efficiency of heat dissipation depends not only on the device internal temperature. The used cooling system is also important and such factors as length of removals, cross-section of the used wires, area of soldering pads, dimensions of the heat-sink can visibly influence parameters of the presented models. In further investigations, the authors will work on the elaboration of a compact thermal model of semiconductor devices, which will take into account all the mentioned factors.

The proposed model can be useful for designers of electronic and power electronic circuits including IGBTs. It can make it possible to more accurately estimate the internal temperature of this device operating at different cooling conditions in comparison to the classical linear thermal models and other nonlinear thermal models given in the literature. Such a model will be also used in electrothermal analyses of circuits including IGBTs.

References

[1] M.H. Rashid, *Power Electronic Handbook*. New York, NY, USA: Academic Press, 2007.
[2] M.K. Kazimierczuk, *Pulse-width Modulated DC-DC Power Converters*. Hoboken, NJ, USA: Wiley, 2008.
[3] R. Perret, *Power Electronics Semiconductor Devices*. Hoboken, NJ, USA: Wiley, Hoboken, 2009.
[4] K. Billings and T. Morey, *Switch-mode Power Supply Handbook*. New York, NY, USA: McGraw-Hill, 2011.
[5] S. Ang and A. Oliva, *Power – Switching Converters*. Boca Raton, FL, USA: CRC Press, 2011.
[6] J. Zarębski and K. Górecki, “The electrothermal large-signal model of power MOS transistors for SPICE,” *IEEE Trans. Power Electron.*, vol. 25, no. 5, pp. 1265–1274, May 2010.
[7] A.R. Hefner and D.M. Diebolt, “An experimentaly verified IGBT model implemented in the saber circuit simulator,” *IEEE Trans. Power Electron.*, vol. 9, no. 5, pp. 532–542, Sep. 1994.
[8] A.R. Hefner and D.L. Blackburn, “An analytical model for the steady state and transient characteristics of the power insulated gate bipolar transistor,” *Solid-State Elect.*, vol. 31, no. 10, pp. 1513–1532, 1988.
[9] F. N. Masana, “Lung/airway dynamic model using ABM elements and PSPICE,” *in Proc. 22nd Int. Conf. Mixed Des. Integr. Circuits Syst.*, 2015, pp. 204–209.
[10] P.A. Mawby, P.M. Igic, and M.S. Towers, “Physically based compact device models for circuit modelling applications,” *Microelectron. J.*, vol. 32, pp. 433–447, 2001.
[11] A.R. Hefner and D.L. Blackburn, “Simulating the dynamic electrothermal behavior of power electronic circuits and systems,” *IEEE Trans. Power Electron.*, vol. 8, no. 4, pp. 376–385, Oct. 1993.
[12] Ł. Starzak *et al.*, “Behavioral approach to SiC MPS diode electrothermal model generation,” *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 630–638, Feb. 2013.
[13] V. Szekely, “A new evaluation method of thermal transient measurement results,” *Microelectron. J.*, vol. 28, pp. 277–292, 1997.

[14] P. Górecki, "Investigation of the influence of thermal phenomena on characteristics of IGBTs contained in power modules," *in Proc. 24th Int. Conf. Mixed Des. Integr. Circuits Syst.*, 2017, pp. 355–359.

[15] K. Górecki and P. Górecki, "Modelling dynamic characteristics of the IGBT with thermal phenomena taken into account," *Microelectron. Int.*, vol. 34, no. 3, pp. 160–164, 2017.

[16] A. Castellazzi, Y. C. Gerstenmaier, R. Kraus, and G. K. M. Wachutka, "Reliability analysis and modeling of power MOSFETs in the 42-V-PowerNet," *IEEE Trans. Power Electron.*, vol. 21, no. 3, pp. 603–612, May 2006.

[17] J. Zarębski and J. Dąbrowski, "Investigations of SiC merged pin Schottky diodes under isothermal and non-isothermal conditions," *Int. J. Num. Model.-Electron. Netw. Devices Fields*, vol. 24, no. 3, pp. 207–217, 2011.

[18] K. Górecki, "Modelling mutual thermal interactions between power LEDs in SPICE," *Microelectron. Rel.*, vol. 55, no. 2, pp. 389–395, 2015.

[19] A. Castellazzi, R. Kraus, N. Seliger, and D. Schmitt-Landsiedel, "Reliability analysis of power MOSFET's with the help of compact models and circuit simulation," *Microelect. Rel.*, vol. 42, pp. 1605–1610, 2002.

[20] M. Ciappa, F. Carbognami, P. Cora, and W. Fichtner, "A novel thermomechanics-based lifetime prediction model for cycle fatigue failure mechanisms in power semiconductors," *Microelectron. Rel.*, vol. 42, pp. 1653–1658, 2002.

[21] N. Narendran and Y. Gu, "Life of LED-based white light sources," *J. Display Technol.*, vol. 1, no. 1, pp. 167–171, 2005.

[22] M.H. Rashid, *SPICE for Power Electronics and Electric Power*. Boca Raton, FL, USA: CRC Press, 2017.

[23] D. Maksimovic, A. M. Stankovic, V. J. Thottuvelil, and G. C. Verghese, "Modeling and simulation of power electronic converters," *Proc. IEEE*, vol. 89, no. 6, pp. 898–912, Jun. 2001.

[24] C. Li *et al.*, "A modified neutral point balancing space vector modulation for three-level neutral point clamped converters in high-speed drives," *IEEE Trans. Ind. Electron.*, vol. 66, no. 2, pp. 910–921, Feb. 2019.

[25] A. Abdelhakim, P. Mattavelli, P. Davari, and F. Blaabjerg, "Performance evaluation of the single-phase split-source inverter using an alternative DC-AC configuration," *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 363–373, Jan. 2018.

[26] K. Górecki, "K. Detka, Application of average electrothermal models in the SPICE-aided analysis of boost converters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 4, pp. 2746–2755, Apr. 2019.

[27] A. Endruschat, C. Novak, H. Gerstner, T. Heckel, C. Joffe, and M. Marz, "A universal SPICE field-effect transistor model applied on SiC and GaN transistors," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 9131–9145, Sep. 2019.

[28] C. Basso, *Switch-Mode Power Supply SPICE Cookbook*. New York, NY, USA: McGraw-Hill, 2001.

[29] N. Mohan, W. P. Robbins, T. M. Undeland, R. Nilssen, and O. Mo, "Simulation of power electronic and motion control systems—An overview," *Proc. IEEE*, vol. 82, pp. 1287–1302, Aug. 1994.

[30] P. E. Bagnoli., C. Casarosa, M. Ciampi, and E. Dallago, "Thermal resistance analysis by induced transient (TRAIT) method for power electronic devices thermal characterization—Part I, Fundamentals and theory," *IEEE Trans. Power Elect.*, vol. 13, no. 6, pp. 1208–19, Nov. 1998.

[31] K. Górecki and J. Zarębski, "Nonlinear compact thermal model of power semiconductor devices," *IEEE Trans. Compon. Packag. Technol.*, vol. 33, no. 3, pp. 643–647, Sep. 2010.

[32] P. Górecki and K. Górecki, "Non-linear compact thermal model of IGBTs," *in Proc. 21st Eur. Microelectron. Packag. Conf. Exhib.*, 2017, pp. 1–5.

[33] K. Górecki and P. Górecki, "A new form of the non-linear compact thermal model of the IGBT," *in Proc. 12th IEEE Int. Conf. Comp., Power Elect. Power Eng.*, 2018, pp. 1–6.

[34] K. Górecki, P. Górecki, and J. Zarębski, "Measurements of parameters of the thermal model of the IGBT module," *IEEE Trans. Instrum. Meas.*, vol. 68, no. 12, pp. 4864–4875, Dec. 2019.

[35] A. Bahman, K. Ma, and F. Blaabjerg, "A lumped thermal model including thermal coupling and thermal boundary conditions for high power IGBT modules," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2518–2530, Mar. 2018.

[36] Y. Chang *et al.*, "A 3D thermal network model for monitoring imbalanced thermal distribution of press-pack IGBT modules in MMC-HVDC applications," *Energies*, vol. 12, no. 7, 2019, Art. no. 1319.

[37] J. Reichl, J. M. Ortiz-Rodriguez, A. Hefner, and J. S. Lai, "3-D thermal component model for electrothermal analysis of multichip power modules with experimental validation," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3300–3308, Jun. 2015.

[38] C. van der Broeck, L. A. Ruppert, A. Hinz, M. Conrad, and R. W. De Doncker, "Spatial electro-thermal modeling and simulation of power electronic modules," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 404–415, Jan./Feb. 2018.

[39] K. Górecki, J. Zarębski, P. Górecki, and P. Ptak, Compact thermal models of semiconductor devices—A review," *Int. J. Electron. Telecommun.*, vol. 65, no. 2, pp. 151–158, 2019.

[40] F. Di Napoli *et al.*, "On-line junction temperature monitoring of switching devices with dynamic compact thermal models extracted with model order reduction," *Energies*, vol. 10, no. 2, 2017, Art. no. 189.

[41] P. Zając and A. Napieralski, Novel thermal model of microchannel cooling system designed for fast simulation of liquid-cooled ICs. *Microelectron. Rel.*, vol. 86, pp. 245–258, 2018.

[42] T. Raszkowski, A. Samson, and M. Zubert, "Influence of temperature and heat flux time lags on the temperature distribution in modern GAAFET structure based on dual-phase-lag thermal model," *Microelectron. Rel.*, vol. 86, pp. 10–19, 2018.

[43] K. Górecki and J. Zarębski "Modeling the influence of selected factors on thermal resistance of semiconductor devices," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 4, no. 3, pp. 421–428, Mar. 2014.

[44] D.L. Blackburn, "Temperature measurements of semiconductor devices—A review," *in Proc. 20th IEEE Semicond. Thermal Measure. Menage. Symp.*, 2004, pp. 70–80.

[45] Y. Yener and S. Kakac, *Heat Conduction*. New York, NY, USA: Taylor & Francis, 2008.

[46] M. Janicki, Z. Sarkany, and A. Napieralski, "Impact of nonlinearities on electronic device transient thermal responses," *Microelectron. J.*, vol. 45, no. 12, pp. 1721–1725, 2014.

[47] F. F. Oettinger and D. L. Blackburn, "Semiconductor measurement technology, thermal resistance measurements," U. S. Department of Commerce, NIST/SP-400/86, 1990.

[48] B. Dziurdzia, K. Górecki, and P. Ptak, "Influence of a soldering process on thermal parameters of large power LED modules," *IEEE Trans. Compon. Packag. Manuf. Technolo.*, vol. 9, no. 11, pp. 2160–2167, Nov. 2019.

[49] D. Schweitzer, "Trends and developments in thermal and mechanical simulation of semiconductor devices," in *Proc. 25th Int. Workshop Thermal Invest. ICs Syst.*, 2019, Programme, p. 10.

[50] A. Castellazzi, "Synthesis and analysis of wide-band-gap based integrated power electronics, enabling exploitation of higher temperature capability by bespoke models and design tools," in *Proc. 25th Int. Workshop Thermal Invest. ICs Syst.*, 2019, Programme, p. 10.

[51] K. Górecki and P. Górecki, "The analysis of accuracy of the selected methods of measuring thermal resistance of IGBTs," *Metrol. Meas. Syst.*, vol. 22, no. 3, pp. 455–464, 2015.

[52] F.F. Oettinger, D.L. Blackburn, and S. Rubin, Thermal characterization of power transistors, *IEEE Trans. Electron Devices*, vol. 23, no. 8, pp. 831–838, Aug. 1976.

[53] Y. Avenas, L. Dupont, and Z. Khatir, "Temperature measurement of power semiconductor devices by thermo-sensitive electrical parameters—A review," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 3081–3092, Jun. 2012.

[54] L. Dupont and Y. Avenas, "Preliminary evaluation of thermo-sensitive electrical parameters based on the forward voltage for online chip temperature measurements of IGBT devices," *IEEE Trans. Ind. Appl.*, vol. 51, no. 6, pp. 4688–4698, Nov./Dec. 2015.

[55] L. Dupont, Y. Avenas, and P.-O. Jeannin, "Comparison of junction temperature evaluations in a power IGBT module using an IR camera and three thermosensitive electrical parameters," *IEEE Trans. Ind. Appl.*, vol. 49, no. 4, pp. 1599–1608, Jul.–Aug. 2013.

[56] G. Zeng, H. Cao, W. Chen, and J. Lutz, "Difference in device temperature determination using p-n junction forward voltage and gate threshold voltage," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2781–2793, Mar. 2019.

[57] J. Zarębski and K. Górecki, "A new measuring method of the thermal resistance of silicon P-N diodes," *IEEE Trans. Instrum. Meas.*, vol. 56, no. 6, pp. 2788–2794, Dec. 2007.

[58] International Rectifier Corp., Insulated gate bipolar transistor with ultrafast soft recovery diode, data sheet, IRG4PC40UD. [Online]. Available: http://www.irf.com/product-info/datasheets/data/irg4pc40ud.pdf, Accessed on: May 22, 2020.