Modulation and Control of Series/Parallel Module for Ripple-Current Reduction in Star-Configured Split-Battery Applications

Zhongxi Li, *Student Member, IEEE*, Ricardo Lizana, *Member, IEEE*, Zhujun Yu, Sha Sha, Angel V. Peterchev, *Senior Member, IEEE*, and Stefan M. Goetz, *Member, IEEE*

***Abstract*— Split-battery converters based on cascaded H-bridges (CHBs) are gaining popularity due to their excellent physical modularity. During operation, however, the batteries experience substantial current ripple. Conventional ripple-current reduction methods rely on bulky passive components or complicated control. This article presents modulation and common-mode voltage injection methods for cascaded double-H-bridge converters (CHB²). The control methods directly mitigate the source of the ripple current—the fluctuating arm power—by exploiting the parallel interconnection across the CHB² arms. In the lab setup, the proposed solution approximately halves the battery current ripple compared to the CHB counterpart. Finally, this article studies component sizing and limitations of the proposed solution.**

***Index Terms*—Cascaded H-bridge, ripple-current reduction, split-battery converter.**

I. Introduction

THERE is a growing interest to employ cascaded H-bridge (CHB) converters in battery energy storage systems (BESS) [1]–[6] and motor drives [7], [8] to replace the conventional two- or three-level converters. In this context, batteries are distributed to H-bridge (HB) modules instead of being hard-wired together. The gained physical modularity allows flexible control over battery subportions [5], [6], [9], excellent output quality, improved fault tolerance [3], [4], [10]–[12], and maximized performance of each cell instead of a limitation by the weakest cell in a hard-wired battery [1], [13]. In particular, the great output quality of CHBs reduces the output filters in grid-connected applications [14]–[18], as well as mitigates the torque ripple and insulation stress in motor drives [9], [19].

Despite numerous advantages, the fluctuating power in the CHB arms produces current ripple at twice the ac frequency on the batteries. The current ripple can cause additional loss, compromise the battery life [20], [21], and consequently limit the system rating. Under reactive loads, the current ripple can stress the batteries with charging–discharging mini cycles, which lowers the coulombic efficiency and capacity [22]–[26]. Indeed, battery cell manufacturers often recommend a current ripple below 5% of the rated current [22], [23], [27].

Passive filters [28]–[30] and dc–dc interfaces [1], [28], [29], [31], [32] are typical approaches to reduce the current ripple in CHB-battery systems. The passive filter usually refers to a resonant circuit tuned to shunt the second-order current ripple [28]. The required passive components are inevitably large because they must absorb the entire oscillatory energy. Alternatively, the dc–dc interfaces can be used to directly control the battery current [1], [28], [29], [31], [32], but bulky passive components are still mandatory due to the large oscillatory energy. A different approach injects zero-sequence quantities to raise the oscillatory power to higher frequencies and consequently shrink the filters [33]–[37]. The main drawbacks, however, include increased conduction loss and limited modulation range.

The challenge of mitigating the current ripple in CHBs stems from the limited power-transfer capability across converter arms, whereas two- or three-level converters cancel the phase power fluctuations at the shared dc bus, none of the HB's switching configurations allows so. Addressing this limitation, previous studies [38]–[40] proposed a double-H-bridge (HB²) module to replace the HB module. The obtained converter, named CHB², features parallel connectivity between the modules that can transfer power across converter arms. In multiphase systems, a transfer of the fluctuating power across the arms can mitigate the current ripple in the modules [39].

Based on CHB²s [39], this article proposes a suitable modulation method and a common-mode voltage injection method to further reduce the ripple current. The new modulation method

Manuscript received January 5, 2019; revised April 17, 2019, July 8, 2019, September 12, 2019, and December 11, 2019; accepted May 1, 2020. Date of publication May 20, 2020; date of current version July 31, 2020. The preliminary study "*Ripple Current Suppression Methods for Star-Configured Modular Multilevel Converters*" was presented on 43rd Annual Conference of the IEEE Industrial Electronics Society, Beijing, 2017. This work was supported in part by the National Science Foundation under Grant 1608929, in part by the North Carolina Biotechnology Center under Grant 2016-CFG-8004, in part by a seed grant from the Duke University Energy Initiative, and in part by Fondecyt Regular under Grant 1201344. Recommended for publication by Associate Editor L. Huber. *(Corresponding author: Stefan M. Goetz.)*

Zhongxi Li, Angel V. Peterchev, and Stefan M. Goetz are with the Duke University, Durham, NC 27708 USA (e-mail: zhongxi.li@duke.edu; angel.peterchev@duke.edu; stefan.goetz@duke.edu).

Ricardo Lizana is with the Universidad Católica de la Santósima Concepción, Concepcion 4090541, Chile (e-mail: ricardolizana@ucsc.cl).

Zhujun Yu is with the Department of Electrical Engineering, Tsinghua University, Beijing 100084, China (e-mail: yuzj18@mails.tsinghua.edu.cn).

Sha Sha is with the California Institute of Technology, Pasadena, CA 91125 USA (e-mail: ssha@caltech.edu).

Color versions of one or more of the figures in this article are available online at https://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2020.2996542

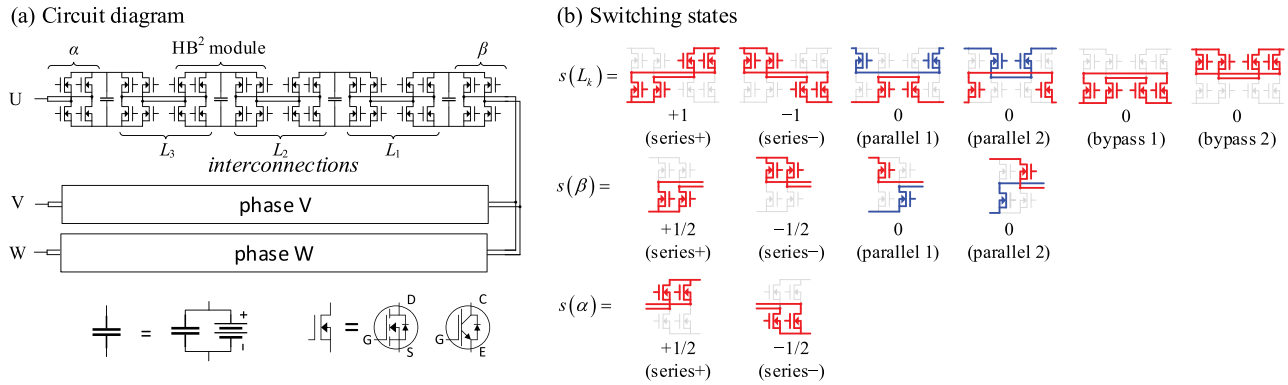

Fig. 1. Star-configured CHB^2 converter with four modules per arm. (a) Power stage, where L_k denotes the kth interconnection. (b) Switching states, where the numbers (i.e., ±1, ±½, and 0) denote the corresponding changes in the arm output voltage level. Red and blue color indicate different potentials.

facilitates the power transfer across the arms of CHB^{2}s while the common-mode voltage injection peak shaves the arms' oscillatory power. On the CHB^2 lab setup, the combination of the improved modulation and the common-mode voltage injection notably reduces the current ripple compared to the previous solution [39] (i.e., CHB^2 with conventional control) and the conventional CHB. Parameter studies are carried out to show advantages and limitations of the proposed solution.

The rest of this article is organized as follows. Section II introduces the star-configured CHB², equivalent circuit, and modulation strategies. Section III discusses an optional common-mode voltage injection to further improve the performance. Section IV compares the losses of the CHB and CHB^2. Section V empirically studies the proposed solution.

II. Cascaded Double-H-Bridge

A. Topology and Operation Principles

Fig. 1 shows a star-configured cascaded double-H-bridge (CHB²) converter. As the building block of CHB^{2}s, each HB^2 module comprises two H-bridges, and the HB^2 modules are cascaded via two-terminal interconnections. As such, the adjacent HB^2 modules can be dynamically configured in series, bypass, or parallel configurations [see Fig. 1(b)]. Whereas the series and bypass states are equivalent to those of CHBs, the parallel state splits the load across multiple modules [41] and allows switched-capacitor-type balancing [40], [42]. The parallel state does not change the arm output voltage and typically replaces bypass states in known modulation strategies [40], [42], [43]. Importantly, we also apply the two-terminal connectivity at the neutral point so that it can temporarily form a shared dc link across the arms via the parallel states. The temporarily shared dc link is the key to canceling the oscillatory arm powers in a way similar to a three-phase full bridge.

Since the parallel interconnection is jointly formed by the adjacent modules, we define the switching states per interconnection instead of per module [40], [41]. An arm with N modules contains $N-1$ interconnections and two arm terminations, named α and β (Fig. 1). The switching sites (i.e., all physical interconnections and α/β terminations) modify the arm output voltage in an independent, additive manner according to

$$v_x = \left[\sum_{k=1}^{N-1} s\left(L_{k,x}\right) + s\left(\alpha_x\right) + s\left(\beta_x\right)\right] \cdot V_b \tag{1}$$

where $s(=-1, 0, +1)$ denotes the output voltage level of the switching state, V_b the voltage of the energy storage, and v_x the arm output voltage, $-NV_\mathrm{b} \le v_\mathrm{x} \le NV_\mathrm{b}$. Symbol x(= u, v, w) denotes phases and k enumerates the interconnections or modules. Equation (1) indicates that CHB^{2}s can be modulated by multicarrier schemes, which will be introduced later.

B. Approximate Equivalent Circuit Model

With frequent parallel interconnections through the three β terminals, the dc links of the three arms can be frequently joined, partially cancelling the arms' oscillating power by trigonometric principle. To quantify this effect, we study the time-averaged behavior of the CHB^2. Assume each interconnection stays in either "+/−1" (series+/−) or "0" (parallel), with duration $|m_k(t)|{\cdot}{f_\mathrm{sw}}^{-1}$ and $[1-|m_k(t)|]{\cdot}{f_\mathrm{sw}}^{-1}$, respectively. Any voltage difference Δv between two adjacent modules drives equalizing charge during parallel states

$$\Delta Q = \frac{\Delta v}{4 \cdot r_\mathrm{on}} \left[1 - |m_k\left(t\right)|\right] f_\mathrm{sw}^{-1} \tag{2}$$

where f_sw is the carrier frequency. We define a virtual impedance r_eq to lump the effects of the circuit parameter and the temporary modulation depth

$$r_\mathrm{eq} = \frac{\Delta v}{\Delta Q \cdot f_\mathrm{sw}} = \frac{4 r_\mathrm{on}}{1 - |m_k\left(t\right)|}. \tag{3}$$

In short, the parallel state effectively produces balancing current $r_\mathrm{eq}/\Delta v$ in response to the voltage difference Δv; the balancing current is impeded by larger r_on or $|m_k(t)|$.

On the other hand, we model the effect of the arm power as N virtual current sources paralleled to the module batteries [5]. The current source $i_{\Delta,x}$ models how ac loads create low-frequency current ripple in batteries

$$i_{\Delta,x} = \frac{v_x i_x - \frac{1}{3}\left(v_u i_u + v_v i_v + v_w i_w\right)}{N V_b}. \tag{4}$$

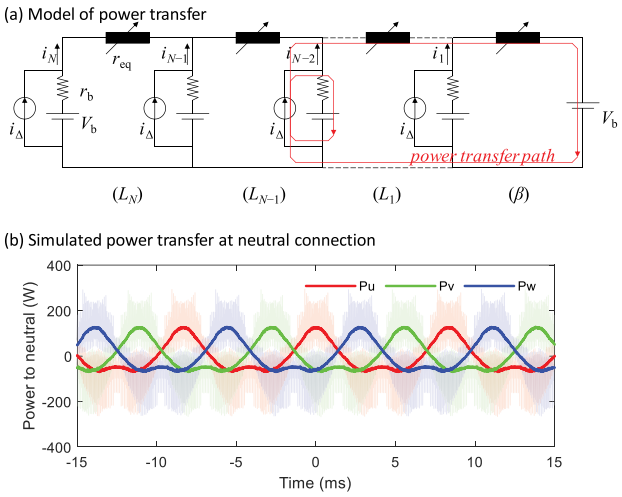

Fig. 2. (a) Equivalent circuit model of power transfer in CHB^{2}s. (b) Simulated transferred power via the neutral connection with proposed PWM and common-mode voltage injection. The data is filtered with a moving window of 0.1 ms. Other settings are listed in Table II.

Fig. 2 demonstrates the equivalent circuit. Only one arm is shown while the net influence of the other arms is approximated by a virtual voltage source V_b due to the circuit symmetry. The equivalent circuit predicts a portion of the ac current $i_{\Delta,x}$ flowing across the power-transfer path and through the other arms (represented by the voltage source) at the neutral point. Such balancing power is essentially driven by the gradients of the capacitor voltages along the arm. The balancing power is periodically relayed by the module capacitors at switching frequencies, as shown in Fig. 2(b). Operating at switching frequencies, the module capacitors do not need to absorb the low-frequency oscillatory energy and therefore can be much smaller than the second-order passive filters [28]. For this reason, there is no need to model capacitors in Fig. 2(a). There is also no need to concurrently parallel all modules. The cancelation mechanism is independent of the output frequency, making the CHB^2 a potential solution also for motor drives.

The modeling of the circuit is simplified to emphasize the power transfer of CHB^{2}s.

Instead of applying a conventional multicarrier modulation, we notice the degree of freedom in the distribution of the modulation indices m_k (1) and form the following optimization problem

$$\begin{cases} m_1^\star, m_2^\star, \ldots, m_N^\star = \arg\min_{m_k} \mathbf{i}_\mathrm{b}^\top \mathbf{i}_\mathrm{b}, \\ \text{s.t.,} \qquad \mathbf{i}_b = A\left(r_\mathrm{on}/r_\mathrm{b}, m_1, m_2, \ldots, m_N\right) \cdot \mathbf{i}_\Delta \\ \qquad\quad m = \Sigma m_k/N, \qquad \forall m_k \in [0,1]. \end{cases} \tag{5}$$

In short, (5) redistributes the modulation reference among the switching sites, such that the battery currents $\mathbf{i}_\mathrm{b}(= [i_{\mathrm{b}1}, i_{\mathrm{b}2}, \ldots, i_{\mathrm{b}N}]^\mathrm{T})$ produce minimal total conduction loss. Variable $\boldsymbol{i}_b$ solves the linear circuit in Fig. 2 through matrix $\mathbf{A}$. The results are listed in Table I with selected conditions. The optimization is challenging to implement due to the nonlinear dependency on the momentary modulation index; however, all results favor lower modulation indices for modules closer to the neutral connection, likely because those modules are more critical for transferring the arm power.

TABLE I
EXAMPLES OF THE OPTIMAL MODULATION INDICES†

m	Optimally re-distributed m_k	Loss‡
0.3	[0.68, 0.39, 0.13, 0.00]	76.5%
0.5	[0.78, 0.57, 0.40, 0.25]	76.9%
0.7	[0.87, 0.74, 0.64, 0.55]	77.8%
0.9	[0.96, 0.92, 0.88, 0.84]	80.8%

†$r_\mathrm{on} = 0.2$ mΩ, $r_\mathrm{b} = 100$ mΩ, corresponding to Table II.
‡Compared to the default PWM at the same condition, i.e., $(\forall m_\mathrm{x} = m)$.

The circuit model also indicates that the ripple-current reduction depends on the ratio of the resistances r_on/r_b. When $r_\mathrm{on}/r_b \to 0$, the resulted low-frequency current ripple asymptotically decreases to zero since the battery ripple current can effortlessly flow through the power-transfer path; when $r_\mathrm{on}/r_b \to \infty$, the current ripple is as large as that in CHBs since the power transfer is blocked by high impedance.

C. Modulation

In this article, we modify a previous multicarrier modulation scheme [39] to incorporate the findings from the equivalent circuit. Specifically, a pair of unipolar carriers C_k^+ and C_k^- is assigned to the kth interconnection ($k = 1, \ldots, N-1$). Since arm terminations (α or β) produce ±½ module voltage, they are modulated by bipolar carriers (C_α and C_β) to keep the modulation linear. The preliminary modulation rules are

$$\begin{aligned} s\left(L_{k,\mathrm{x}}\right)_{k=1,\ldots,N-1} &= \begin{cases} +1, & \text{if } m_\mathrm{x}(t) \geq C_k^+(t) \\ -1, & \text{if } m_\mathrm{x}(t) \leq C_k^-(t) \\ 0, & \text{if } C_k^-(t) < m_\mathrm{x}(t) < C_k^+(t) \end{cases} \\ s\left(\alpha_\mathrm{x}/\beta_\mathrm{x}\right) &= \begin{cases} +1/2, & \text{if } m_\mathrm{x}(t) \geq C_{\alpha/\beta}(t) \\ -1/2, & \text{if } m_\mathrm{x}(t) < C_{\alpha/\beta}(t) \end{cases} \end{aligned} \tag{6}$$

where $m_x(t) = v_{\mathrm{ref},_x}(t)/(NV_b)$ denotes the momentary modulation index shared by all switching sites of the same arm. The next step checks if $s(\beta_u) = s(\beta_v) = s(\beta_w)$; if this condition holds, we simply set $s(\beta_u) = s(\beta_v) = s(\beta_w) = 0$, which prioritizes a shared dc link across the arms without changing the output voltage.

According to the optimization results of (5), modules that are close to the neutral connection should spend slightly more time in parallel, whereas the other modules should be in the series more often to compensate the lost voltage levels. Instead of changing the individual references, we modify the carriers to approach this idea. In Fig. 3(b), carrier C_β is split in halves and placed near the maximum modulation ranges. With the modulation rule above, references m_u, m_v, and m_w are often concurrently larger or smaller than C_β, and therefore the condition $s(\beta_\mathrm{u}) = s(\beta_\mathrm{v}) = s(\beta_\mathrm{w})$ occurs frequently. The other carriers are rescaled between $-(N - ½)/N$ and $+(N - ½)/N$ to keep the modulation linear. Due to the modulation linearity and the fact that the parallel state does not generate different output voltage than the bypass state, the CHB^2 under the improved modulation

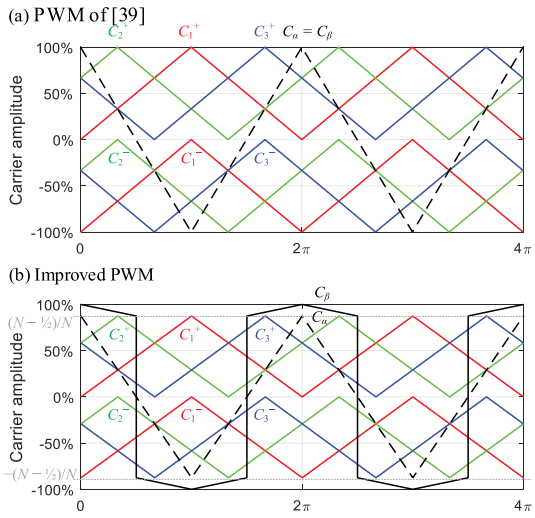

Fig. 3. Carrier settings for a four-module CHB^2 arm. (a) Carrier setting from [39]. (b) Improved carrier setting prioritizing power transfer across the neutral interconnection (β termination parts).

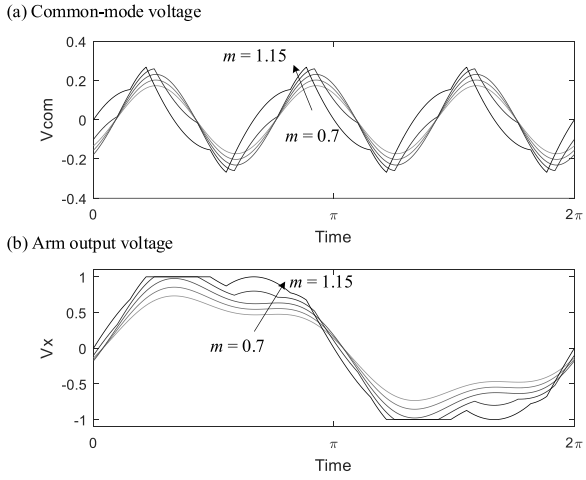

Fig. 4. (a) Optimal common-mode voltage waveforms. (b) Synthesized arm output voltage. The flattened section at $v_x = \pm 1$ and the irregular shapes at high modulation indices reflect the boundary of the linear modulation. The power factor is 0.9, and $\mu = 0.5$.

strategy generates similar output quality as in previous work [39] and for the CHB counterpart. In practice, the CHB^2 can have slightly better quality due to its smaller voltage ripple in the dc links (see Figs. 10 and 11). Fig. 9 provides comprehensive comparisons between the CHB and CHB^2, with and without the improved modulation method.

III. Common-Mode Voltage Injection

Appropriate common-mode voltage injection can virtually exchange power among the arms, which can be used to reduce the ripple current for both CHBs and CHB^{2}s. Denote v'_x ($x = u$, v, w) as the intended arm voltage reference without common-mode voltage injection, i_x the arm current. To find the optimal common-mode voltage $v_{\rm com}$, we minimize the ripple current, which amounts to instantaneous battery conduction loss as well. As such

$$\begin{aligned} v_{\rm com} &= \arg\min_{v_{\rm com}\in\mathbb{V}} \left(\frac{p_u}{NV_b}\right)^2 + \left(\frac{p_v}{NV_b}\right)^2 + \left(\frac{p_w}{NV_b}\right)^2 \\ \text{s.t. } \bar{p} &= (p_u + p_v + p_w)/3 \\ p_x &= v_x \cdot i_x = (v'_x + v_{\rm com}) \cdot i_x \\ \mathbb{V} &= \left[\max_{x\in\{u,v,w\}} \left(-N\cdot V_b - v'_x\right), \min_{x\in\{u,v,w\}} \left(N\cdot V_b - v'_x\right)\right]. \end{aligned} \tag{7}$$

The constraint $v_{\rm com} \in \mathbb{V}$ accounts for the linear modulation range and can achieve the maximum modulation depth of $2/\sqrt{3}$ (i.e., the limit for three-phase converters). The solution is

$$v^\star_{\rm com} = \begin{cases} v^\star_{\rm unc}, & \text{if } v^\star_{\rm unc} \in \mathbb{V} \\ \min \mathbb{V}, & \text{if } v^\star_{\rm unc} < \min \mathbb{V} \\ \max \mathbb{V}, & \text{if } v^\star_{\rm unc} > \max \mathbb{V} \end{cases} \tag{8}$$

where

$$v^\star_{\rm unc} = -\mu \frac{i_u^2 v'_u + i_v^2 v'_v + i_w^2 v'_w}{i_u^2 + i_v^2 + i_w^2}. \tag{9}$$

For symmetrical, linear loads with sinusoidal arm voltages (i.e., $v'_u = V\sin\omega t$),

$$v^\star_{\rm unc} = \tfrac{1}{2}\mu V \sin(3\omega t - 2\varphi) \tag{10}$$

where φ is the load angle.

In the solution, we add to the common-mode voltage a multiplier $0 \le \mu \le 1$ to further adjust the current ripple. The unconstrained solution (9) with $\mu = 1$ is the unique optimum if it also satisfies the modulation constraint; otherwise, solution (9) is clipped to the modulation range $\mathbb{V}$, hence (8). The optimality of (8) is guaranteed by the convexity of the original problem (7). Compared to methods that aim to extend the operation range [44]–[48], the proposed $v_{\rm com}$ adapts to the load angle and additionally minimizes the instantaneous battery ripple current. Compared to the interarm power transfer methods [3], [6], [49], the proposed $v_{\rm com}$ applies to arbitrary loads. At a high modulation index, the proposed $v_{\rm com}$ deforms to comply with $v_{\rm com} \in \mathbb{V}$ (Fig. 4) and minimizes the ripple current for the rest of the load cycle; in contrast, methods akin to [49] would entirely disallow the injection whenever the peak arm voltage reaches the upper limit. For CHB^{2}s, both the common-mode voltage injection and the hardware parallelization help mitigate the ripple current but via completely different mechanisms.

With the modulation constraint already committed by (8), one can freely change μ without affecting the output voltage. Setting $\mu = 1$ optimizes CHBs since it minimizes (7). For CHB^{2}s, $\mu = 1$ is not the best choice since it increases the peak arm voltage and shortens the duration in parallel interconnection. One therefore needs to find a moderate $\mu(< 1)$ to peak shave the arm powers without hampering the switched-capacitor power transfer. Rigorous optimization over μ is hard, but empirical results suggest $\mu = 0.5$ for most cases (Fig. 5). A direct comparison between

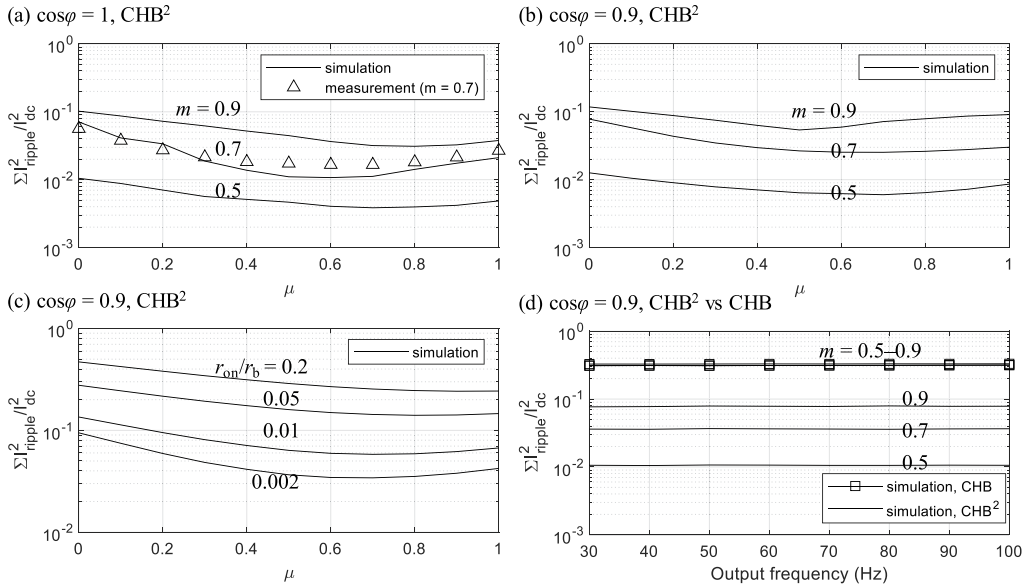

Fig. 5. Ripple current amplitude of the CHB^2 under (a–b) various power factors and modulation indices, (c) various component impedances, and (d) various output frequencies.

this article (i.e., improved pulsewidth modulation (PWM) and $\mu = 0.5$ on CHB^2) and the previous work [39] (CHB^2 with $\mu = 1$) is given in Fig. 9(b1–2).

Fig. 5 compares the current ripple under various μ to isolate the contribution of the improved common-mode injection method. The improved PWM is used. For a moderate range of the parameter $r_{\rm on}/r_b$, the common-mode voltage with amplitudes $\mu = 0.5$–0.7 notably reduces the current ripple compared to the previously suggested $\mu = 1$ [39] or $\mu = 0$ (no-injection). Very large $r_{\rm on}/r_b$, however, favors $\mu = 1$ because the power-transfer channel becomes less effective to pass the balancing current. In the following sections, we use $\mu = 0.5$ for the CHB² and $\mu = 1$ for the CHB. Finally, Fig. 5(d) evaluates the ripple current under various output frequencies. For CHBs, the independence of the output frequencies is expected since very small capacitors are used; for CHB^{2}s, the result indicates that the ripple-current reduction is mostly ascribed to the switched-capacitor power transfer of the CHB^2, rather than the low-frequency filtering effect of the capacitor.

IV. Power Loss

This section compares the power losses of CHB and CHB² under the setting of Table II. Notice that if the CHB and CHB^2 have equal $r_{\rm on}$ per switch, any loss comparison would be trivially in favor of CHB^2 because the CHB^2 can at least mimic the operation of CHBs while using more silicon in parallel. Since the two topologies use different numbers of transistors, a fair comparison requires equal semiconductor budget for both, i.e., each transistor in the CHB² is set to have half the silicon area and thus twice the $r_{\rm on}$ compared to that of the CHB. In what follows, we show such seemingly disadvantageous setting for CHB^2 is overcompensated by its topology.

TABLE II
Parameters for the Simulation and Experiment Models

		CHB^2	CHB
Test power	P	480 W ($m = 0.7$)	
No. of modules	$3N$	3×4	
Nominal module voltage	$V_{\rm b}$	10 V	
Module transistors†		8×1 FETs ($r_{\rm on}$ = 0.2 mΩ)	4×2 FETs ($r_{\rm on}$ = 0.1 mΩ)
Module battery type		Lead-acid 1.3 Ah ($r_{\rm b}$ = 0.1 Ω)	
Module filter capacitance (unit capacitance constant)	C ($\tau_{\rm c}$)	1.6 mF (0.6 ms)	
Module filter inductance	L	10 μH	
Module switching frequency	$f_{\rm sw}$	10 kHz	
Common-mode voltage	μ	0.5	1.0

†Each topological transistor is implemented with multiple field-effect-transistors in parallel (IPT004N03L, Infineon Technologies).

A. Losses That Are Theoretically Comparable

For start, we only consider the conduction losses on the batteries and transistors. According to Appendix, such setting furnishes a theoretical result that CHB^{2}s always generate less conduction loss than the CHBs of matched hardware settings. The result pertains only to the circuit topology and is independent of parameters. From circuit's perspective, CHB^{2}s generate less conduction loss because CHB^{2}s provide more current paths (the parallel paths, in particular) than CHBs, on which the current naturally distributes to minimize the energy loss.

We carry out simulations to quantify the overall losses including the switching loss and the capacitor loss. The transistors are modeled as IPT004N03L (Infineon Technologies). Fig. 6 verifies two analytical results of Appendix B: 1) CHB^2's conduction loss (from transistor and capacitor) is smaller than that of the CHB. 2) The CHB^2 becomes more advantageous as $r_{\rm b}/r_{\rm eq}(r_{\rm on})$ increases.

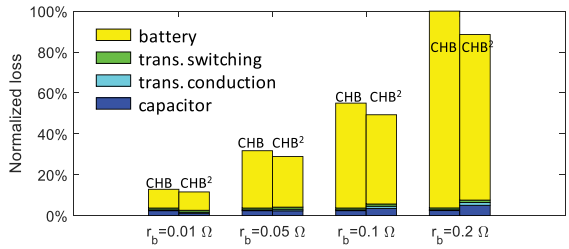

Fig. 6. Losses of the CHB and the CHB^2 models with different battery ESRs. Across all cases the transistor ESR is fixed. The peak modulation index of the fundamental component is 0.7 across all cases. Both models use the same total silicon area (Table II).

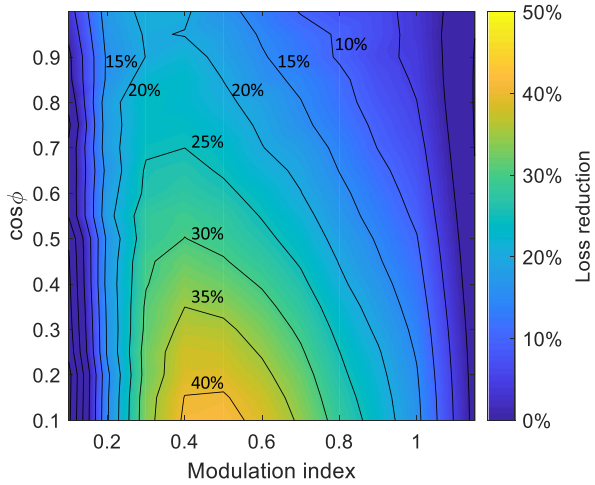

Fig. 7. Reduced loss (batteries, capacitors, and transistors) of the CHB² compared to the CHB. The maximum loss reduction occurs at high reactive loads. All settings correspond to Table II.

B. Losses That Are Parameter-Dependent

The downside of CHB^{2}s is that the balancing current influences the switching loss and capacitor loss. These losses are parameter-dependent, which may or may not be in favor of the CHB^2. Regardless, in the context of modular multilevel converters, the switching loss is usually insignificant by design. The capacitor loss is also easily controllable in CHB^2 because: 1) the capacitors in CHB^{2}s only absorb high-frequency current and can be much smaller than that of the CHB counterparts, and 2) film capacitors typically have submilliohm ESRs. One may adjust the switching frequency to tradeoff between the capacitor loss and the switching loss or optimize the capacitor design. This article does not further explore these options; rather, a wide-range of settings are simulated in Figs. 6 and 7, wherein the CHB^2 outperforms the CHB in most cases.

Across all cases, the battery ESR is set to be higher than the transistor $r_{\rm on}$ to reflect the reality that the cost per energy-loss unit on the battery side is by orders of magnitude larger than for transistors.

The simulations above ignore stray inductance in the system. The peak balancing current is therefore overestimated, causing higher loss in capacitors and transistors for the CHB^2. In practice, the connection cables between modules often provides sufficient stray inductance to suppress the balancing current [50], despite not intended. For instance, a 10-cm long cable can present 100 nH [51]; with a 1.6-mF capacitor, the cable is sufficient to dampen the inrush balancing current.

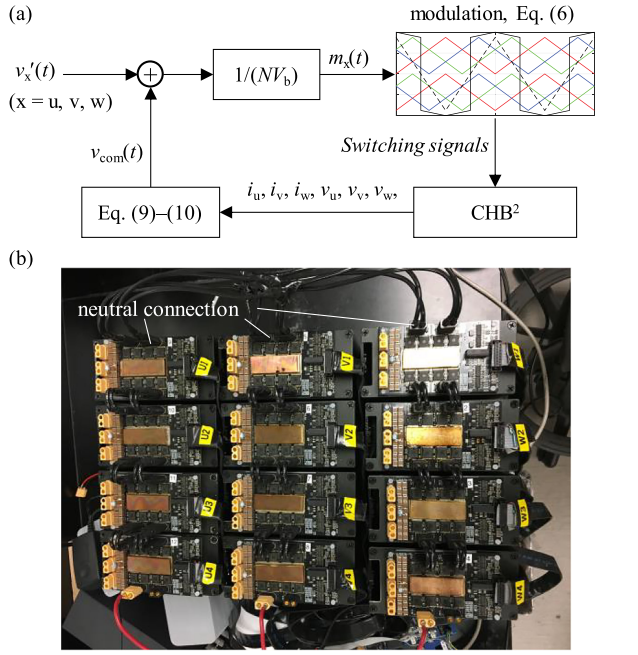

Fig. 8. (a) Block diagram summarizing the common-mode injection and the modulation methods. (b) Experimental setup.

V. Experiment Results

A. Power Stage

The CHB²-based ripple-current suppression is verified on a three-phase laboratory setup (Fig. 8) with symmetrical passive loads. There are four modules per arm, wired as in Fig. 1(a). Each module incorporates a lead-acid battery and a capacitor with $C = 1.6$ mF, or unit capacitance constant of $\tau_{\rm c} = 12 \times \frac{1}{2}CV_{\rm mdl}^2/S = 0.6$ ms [52]. A small inductor (10 μH) is connected in series to the battery for suppressing the switching-frequency currents as well as introducing a controllable impedance in series with the battery. The combination of the inductor and the capacitor is small (the resonant frequency is 1.26 kHz) and does not intend low-frequency filtering. For comparison, a conventional CHB setup is built with the same components. Each switch of the CHB modules is implemented with two transistors (in parallel) of the CHB² module so that both systems use the same silicon area. The system operates at 60 Hz. Table II lists the implementation details.

B. Experimental Results

Fig. 9 compares the proposed control methods with a previous one [39]. Either the improved PWM or the proposed common-mode voltage can individually reduce the current ripple at both CHB^2 and CHB topologies under the same conditions.

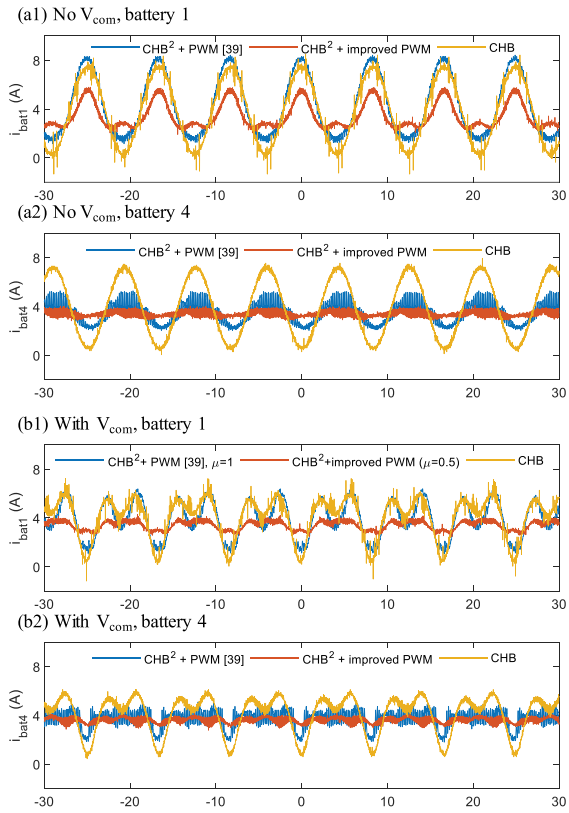

Fig. 9. Current measurements of the batteries that are farthest (a1) and nearest (a2) to the neutral connection. No common-mode voltage is injected. In subplots (b1) and (b2), the common-mode voltages are injected: for CHB^2 with the PWM method of [39] and CHB, $\mu = 1$; for CHB^2 with the improved PWM, $\mu = 0.5$. The peak modulation index is 0.7 across all cases. The rest of the setting is listed in Table II.

Fig. 10 compares CHB^2 and CHB under their respective optimal controls. The CHB^2 shows a notable reduction in the battery current ripples [Fig. 10(a)]. The output current of the CHB is distorted because of the larger capacitor voltage ripple.

Fig. 11 compares CHB^2 and CHB with conventional controls. In the CHB^2, all but the battery near the neutral point experience large peak current as predicted by the circuit model, but they are still smaller than those of the CHB.

Under the proposed modulation scheme, the CHB^2 tracks the reference with three adjacent voltage levels as opposed to CHB's two levels. As such, the output current of the CHB^2 contains more switching harmonics but the difference is very subtle (Figs. 10 and 11). The output voltage range, however, is the same across the topologies.

C. Parameter Study

We use relative ripple content $\Sigma {I_{\rm ripple}}^2/{I_{\rm dc}}^2$ (i.e., the ratio between the sums of the ac and dc component power) for parameter studies.

1) Modulation Index: Fig. 12(a) does not influence the relative ripple content in the CHB but impacts CHB² by limiting the duty cycle in the parallel connections. However, even at the maximum modulation index, the CHB² still has substantially lower ripple power. Across all cases the power factor is chosen to be 1, which is the worst case for CHB²s because the peaks of the arm power coincide with the peaks of the momentary modulation index and hence the largest momentary impedance of the power-transfer channel.

2) Common-Mode Voltage: Fig. 12(b) influences CHB and CHB² in slightly different manners. As shown in the previous section, partial common-mode voltage with $\mu = 0.5$–0.7 is appropriate for the CHB^2, whereas $\mu = 1$ optimizes CHBs.

3) Component ESR: Fig. 12(c) and particularly the ratio $r_{\rm on}/r_{\rm b}$ have a large influence on the CHB² as predicted by the circuit model. A cross validation is given in Fig. 12(c), where $r_{\rm on}/r_{\rm b} = 0.002$ (default) provides relatively good performance. Further decrease in $r_{\rm on}/r_{\rm b}$ is less worthwhile because the battery loss is then dominated by the dc component. If the batteries have low ESR (e.g., large lithium-ion batteries for high capacitance in a low-power system), it can be hard to achieve a sufficiently low $r_{\rm on}/r_{\rm b}$. In this case, small inductors can be applied in series to the batteries in order to provide more apparent impedance at the switching frequency.

4) Numbers of Modules Per Arm: In Fig. 12(d), as the number of modules per arm increases, the length and the overall impedance of the power-transfer channel through the neutral point of CHB² seen by the outmost modules grows as well. The increase in the impedance limits the ripple-current reduction. However, since the power-transfer mechanism does not entirely vanish, all batteries in the CHB² have less conduction loss than those in the CHB, despite the same passive components and the silicon area.

5) Switching Frequency and Module Capacitance: In Fig. 12(e)–(f), with the proposed common-mode injection method and topology, the original double-line frequency ripple current spreads out in the frequency spectrum because of the power transfer at switching frequencies. As such, there is no longer a distinct frequency distribution in the ripple current as in CHBs, and increasing the switching frequency in CHB^{2}s reduces the entire spectrum of the ripple and hence the lumped $\Sigma {I_{\rm ripple}}^2/{I_{\rm dc}}^2$. Higher switching rate facilitates ripple-reduction because it lowers the temporary power storage in the module capacitors before the reactive arm power is transferred to the next module or to the other arms during the subsequent switching cycle. The stored energy drives the capacitor voltage and the current ripple in the batteries. Conversely, increasing the module capacitance proportionally lowers the required switching frequency for the same performance. The complementary roles of the switching frequency and the module capacitance are discussed in the literature [38]. The product $f_{\rm sw}C$ approximately characterizes the ripple-current suppression performance. To verify this, we simulate the CHB² topology with random combinations of $f_{\rm sw}$ and C in MATLAB/Simulink, while keeping the other settings the same as Table II. The simulation results share a similar trend with the measurements [Fig. 12(f)], and the setting of $f_{\rm sw}C = 20$ kHz $\times$ mF, for example, produces acceptable performance.

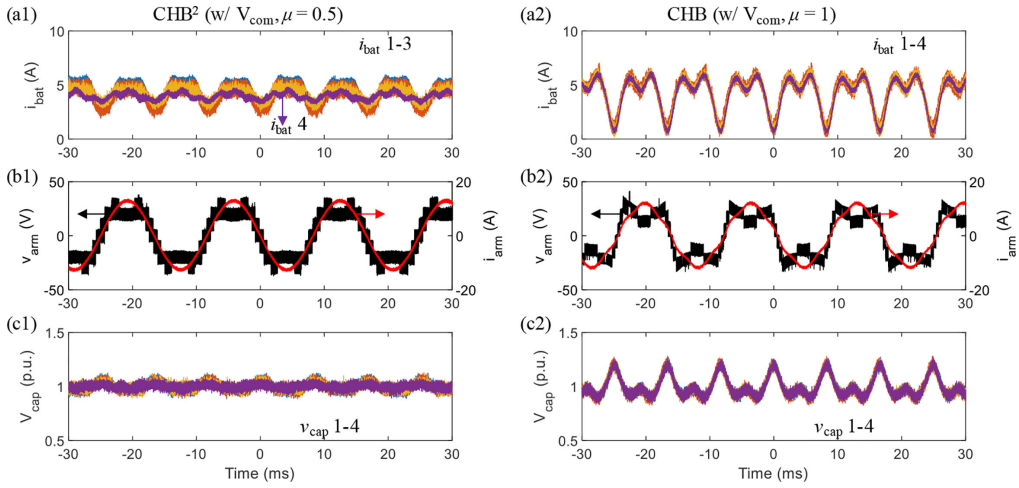

Fig. 10. Experimental waveforms of the CHB^2 and the CHB with the respective optimal v_{com}. (a1–2) The battery output currents. (b1–2) The current and voltage of arm U. (c1–2) Normalized capacitor voltages. For both configurations $m = 0.7$, $P = 480$ W, and the target line–line voltage is 48.5 V (peak).

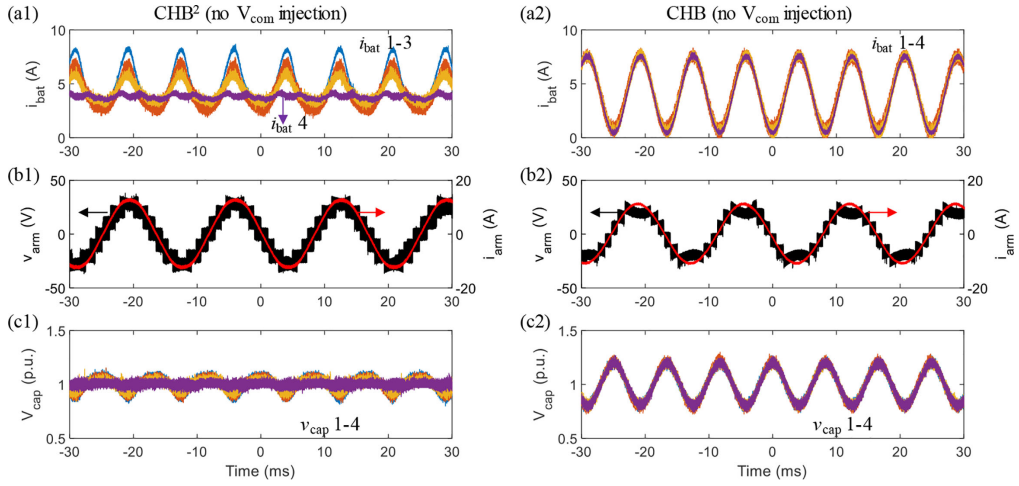

Fig. 11. Experimental waveforms of the CHB^2 and the CHB without v_{com}. (a1–2) Battery output currents. (b1–2) Current and voltage of arm U. (c1–2) Normalized capacitor voltages. For both configurations $m = 0.7$, $P = 480$ W, and the target line–line voltage is 48.5 V (peak).

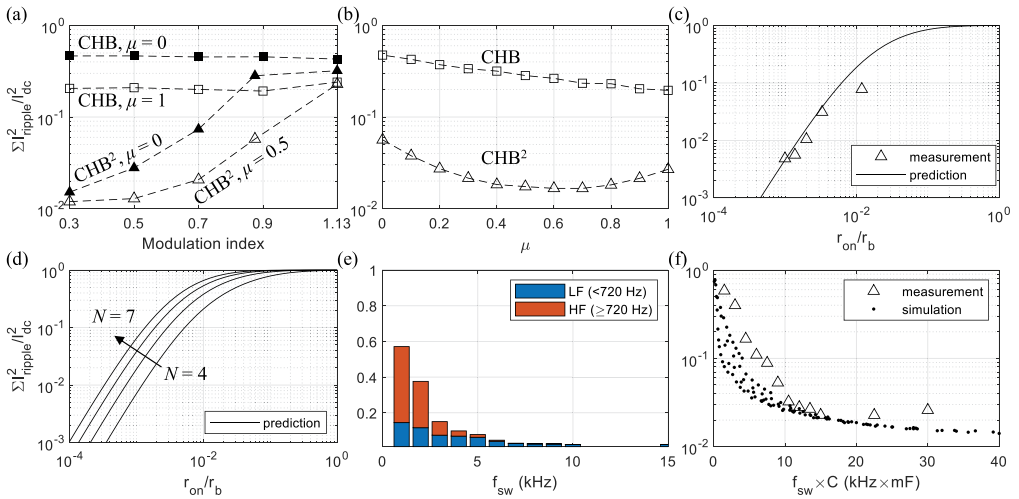

Fig. 12. Parameter study. (a) Modulation index. (b) Injected common-mode voltage amplitude. (c) Component ESRs. (d) Number of modules per arm (the ripple power is averaged from all batteries). (e) Module switching frequency. (f) Module capacitance. All data are experimental measurements unless otherwise noted.

VI. Conclusion

Large low-frequency current ripples in CHBs hamper the use of split-battery converters. Prior approaches to reduce the ripple current in CHB-battery systems impose large costs associated with bulky passive components and/or larger transistors, which offset the advantages of CHBs and make them less competitive compared to conventional two-/three-level counterparts.

This article proposes modulation and common-mode voltage injection methods for cascaded CHB^2 that directly mitigate the source of the ripple current—fluctuating arm power—by exploiting the parallel interconnection across the CHB^2 arms. Compared to CHBs, the ripple current of CHB^2 is substantially reduced. Parameter studies show that the proposed methods are most beneficial for low on-state transistor impedance and high battery ESR.

On the control side, the proposed methods are easy to implement and work on any output frequency as well as modulation index. On the hardware side, the CHB^2 demands no more silicon or passive components compared to a CHB counterpart.

Appendix

A. Conduction Losses

The conduction losses of the CHB and CHB^2 are

$$E_{\mathrm{CHB}} = \underbrace{E^{\mathrm{CHB}}_{\mathrm{b(dc)}} + E^{\mathrm{CHB}}_{\mathrm{b(ac1)}}}_{\text{battery}} + \underbrace{E^{\mathrm{CHB}}_{\mathrm{t(ac1)}}}_{\text{transistor}}$$

$$E_{\mathrm{CHB^2}} = \underbrace{E^{\mathrm{CHB}^2}_{\mathrm{b(dc)}} + E^{\mathrm{CHB}^2}_{\mathrm{b(ac1)}} + E^{\mathrm{CHB}^2}_{\mathrm{b(ac2)}}}_{\text{battery}} + \underbrace{E^{\mathrm{CHB}^2}_{\mathrm{t(ac1)}} + E^{\mathrm{CHB}^2}_{\mathrm{t(ac2)}}}_{\text{transistor}}$$

where "ac1" denotes the fundamental ac component; "ac2" denotes high-frequency ac components due to parallelization and energy transfer, which only show up in CHB^2. Furthermore

$$E^{\mathrm{CHB}}_{\mathrm{b(dc)}} = E^{\mathrm{CHB}^2}_{\mathrm{b(dc)}}\,,\; E^{\mathrm{CHB}}_{\mathrm{t(ac1)}} = E^{\mathrm{CHB}^2}_{\mathrm{t(ac1)}}$$

under matched operating condition and component budgets. Ruling out these identical parts, we only need to compare

$$E'_{\mathrm{CHB}} = E^{\mathrm{CHB}}_{\mathrm{b(ac1)}}\; vs.\; E'_{\mathrm{CHB^2}} = E^{\mathrm{CHB}^2}_{\mathrm{b(ac1)}} + E^{\mathrm{CHB}^2}_{\mathrm{b(ac2)}} + E^{\mathrm{CHB}^2}_{\mathrm{t(ac2)}}.$$

E'_{CHB2} is precisely the conduction loss of the circuit model in Fig. 2(a), for which we denote $\mathbf{i} = [i_1, i_2, \ldots, i_N]^{\mathrm{T}}$ to gather all currents flowing out of each module's energy storage elements. Current $\boldsymbol{i}$ represents the circulating current due to power transfer. Since i_Δ is the fundamental ac current enforced by the load, the battery currents are $\mathbf{i}_{\mathrm{b}} = i_\Delta \mathbf{1} - \boldsymbol{i}$, where $\mathbf{1}$ is a column vector of 1's. For simplicity, we equalize the momentary modulation index for all modules. According to the circuit model in Fig. 2(a), the currents are solved by

$$\mathbf{i} = i_\Delta \left(I + \tfrac{r_{\mathrm{eq}}}{r_{\mathrm{b}}} M\right)^{-1} \mathbf{1}$$

where

$$M = \begin{bmatrix} 1 & 1 & \ldots & 1 \\ 1 & 2 & \ldots & 2 \\ \vdots & \vdots & \ddots & \vdots \\ 1 & 2 & \ldots & N \end{bmatrix}.$$

Importantly, M is symmetrical and can be diagonalized as $M = V^{\mathrm{T}} D V$, where V is a real orthogonal matrix and D is diagonal. Therefore

$$\begin{aligned} E^{\mathrm{CHB}^2}_{b(\mathrm{ac1})} + E^{\mathrm{CHB}^2}_{b(\mathrm{ac2})} &= r_b \mathbf{i}_b{}^{\mathrm{T}} \mathbf{i}_b \\ &= r_b {i_\Delta}^2 \left\| \left(I - \left(I + \tfrac{r_{\mathrm{eq}}}{r_b} M \right)^{-1} \right) \mathbf{1} \right\|_2^2 \\ &= r_b {i_\Delta}^2 \cdot (V\mathbf{1})^{\mathrm{T}} \left(I - \left(I + \tfrac{r_{\mathrm{eq}}}{r_b} D \right)^{-1} \right)^2 V\mathbf{1}. \end{aligned}$$

Similarly

$$\begin{aligned} E^{\mathrm{CHB}^2}_{t(\mathrm{ac2})} = r_{\mathrm{eq}} i^{\mathrm{T}} i &= r_{\mathrm{eq}} {i_\Delta}^2 \left\| U \left(I + \tfrac{r_{\mathrm{eq}}}{r_b} M \right)^{-1} \mathbf{1} \right\|_2^2 \\ &= r_{\mathrm{eq}} {i_\Delta}^2 \cdot (V\mathbf{1})^{\mathrm{T}} D \left(I + \tfrac{r_{\mathrm{eq}}}{r_b} D \right)^{-2} V\mathbf{1}. \end{aligned}$$

Together

$$\begin{cases} E'_{\mathrm{CHB^2}} = E^{\mathrm{CHB}^2}_{\mathrm{b(ac1)}} + E^{\mathrm{CHB}^2}_{\mathrm{b(ac2)}} + E^{\mathrm{CHB}^2}_{\mathrm{t(ac2)}} = r_{\mathrm{b}} {i_\Delta}^2 (V\mathbf{1})^{\mathrm{T}} \Lambda V\mathbf{1}, \\ \Lambda = \tfrac{r_{\mathrm{eq}}}{r_{\mathrm{b}}} D \left(I + \tfrac{r_{\mathrm{eq}}}{r_{\mathrm{b}}} D \right)^{-1}. \end{cases} \tag{11}$$

One the other hand, for CHB

$$E'_{\mathrm{CHB}} = N r_b {i_\Delta}^2. \tag{12}$$

Remark: The above derivations are based on Fig. 2(a), which averages out high-frequency components in $\boldsymbol{i}$ and $\boldsymbol{i}_{\mathrm{b}}$. One should not take $r_{\mathrm{b}} \boldsymbol{i}_{\mathrm{b}}{}^{\mathrm{T}} \boldsymbol{i}_{\mathrm{b}}$ and $r_{\mathrm{eq}} \boldsymbol{i}^{\mathrm{T}} \boldsymbol{i}$ for granted due to the involvement of quadratic computations. The battery loss $r_{\mathrm{b}} \boldsymbol{i}_{\mathrm{b}}{}^{\mathrm{T}} \boldsymbol{i}_{\mathrm{b}}$ is indeed accurate because $\boldsymbol{i}_{\mathrm{b}}$ does not contain switching frequencies thanks to the filter capacitor. The transistor part $r_{\mathrm{eq}} \boldsymbol{i}^{\mathrm{T}} \boldsymbol{i}$ is also accurate because $r_{\mathrm{eq}} \boldsymbol{i}^{\mathrm{T}} \boldsymbol{i} = (1-|m|) 4 r_{\mathrm{on}} \boldsymbol{i}^{\mathrm{T}} / (1-|m|) \cdot \boldsymbol{i} / (1-|m|)$, where the right hand side spells out the transient conduction loss during switchings.

B. Proof of $E_{CHB2} < E_{CHB}$

Comparing E_{CHB2} and E_{CHB} amounts to comparing E'_{CHB2} and E'_{CHB}, which, according to (11)–(12), amounts to comparing two scalars $(V\mathbf{1})^{\mathrm{T}} \Lambda (V\mathbf{1})$ and N. From (11) we know Λ is a diagonal matrix; denote its maximum entry as $\Lambda_{(\max)}$. Therefore

$$(V\mathbf{1})^{\mathrm{T}} \Lambda V\mathbf{1} = (V\mathbf{1}, \Lambda V\mathbf{1}) \le \Lambda_{(\max)} (V\mathbf{1}, V\mathbf{1}) = N \Lambda_{(\max)}$$

where the inequality comes from Rayleigh quotient. The final missing step is to show $\Lambda_{(\max)} < 1$; we notice that matrix M can be written as $M = U^{\mathrm{T}} U$, where U is an upper triangular matrix of 1's. Since U is invertible, M is positive definite, meaning all diagonal entries of D are positive. According to (11), $0 < \Lambda_{(\max)} < 1$. Putting everything together

$$\begin{aligned} E_{\mathrm{CHB^2}} - E_{\mathrm{CHB}} &= E'_{\mathrm{CHB^2}} - E'_{\mathrm{CHB}} \\ &= r_b {i_\Delta}^2 \left(\mathbf{1}^{\mathrm{T}} V^{\mathrm{T}} \Lambda V\mathbf{1} - N \right) < 0. \end{aligned}$$

■

Remark: Relation $E_{\mathrm{CHB2}} < E_{\mathrm{CHB}}$ merely depends on the properties of M and hence the topology of CHB^2. Circuit parameters and modulation settings such as $r_{\mathrm{eq}}(r_{\mathrm{on}})$, r_b do not change

the fact that $E_{\mathrm{CHB2}} < E_{\mathrm{CHB}}$. Nevertheless, (11) indicates that the CHB^2's loss increases with ratio r_{eq}/r_b. As r_{eq}/r_b increases (e.g., either due to large r_{on} or less time in parallel states), $E_{\mathrm{CHB2}} \to E_{\mathrm{CHB}}$ asymptotically. Finally, note that the above result assumes equal modulation index for all modules, which, according to (5), may not fully exploit the advantages of CHB^{2}s.

REFERENCES

[1] L. Baruschka and A. Mertens, "Comparison of cascaded H-bridge and modular multilevel converters for BESS application," in *Proc. IEEE Energy Convers. Congr. Expo.: Energy Convers. Innov. Clean Energy Future*, 2011, pp. 909–916.

[2] G. Wang *et al.*, "A review of power electronics for grid connection of utility-scale battery energy storage systems," *IEEE Trans. Sustain. Energy*, vol. 7, no. 4, pp. 1778–1790, Oct. 2016.

[3] H. Akagi and L. Maharjan, "A battery energy storage system based on a multilevel cascade PWM converter," in *Proc. Brazilian Power Electron. Conf.*, 2009, pp. 9–18.

[4] L. Maharjan, T. Yamagishi, H. Akagi, and J. Asakura, "Fault-tolerant operation of a battery-energy-storage system based on a multilevel cascade PWM converter with star configuration," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2386–2396, Sep. 2010.

[5] M. Vasiladiotis and A. Rufer, "Analysis and control of modular multilevel converters with integrated battery energy storage," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 163–175, Jan. 2015.

[6] J. Asakura and H. Akagi, "State-of-charge (SOC)-balancing control of a battery energy storage system based on a cascade PWM converter," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1628–1636, Jun. 2009.

[7] M. Tsirinomeny and A. Rufer, "Configurable modular multilevel converter (CMMC) for flexible EV," in *Proc. 17th Eur. Conf. Power Electron. Appl.*, 2015, pp. 1–8.

[8] Z. Gao and Q. Lu, "A hybrid cascaded multilevel converter based on three-level cells for battery energy management applied in electric vehicles," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7326–7349, Jul. 2019.

[9] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, 1999.

[10] J. Rodriguez, P. W. Hammond, J. Pontt, R. Musalem, P. Lezana, and M. J. Escobar, "Operation of a medium-voltage drive under faulty conditions," *IEEE Trans. Ind. Electron.*, vol. 52, no. 4, pp. 1080–1085, Aug. 2005.

[11] W. Song and A. Q. Huang, "Control strategy for fault-tolerant cascaded multilevel converter based STATCOM," in *Proc. APEC 22nd Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2007, pp. 1073–1076.

[12] Sanmin Wei, Bin Wu, Fahai Li, and Xudong Sun, "Control method for cascaded H-bridge multilevel inverter with faulty power cells," in *Proc. APEC 18 th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2003, vol. 1, pp. 261–267.

[13] J. I. Y. Ota, T. Sato, and H. Akagi, "Enhancement of performance, availability, and flexibility of a battery energy storage system based on a modular multilevel cascaded converter (MMCC-SSBC)," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2791–2799, Apr. 2016.

[14] J. Svensson, "Improved power system stability and reliability using innovative energy storage technologies," in *Proc. 8th IEE Int. Conf. AC and DC Power Transmiss.*, 2006, vol. 2006, pp. 220–224.

[15] Y. Iijima *et al.*, "Development and field experiences of NAS battery inverter for power stabilization of a 51 MW wind farm," in *Proc. ECCE Asia Int. Power Electron. Conf.* 2010, pp. 1837–1841.

[16] H. Li, Y. Iijima, and N. Kawakami, "Development of power conditioning system (PCS) for battery energy storage systems," in *Proc. IEEE ECCE Asia Downunder - 5th IEEE Annu. Int. Energy Convers. Congr. Exhib.*, 2013, pp. 1295–1299.

[17] L. H. Walker, "10-MW GTO converter for battery peaking service," *IEEE Trans. Ind. Appl.*, vol. 26, no. 1, pp. 63–72, Jan./Feb. 1990.

[18] N. W. Miller, R. S. Zrebiec, G. Hunt, and R. W. Deimerico, "Design and commissioning of a 5 MVA, 2.5 MWh battery energy storage system," in *Proc. Transmiss. Distribution Conf. Expo.*, 2002, pp. 339–345.

[19] M. Hagiwara, K. Nishimura, and H. Akagi, "A medium-voltage motor drive with a modular multilevel PWM inverter," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1786–1799, Jul. 2010.

[20] K. Qian, C. Zhou, Y. Yuan, and M. Allan, "Temperature effect on electric vehicle battery cycle life in vehicle-to-grid applications," in *Proc. China Int. Conf. Electricity Distribution*, 2010, pp. 1–6.

[21] J. M. Tarascon, A. S. Gozdz, C. Schmutz, F. Shokoohi, and P. C. Warren, "Performance of Bellcore's plastic rechargeable Li-ion batteries," *Solid State Ionics*, vol. 86–88, pp. 49–54, Jul. 1996.

[22] A.. Ruddell *et al.*, "Analysis of battery current microcycles in autonomous renewable energy systems," *J. Power Sources*, vol. 112, no. 2, pp. 531–546, Nov. 2002.

[23] T. Note and B. Continuity, "Effects of AC ripple current on VRLA battery life," Emerson Network Power, St. Louis, MO, USA, Tech. Note, 2013.

[24] C. Ropeter, H. Wenzl, H. Beck, and E. A. Wehrmann, "The impact of microcycles on batteries in different applications," in *Proc. 18th Int. Electric Vehicle Symp.,* Berlin, Germany, 2001.

[25] R. F. Nelson and M. A. Kepros, "AC ripple effects on VRLA batteries in float applications," in *Proc. 14th Annu. Battery Conf. Appl. Advances Conf.*, 2008, pp. 281–289.

[26] A. I. Harrison, "Batteries and AC phenomena in UPS systems: the battery point of view," in *Proc. 11th Int. Telecommun. Energy Conf.*, 1989, pp. 12.5/1–12.5/6.

[27] O. Satilmis and E. Mese, "Investigating DC link current ripple and PWM modulation methods in electric vehicles," in *Proc. 3rd Int. Conf. Electric Power Energy Convers. Syst.*, 2013, pp. 1–6.

[28] M. Vasiladiotis, "Modular multilevel converters with integrated split battery energy storage," No. THESIS. EPFL, 2014.

[29] I. Trintis, S. Munk-Nielsen, and R. Teodorescu, "Cascaded H-bridge with bidirectional boost converters for energy storage," in *Proc. 14th Eur. Conf. Power Electron. Appl.*, 2011, pp. 1–9.

[30] X. Zhou, X. Yu, S. Lukic, and A. Huang, "LCL filter utilized in battery charging applications to achieve compact size and low ripple charging," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2012, pp. 660–665.

[31] I. Trintis, S. Munk-Nielsen, and R. Teodorescu, "A new modular multilevel converter with integrated energy storage," in *Proc. IECON 37th Annu. Conf. IEEE Ind. Electron. Soc.*, 2011, pp. 1075–1080.

[32] X. Liu, H. Li, and Z. Wang, "A fuel cell power conditioning system with low-frequency ripple-free input current using a control-oriented power pulsation decoupling strategy," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 159–169, Jan. 2014.

[33] L. He, K. Zhang, J. Xiong, S. Fan, and Y. Xue, "Low-frequency ripple suppression for medium-voltage drives using modular multilevel converter with full-bridge submodules," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 657–667, Jun. 2016.

[34] A. Antonopoulos, L. Ängquist, S. Norrga, K. Ilves, L. Harnefors, and H. P. Nee, "Modular multilevel converter AC motor drives with constant torque from zero to nominal speed," *IEEE Trans. Ind. Appl.*, vol. 50, no. 3, pp. 1982–1993, May 2014.

[35] M. Vasiladiotis, N. Cherix, and A. Rufer, "Accurate capacitor voltage ripple estimation and current control considerations for grid-connected modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4568–4579, Sep. 2014.

[36] M. Hagiwara, I. Hasegawa, and H. Akagi, "Start-up and low-speed operation of an electric motor driven by a modular multilevel cascade inverter," *IEEE Trans. Ind. Appl.*, vol. 49, no. 4, pp. 1556–1565, Jul. 2013.

[37] Z. Li, R. Lizana, S. M. Lukic, A. V. Peterchev, and S. M. Goetz, "Current injection methods for ripple-current suppression in delta-configured split-battery energy storage," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7411–7421, Aug. 2019.

[38] S. M. Goetz, A. V. Peterchev, and T. Weyh, "Modular multilevel converter with series and parallel module connectivity: Topology and control," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 203–215, Jan. 2015.

[39] Z. Li, R. Lizana, A. V. Peterchev, and S. M. Goetz, "Ripple current suppression methods for star-configured modular multilevel converters," in *Proc. IECON 43rd Annu. Conf. IEEE Ind. Electron. Soc.*, 2017, no. 1, pp. 1505–1510.

[40] Z. Li, R. Lizana, S. Sha, Z. Yu, A. V. Peterchev, and S. M. Goetz, "Module implementation and modulation strategy for sensorless balancing in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8405–8416, Sep. 2019.

[41] S. M. Goetz, Z. Li, X. Liang, C. Zhang, S. M. Lukic, and A. V. Peterchev, "Control of modular multilevel converter with parallel connectivity—Application to battery systems," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8381–8392, Nov. 2017.

[42] S. M. Goetz, Z. Li, A. V. Peterchev, X. Liang, C. Zhang, and S. M. Lukic, "Sensorless scheduling of the modular multilevel series-parallel converter: Enabling a flexible, efficient, modular battery," in *Proc. Conf. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 2349–2354.

[43] Z. Li, R. Lizana, A. V. Peterchev, and S. M. Goetz, "Distributed balancing control for modular multilevel series/parallel converter with capability of sensorless operation," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2017, pp. 1787–1793.

[44] D. G. Holmes, "The significance of zero space vector placement for carrier-based PWM schemes," *IEEE Trans. Ind. Appl.*, vol. 32, no. 5, pp. 1122–1129, Sep./Oct. 1996.
[45] N. O. Çetin and A. M. Hava, "Scalar PWM implementation methods for three-phase three-wire inverters," in *Proc. ELECO 6th Int. Conf. Electr. Electron. Eng.*, 2009, pp. 447–451.
[46] A. Iqbal, E. Levi, M. Jones, and S. N. Vukosavic, "Generalised sinusoidal PWM with harmonic injection for multi-phase VSIs," in *Proc. –37th Annu. Power Electron. Specialist Conf.*, 2006.
[47] J. Jose, G. N. Goyal, and M. V. Aware, "Improved inverter utilisation using third harmonic injection," in *Proc. Joint Int. Conf. Power Electron., Drives Energy Syst.*, 2010.
[48] W. Zheng, C. Zhu, Z. Zeng, Q. Yuan, H. Yang, and R. Zhao, "An optimized algorithm for SVPWM based on three-phase stationary frame," in *Proc. IEEE Ind. Appl. Soc. Annu. Meeting*, 2015.
[49] P. Sochor and H. Akagi, "Theoretical comparison in energy-balancing capability between star- and delta-configured modular multilevel cascade inverters for utility-scale photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1980–1992, Mar. 2016.
[50] Z. Li, R. Lizana, Z. Yu, S. Sha, A. V. Peterchev, and S. Goetz, "A modular multilevel series/parallel converter for wide frequency range operation," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9854–9865, Oct. 2019.
[51] J. N. Snyder and F. C. Grover, *Inductance Calculations Working Formulas and Tables*, vol. 18, Chelmsford, MA, USA: Courier Corporation, 2006.
[52] H. Fujita, S. Tominaga, and H. Akagi, "Analysis and design of a DC voltage-controlled static var compensator using quad-series voltage-source inverters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 4, pp. 970–978, 1996.

Zhongxi Li (Student Member, IEEE) received the B.S. degree from the Department of Electrical Engineering, Tsinghua University, Beijing, China, in 2015. He is currently working toward the Ph.D. degree with Duke University, Durham, NC, USA.

He was a Visiting Scholar with FREEDM Systems Center at NC State University, Raleigh, NC, USA, where he worked on multilevel converters, and CURENT Engineering Research Center at the University of Tennessee, Knoxville, TN, USA, where he worked on testing wide-bandgap semiconductor switches. His research interests include modular pulse synthesizers for magnetic neurostimulation and noninvasive brain stimulation as well as design and control of modular multilevel converters.

Ricardo Lizana (Member, IEEE) was born in Rancagua, Chile, in 1985. He received the M.Sc. and D.Sc. degrees in electronic engineering from Universidad Tecnica Federico Santa Maria, Valparaiso, Chile, in 2011 and 2015, respectively.

In 2015, he joined the Universidad Catolica de la Santisima Concepcion, Concepcion, Chile, where he is currently a Lecturer with the Departamento de Ingenieria Electrica (DIE). In 2017, he was a Postdoctoral Fellow at Duke University, Durham, NC, USA. His main research interests include high power converters, HVdc transmission systems and renewable energy systems.

Dr. Lizana received the Ph.D. Scholarship from the Chilean National Commission for Scientific and Technological Research (CONICYT) in 2011, the Emerging Leaders in the Americas Program Scholarship from the Canadian Bureau for International Education in 2012, and the Second-Best Paper Award from the IEEE TRANSACTIONS ON POWER ELECTRONICS in 2015.

Zhujun Yu received the B.S. degree in 2018 from the department of Electrical Engineering, Tsinghua University, Beijing, China, where she is currently working toward the Ph.D. degree in electrical engineering.

She was a Visiting Scholar at BSEL Lab, Duke University, where she worked on multilevel converters. Her research interests include simulation of power electronic systems and control strategies of power converters.

Sha Sha received the B.S. degree from the Department of Electrical Engineering, Tsinghua University, Beijing, China, in 2018. She is a currently working toward the master's degree in electrical engineering with the California Institute of Technology, Pasadena, CA, USA.

She was a Visiting Scholar at BSEL Lab, Duke University, Durham, NC, USA, where she worked on multilevel converters. Her research interests include power electronics and routing for power grid based on power routers.

Angel V. Peterchev (Senior Member, IEEE) received the A.B. degree in physics and engineering sciences from Harvard University, Cambridge, MA, USA, in 1999, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley, CA, USA, in 2002 and 2005, respectively.

He is presently an Associate Professor with tenure in the Departments of Psychiatry & Behavioral Sciences, Electrical & Computer Engineering, Biomedical Engineering, and Neurosurgery at Duke University. Previously, he was an Assistant Professor with Columbia University and has also worked at the Portable Power Systems Group, National Semiconductor Corp. (now Texas Instruments). His research interests include the design, modeling, and optimization of systems for noninvasive brain stimulation and for electrical energy conversion. In the field of brain stimulation, he has contributed to novel devices, modeling, and experimental studies of transcranial magnetic and electric stimulation. In the field of energy, he has contributed to the development of control systems and topologies for fast, efficient power converters including applications to microprocessor power supplies, portable electronics, integrated magnetics, and modular multilevel converters.

Stefan M. Goetz (Member, IEEE) received the undergraduate and graduate degrees from TU Muenchen, Germany. He received the doctoral training at TU Muenchen as well as Columbia University, and received the Ph.D. degree from TU Muenchen, in 2012.

He is currently an Assistant Professor with Duke University. His research interests include precise high-power pulse synthesizers for magnetic neurostimulation and noninvasive brain stimulation as well as integrative power electronics solutions for microgrids and electric vehicle applications.

Dr. Goetz was the recipient of a Ph.D. thesis prize from TU Muenchen for a thesis on medical applications of power electronics.