Letters

Isolated Ultrafast Gate Driver with Variable Duty Cycle for Pulse and VHF Power Electronics

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***Abstract*—Ultrafast and isolated gate drivers advance the development of pulse and very high frequency power electronics for applications that include LiDAR, space systems, miniaturized hardware, and testing of emerging ultrafast devices. The isolated ultrafast gate driver in this letter achieves a gate voltage slew rate above 12 GV/s with rise and fall times below 260 ps with the proper choice of components. Magnetic isolation provides transient immunity and positive feedback enables dynamic dc restoration to allow arbitrarily long ON- and OFF-times and preserve variable duty cycles. With the isolated ultrafast gate driver, an EPC 2038 GaN FET achieves a drain voltage slew rate of over 37 GV/s when hard-switching and improves total efficiency by 8% (including gating loss) with a careful choice of logic inverters in a symmetric 100 MHz current-mode class D (CMCD) wireless power transfer system. The ultrafast gate driver with isolation and positive feedback was implemented with a commercial radio frequency signal transformer and discrete logic inverters and validated in a hard-switching double pulse test, a narrow pulse test repeating at 165 MHz, and a 100 MHz soft-switching CMCD resonant converter.**

***Index Terms*—Current-mode class D (CMCD), double pulse test (DPT), GaN, gate driver, isolation, LiDAR, positive feedback, pulse, ultrafast, very high frequency (VHF).**

I. Introduction

ULTRAFAST gate drivers are needed in LiDAR for range accuracy and resolution [1], [2], in very high frequency (VHF) for minimizing loss and expanding the range of operation [3], [4], in space applications for increasing reliability through isolation [5], and in the double pulse test (DPT) of emerging ultrafast devices including new generations of GaN [6], [7]. The specific requirements and challenges in the isolated ultrafast gate driver design include:

(1) *Ultrafast slew rate* to ensure fast switching transitions that are needed for narrow pulses and VHF so that the transitions do not excessively limit the minimum ON- and OFF-times and dominate the switching periods. Fast switching transitions also reduce switching losses in pulsewidth modulation (PWM) converters [8]–[10] and in the turn-OFF of resonant converters like current-mode class D (CMCD) converters [11], [12].

(2) *Isolation* to separate the control signal from the gate so that the gate drive voltage can be referenced to the same potential as the source terminal of the power device, which is particularly a concern in high-side switches. In addition to the isolation of the gate driver control signal, high-side drivers require isolated power supplies, which is challenging at VHF because of coupling capacitance. A 75 MHz high-side gate driver had been demonstrated in [10] using isolated power supplies. Even in ground-referenced power switches, isolation provides immunity from the source inductance combined with high di/dt (from high currents and/or fast transitions), which can cause power device mistriggering when the transients exceed the threshold voltage; this can be especially problematic in devices where the ON-state and OFF-state gate drive voltages are adversely limited by low gate breakdown voltages. Compared to other isolation methods, transformer coupling typically provides better common-mode immunity at high speeds.

(3) *Variable frequency, duty cycle, and arbitrarily long on- and off-times* to adjust frequency, pulsewidth, zero voltage switching timing, dead time, or overlap for voltage/current modulation or because of parasitics and component tolerance, temperature variation, and nonlinearity in both pulse [1], [2], [6], [7], PWM [5], [8], [10], and resonant converters [3], [4], [11]–[13]. During start-up or closed-loop control conditions, arbitrary duration pulses are often necessary to drive the gate when the converter deviates from steady-state operation. To preserve duty cycle and arbitrarily long ON- and OFF-times, high-speed isolation methods (e.g., capacitive or transformer coupling) will require a method for dynamic dc restoration.

(4) *Flexible control inputs* to interface with ultrahigh-speed controllers and logic that operate at lower voltages, require impedance matching, render differential signaling, or are susceptible to loading conditions.

(5) *Small gating loss* to mitigate the escalating losses from switching devices at VHF, where gating loss can be as much as 40% of the loss budget at 30 MHz [4].

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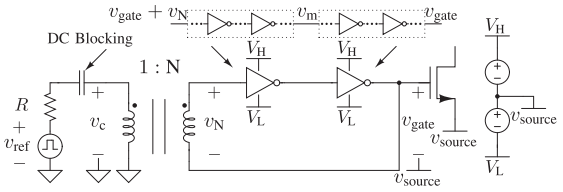

Fig. 1. Isolated ultrafast gate driver architecture uses a transformer and logic inverters with positive feedback. Inverters could be a composite of cascaded and scaled inverters. In the hardware implementation, the turns ratio of the transformer is 1:2 and the logic inverter pair has one logic inverter per stage with a single-ended control signal.

In contrast to the new isolated ultrafast gate driver described in this letter, prevailing state-of-the-art gate drivers meet some, but not all of these requirements. In particular, as transition times approach 100 ps and as switching frequencies reach deeper into VHF, isolation together with arbitrarily long ON- and OFF-times, to our knowledge, had not been achieved. Methods using transformer isolation can transmit fast pulses at VHF with small propagation delay but cannot sustain arbitrarily long pulses [14]. Commercial gate drivers like the TI LMG1020 can operate at switching frequencies up to 60 MHz with 400 ps typical rise and fall times. A resonant gate driver is a prevailing choice for reducing the gating loss at VHF [4], [13] but usually exacerbates the time interval in the "linear region" of the power device [3], [4] and can result in higher loss regardless of whether the gate waveform is sinusoidal [13] or trapezoidal [4], [13]. Also, resonant gate drivers usually have a fixed frequency and duty cycle for a particular configuration and set of components. Sinusoidal, trapezoidal, and hard-switching gate drivers have been demonstrated at 100 MHz and above [3], [8], [13] but at lower slew rates and without isolation. Commercial digital isolators have been used at 27.12 MHz [11] and 75 MHz [10]; because of low slew rates, they cannot transmit very short pulses and have a limited maximum operational frequency with relatively large propagation delay.

In this letter, we present an architecture for an isolated ultrafast gate driver and hardware examples that allow arbitrarily long ON- and OFF-times yet capable of 1) below 260 ps rise and fall times, 2) isolation with dynamic dc restoration, and 3) variable frequency and duty cycle preservation. We perform a double pulse test (DPT) with hard-switching and investigate operation in a current-mode class D (CMCD) resonant converter operating at 100 MHz with EPC 2038. In addition, hardware results show that a pulse repetition rate at 165 MHz is possible and that a design driving a higher power GaN FET at 100 MHz with 16× higher gate charge than the EPC 2038 with rise and fall times below 270 ps is implementable.

II. Operation

A. Isolated Ultrafast Gate Driver Architecture

The isolated ultrafast gate driver in this letter is shown in Fig. 1, which consists of a broadband signal transformer and composite logic inverters with an even number of stages. The transformer provides isolation, boosts the control signal v_c by the turns ratio 1:N, and matches impedance if necessary. The control voltage v_c could be either single-ended or differential (single-ended in Fig. 1). The composite logic inverters have input voltage ($v_N + v_{gate}$), intermediate voltage v_m between the pair, and output voltage v_{gate}, which drives the power device and is also connected to the secondary winding of the transformer to provide positive feedback for *dynamic dc restoration*, where the offset dc voltage to the transformer secondary depends on the output state. This results in the gate driver output state being held despite the inevitable voltage decay or *droop* in the secondary winding. Volt-second balance of the transformer and charge balance of the dc blocking capacitor eventually cause droop.

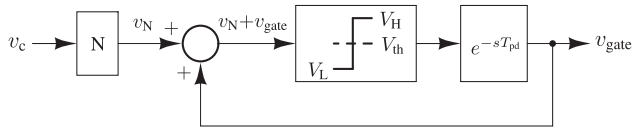

Fig. 2. Block diagram of the positive feedback mechanism in the isolated ultrafast gate driver architecture.

The aggregate propagation delay from v_{in} to v_{gate} in the forward path is T_{pd}, which is the sum of the propagation delays of the logic inverters. Each logic inverter is powered by V_H and V_L. The inputs to the logic inverters are clamped with the restrictions on clamp voltages enforced to be $V_{clampL} < V_L$ and $V_{clampH} > V_H$ for proper operation.

Each composite logic inverter can be implemented, for example, in an integrated circuit, as a composite of cascaded inverters each with scaled devices to minimize aggregate propagation delay for a particular current drive required by a power device. In discrete implementations, parallel inverters can be used to increase the current drive.

B. Waveforms

Some simplifying assumptions are used to assist with analysis.

1) The transformer maintains the voltage relationship from the turns ratio instantaneously across the primary and secondary windings because leakage inductance is negligible so that $v_N(t) = N\, v_c(t)$.
2) The logic inverter threshold is $V_{th} = \frac{1}{2}(V_H + V_L)$.
3) Successful triggering of the first logic inverter input with ($v_N + v_{gate}$) exceeding the threshold V_{th} results in positive feedback after a delay of T_{pd}, as shown in Fig. 2.

The effect of leakage inductance is described in Section III-A.

1) Periodic Short-Pulse Operation: We define periodic short-pulse operation as the periodic steady-state regime where ON- and OFF-times are sufficiently short so that the voltage droop on the transformer secondary is negligible.

The following analysis assumes that the logic inverters are unclamped for ease of explanation; this simplification can be justified by the fact that the timing of the edges is unchanged for the clamped case. Assuming a midpoint threshold voltage V_{th} helps illustrate the operating principles through a straightforward analysis; in reality, the threshold voltages may be different for low-to-high and high-to-low transitions, which can be accounted by a change in ON-time and OFF-time durations and an

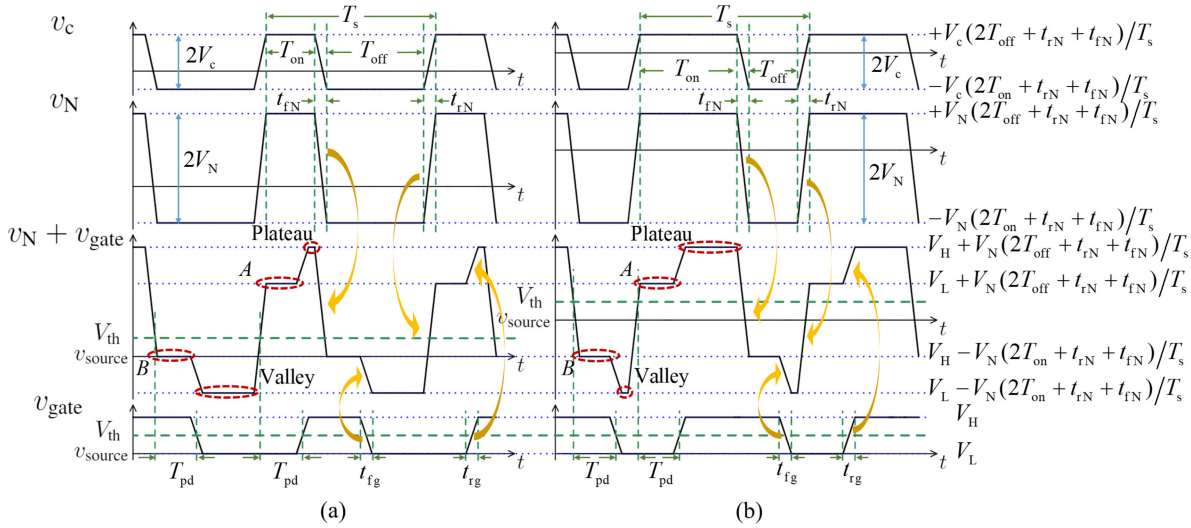

Fig. 3. Steady-state waveforms of the isolated ultrafast gate driver operating in the periodic short-pulse regime at (a) equal to or below 50% duty cycle and (b) above 50% duty cycle.

asymmetry in rise and fall propagation delays. Fig. 3 represents the steady-state waveforms of the periodic short-pulse regime of the isolated ultrafast gate driver when the duty cycle is equal to or below 50% in Fig. 3(a) and when the duty cycle is above 50% in Fig. 3(b).

The input voltage for the composite of cascaded logic inverters ($v_N + v_{gate}$) is crucial in determining the behavior; this consists of a periodic waveform usually with four voltage levels: A plateau, a valley, ledge A on the rise, and ledge B on the fall. The voltage quantities that are labeled in Fig. 3 are referenced to the source voltage v_{source} and are a function of ON-time T_{on}, OFF-time T_{off}, rise time t_{rN}, and fall time t_{fN}. The peak-to-peak values of v_c and v_N are $2V_c$ and $2V_N$, respectively. Ledge A on the rise of ($v_N + v_{gate}$) results from the combination of the rise of v_N and from the positive feedback of the subsequent rise of v_{gate}. Similarly, ledge B results from the combination of the fall of v_N and the fall of v_{gate}.

2) Arbitrary Long-Pulse Operation: We define arbitrary long-pulse operation as the regime where arbitrarily long ON- or OFF-times have resulted in the decay of the transformer secondary voltage to nearly zero. Volt-second balance of the transformer and charge balance of the dc blocking capacitor eventually cause the decay. A well-known gate driver circuit [15] without dynamic dc restoration from positive feedback is shown in Fig. 4(b); droop eventually results in a mistrigger and the output voltage does not hold its state as shown in Fig. 4(a).

The isolated ultrafast gate driver with positive feedback allows dynamic dc restoration, which preserves the arbitrarily long ON- and OFF-times of t_1, t_2, and t_3 in Fig. 5 using the same reference signal as Fig. 4(a). To simplify the description of the operation with dynamic dc restoration, we assume that the pulse starts with the initial voltage in the transformer having had decayed to zero and that the voltage at the logic inverter is at a valid logic voltage state (V_L in Fig. 5). A rising edge from the reference signal v_{ref} manifests as a rising on the logic inverter input voltage ($v_N + v_{gate}$), which subsequently decays with time constant τ.

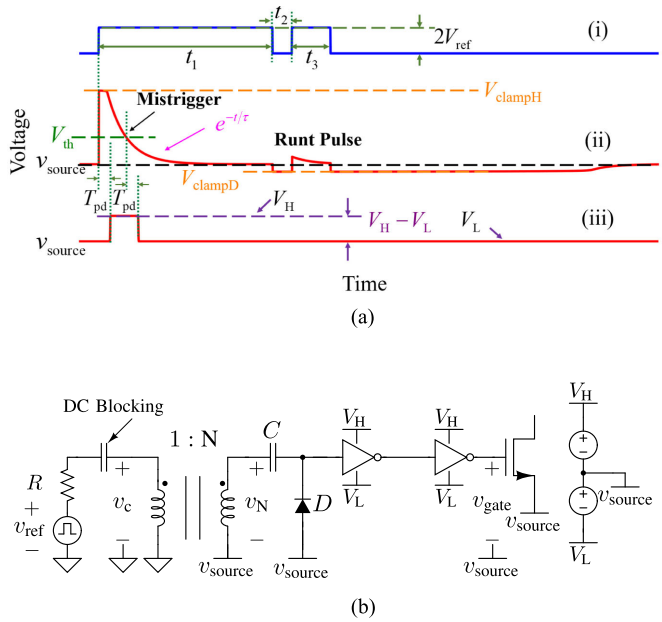

Fig. 4. Time-domain waveforms illustrate arbitrary long-pulse behavior for the well-known circuit in [15, p. 32]. Voltage droop causes the gate driver output to not sustain for the duration of the long reference signal pulse, which also causes mistriggering in subsequent pulses. (a) Waveforms: (i) reference signal v_{ref}; (ii) logic inverter input voltage ($v_N + v_{gate}$); (iii) gate driver output voltage v_{gate}. (b) Circuit.

A second rising edge at the input of the logic inverter manifests from the positive feedback from the gate driver output after the composite propagation delay T_{pd}. This positive feedback creates an offset to the transformer secondary voltage that remains even after the voltage across the secondary winding voltage v_N has drooped to zero, hence holding the input to the logic inverter at a valid logic state (V_H in Fig. 5). This valid input V_H holds a valid V_H at the gate driver output indefinitely until a falling edge from the reference signal. The behavior is similar for a V_H to V_L pulse.

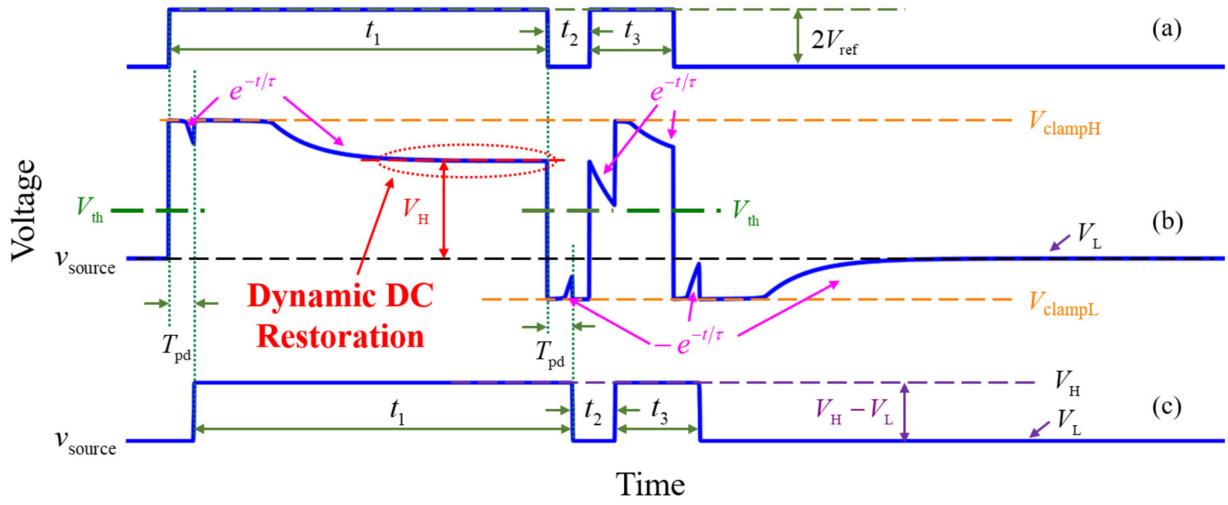

Fig. 5. Time domain diagrams of the isolated ultrafast gate driver illustrate behavior from a combination of a long pulse and an intermediate duration before a second pulse. (a) Reference signal v_{ref}. (b) Logic inverter input voltage ($v_{\text{N}} + v_{\text{gate}}$). (c) Gate driver output voltage v_{gate}. Note that in this figure, $V_{\text{L}} = v_{\text{source}}$.

C. Design Criteria for the Isolated Ultrafast Gate Driver

In this section, we discuss the sufficient conditions for the proper operation of this gate driver. Transformer isolation in Fig. 1 requires zero average voltage at the primary, which is ensured by a dc blocking capacitor.

1) Periodic Short-Pulse Operation: The sufficient condition for the upper bound on the aggregate propagation delay is

$$T_{\text{pd}} < \min\{T_{\text{on}}, T_{\text{off}}\} - 0.5\max\{t_{\text{rg}}, t_{\text{fg}}\} \tag{1}$$

where t_{rg} and t_{fg} are, respectively, the rise and fall times of v_{gate}, which ensures nonzero durations for the plateaus and valleys in Fig. 3. In addition, ledge B must be below the threshold V_{th} and ledge A must be above to ensure that the first logic inverter will be triggered, which requires

$$V_{\text{N}} > \frac{T_{\text{s}}}{2\left(2\cdot\min\{T_{\text{on}}, T_{\text{off}}\} + t_{\text{rN}} + t_{\text{fN}}\right)}(V_{\text{H}} - V_{\text{L}}) \tag{2}$$

where t_{rN} and t_{fN} are the rise and fall times of v_{N} shown in Fig. 3. As long as conditions (1) and (2) are maintained, voltage clamping at the input of the logic inverter does not change the trigger points even though the waveforms are modified. In choosing V_{c}, it is important to note that in practice, the transformer coupling coefficient k should be included with turns ratio N so that $V_{\text{c}} = V_{\text{N}}/k\,\text{N}$.

2) Arbitrary Long-Pulse Operation: For proper operation, the pulsewidths need to satisfy $\min\{t_1, t_2, t_3\} > T_{\text{pd}}$ from (1). There is a condition on the minimum value of the peak-to-peak open-circuit voltage at the transformer secondary

$$2V_{\text{N}} \geq V_{\text{clampH}} - V_{\text{clampL}}. \tag{3}$$

Additional conditions for arbitrary long-pulse operation are minimum and maximum limits on the droop time constant τ. The droop time constant, which can be considered as a design variable, is determined by the magnetizing inductance of the transformer and the resistance represented by R for a large dc blocking capacitor in Fig. 1. The maximum value of τ is determined by the minimum design requirement for t_1 and t_2 and the technology limitations on T_{pd} and V_{th} but can be adjusted by choice of logic levels V_{H} and V_{L}, and clamp voltages V_{clampH} and V_{clampL} if allowed by technology choice (e.g., IC design/process or discrete logic inverter)

$$\tau < \min\left\{\frac{V_{\text{clampH}} - V_{\text{H}}}{V_{\text{H}} - V_{\text{th}}}\,t_1 + \frac{V_{\text{H}} - V_{\text{L}}}{V_{\text{H}} - V_{\text{th}}}\,T_{\text{pd}},\right.$$
$$\left.\frac{V_{\text{L}} - V_{\text{clampL}}}{V_{\text{th}} - V_{\text{L}}}\,t_2 + \frac{V_{\text{H}} - V_{\text{L}}}{V_{\text{th}} - V_{\text{L}}}\,T_{\text{pd}}\right\}. \tag{4}$$

The minimum value of τ is only determined by technology limitations and voltage level choices

$$\tau > \max\left\{\frac{T_{\text{pd}}}{\ln\left(\frac{V_{\text{clampH}} - V_{\text{L}}}{V_{\text{th}} - V_{\text{L}}}\right)}, \frac{T_{\text{pd}}}{\ln\left(\frac{V_{\text{H}} - V_{\text{clampL}}}{V_{\text{H}} - V_{\text{th}}}\right)}\right\}. \tag{5}$$

Equations (4) and (5) can be combined to calculate lower bounds on t_1 and t_2 that may supersede the limit from (1)

$$t_1 > \frac{V_{\text{H}} - V_{\text{th}}}{V_{\text{clampH}} - V_{\text{H}}}T_{\text{pd}} \times \left[\frac{1}{\ln\left(\frac{V_{\text{clampH}} - V_{\text{L}}}{V_{\text{th}} - V_{\text{L}}}\right)} - \frac{V_{\text{H}} - V_{\text{L}}}{V_{\text{H}} - V_{\text{th}}}\right] \tag{6}$$

$$t_2 > \frac{V_{\text{th}} - V_{\text{L}}}{V_{\text{L}} - V_{\text{clampL}}}T_{\text{pd}} \times \left[\frac{1}{\ln\left(\frac{V_{\text{H}} - V_{\text{clampL}}}{V_{\text{H}} - V_{\text{th}}}\right)} - \frac{V_{\text{H}} - V_{\text{L}}}{V_{\text{th}} - V_{\text{L}}}\right]. \tag{7}$$

Together, (1) and (3)–(7) are a set of sufficient conditions for operation in combined long-pulse and short-pulse regimes as exemplified by Fig. 5, which is similar to a DPT. If t_1 is a long pulse, which means the current in the transformer primary converges to $2\,V_{\text{ref}}/R$, then the minimum requirement on t_2 is that the transformer has sufficiently reset before the leading edge of t_3 so that the logic inverter input voltage reaches the threshold V_{th} on this edge; it is worth noting that τ can also be considered as the transformer reset time constant. Condition (5) ensures that the input voltage of the logic inverter remains correctly asserted

after the reference signal assertion at the leading edge of t_2 through the duration of the propagation delay T_{pd} so that the positive feedback affirmatively returns the valid value asserted by the reference signal. Condition (4) is derived from the fact that the input voltage to the logic inverter, after the reference signal assertion at the leading edge of t_3, must remain correctly asserted above the threshold voltage V_{th} at the logic inverter input. The behavior of all subsequent pulses can be inferred from this same analysis.

III. Implementation and Validation

A. Signal Transformer Design

Dynamic dc restoration using positive feedback eases the signal transformer design requirements because of droop tolerance and potentially improves isolation. Droop tolerance allows lower magnetizing inductance within the limits given by (4) and (5). Together with fewer required turns, intrawinding (turn-to-turn) capacitance is decreased and higher self-resonant frequency is possible. Leakage inductance trades off with interwinding (primary–secondary coupling) capacitance. For example, bifilar windings have low leakage inductance but high interwinding capacitance, whereas 180° sector windings have the opposite; a sector wound transformer can be used to trade off leakage inductance with interwinding capacitance [16]. The maximum tolerable interwinding capacitance is application dependent; it depends on the dv/dt of v_{source} relative to control voltage ground. Two factors limit the tolerable leakage inductance.

1) The resonance formed by the secondary-referred leakage inductance and the input capacitance at the logic inverter often have a frequency whose period T_{lc} is much smaller than the minimum ON- or OFF-time

$$T_{\text{lc}} \ll \min\left\{T_{\text{on}},\, T_{\text{off}}\right\}.$$

2) The attenuated V_{c} from the voltage divider formed by the primary magnetizing inductance L_μ and leakage inductance L_{ll} must satisfy the maximum among voltages specified in (2) and (3)

$$\frac{L_\mu}{L_{\text{ll}} + L_\mu}\text{N}V_{\text{c}} > V_{\text{N}}.$$

This attenuation can be accommodated by higher control voltage V_{c}.

Dynamic dc restoration prevents droop from encroaching on the logic inverter input noise margins by maintaining a valid input state; this enables better tolerance to ringing and thus may allow higher leakage inductance, which subsequently can mean lower interwinding/coupling capacitance.

B. Component Selection

The core of the isolated ultrafast gate driver is composed of a radio frequency (RF) signal transformer and high-speed logic inverters. WBC4-14 L from Coilcraft has a turns ratio of 1:2 and a bandwidth from 1.5 MHz to 1.2 GHz. Six different logic inverters were tested as shown in Table I and Fig. 6; these inverters included buffered (*suffix xxx04*) and unbuffered (*suffix xxxU04*) variants from three companies: TI, NXP, and OnSemi. We drive an EPC 2038 GaN FET because it can be employed in pulsed lasers for LiDAR and is useful for VHF power electronics because of its small output capacitance C_{oss}. The gate charge of the EPC 2038 ($Q_{\text{g}} = 44$ pC) requires an average driving current at switching frequency f_{s} of $I_{\text{avg}} = Q_{\text{g}}\, f_{\text{s}}$, which is 4.4 mA at 100 MHz, which means that any of the individual logic inverters in Table I has the driving capability.

TABLE I
Experimental Comparison Using Dual Logic Inverters for Isolated Ultrafast Gate Drivers at 100 MHz Switching

Component (Manufacturer)	t_{r} (ps)	t_{f} (ps)	P_{loss} (mW)
SN74LVC2G04 (TI)	259	245	108
NL27WZ04 (On Semi)	255	462	120
74LVC2G04 (NXP)	228	496	146
SN74LVC2GU04 (TI)	301	686	183
NL27WZU04 (On Semi)	345	928	189
74LVC2GU04 (NXP)	273	911	220

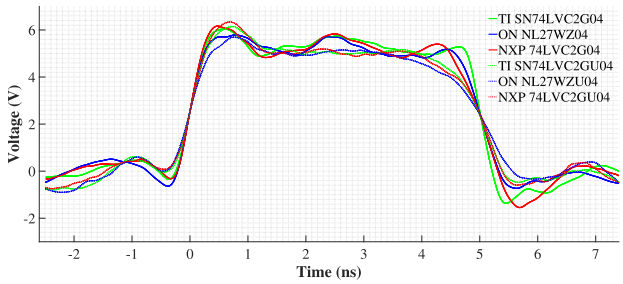

Fig. 6. Single-cycle gate voltage comparison among different dual logic inverters. The experimental data were collected with a 4 GHz measurement system with 1 TS/s sampling rate and replotted in Matlab.

Each of the logic inverters in Table I is contained in a dual package and was tested under identical conditions ($V_{\text{H}} = 5$ V and $V_{\text{L}} = 0$ V) using the same DPT circuit. The superimposed gate voltages are shown in Fig. 6 at a duty cycle that is approximately 50%. Table I shows each rise time t_{r} and fall time t_{f}, which are calculated over the 20%–80% amplitude interval along with the corresponding gating loss P_{loss} at 100 MHz.

Gate voltages and timing intervals were measured using a 4 GHz TAP4000 active probe and a 4 GHz 6-series mixed-signal oscilloscope with a 1 TS/s sampling rate, both from Tektronix. The TAP4000 is a 10× active voltage probe with an 8 V dynamic range and less than 0.8 pF of probe capacitance, which represents minimal loading for measurements on the equivalent 8 pF EPC 2038 gate capacitance. Gating loss was measured using two 6.5-digit 34465A multimeters from Keysight.

In practice, several factors influence the propagation delay of the logic inverters and so the worst-case value should be used from the datasheet that corresponds to the expected operating range. Higher die temperature increases the propagation delay, but higher power supply voltage decreases it.

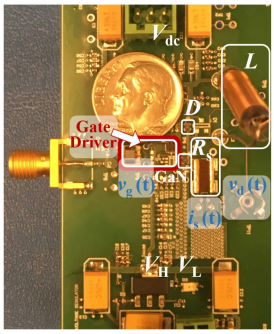

Fig. 7. PCB of the DPT circuit with the miniaturized isolated ultrafast gate driver for EPC 2038 with WBC4-14 L and SN74LVC2G04.

The input and output of logic inverters have clamp diodes to protect against over- and under-voltages. These clamps are rated for a specific current; for example, the SN74LVC2G04 has an absolute maximum allowable clamp current of 50 mA. The maximum current at the transformer secondary is typically limited by the surge impedance, which corresponds to the reflected characteristic impedance across the RF signal transformer; also, an explicit resistor (e.g., for matching) will also limit this current.

The SN74LVC2G04 from Texas Instruments, which has a buffered output, has the best overall performance in t_r, t_f, and P_{loss}; rise and fall slew rates are 12.0 and 12.7 GV/s, respectively.

C. Double Pulse Test Circuit

The DPT is one of the critical methods to evaluate the performance of a gate driver under hard-switching conditions [17] and arbitrary long-pulse operation. We evaluate the EPC 2038 in the isolated ultrafast gate driver at 45 V and 0.3 A drain voltage and current, respectively. The DPT circuit was implemented using a diode-connected EPC 2038 with the gate shorted to the source (which conducts as a freewheeling diode with the current in the reverse direction), a 56 μH inductor (EPCOS B8211E series) as the inductive load, and a 5 Ω shunt resistor (Vishay VCS1625ZP) as the current sensor.

There are several considerations for printed circuit board (PCB) layout. These include maintaining adequate clearance between the ground planes on the control side and the power side to minimize the stray coupling capacitance. For power devices with high di/dt, using Kelvin connections to the source for gate driving results in a smaller voltage transient on v_{source} in Fig. 1. Fig. 7 shows the PCB and Fig. 8 shows typical DPT waveforms with corresponding slew rates labeled.

A continuous 100 MHz control signal with 40% duty cycle was also evaluated using the same circuit for DPT. Fig. 9 shows the time-domain waveforms: v_c, v_N, v_{gate}, and $v_N + v_{gate}$, which is similar to Fig. 3; although the maximum and minimum voltages of $v_N(t) + v_{gate}(t)$ are clamped, the timing validates the approximations in Section II.

A continuous 165 MHz control signal with narrow pulses was also evaluated using the same circuit for DPT. Fig. 10 shows the time-domain waveform of v_{gate}. The gate voltage has rise and fall

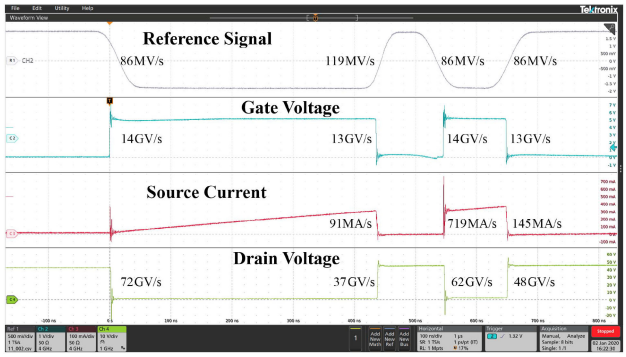

Fig. 8. Typical waveforms of DPT. The gate voltage $v_g(t)$ was measured with a 4 GHz TAP4000 active probe, the source current $i_s(t)$ was measured with a 4 GHz TDP7704 probe in differential mode and a sense resistor, and the drain voltage $v_d(t)$ was measured with a 1 GHz TPP1000 passive probe. The test points on the PCB are marked in Fig. 7.

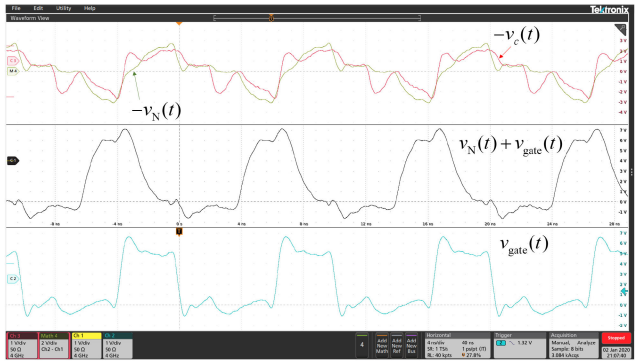

Fig. 9. Demonstration of the gate voltage with a duty cycle of 40% at 100 MHz. $v_{gate}(t)$ and $v_N(t) + v_{gate}(t)$ were measured with 4 GHz TAP4000 active probes while $v_c(t)$ was measured with a 4 GHz TDP7704 probe in differential mode. Four voltage levels: plateau, valley, ledge A, and ledge B from Section II, can be observed in $v_N(t) + v_{gate}(t)$, which are clamped by the logic inverter input diodes. The discrepancy between the scope traces for $v_c(t)$ and $v_N(t)$ and the idealized waveforms in Fig. 3 can be attributed to the resonance between the transformer leakage inductance and the input capacitance of the logic inverter gate. In addition, impedance mismatches occur in the signal path from the input cable, PCB traces, and component parasitics.

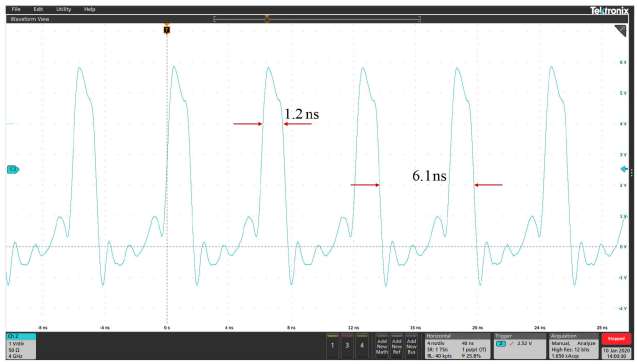

Fig. 10. Demonstration of the gate voltage with a narrow pulse of 1.237 ns at 164.6 MHz repetition rate. $v_{gate}(t)$ was measured with a 4 GHz TAP4000 active probe. The rise and fall times are 280 and 263 ps, respectively, with corresponding slew rates of 10.94 and 11.65 GV/s.

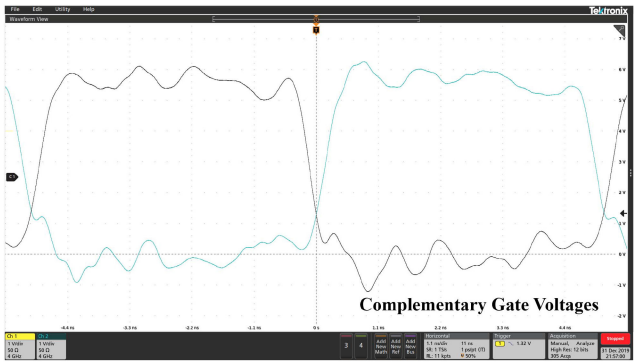

Fig. 11. Complementary gate voltages in the CMCD power converter with a TI SN74LVC2G04 as the logic inverters using 4 GHz TAP4000 active probes and 1 TS/s sampling rate.

TABLE II
END-TO-END EXPERIMENTAL WPT PERFORMANCE OF THE GATE DRIVERS

Gate Driver Type	P_o (W)	P_{gate} (W)	η w/o P_{gate} (%)	η_{total} (%)
SN74LVC2G04	2.59	0.259	70.8	66.2
NL27WZU04	2.35	0.404	64.4	58.0

times of 280 and 263 ps, respectively, and corresponding slew rates of 10.94 and 11.65 GV/s. The pulsewidth is as narrow as 1.237 ns when measuring at 80% of the driving voltages $V_H = 5$ V and $V_L = 0$ V. The gating loss is 183 mW.

The strategies employed in this gate driver topology could possibly be used for isolated control feedback loops in VHF converters as it provides fast response and pulse preservation.

D. Symmetric CMCD WPT System

The isolated ultrafast gate driver was used in a symmetric CMCD wireless power transfer (WPT) system operating at 100 MHz, whose design and implementation details can be found in [12]. With the gate driver using a dual inverter gate SN74LVC2G04, the gating loss P_{gate} is 0.26 W, which is a 57% improvement from the previous 0.61 W in [12] using the same driving voltages $V_H = 5.5$ V and $V_L = 0$ V. The gate voltages are shown in Fig. 11, which are required to have greater than 50% duty cycle for proper switch overlap. The rise and fall times are below 300 ps with a slew rate above 10 GV/s. The system achieves an output power P_o of 2.6 W, dc–dc efficiency η (without P_{gate}) of 71%, and a total efficiency (including gating loss) η_{total} of 66%, as shown in Table II. The hardware is shown in Fig. 12.

Implementation with a different logic inverter NL27WZU04 under the same gate driver conditions resulted in slower rise and fall times, as observed in Fig. 6 and Table I. Maintaining the same input power P_{in} at 3.6 W and identical setups [12], the WPT system using the NL27WZU04 has significantly lower output power P_o, dc–dc efficiency η without P_{gate}, and η_{total}, along with higher gating loss P_{gate}, as shown in Table II.

Based on these comparisons of the effect of gate driver speeds on resonant converter efficiencies, a properly designed isolated ultrafast gate driver results in a significant improvement.

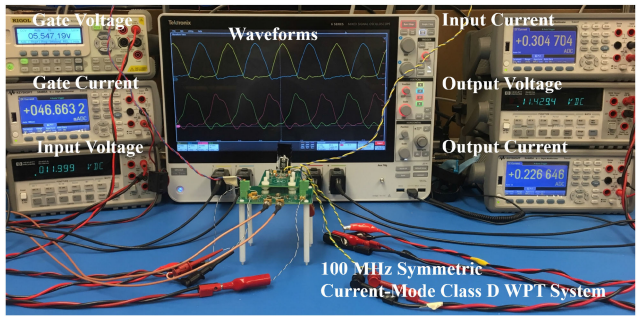

Fig. 12. Hardware test and measurement of the ultrafast gate driver in a 100 MHz symmetric CMCD WPT system. $P_{in} = 3.656$ W, $P_o = 2.590$ W, $P_{gate} = 0.259$ W, η (without P_{gate}) = 70.8%, and $\eta_{total} = 66.2\%$.

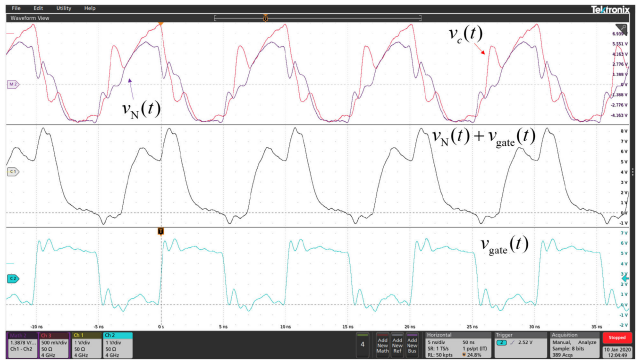

Fig. 13. Higher power GaN FET GS-065-004-1-L from GaN Systems is used to test the capability of the isolated ultrafast gate driver. The duty cycle is 55%. $v_{gate}(t)$ and $v_N(t) + v_{gate}(t)$ were measured with 4 GHz TAP4000 active probes, while $v_c(t)$ was measured with a 4 GHz TDP7704 probe in differential mode. The rise and fall times are 206 and 268 ps, respectively, with corresponding slew rates of 16.01 and 12.31 GV/s.

E. Higher Power GaN FET

An isolated ultrafast gate driver for higher power devices requires higher current capability. Fig. 13 shows the results for the GS-065-004-1-L from GaN Systems with a voltage rating of 650 V and a current rating of 3.5 A. It requires a gate drive average current of 70 mA at 100 MHz, which is approximately 16× that of the EPC 2038 and needs parallel logic inverter gates to provide the output current capability. A single logic inverter SN74LVC1G04 is used for the first stage and six dual logic inverters SN74LVC2G04 are used in parallel for a total of twelve for the second stage. The rise and fall times are 206 and 268 ps, respectively, with corresponding slew rates of 16.01 and 12.31 GV/s. The gating loss is 1.436 W at $V_H = 5.5$ V and $V_L = 0$ V.

IV. CONCLUSION

An isolated, variable duty cycle, ultrafast gate driver capable of arbitrarily long ON- and OFF-times has been presented, analyzed, and evaluated. The ultrafast gate driver can operate at 100 MHz with a noteworthy slew rate of above 12 GV/s and gating loss of 108 mW per switch at a driving voltage of 5 V, and deliver narrow 1.2 ns pulses at 165 MHz. It can drive a pulse power device with a drain slew rate of more than 37 GV/s.

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