Interleaved Multilevel Boost Converter With Minimal Voltage Multiplier Components for High-Voltage Step-Up Applications

Mohammad Meraj, *Member, IEEE*, Mahajan Sagar Bhaskar, *Member, IEEE*, Atif Iqbal, *Senior Member, IEEE*, Nasser Al-Emadi, *Member, IEEE*, and Syed Rahman

***Abstract*—In this article, a new interleaved multilevel boost converter (interleaved-MBC) is suggested with minimal voltage multiplier (VM) cells for high-voltage step-up applications. The interleaved-MBC is derived in such a way that the maximum utilization of the VM circuit operation can be achieved by the interleaved structure. Furthermore, compared to existing multilevel interleaved converters, the reduced number of capacitors and diode with equal voltage rating makes it more attractive. Similar to the existing multilevel converter, the feature of the interleaved-MBC provides the extension of the number of levels to achieve the necessary voltages just by adding similar capacitor–diode stages (single capacitor and single diode are required to increase the stage by one). The features like continuous input current, low-input ripples, high voltage conversion ratio, and reduced stress on devices make the proposed converter more suitable for the voltage step-up applications, such as dc link, hybrid distribution systems, hybrid photovoltaic systems, etc. The detailed analysis of the converter is carried out by considering the nonidealities in the power circuit. The operation of the interleaved-MBC is presented for continuous and discontinuous conduction modes with boundary conditions. The components selection criterion and the comparison of converters are presented with suitable discussions. The converter is experimentally tested, and the obtained results validate its performance and functionality.**

***Index Terms*—Boost converter, high voltage gain, interleaved, multilevel converter, reduced components and devices, voltage multiplier (VM), voltage stress.**

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NOMENCLATURE

L_1, L_2	Inductors.
$D_1, D_2, \ldots, D_N$	Diodes.
$C_1, C_2, \ldots, C_N$	Capacitors.
Q_1, Q_2	Switches.
V_i, V_o	Average of input and output voltages (v_i, v_o), respectively.
I_i, I_o	Average of input and output currents (i_i, i_o), respectively.
G or V_o/V_i	Voltage gain.
$L_{1,\text{crit}}, L_{2,\text{crit}}$	Critical inductances.
$C_{1,\text{crit}}, C_{2,\text{crit}}, \ldots$	Critical capacitances.
$T, f, D,$ and N	Time period, frequency, duty cycle, and level, respectively.
v_{L1}, v_{L2}	Voltages across inductors L_1 and L_2.
$\Delta i_{L1}, \Delta i_{L2}$	Ripples in inductor L_1, L_2 currents.
I_{L1}, I_{L2}	Average values of inductor currents i_{L1}, i_{L2}.
$v_{C1}, v_{C2}, \ldots$	Voltages across capacitors C_1, C_2, ….
$\Delta v_{C1}, \Delta v_{C2}, \ldots$	Ripples voltages across capacitors C_1, $C_2, \ldots$.
$V_{C1}, V_{C2}, \ldots$	Average voltages across capacitors C_1, $C_2, \ldots$.
$i_{C1}, i_{C2}, \ldots$	Currents through capacitors C_1, $C_2, \ldots$.
$I_{C1,\text{rms}}, I_{C2,\text{rms}}, \ldots$	RMS currents through capacitors C_1, $C_2, \ldots$.
$v_{D1}, v_{D2}, \ldots$	Voltages across diodes $D_1, D_2, \ldots$.
i_{Q1}, i_{Q2}	Currents through switches Q_1 and Q_2, respectively.
V_{Q1}, V_{Q2}	Average values of switch voltages v_{Q1}, v_{Q2}, respectively.
I_{Q1}, I_{Q2}	Average values of switches currents i_{Q1}, i_{Q2}, respectively.
$I_{Q1,\text{rms}}, I_{Q2,\text{rms}}$	RMS currents through switches Q_1, Q_2, respectively.
$I_{Q1,p}, I_{Q2,p}$	Peak currents through switches Q_1, Q_2, respectively.
$I_{D1}, I_{D2}, \ldots$	Average values of diode currents $i_{D1}, i_{D2}, \ldots$.
$V_{D1,\text{PIV}}, V_{D2,\text{PIV}}, \ldots$	PIVs of diodes $D_1, D_2, \ldots$.

$I_{D1,\mathrm{rms}}$, $I_{D2,\mathrm{rms}}$, ...	RMS currents through diodes D_1, D_2, ...
R_{L1}, R_{L2}	Internal resistance of inductor L_1, L_2.
R_{DF}, V_{DF}	Diode resistance and threshold voltage.
R_Q and R_o	ON-state resistances of switches and loads.
P_{L1}, P_{L2}	Power losses across inductors.
$P_{D,\mathrm{total}}$, $P_{C,\mathrm{total}}$	Power losses across diodes and capacitors, respectively.
P_{loss}, η_{con}	Total power loss and efficiency, respectively.
β_{odd}, β_{even}	Normalized inductor time constants.
$\beta_{\mathrm{crit}}(D_1, D_1\prime)$	CCM and DCM boundary surface.

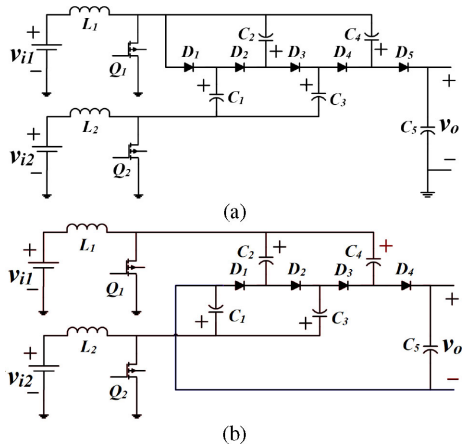

Fig. 1. Recently proposed power converters. (a) Interleaved converter in [26]. (b) Interleaved converter in [27].

I. Introduction

NOWDAYS multilevel converters are gaining popularity due to the requirement of renewable energy sources and the development in the technologies of semiconductors and reactive elements. Based on the choice of dc–dc converters, one can generate both inverting and noninverting voltages at the output. In various applications, such as telecom modules, data acquisition systems, dc link, hybrid distribution systems, photovoltaic systems, OLED microdisplay boards (mobile phone to advertisement), control boards (microprocessors and digital converters), and random access memory, negative-voltage supplies are required [1]–[5]. Additionally, in the multilevel inverters for grid integration and electric motor drives applications, the front-end dc–dc converter can be inverting, which can self-balance its capacitor voltages to achieve the desired number of levels [6], [7]. These kinds of applications require the reduced size, weight, and losses of the converter. Inverting voltages provided by the pulsewidth-modulated buck–boost converter are the classical choice [8]. The major drawbacks of these converters are the requirement of high-voltage rating devices and a large number of control devices. Switched capacitors (SC) converter has grabbed the attention due to small voltage and current rating components/devices, and few magnetic components [9], [10]. This feature allows SC converters to go for the higher power density and full on-chip combination compared with the traditional converter. The main drawbacks of these converters are the requirement of a large number of control switches to control the flow of the current for charging and discharging of the capacitors, narrowed regulating capability, and discontinuous input current in some cases. In [11], integrating an SC circuit and coupled inductor converters has been proposed. This integration removes the problem of discontinuous input currents. Nevertheless, the leakage inductive energy of the coupled inductors forms voltage spikes on the semiconductors. Therefore, an additional passive-clamp circuit must be added to supply purified energy to load. In switched inductor (SI) configurations, there are no voltage spikes unlike coupled inductors [12], however, require several inductors and semiconductor devices. In multikilowatt power applications, the usage of the several inductors can increase the cost and the size, and can also reduce the power density. In [13] and [14], SC and SI converters have been proposed to increase the voltage conversion ratio. A combination of SC and SI along with basic buck, boost and buck–boost, and SEPIC converters has been reported in [15], which results in improving the voltage conversion ratio and reducing the voltage stress on the devices, however, requires the large number of components and devices.

Voltage multipliers (VM) can be categorized as multiple stages of an SC configuration [16], [17]. The Cockcroft–Walton VM circuit developed in 1932 is the most commonly used circuit in the wide range of ac–dc high step-up applications [17] and is recently adopted for the dc–dc step-up applications [19], [20]. Interestingly, the usage of these VMs is increasing in dc–dc converters due to low and equal voltage stress on the diodes and capacitors; output voltage easily increases by just adding multiple stages; low weight, compactness, and cost-effectiveness can lead to a monolithic structure; and the voltage output can be reversed from noninverting to inverting and *vice versa* by reversing the polarity of the capacitors and diodes [20], [21]. In [22] and [23], the classical boost converter is attached with a VM to achieve high voltage conversion ratio. To increase the voltage gain by N times, the power circuitry required $2N-1$ diodes and $2N-1$ capacitors. However, the use of high number of diodes and capacitors results in a large power circuit and, thus, requires a complex control algorithm due to high order of the converter. Moreover, current-dependent voltage drops and the drop across diodes are the main problems accompanied by a VM that can deteriorate the converter's output quality, especially with more number of stages, the efficiency is less. Furthermore, a VM is attached to a front-end structure of the interleaved converter in order to obtain fewer ripples in the input current [22], [24], [25]. The ripple in the input current is reduced, and the converter is suitable for floating loads. However, there is a requirement of high number of diodes and capacitors, which increases the size and the order of the converter. Therefore, the power circuit is large and requires a complex control algorithm due to high order of the converter. To overcome these drawbacks, recently a different combination of the interleaved converter with VM is proposed to achieve a higher voltage conversion ratio with reduced input current ripple [26], [27]. The power circuitry proposed in [26] is shown in Fig. 1(a). However, the

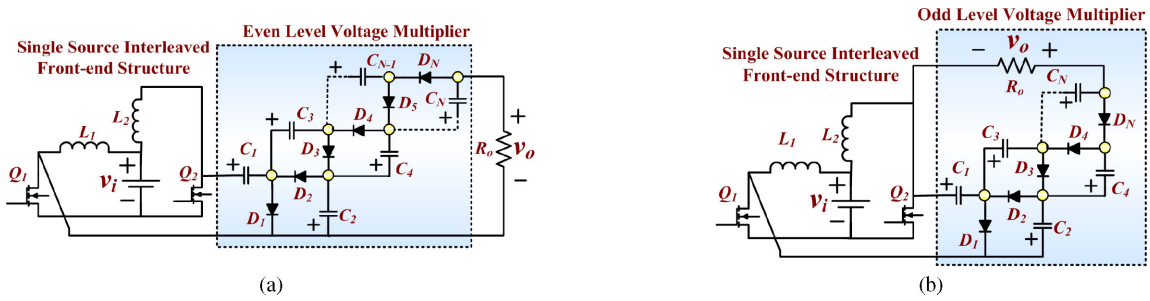

Fig. 2. Generalized structure of the proposed converter. (a) For even number of levels. (b) For odd number of levels.

voltage stress across components is asymmetrical and requires high-voltage rating capacitors and diodes as the number of levels increases. Moreover, a single capacitor is connected across the load; hence, a large voltage rating capacitor is required. These requirements make circuit costly, large, and difficult to control the voltage across each capacitor. The interleaved converter presented in [26] is examined again and the new structure is proposed with a reduced number of diodes [27]. The newly derived structure is shown in Fig. 1(b). However, the suggested converter structure is not providing a solution to reduce voltage stress across the diode and still requires a large-voltage rating capacitor at the output. Moreover, the extension of the converter structure for a greater number of levels is not suggested in [27].

In this article, a new interleaved multilevel boost converter (interleaved-MBC) structure is presented to increase the voltage conversion ratio with minimal VM components. In the proposed converter, equal voltage rating capacitors and diodes are suitable to increase the stages of the converter. The detailed analysis in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) operation of the proposed converter is presented. The design methodology and comparison of high voltage gain converters are discussed. The proposed converter operation and performance are validated through the experimental work. The article is organized as follows. The circuitry of the proposed converter and its operation is explained in Section II. Section III deals with the steady-state analysis of interleaved-MBC in CCM and DCM along with the boundary condition. The state-space modeling of the converter is explained in Section IV. Design methodology and comparisons are given in Sections V and VI. The experimental results of the designed prototype are provided in Section VII. Finally, Section VIII concludes the article.

II. Interleaved-MBC

The proposed Interleaved-MBC circuitry is derived from the combination of the front-end structure of classical interleaved converter and VM cells to double the voltage and minimize the input current ripple as compared to the MBC. The voltage conversion ratio of the interleaved-MBC is directly proportional to the number of VM cells (levels) and is inversely proportional to $1-D$, where D is the duty cycle. Fig. 2(a) and (b) shows the power circuitry of the N-level interleaved-MBC for even and odd number of levels, respectively, where N is a level or number of capacitors or diodes. In an interleaved-MBC, a single diode

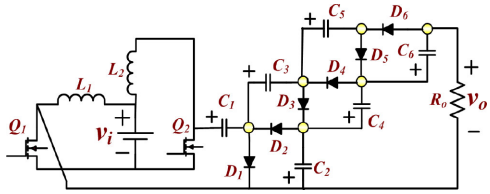

Fig. 3. Power circuit of six-level interleaved MBC.

and single capacitor are required to increase the stage by one; whereas, in a classical MBC, two diode and two capacitors are required to increase the stage [23], [24]. The other benefit of the proposed converter is that the requirement of inductor and switches is not increasing with the number of levels. Therefore, an N-level interleaved-MBC configuration requires only two inductors, two control switches, N number of diodes, and N number of capacitors. Hence, circuit components and devices are reduced and confirm the maximum utilization of VM cells.

A. Operating Modes for the Proposed Converter (N is Even)

The proposed converter with six levels is shown in Fig. 3, and possible modes are explained as follows.

1) Switches Q_1 and Q_2 Are ON (Mode I): Fig. 4(a) depicts the equivalent circuit of the interleaved-MBC for Mode I. In this mode, both the inductors L_1 and L_2 charged from an input voltage source (v_i) through the switches Q_1 and Q_2, respectively. The inductor currents i_{L1} and i_{L2} are increasing linearly. Therefore, the slope of the current through inductor L_1 is positive and can be written as

$$\frac{di_{L1}}{dt} = \left(\frac{1}{L_1}\right) v_i = \left(\frac{1}{L_1}\right)(V_i + \Delta v_i) \approx \left(\frac{1}{L_1}\right) V_i. \quad (1)$$

In a similar way, the slope of the current through inductor L_2 is positive and can be written as

$$\frac{di_{L2}}{dt} = \left(\frac{1}{L_2}\right) v_i = \left(\frac{1}{L_2}\right)(V_i + \Delta v_i) \approx \left(\frac{1}{L_2}\right) V_i. \quad (2)$$

During this mode, the voltage across diode D_1 is negative due to capacitor C_1, the voltage across diode D_2 is negative due to the voltage across capacitors C_1 and C_2, the voltage across diode D_3 is negative due to the voltage across capacitors C_1, C_2, and C_3, and so on. Therefore, all the diodes are reversed biased and capacitors C_2, C_4, and C_6 feed power to load R_o.

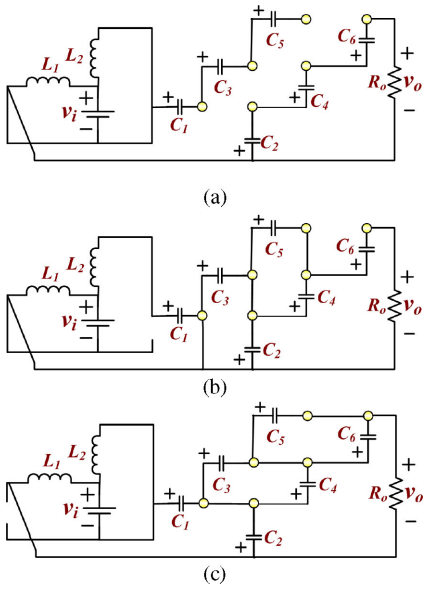

Fig. 4. Equivalent circuit for six-level converter. (a) Mode I. (b) Mode II. (c) Mode III.

2) Switch Q_1 *Is* ON *and* Q_2 *Is* OFF *(Mode II):* Fig. 4(b) depicts the equivalent circuit of the interleaved-MBC for Mode II. In this mode, inductor L_1 is charged from an input source (v_i) through switch Q_1. The current through inductor L_1 is increasing linearly. Therefore, the slope of the current through inductor L_1 is positive and can be written as

$$\frac{di_{L1}}{dt} = \left(\frac{1}{L_1}\right) v_i = \left(\frac{1}{L_1}\right) (V_i + \Delta v_i) \approx \left(\frac{1}{L_1}\right) V_i. \quad (3)$$

The series combination of input source (v_i) and inductor L_2 charged capacitor C_1 through diode D_1 and switch Q_1. At the same time, the energy stored in the even capacitors C_2 and C_4 is transferred to odd capacitors C_3 and C_5 through switch Q_1 and diode D_3, and switch Q_1 and diode D_5, respectively (path: C_2–Q_1–v_i–L_2–C_1–C_3–D_3 and C_4–C_2–Q_1–v_i–L_2–C_1–C_3–C_5–D_5). During this mode, the voltage across diode D_2 is negative due to the voltage of capacitor C_2, the voltages across diodes D_4 and D_6 are negative due to the voltage of capacitors C_4 and C_6, respectively. Therefore, diodes D_2, D_4, and D_6 are reversed biased. The capacitors C_2, C_4, and C_6 feed power to load R_o. The current through inductor L_2 is decreasing linearly; therefore, the slope of the current through inductor L_2 is negative and can be written as

$$\frac{di_{L2}}{dt} \begin{cases} = \left(\frac{1}{L_2}\right)(v_i - v_{C1}) = \left(\frac{1}{L_2}\right)(v_i - v_{C1} - v_{C3} + v_{C2}) \\ = \left(\frac{1}{L_2}\right)(v_i - v_{C1} - v_{C3} - v_{C5} + v_{C2} + v_{C4}). \end{cases} \quad (4)$$

3) Switch Q_1 *Is* OFF *and* Q_2 *Is* ON *(Mode III):* Fig. 4(c) depicts the equivalent circuit of the interleaved-MBC for Mode III. In this mode, inductor L_2 is charged by an input voltage source (v_i) through switch Q_2. The combination of input source (v_i), inductor L_1, and capacitor C_1 charges capacitor C_2 through switch Q_2 and diode D_2. At the same time, the energy stored in the capacitors C_3 and C_5 is transferred to the capacitors C_4 and C_6 through switch Q_2 and diode D_4, and switch Q_2 and diode D_6, respectively (path: C_3–C_1–Q_2–v_i–L_1–C_2–C_4–D_4 and C_5–C_3–C_1–Q_2–v_i–L_1–C_2–C_4–C_6–D_6). During this mode, the voltage across diode D_1 is negative due to input voltage, inductor L_1 voltage, and capacitor C_1 voltage. The voltages across diodes D_3 and D_5 are negative due to the conduction of diodes D_2 and D_4, and voltages across capacitors C_3 and C_5. The combination of input voltage source (v_i), voltage across inductor L_1, and capacitors C_1, C_3, and C_5 feeds power to load R_o. The current through inductor L_1 is decreasing linearly. Therefore, the slopes of the inductor L_1 currents are negative and can be written as

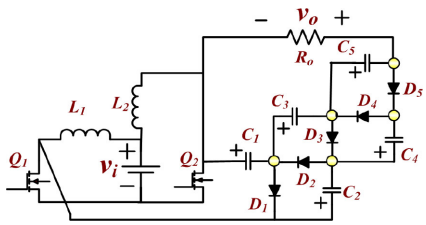

Fig. 5. Power circuit of five-level interleaved MBC.

$$\frac{di_{L1}}{dt} \begin{cases} = \left(\frac{1}{L_1}\right)(v_i - v_{C2} + v_{C1}) \\ = \left(\frac{1}{L_1}\right)(v_i - v_{C2} + v_{C1} - v_{C4} + v_{C3}) \\ = \left(\frac{1}{L_1}\right)(v_i - v_{C2} + v_{C1} - v_{C4} + v_{C3} - v_{C6} + v_{C5}). \end{cases} \quad (5)$$

The current through inductor L_2 is increasing linearly. Therefore, the slope of the current through inductor L_2 is positive and can be written as

$$\frac{di_{L2}}{dt} = \left(\frac{1}{L_2}\right) v_i = \left(\frac{1}{L_2}\right) (V_i + \Delta v_i) \approx \left(\frac{1}{L_2}\right) V_i. \quad (6)$$

Assume, the capacitor voltage ripples are small and the relation between VM capacitor voltages are obtained as

$$V_{C2} = V_{C3} = V_{C4} = V_{C5} = V_{C6}. \quad (7)$$

The relation voltages across capacitors and output voltage can be obtained as follows:

$$V_o = -(V_{C2} + V_{C4} + V_{C6}). \quad (8)$$

*B. Operating Modes for the Proposed Converter (*N *Is Odd)*

The proposed converter with five levels is shown in Fig. 5 and the possible modes of the converter are explained as follows.

1) Switches Q_1 *and* Q_2 *Are* ON *(Mode I):* Fig. 6(a) depicts the equivalent circuit of the interleaved-MBC for Mode I. In this mode, both the inductors L_1 and L_2 charged from an input

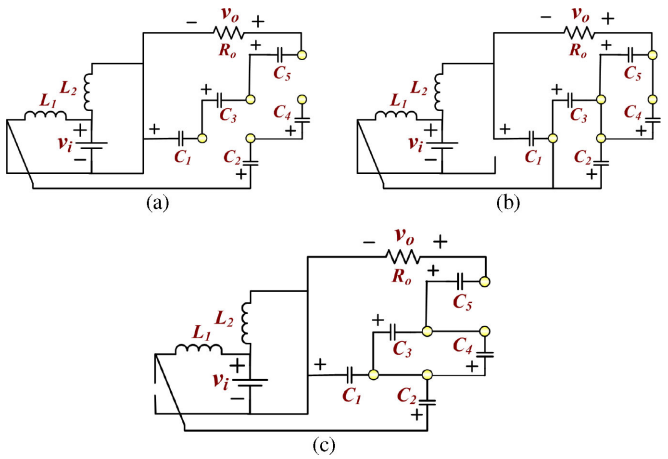

Fig. 6. Equivalent circuit for five-level converter. (a) Mode I. (b) Mode II. (c) Mode III.

voltage source (v_i) through the switches Q_1 and Q_2, respectively. The inductor currents i_{L1} and i_{L2} are increasing linearly. Therefore, the slope of the current through inductor L_1 is positive and can be written as

$$\frac{di_{L1}}{dt} = \left(\frac{1}{L_1}\right) v_i = \left(\frac{1}{L_1}\right)(V_i + \Delta v_i) \approx \left(\frac{1}{L_1}\right) V_i. \quad (9)$$

In a similar way, the slope of the current through inductor L_2 is positive and can be written as

$$\frac{di_{L2}}{dt} = \left(\frac{1}{L_2}\right) v_i = \left(\frac{1}{L_2}\right)(V_i + \Delta v_i) \approx \left(\frac{1}{L_2}\right) V_i. \quad (10)$$

During this mode, the voltage across diode D_1 is negative due to capacitor C_1, the voltage across diode D_2 is negative due to the voltage across capacitor C_1 and C_2, the voltage across diode D_3 is negative due to the voltage across capacitors C_1, C_2, and C_3, and so on. Therefore, all the diodes are reversed biased and the combination of capacitors C_1, C_3, C_5 feeds power to load R_o.

2) Switch Q_1 *Is ON and* Q_2 *Is OFF (Mode II):* Fig. 6(b) depicts the equivalent circuit of the interleaved-MBC for Mode II. In this mode, inductor L_1 is charged from an input source (v_i) through switch Q_1. The current through inductor L_1 is increasing linearly. Therefore, the slope of the current through inductor L_1 is positive and can be written as

$$\frac{di_{L1}}{dt} = \left(\frac{1}{L_1}\right) v_i = \left(\frac{1}{L_1}\right)(V_i + \Delta v_i) \approx \left(\frac{1}{L_1}\right) V_i. \quad (11)$$

The series combination of input source (v_i) and inductor L_2 charges capacitor C_1 through diode D_1 and switch Q_1. At the same time, the energy stored in the even capacitors C_2 and C_4 is transferred to odd capacitors C_3 and C_5 through switch Q_1 and diode D_3, and switch Q_1 and diode D_5, respectively (path: C_2–Q_1–v_i–L_2–C_1–C_3–D_3 and C_4–C_2–Q_1–v_i–L_2–C_1–C_3–C_5–D_5). During this mode, the voltages across diodes D_2 and D_4 are negative due to the voltage of capacitors C_2 and C_4, respectively. Therefore, diodes D_2 and D_4 are reversed biased. The combination of capacitors C_2 and C_4, input voltage, and inductor L_2 feeds power to load R_o. The current through inductor L_2 is decreasing linearly; therefore, the slope of the current through inductor L_2 is negative and can be written as

$$\frac{di_{L2}}{dt} \begin{cases} = \left(\frac{1}{L_2}\right)(v_i - v_{C1}) = \left(\frac{1}{L_2}\right)(v_i - v_{C1} + v_{C2} - v_{C3}) \\ = \left(\frac{1}{L_2}\right)(v_i - v_{C1} + v_{C2} - v_{C3} + v_{C4} - v_{C5}). \end{cases} \quad (12)$$

3) Switch Q_1 *Is OFF and* Q_2 *Is ON (Mode III):* Fig. 6(c) depicts the equivalent circuit of the interleaved-MBC for Mode III. In this mode, inductor L_2 is charged by an input voltage source (v_i) through switch Q_2. The combination of input source (v_i), inductor L_1, and capacitor C_1 charges capacitor C_2 through switch Q_2 and diode D_2. At the same time, the energy stored in capacitor C_3 is transferred to capacitor C_4 through switch Q_2 and diodes D_4 (path: C_3–C_1–Q_2–v_i–L_1–C_2–C_4–D_4). During this mode, the voltage across diode D_1 is negative due to input voltage, inductor L_1 voltage, and capacitor C_1 voltage. The voltages across diodes D_3 and D_5 are negative due to the conduction of diodes D_2 and D_4, and capacitors C_3 and C_5 voltage. The combination of capacitors C_1, C_3, and C_5 feeds power to load R_o. The current through inductor L_1 is decreasing linearly. Therefore, the slopes of the inductor L_1 currents are negative and can be written as

$$\frac{di_{L1}}{dt} = \left(\frac{1}{L_1}\right)(v_i - v_{C2} + v_{C1}) = \left(\frac{1}{L_1}\right)\begin{pmatrix} v_i - v_{C2} \\ +v_{C1} - v_{C4} + v_{C3} \end{pmatrix}. \quad (13)$$

The current through inductor L_2 is increasing linearly. Therefore, the slope of the current through inductor L_2 is positive and can be written as

$$\frac{di_{L2}}{dt} = \left(\frac{1}{L_2}\right) v_i = \left(\frac{1}{L_2}\right)(V_i + \Delta v_i) \approx \left(\frac{1}{L_2}\right) V_i. \quad (14)$$

Assume, the capacitor voltage ripples are small and the relation between VM capacitor voltages are obtained as

$$V_{C2} = V_{C3} = V_{C4} = V_{C5}. \quad (15)$$

The relation voltages across capacitors and output voltage can be obtained as follows:

$$V_o = -(V_{C1} + V_{C3} + V_{C5}). \quad (16)$$

Let us assume D is the duty cycle for switches Q_1 and Q_2. The switches of the proposed converter operates in 180° phase shift in such a way that $2D \geq 1$ to achieve higher voltage gain and interleaved operation. Using the aforementioned condition, the converter operates in two modes (when $2D = 1$) or in three modes (when $2D > 1$). The typical characteristics waveforms of a converter are shown in Fig. 7. It is noteworthy that $2D < 1$ condition is not of interest since it provides lower voltage gain and high input current ripple. Moreover, there will be no path for the currents across inductors L_1 and L_2 (i_{L1} and i_{L2}) due to

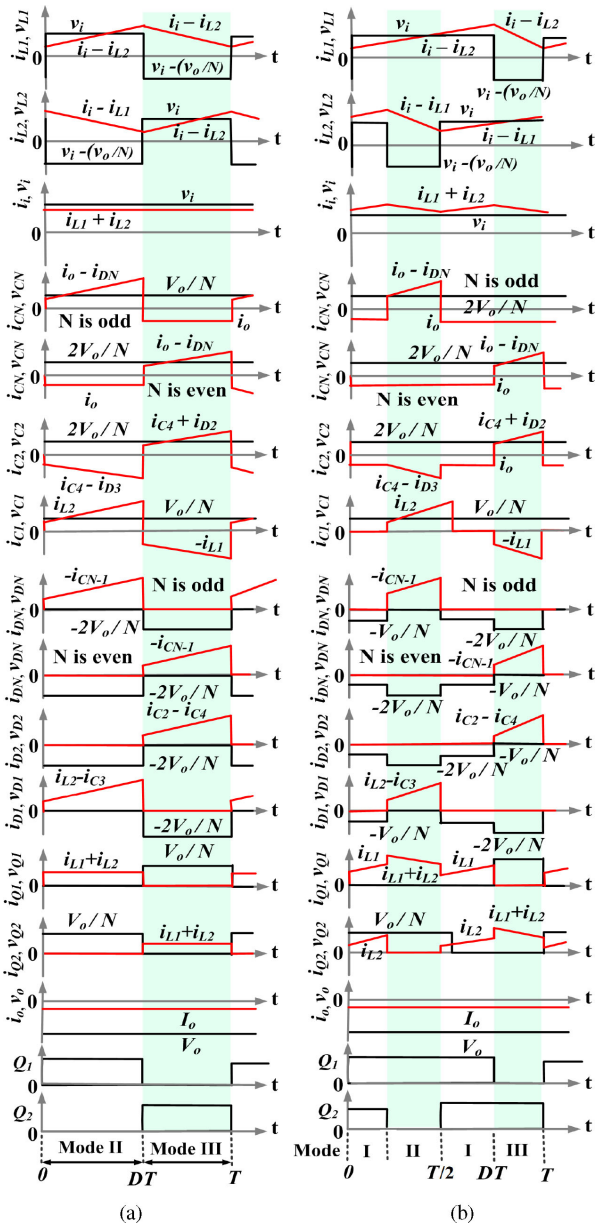

Fig. 7. Typical characteristics waveform. (a) $2D = 1$. (b) $2D > 1$.

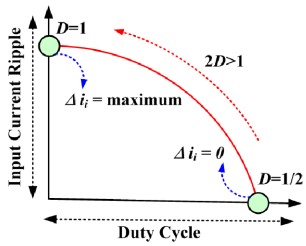

Fig. 8. Relation between input ripple versus duty cycle.

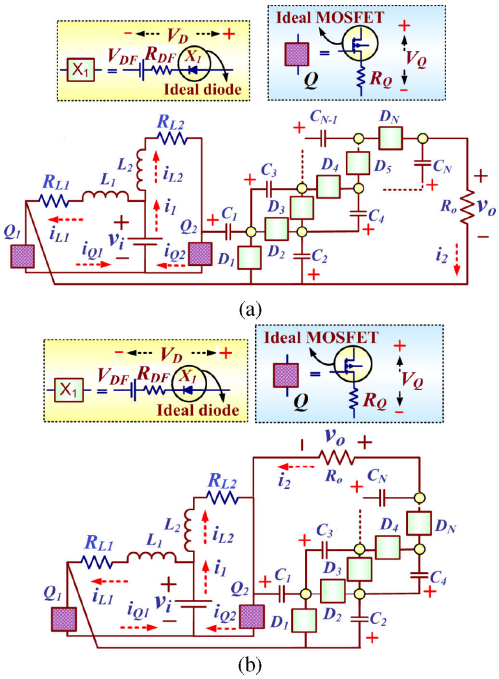

Fig. 9. Power circuit of the interleaved-MBC by considering the nonidealities. (a) For even level. (b) For odd level.

the voltage across all the capacitors, which makes all the diode reversed biased when a converter operates under condition $2D < 1$. The switches of the converter must be operated with phase shifted by 180° (degrees) to achieve the minimum input current ripple (Δi_i). Fig. 8 shows the relation between input ripple and duty cycle. Similar to the classical interleaved converter, input current ripple (Δi_i) of the interleaved-MBC theoretically becomes zero at 50% duty and will be increased as the duty increases. It is noteworthy that one can operate converter at high duty ratio to achieve high voltage conversion ratio by compromising inductor current ripples. It is notable that both the switches have to be controlled with the same percent of duty with 180° phase shifted to operate the entire converter in a symmetrical manner. The operation modes of odd- and even-level proposed converters are summarized in Table I.

III. Steady-State Analysis of the Interleaved-MBC

A. Output Voltage Analysis in CCM

Fig. 9 depicts the power circuit of the interleaved-MBC by considering the nonidealities all the diodes and switches. The internal resistance of the inductors L_1 and L_2 are considered as R_{L1} and R_{L2}, respectively. The voltage drop across the semiconductors (diode and switch) depends on current flowing through them;$i_Q R_Q$ and$i_D R_{DF} + V_{DF}$ are the voltage drops across the switch and diode, respectively, where,R_{DF} and R_Q are the forward resistance of the diode and ON-state resistance of the switch, respectively. Also, i_D and i_Q are the currents flowing through the diode and switch, respectively. For ease, the drops across the diode and switch are considered as V_D and V_Q, respectively. The capacitors are considered large enough to keep constant voltage without any ripple. However, practically a small voltage drop can be observed because of the equivalent series resistance (ESR) of the capacitor.

When switch Q_1 is turned ON for DT time (Modes I and II), where T is the switching time period: In this case, the voltage

TABLE I
SUMMARY OF OPERATION MODES

Levels	Duty cycle	Modes	C_1	C_2	C_3	C_4	C_N	D_1	D_2	D_3	D_4	D_N	characteristics
N is Even	*D>0.5*	I	-	↓	-	↓	↓	RB	RB	RB	RB	RB	High output voltage
		II	↑	↓	↑	↓	↓	FB	RB	FB	RB	RB	
		III	↓	↑	↓	↑	↑	RB	FB	RB	FB	FB	
	D=0.5	II	↑	↓	↑	↓	↓	FB	RB	FB	RB	RB	Low input ripple
		III	↓	↑	↓	↑	↑	RB	FB	RB	FB	FB	
N is Odd	*D>0.5*	I	↓	-	↓	-	↓	RB	RB	RB	RB	RB	High output voltage
		II	↑	↓	↑	↓	↑	FB	RB	FB	RB	FB	
		III	↓	↑	↓	↑	↓	RB	FB	RB	FB	RB	
	D=0.5	II	↑	↓	↑	↓	↑	FB	RB	FB	RB	FB	Low input ripple
		III	↓	↑	↓	↑	↓	RB	FB	RB	FB	RB	

Note: ↑ represent charging of capacitor, ↓ represent discharging of capacitor, FB represent forward biased, and RB represent reversed biased.

across inductor L_1 can be expressed as follows:

$$v_{L1} = v_i - \wp_1 = V_i - V_Q - i_{L1}R_{L1} + \Delta v_i \tag{17}$$

where Δv_i is the ripple in the input voltage, and $\wp_1$ is the drop in voltage and can be written as

$$\wp_1 = V_Q + i_{L1}R_{L1}. \tag{18}$$

By neglecting the ripple in input voltage, the voltage across inductor L_1 can be rewritten as

$$v_{L1} \cong V_i - V_Q - i_{L1}R_{L1}. \tag{19}$$

During *DT* time, the inductor L_1 current slope is positive and the current is rising with a constant slope.

Similarly, when switch Q_2 is turned ON for *DT* time (Modes I and III), inductor L_2 current slope is positive and the voltage across inductor L_2 can be expressed as follows:

$$v_{L2} = v_i - \wp_3 = V_i - V_Q - i_{L2}R_{L2} + \Delta v_i \tag{20}$$

where $\wp_3$ is the drop in voltage and can be written as

$$\wp_3 = V_Q + i_{L2}R_{L2}. \tag{21}$$

By neglecting the ripple in the input voltage, the voltage across inductor L_2 can be rewritten as

$$v_{L2} \cong V_i - i_{L2}R_{L2} - V_Q. \tag{22}$$

When switch Q_1 is turned OFF for the *(1−D)T* time (Mode III), the inductor L_1 is linearly discharging with a constant slope and the voltage across inductor L_1 can be expressed as follows:

$$v_{L1} = v_i - V_{C2} + V_{C1} - \wp_4 = V_i + \Delta v_i - V_{C2} + V_{C1} - \wp_4 \tag{23}$$

where $\wp_4$ is the drop in voltage and can be written as

$$\wp_4 = V_Q + i_{L1}R_{L1} + V_D. \tag{24}$$

By neglecting the ripple in the input voltage, the voltage across inductor L_2 can be rewritten as

$$v_{L1} \cong V_i - V_{C2} + V_{C1} - V_Q - i_{L1}R_{L1} - V_D. \tag{25}$$

When switch Q_2 is turned OFF for *(1−D)T* time (Mode II), the inductor L_2 is linearly discharging with a constant slope and the voltage across inductor can be expressed as follows:

$$v_{L2} = -V_{C1} + v_i - \wp_2 \tag{26}$$

where $\wp_2$ is the drop in voltage and can be written as

$$\wp_2 = V_Q + i_{L2}R_{L2} + V_D. \tag{27}$$

By neglecting the ripple in the input voltage, the voltage across inductor L_2 can be rewritten as

$$v_{L2} \cong V_i - V_Q - i_{L2}R_{L2} - V_D - V_{C1}. \tag{28}$$

By applying the volt–second balance equation separately for the inductors L_1 and L_2, the voltages across capacitor C_1 is obtained as follows:

$$V_{C1} = \frac{V_i}{1-D} - \frac{i_{L2}R_{L2} + V_Q + V_D(1-D)}{1-D}. \tag{29}$$

The voltages across capacitor C_2 is obtained as follows:

$$V_{C2} = \frac{2V_i}{1-D} - \frac{i_{L1}R_{L1} + i_{L2}R_{L2} + 2V_Q + 2V_D(1-D)}{1-D}. \tag{30}$$

Using (29) and (30) and KVL, the voltage across capacitors C_3 is obtained as follows:

$$V_{C3} = \frac{2V_i}{1-D} - \frac{i_{L1}R_{L1} + i_{L2}R_{L2} + 2V_Q + 3V_D(1-D)}{1-D}. \tag{31}$$

The voltage across capacitor C_4 is obtained as follows:

$$V_{C4} = \frac{2V_i}{1-D} - \frac{i_{L1}R_{L1} + i_{L2}R_{L2} + 2V_Q + 4V_D(1-D)}{1-D}. \tag{32}$$

It is notable that after capacitor C_4, the voltage across the capacitor is not affected by the diodes. Thus, the voltages of capacitors C_5, C_6, C_7 …, and C_N are same as the voltage across

capacitor C_4 and are expressed as

$$\underbrace{V_{Ci}}_{i=5 \text{ to } N} = \frac{2V_i}{1-D} - \frac{i_{L1}R_{L1} + i_{L2}R_{L2} + 2V_Q + 4V_D(1-D)}{1-D}. \quad (33)$$

If $N = 1$, the output voltage of the proposed converter can be obtained as follows:

$$V_o = -V_{C1} = -\left(\frac{V_i}{1-D} - \frac{i_{L2}R_{L2} + V_Q + V_D(1-D)}{1-D}\right). \quad (34)$$

If the number of levels of the proposed converter is even, then the number of even and odd capacitors will be equal. Also, the voltage across the load will be the summation of the voltages of even capacitors. The output voltage of the proposed converter for even number of levels can be obtained as follows:

$$V_{(N=\text{even})} = -\left(V_{CN} + \cdots + V_{C6} + V_{C4} + V_{C2}\right). \quad (35)$$

Using (35), the output voltage of the proposed converter for even-level converters can be obtained as follows:

$$V_{o(N=\text{even})} = -\left(\frac{NV_{C2}}{2(1-D)} - \begin{pmatrix} \frac{N}{2}\left(\frac{i_{L1}R_{L1}+i_{L2}R_{L2}+2V_Q}{1-D}\right) \\ -(\frac{N}{2}-1)4V_D - 2V_D \end{pmatrix}\right). \quad (36)$$

If the number of levels of the proposed converter is odd and greater than 1, then the number of the odd capacitors will be more than the even capacitors. Hence, the voltage across the load will be the addition of the voltages of odd capacitors. The output voltage of the proposed converter for odd number of levels can be obtained as follows:

$$V_o(N = \text{odd}) = -\left(V_{CN} + \cdots + V_{C3} + V_{C5} + V_{C1}\right). \quad (37)$$

Using (36), the output voltage of the proposed converter for the odd-level converter can be obtained as (38) shown at the bottom of page.

For the ideal case, the voltages across the capacitors are obtained as follows:

$$V_{C1} = \frac{V_i}{1-D}, V_{C2} = \frac{2V_i}{1-D},$$
$$V_{C3} = \frac{2V_i}{1-D}, \ldots, V_{CN} = \frac{2V_i}{1-D}. \quad (39)$$

The voltage across the load in an ideal case for the even- and odd-level proposed converter can be obtained as follows:

$$V_{o(N=\text{even})} = \frac{-NV_i}{1-D}, \quad V_o(N = \text{odd}) = \frac{-NV_i}{1-D}. \quad (40)$$

Therefore, the voltage conversion ratio is dependent on the number of levels (N) and duty cycle (D). Fig. 10(a) and (b) shows the plot of the output voltage gain and the ratio of voltage across the capacitor and the input voltage (v_i) versus the duty cycle (D), respectively. It is observed that the voltage gain is increased if number of levels and duty cycle increases. It is observed that the voltages across all the capacitors (except capacitor C_1) are equal. Therefore, the VM circuitry allows low and equal rating capacitors.

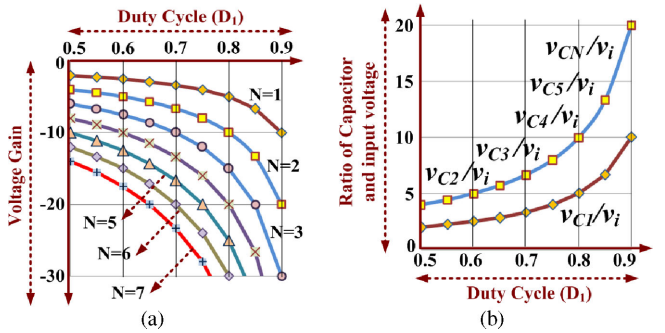

Fig. 10. (a) Output voltage versus duty ratio. (b) Ratio of capacitor voltage and input voltage versus duty ratio.

B. Output Voltage Analysis in DCM

Consider both the switches Q_1 and Q_2 turned ON and OFF with 180° phase difference. d_1T is a time required for both inductors' current to reach maximum value from the zero, d_2T is a time required for both inductors' current to reach zero from the maximum value, and d_3T is a time in which the inductor's current remains zero. The relation of d_1, d_2, and d_3 is given by

$$d_1 + d_2 + d_3 = 1, T = 1/f \quad (41)$$

where f is the switching frequency. The general condition to operate converter in CCM and DCM in term of average current through inductor L_1 (I_{L1}) and its ripple (Δi_{L1}) is derived as follows:

$$\text{CCM}\left\{-I_{L1} + \Delta i_{L1}(t) = -\int_0^T \left(\frac{v_{L_1}}{L_1}\right) dt + \Delta i_{L1}(t) < 0 \right. \quad (42)$$

$$\text{DCM}\left\{-I_{L1} + \Delta i_{L1}(t) = -\int_0^T \left(\frac{v_{L_1}}{L_1}\right) dt + \Delta i_{L1}(t) > 0. \right. \quad (43)$$

The general condition to operate the converter under CCM and DCM conditions in term of average current through inductor

$$V_o\,(N = \text{odd}, N \neq 1) = -\left(\frac{(N+1)V_{C1}}{2} + \frac{\frac{N-1}{2}\begin{pmatrix} V_i - i_{L2}R_{L2} \\ -V_Q - V_D(1-D) \end{pmatrix}}{1-D} - (N-2)V_D\right) \quad (38)$$

$L_2\,(I_{L2})$ and its ripple (Δi_{L2}) is derived as follows:

$$\text{CCM}\left\{-I_{L2}+\Delta i_{L2}(t)=-\int_0^T\left(\frac{v_{L_2}}{L_2}\right)dt+\Delta i_{L2}(t)<0\right. \tag{44}$$

$$\text{DCM}\left\{-I_{L2}+\Delta i_{L2}(t)=-\int_0^T\left(\frac{v_{L_2}}{L_2}\right)dt+\Delta i_{L2}(t)>0\,.\right. \tag{45}$$

During d_3T time, the inductor voltages are given by

$$v_{_{L1}}(t)=V_{L1}=v_{_{L2}}(t)=V_{L2}=0. \tag{46}$$

If $N=1$, the relation between the capacitor voltages and the output multilevel voltage (v_o) is expressed as

$$\text{if}\,N=1\Rightarrow v_{_o}(t)\approx I_oR_o\Rightarrow V_o=-V_{C1}. \tag{47}$$

If $N\neq 1$, the relation between the capacitor voltages and the output multilevel voltage (v_o) is expressed as

$$\begin{aligned}&\text{if}\,N\neq 1\Rightarrow v_o(t)\approx I_oR_o\\&\Rightarrow V_o=-\frac{NV_{C2}}{2},=-\frac{NV_{C3}}{2},=\ldots.\end{aligned} \tag{48}$$

If N is odd and switch Q_1 is OFF, then the dc component of the load current is same as the dc component of the inductor current $L_1\,(I_{L1})$. The relation for an odd-level proposed converter is obtained as

$$\text{if}\;N\;\text{is odd},I_{L1}(D_1')=-\frac{V_o}{R_o}\Rightarrow I_{L1}=\frac{NV_i}{(d'_1)^2R_o} \tag{49}$$

where $d'_1=1-d_1$. In a similar manner, if N is even and switch Q_2 is OFF, then the dc component of the load current is equal to the dc component of inductor current $L_2\,(I_{L2})$. The relation for an odd-level proposed converter is obtained as

$$\text{if}\;N\;\text{is even},I_{L2}\,(d'_1)=-\frac{V_o}{R_o}\Rightarrow I_{L2}=\frac{NV_i}{(d'_1)^2R_o}. \tag{50}$$

Both the switches operate at the same duty. Thus, the dc components are same for any number of levels in the proposed converter. By simplification, the DCM boundary condition is expressed as follows:

$$\left(\frac{TV_1d_1}{L_1}=\frac{TV_1d_1}{L_2}\right)>I_{L1}=I_{L2}=\frac{NV_i}{(d'_1)^2R_o}. \tag{51}$$

Using (51), the boundary condition can be written as

$$\frac{d_1(d'_1)^2}{N}>\left(\frac{L_1}{TR_o}=\frac{L_2}{TR_o}\right) \tag{52}$$

where L_1/TR_o and L_2/TR_o are normalized inductor time constants for L_1 and L_2, respectively, and $\beta_{\text{crit}}(d_1,\,d_1\prime)$ is critical DCM and CCM boundary surface.

The equation for DCM and CCM boundary surface for even level can be obtained as follows:

$$\beta_{\text{crit}}(d_1,d'_1)>\left(\beta_{\text{even}}=\frac{L_2}{TR_o}\right) \tag{53}$$

where normalized inductor time constant for even level is represent by β_{even}. The equation for DCM and CCM boundary surface for odd level can be obtained as follows:

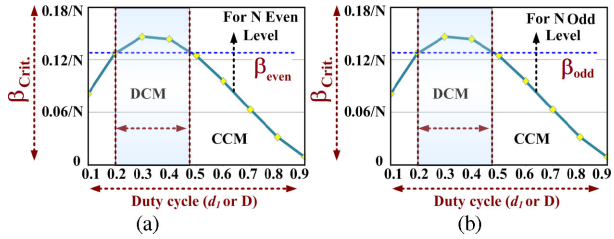

Fig. 11. Boundary for CCM and DCM operation of interleaved-MBC. (a) Even level. (b) Odd level.

$$\beta_{\text{crit}}(d_1,d_1')>\left(\beta_{\text{odd}}=\frac{L_1}{TR_o}\right) \tag{54}$$

where normalized inductor time constant for odd level is represented by β_{odd}. Fig. 11(a) and (b) depicts the DCM and CCM boundary surface for even and odd levels. The DCM is occurred when $\beta_{\text{even}}<\beta_{\text{crit}}$ for even stage and $\beta_{\text{odd}}<\beta_{\text{crit}}$ for odd stage. It is noteworthy that for both cases (even and odd levels), the boundary conditions are same and dependent on L_1, L_2, R_o, d_1, and T. The output voltage for one-level proposed converter is obtained as follows:

$$\text{if}\;N=1,\;\text{then}\;V_o=-V_{C1} \tag{55}$$

The voltage across the load for DCM in terms of capacitor voltages for even level is expressed as follows:

$$V_{o(N=\text{even})}=-\left(V_{CN}+\cdots+V_{C6}+V_{C4}+V_{C2}\right). \tag{56}$$

Using inductor volt–second balance method, the output voltage for even level can be obtained as

$$\begin{aligned}&V_{o(N=\text{even})}=\\&-\left(\frac{N}{2}\left(\frac{\begin{array}{l}(d_1+d_2)(V_i-i_{L2}R_{L2}\\-V_Q)-V_Dd_2+d_2V_{C1}\end{array}}{d_2}\right)-(N-2)V_D\right).\end{aligned} \tag{57}$$

The voltage across the load for DCM in terms of capacitor voltages for odd level is expressed as follows:

$$V_{o(N=\text{odd})}=-\left(V_{CN}+\cdots+V_{C3}+V_{C5}+V_{C1}\right). \tag{58}$$

Using inductor volt–second balance method, the output voltage for even level can be obtained as (59), shown at the bottom of the next page.

In an ideal case, the output voltage for even number of levels is obtained as follows:

$$\begin{aligned}V_{o(N=\text{even})}&=-\frac{N}{2}\left(\frac{(d_1+d_2)V_i}{d_2}+V_{C1}\right)\\&=-N\frac{(d_1+d_2)V_i}{d_2}.\end{aligned} \tag{60}$$

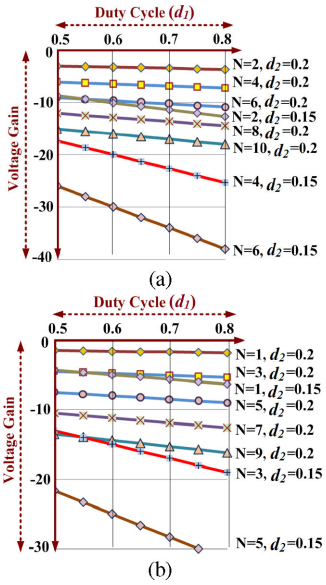

Fig. 12. Plot of voltage gain versus duty cycle. (a) For even-level converter. (b) For odd-level converter.

In an ideal case, the output voltage for even number of levels is obtained as follows:

$$V_o\,(N=\text{odd}, N\neq 1) = -N\frac{(d_1+d_2)V_i}{d_2}. \tag{61}$$

The plots of output voltage versus duty cycle d_1 with considering $d_2 = 0.2$ (i.e., 20% of T is the time required for inductor current to reach zero from maximum value) are shown for even and odd levels in Fig. 12(a) and (b), respectively. In DCM case, it is found that the output voltage is reliant on the number of stages (N), d_1, and d_2.

IV. State-Space Modeling

In this section, the state-space modeling of two-stage converter is explained. The state-space matrix for Mode I (switches Q_1 and Q_2 are ON) can be obtained as follows:

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{dv_{C1}}{dt} \\ \frac{dv_{C2}}{dt} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{RC_2} \end{bmatrix}}_{A_I} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \\ 0 \end{bmatrix}}_{B_I} V_i;$$

$$\begin{bmatrix} v_o \\ i_i \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 & 0 & -1 \\ 1 & 1 & 0 & 0 \end{bmatrix}}_{C_I} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix}. \tag{62}$$

The state-space matrix for Mode II (Switch Q_1 is ON and Q_2 is OFF) can be obtained as follows:

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{dv_{C1}}{dt} \\ \frac{dv_{C2}}{dt} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{L_2} & 0 \\ 0 & \frac{-1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{RC_2} \end{bmatrix}}_{A_{II}} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \\ 0 \end{bmatrix}}_{B_{II}} V_i;$$

$$\begin{bmatrix} v_o \\ i_i \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 & 0 & -1 \\ 1 & 1 & 0 & 0 \end{bmatrix}}_{C_{II}} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix}. \tag{63}$$

The state-space matrix for Mode III (Switch Q_1 is OFF and Q_2 is ON) can be obtained as follows:

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{dv_{C1}}{dt} \\ \frac{dv_{C2}}{dt} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 & \frac{1}{L_1} & \frac{-1}{L_1} \\ 0 & 0 & 0 & 0 \\ \frac{-1}{C_1} & 0 & 0 & 0 \\ \frac{1}{C_2} & 0 & 0 & \frac{-1}{RC_2} \end{bmatrix}}_{A_{III}} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \\ 0 \end{bmatrix}}_{B_{III}} V_i;$$

$$\begin{bmatrix} v_o \\ i_i \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 & 0 & -1 \\ 1 & 1 & 0 & 0 \end{bmatrix}}_{C_{III}} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix}. \tag{64}$$

To obtain an average state-space model, these three modes are merged by means of their respective duty cycles d. Average values of matrices A, B, and C (D = 0) are obtained as

$$X = X_I \times (2d-1) + X_{II} \times (1-d) + X_{III} \times (1-d) \tag{65}$$

where X is the resultant average matrix obtained from mode matrices X_I, X_{II}, and X_{III} in Modes I, II, and III, respectively,

$$V_{o(N=\text{odd})} = -\left(\frac{(N+1)\,V_{C1}}{2} + \frac{\frac{N-1}{2}\begin{pmatrix}(d_1+d_2)(V_i- \\ i_{L2}R_{L2}-V_Q) \\ -V_D d_2\end{pmatrix}}{d_2} - (N-2)V_D \right) \tag{59}$$

and the matrices are obtained as

$$A=\begin{bmatrix} 0 & 0 & \frac{1-d}{L_1} & \frac{d-1}{L_1} \\ 0 & 0 & \frac{d-1}{L_1} & 0 \\ \frac{d-1}{C_1} & \frac{1-d}{C_1} & 0 & 0 \\ \frac{1-d}{C_2} & 0 & 0 & \frac{d-3/2}{RC_2} \end{bmatrix};\quad B=\begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \\ 0 \end{bmatrix};$$
$$C=\begin{bmatrix} 0 & 0 & 0 & -1 \\ 1 & 1 & 0 & 0 \end{bmatrix}. \tag{66}$$

Perturbations are introduced into the system, i.e., when disturbance occur, response consists of steady-state and transient parts. After introducing the perturbations, the obtained system is isolated into ac and dc parts. The ac transient part is obtained as (67). Assume inductors are equal to *L* and capacitors are equal to *C*. Then, (67) can be modified as (68). Transfer function of the system can be obtained from the relation TF = C(SI−A)$^{-1}$B+D. The transfer function between output voltage $\hat{v}_o$ and duty ratio $\hat{d}$ is obtained as follows:

$$\begin{bmatrix} \frac{d\hat{i}_{L1}}{dt} \\ \frac{d\hat{i}_{L2}}{dt} \\ \frac{d\hat{v}_{C1}}{dt} \\ \frac{d\hat{v}_{C2}}{dt} \end{bmatrix}=\begin{bmatrix} 0 & 0 & \frac{1-\hat{d}-D}{L_1} & \frac{\hat{d}+D-1}{L_1} \\ 0 & 0 & \frac{\hat{d}+D-1}{L_2} & 0 \\ \frac{\hat{d}+D-1}{C_1} & \frac{1-\hat{d}-D}{C_1} & 0 & 0 \\ \frac{1-\hat{d}-D}{C_2} & 0 & 0 & \frac{\hat{d}+D-3/2}{RC_2} \end{bmatrix} \times \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{v}_{C1} \\ \hat{v}_{C2} \end{bmatrix}+\begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \\ 0 \end{bmatrix}\hat{v}_i;$$

$$\begin{bmatrix} \hat{v}_o \\ \hat{i}_i \end{bmatrix}=\begin{bmatrix} 0 & 0 & 0 & -1 \\ 1 & 1 & 0 & 0 \end{bmatrix}\begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{v}_{C1} \\ \hat{v}_{C2} \end{bmatrix} \tag{67}$$

$$\begin{bmatrix} \frac{d\hat{i}_{L1}}{dt} \\ \frac{d\hat{i}_{L2}}{dt} \\ \frac{d\hat{v}_{C1}}{dt} \\ \frac{d\hat{v}_{C2}}{dt} \end{bmatrix}=\begin{bmatrix} 0 & 0 & \frac{1-D}{L} & \frac{D-1}{L} \\ 0 & 0 & \frac{D-1}{L} & 0 \\ \frac{D-1}{C} & \frac{1-D}{C} & 0 & 0 \\ \frac{1-D}{C} & 0 & 0 & \frac{D-3/2}{RC} \end{bmatrix}\begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{v}_{C1} \\ \hat{v}_{C2} \end{bmatrix}+\begin{bmatrix} \frac{1}{L} & \frac{V_{C2}-V_{C1}}{L} \\ \frac{1}{L} & \frac{V_{C1}}{L} \\ 0 & \frac{I_{L1}-I_{L2}}{C} \\ 0 & \frac{-I_{L1}+V_{C2}}{C} \end{bmatrix}\begin{bmatrix} \hat{v}_i \\ \hat{d} \end{bmatrix};$$

$$\begin{bmatrix} \hat{v}_o \\ \hat{i}_i \end{bmatrix}=\begin{bmatrix} 0 & 0 & 0 & -1 \\ 1 & 1 & 0 & 0 \end{bmatrix}\begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{v}_{C1} \\ \hat{v}_{C2} \end{bmatrix} \tag{68}$$

$$\frac{\hat{v}_o}{\hat{d}}=\begin{bmatrix} 0 \\ 0 \\ 0 \\ -1 \end{bmatrix}^T\begin{bmatrix} s & 0 & \frac{D-1}{L} & \frac{1-D}{L} \\ 0 & s & \frac{1-D}{L} & 0 \\ \frac{1-D}{C} & \frac{D-1}{C} & s & 0 \\ \frac{D-1}{C} & 0 & 0 & s+\frac{-D+3/2}{RC} \end{bmatrix}^{-1} \times \begin{bmatrix} \frac{V_{C2}-V_{C1}}{L} \\ \frac{V_{C1}}{L} \\ \frac{I_{L1}-I_{L2}}{C} \\ \frac{-I_{L1}+V_{C2}}{C} \end{bmatrix}. \tag{69}$$

To find A^{-1}, first $|A|$ must be determined as

$$|A|=(-1)^5\left(\frac{D-1}{C}\right)\begin{vmatrix} 0 & \frac{D-1}{L} & \frac{1-D}{L} \\ s & \frac{1-D}{L} & 0 \\ \frac{D-1}{C} & s & 0 \end{vmatrix} + (-1)^8\left(s+\frac{-D+3/2}{RC}\right)\begin{vmatrix} s & 0 & \frac{D-1}{L} \\ 0 & s & \frac{1-D}{L} \\ \frac{1-D}{C} & \frac{D-1}{C} & s \end{vmatrix} \tag{70}$$

along with (71), shown at the bottom of the next page. Let assume,

$$A^{-1}=\frac{1}{|A|}\begin{bmatrix} a & b & c & d \\ e & f & g & h \\ i & j & k & l \\ m & n & o & p \end{bmatrix}.$$

Using (69)–(71), the ratio of output voltage $\hat{v}_o$ and duty ratio $\hat{d}$ is obtained as

$$\frac{\hat{v}_o}{\hat{d}}=\frac{1}{|A|}\times\begin{bmatrix} -m & -n & -o & -p \end{bmatrix}\times\begin{bmatrix} \frac{V_{C2}-V_{C1}}{L} \\ \frac{V_{C1}}{L} \\ \frac{I_{L1}-I_{L2}}{C} \\ \frac{-I_{L1}+V_{C2}}{C} \end{bmatrix} = \frac{1}{|A|}\times\begin{pmatrix} -m\times\frac{V_{C2}-V_{C1}}{L} \\ -n\times\frac{V_{C1}}{L}+ \\ o\times\frac{I_{L1}-I_{L2}}{C} \\ -p\times\frac{-I_{L1}+V_{C2}}{C} \end{pmatrix}. \tag{72}$$

The values of *m, n, o,* and *p* are obtained as follows:

$$m=-\left(\frac{1-D}{L}s^2+\frac{(1-D)^3}{L^2C}\right),\quad n=-\frac{(1-D)^3}{L^2C}$$
$$o=\left(\frac{(1-D)^2}{LC}s\right),\quad p=\left(s^3+2\frac{(1-D)^2}{LC}s\right). \tag{73}$$

Substituting (73) into (72)

$$\frac{\hat{v}_o}{\hat{d}} = \frac{RC}{L} \times \frac{\begin{pmatrix} L^3(-I_{L1}+V_{C2})s^3+(LC(1-D)(V_{C2}-V_{C1}))s^2+ \\ \left(L(1-D)^2(3I_{L1}-I_{L2}-2V_{C2})\right)s+(1-D)^3V_{C2} \end{pmatrix}}{\begin{pmatrix} RL^2C^2s^4+(3/2-D)L^2Cs^3+3RLC(1-D)^2s^2 \\ +(3-2D)(1-D)^2Ls+(1-D)^4R \end{pmatrix}}. \tag{74}$$

V. Design and Efficiency and Comparison

A. Design of Reactive Components

The average currents of inductors L_1 and L_2 (I_{L1} and I_{L2}) for even level converter can be expressed as

$$I_{L1} = -\frac{NI_o}{2(1-D)}, \quad I_{L2} = -\frac{NI_o}{2(1-D)}; \quad \text{when } N = 2, 4, \ldots. \tag{75}$$

For an even number of voltage levels, it is observed that the currents through inductors L_1 and L_2 have equal magnitude and the values are depends on the number of stages. The average currents of inductors L_1 and L_2 (I_{L1} and I_{L2}) for odd level converter can be expressed as

$$I_{L1} = -\frac{(N-1)I_o}{2(1-D)}, \quad I_{L2} = -\frac{(N+1)I_o}{2(1-D)}; \quad \text{when } N = 1, 3, \ldots. \tag{76}$$

The root-mean-square (rms) current through inductors L_1 ($I_{L1,\mathrm{rms}}$) for an even-level converter can be expressed as

$$I_{L1,\mathrm{rms}} = \sqrt{\frac{1}{4}\left(\frac{NI_o}{1-D}\right)^2 + \left(\frac{v_iD}{2\sqrt{3}L_1f}\right)^2}; \quad \text{when } N = 2, 4, \ldots. \tag{77}$$

The rms current through inductors L_2 ($I_{L2,\mathrm{rms}}$) for an even-level converter can be expressed as

$$I_{L2,\mathrm{rms}} = \sqrt{\frac{1}{4}\left(\frac{NI_o}{1-D}\right)^2 + \left(\frac{v_iD}{2\sqrt{3}L_2f}\right)^2}; \quad \text{when } N = 2, 4, \ldots. \tag{78}$$

The rms current through inductors L_1 ($I_{L1,\mathrm{rms}}$) for an odd-level converter can be expressed as

$$I_{L1,\mathrm{rms}} = \sqrt{\frac{1}{4}\left(\frac{(N-1)\,I_o}{1-D}\right)^2 + \left(\frac{v_iD}{2\sqrt{3}L_1f}\right)^2}; \quad \text{when } N = 1, 3, \ldots. \tag{79}$$

The rms current through inductors L_2 ($I_{L2,\mathrm{rms}}$) for an odd-level converter can be expressed as

$$I_{L2,\mathrm{rms}} = \sqrt{\frac{1}{4}\left(\frac{(N+1)\,I_o}{1-D}\right)^2 + \left(\frac{v_iD}{2\sqrt{3}L_2f}\right)^2}; \quad \text{when } N = 1, 3, \ldots. \tag{80}$$

The peak current of inductors L_1 ($I_{L1,p}$) for an even-level converter can be expressed as

$$I_{L1,p} = -\frac{1}{2}\left(\frac{NI_o}{1-D}\right) + \frac{1}{2}\left(\frac{v_iD}{L_1f}\right); \text{when } N = 2, 4, \ldots. \tag{81}$$

The peak current of inductors L_2 ($I_{L2,p}$) for an even-level converter can be expressed as

$$I_{L2,p} = -\frac{1}{2}\left(\frac{NI_o}{1-D}\right) + \frac{1}{2}\left(\frac{v_iD}{L_2f}\right); \text{ when } N = 2, 4, \ldots. \tag{82}$$

The peak current of inductors L_1 ($I_{L1,p}$) for an odd-level converter can be expressed as

$$I_{L1,p} = -\frac{1}{2}\left(\frac{N-1}{1-D}\right)I_o + \frac{1}{2}\left(\frac{v_iD}{L_1f}\right); \quad \text{when } N = 1, 3, \ldots. \tag{83}$$

The peak current of inductors L_2 ($I_{L2,p}$) for an odd-level converter can be expressed as

$$I_{L2,p} = -\frac{1}{2}\left(\frac{N+1}{1-D}\right)I_o + \frac{1}{2}\left(\frac{v_iD}{L_2f}\right); \quad \text{when } N = 1, 3, \ldots. \tag{84}$$

The critical values of inductance for assumed current ripples can be obtained as

$$L_1 = \frac{1}{\Delta I_{L1}}\left(\frac{V_i \times D}{f}\right), \quad L_2 = \frac{1}{\Delta I_{L2}}\left(\frac{V_i \times D}{f}\right). \tag{85}$$

The critical values of capacitance are calculated based on the capacitor of *N* level for assumed voltage ripples as follows:

$$C_k = \frac{-V_oTD}{R_o\Delta v_{Ck}}; \text{ where } k = 1, 2, \ldots, N. \tag{86}$$

The voltage rating of capacitors can be obtained as

$$V_{C1} = \frac{V_i}{1-D}, \quad VC_k = \frac{2V_i}{1-D}; \text{ where } k = 2, 3, \ldots, N. \tag{87}$$

B. Selection of Semiconductor Devices

The voltages across switches can be obtained as

$$V_{Q1} = V_{Q2} = \frac{V_i}{1-D} = -\frac{1}{N}V_o; \text{ where } N = 1, 2, \ldots. \tag{88}$$

It is observed that the required switch voltage rating is less by *1/N* factor compared to output voltage. Therefore, low-voltage rating switches are suitable for the proposed converter.

$$|A| = \frac{RL^2C^2s^4 + (1.5-D)L^2Cs^3 + 3RLC(1-D)^2s^2 + (3-2D)(1-D)^2Ls + (1-D)^4R}{RL^2C^2} \tag{71}$$

The average current through switches can be expressed as

$$\begin{cases} I_{Q1} = -I_o \times \left(\frac{N}{2}\left(\frac{2D-1}{1-D}\right) + N\right) \\ I_{Q2} = -I_o \times \left(\frac{N}{2}\left(\frac{2D-1}{1-D}\right) + N\right) \end{cases}; \text{ where } N = 1, 2, \ldots. \tag{89}$$

The rms current through switches can be expressed as

$$\begin{cases} I_{Q1,\mathrm{rms}} = -I_o\sqrt{\left(\frac{N}{2(1-D)}\right)^2(2D-1) + \left(\frac{N}{1-D}\right)^2(1-D)} \\ I_{Q2,\mathrm{rms}} = -I_o\sqrt{\left(\frac{N}{2(1-D)}\right)^2(2D-1) + \left(\frac{N}{1-D}\right)^2(1-D)} \\ \text{where } N = 1, 2, \ldots. \end{cases} \tag{90}$$

The peak current through switches can be expressed as

$$I_{Q1,p} = \frac{-NI_o}{1-D} + \frac{v_i D}{2L_1 f}, \quad I_{Q2,p} = \frac{-NI_o}{1-D} + \frac{v_i D}{2L_2 f}; \quad \text{where } N = 1, 2, \ldots. \tag{91}$$

The voltage stress of diodes depends on the capacitor voltages since diodes are connected between capacitors. The peak inverse voltage (PIV) of the diodes can be obtained as

$$V_{Dk} = \frac{2V_i}{1-D}; \text{ where } k = 1, 2, \ldots, N. \tag{92}$$

The current rating of the diodes can be obtained as

$$I_{Dk} > I_{L1} \text{ and } I_{L2}; \text{ where } k = 1, 2, \ldots, N. \tag{93}$$

C. Losses and Efficiency

The total input power (P_i) of the converter can be expressed as follows:

$$P_i = V_i I_{L1}(2D-1) + V_i I_{L2}(2D-1) + 2V_i I_{L1}(1-D) + 2V_i I_{L2}(1-D). \tag{94}$$

The output power (P_o) of the converter can be obtained by

$$P_o = V_o^2/R_o. \tag{95}$$

The copper loss in the inductors L_1 and L_2 can be obtained by

$$P_{L,\mathrm{Cu}} = P_{L1} + P_{L2} = {I_{L1,\mathrm{rms}}}^2 R_{L1} + {I_{L2,\mathrm{rms}}}^2 R_{L2}. \tag{96}$$

The conduction loss of the switches Q_1 and Q_2 can be obtained by

$$P_{Q,\mathrm{cond}} = P_{Q1} + P_{Q2} = {I_{Q1,\mathrm{rms}}}^2 R_Q + {I_{Q2,\mathrm{rms}}}^2 R_Q. \tag{97}$$

The switching losses in the switches Q_1 and Q_2 are $P_{Q1,\mathrm{sw}}$ and $P_{Q2,\mathrm{sw}}$, respectively. The total losses in the switches can be obtained by

$$P_{Q,\mathrm{total}} = \left({I_{Q1,\mathrm{rms}}}^2 + {I_{Q2,\mathrm{rms}}}^2\right) R_Q + P_{Q1,\mathrm{sw}} + P_{Q2,\mathrm{sw}}. \tag{98}$$

The total power loss due to diodes can be obtained by

$$P_{D,\mathrm{total}} = \begin{pmatrix} \left({I_{D1,\mathrm{rms}}}^2 + {I_{D2,\mathrm{rms}}}^2 + \cdots + {I_{DN,\mathrm{rms}}}^2\right) R_{dF} \\ + V_{FD}\left(I_{D1,\mathrm{avg}} + I_{D2,\mathrm{avg}} + \cdots + I_{D3,\mathrm{avg}}\right) \end{pmatrix}. \tag{99}$$

The conduction loss due to ESR of capacitors can be obtained by

$$P_{C,\mathrm{total}} = {I_{C1,\mathrm{rms}}}^2 R_{C1} + {I_{C2,\mathrm{rms}}}^2 R_{C2} + \cdots + {I_{CN,\mathrm{rms}}}^2 R_{CN}. \tag{100}$$

The efficiency of the converter can be obtained by

$$\eta_{\mathrm{con}}\mathrm{in}\% = \left(1 - \frac{P_{\mathrm{loss}}}{P_i}\right) \times 100 = \frac{1}{1 + (P_{\mathrm{loss}}/P_o)} \times 100 \tag{101}$$

where P_{loss} is the total loss in the converter, which can be obtained by

$$P_{\mathrm{loss}} = P_{L,\mathrm{Cu}} + P_{Q,\mathrm{total}} + P_{D,\mathrm{total}} + P_{C,\mathrm{total}}. \tag{102}$$

VI. Comparison of Converters

Table II compares the recently proposed topologies with the proposed converter in detail. In [9], a new converter structure is suggested by utilizing SC network. This converter required three capacitors and three diodes, and provides a higher voltage gain with less normalized voltage across switch and diode compared to the classical boost converter. However, the converter structure is not multilevel and interleaved. The voltage gain is limited, high input ripple, and required high-voltage rating capacitor at the output side and high-rating inductor at the input side. In [10], active and SC networks are used to achieve higher positive voltage gain. This converter consists of two inductors and two switches along with diode–capacitor circuitry. This circuitry required two diodes and two capacitors to increase stage by one, whereas in the proposed converter only one diode and one capacitor are required to increase the stage by one. Moreover, the input current ripple is high due to the absence of the interleaved frontend structure.

In [20], a hybrid boost converter is suggested to enhance voltage gain using one inductor and one switch. However, the voltage gain of the converter is positive and restricted due to the requirement of a large number of diodes and capacitors required to design level of the converter. Moreover, the structure is not interleaved, high-current ripple at the input side. In [22], negative and positive VMs are utilized in an interleaved manner in order to reduce input ripples and to achieve high positive voltage gain. However, *2N−1* diodes and *2N−1* diodes are required to design *N* level. The required number of diodes and capacitors in the proposed converter are less compared to the converter presented [22]. Also, compared to that in [22], the main advantage of the proposed converter is that the current loops are reduced by reducing the components or stages to achieve high output voltage. In [22], the ground of the input and output is isolated, which is similar to the proposed converter. The circuitry in [22] required two capacitors and two diodes to increase the output level by one, whereas in the proposed converter only one diode and one capacitor are required to increase the stage by one.

In [23], the classical boost converter front-end structure is used with VM to generate a high output voltage. The converter proposed in [23] required $2N-1$ capacitors and $2N-1$ diodes to design *N*-level VM. It is noted that, in [23], two capacitor and two diodes are required to increase the output stage by one. However, the proposed structure is designed by combining the interleaved

TABLE II
COMPARISON OF CONVERTERS

Parameters	Converters								
	[9]	[10]	[20]	[22]	[23]	[24]-[25]	[26]	[27]	Proposed
Number of stages	-	2	2	N	N	2	N	N	N
Number of switches	1	2	1	2	1	2	2	2	2
Number of inductors	1	2	1	2	1	3	2	2	2
Number of capacitors	3	3	4	2N-1	2N-1	3	N+1	5	N
Number of diodes	3	3	4	2N-1	2N-1	3	N+1	4	N
Gain ($G=V_o/V_i$)	$\frac{2}{1-D}$	$\frac{3+D}{1-D}$	$\frac{3-D}{1-D}$	$\frac{N}{1-D}$	$\frac{N}{1-D}$	$\frac{1}{D(1-D)}$	$\frac{N+1}{1-D}$	$\frac{4}{1-D}$	$\frac{N}{1-D}$
Output diode voltage/input voltage	G/2	(G+1)/2	(G-1)/2	G/N	G/N	D_1=G(1-D), D_2 and D_3=GD	G	G/2	2G/N
Switch voltage/input voltage	G/2	(G+1)/4	(G-1)/2	G/N	G/N	Q_1=G(1-D), Q_2=GD	G/5	G/2	G/N
capacitor voltage/input voltage	G	(G+1)/4	(G-1)/2	G/N	G/N	C_1=G(1-D), C_2=GD	G	G	2G/N
Symmetrical capacitors & diodes for extension	X	Yes	Yes	Yes	Yes	X	No	X	Yes
Single capacitor at load	Yes	No	No	No	No	No	Yes	Yes	No
stack of capacitors at output	No	Yes	Yes	Yes	Yes	Yes	No	No	Yes
Interleaved structure	No	No	No	Yes	No	Yes	Yes	Yes	Yes
Multilevel structure	No	Yes (2 Stage)	Yes	Yes	Yes	Yes (2 Stage)	Yes	No	Yes
Number of capacitor required for increasing 1 stage	X	2	4	2	2	X	1	X	1
Number of diodes required for increasing 1 stage	X	2	4	2	2	X	1	X	1
Efficiency	94%	92.5%	94%	89%	89%	91.5%	92%	91.4%	93.56%
Type of output load with respect to Input voltage	Floating	Floating	Floating	Floating	Ground	Floating	Ground	Floating	Floating

structure with VM, which results in higher output voltage with less number of components. The proposed converter required only one diode and one capacitor to increase the stage by one. Therefore, for generating the desired output voltage from the given input voltage, the proposed converter will utilize less number of capacitors and diodes than those in [23]. Also, compared to the work in [23], the main advantages of the proposed converter are the current loops that are reduced by reducing the components or stages to achieve the same output voltage that increases the efficiency and provides a solution to achieve higher output voltage using less number of components, and input current ripple is minimum due to the interleaved structure. Furthermore, compared to the work in [23], the inductor with low current capability is also suitable for the proposed converter due to the interleaved structure. In [24] and [25], two stages of diode–capacitor (three capacitors and four diodes) utilized in an interleaved manner in order to reduce input ripples and to improve voltage gain. The propose circuit suggested in [24] and [25] required three inductors and two switches and the voltage gain is limited. Furthermore, the structure is 2-level, and capacitor stacks are available at the output side. However, the voltages across load-side capacitors and diodes are not equal.

In [26], the interleaved front-end boost structure is used with intermediate VM cell to achieve higher voltage gain and low input current ripple. Compared to the proposed converter, this converter required high-voltage rating capacitor and diode at the output side. Compared to the proposed converter, same number of reactive components is required to achieve given voltage gain. However, in [26], the ratings of all the used capacitors are not the same, which makes circuit costly and complex. Also, the rating of the capacitor increases with the number of levels. Furthermore, in [27], the interleaved converter is used with a Dickson charge pump. This structure required one diode less compared to the converter in [26]. However, the structure presented in [27] is not possible to extend for higher voltage gain. Moreover, this converter also required high-voltage rating capacitor and diode at the output side. Therefore, compared to the available converter, the proposed converter provides a solution to attain a high voltage gain and low input current ripple, with utilizing reduced number of components and devices. Moreover, the proposed converter consisted stack of the output capacitor and required equal voltage rating components and device to increase levels.

VII. EXPERIMENTAL INVESTIGATION

The steady-state operation of the proposed interleaved-MBC is validated through the experimental work. The photograph of the implemented prototype is shown in Fig. 13 and specifications are given in Table III. The duty cycle is calculated by including the term efficiency for more practical value. The required duty cycle is calculated as follows:

$$D = 1 - \frac{NV_i}{V_o}\eta_{\text{worst}} = 1 - \frac{6 \times 20}{-(-300)} \times 0.90 = 0.64 \quad (103)$$

where η_{worst} is the expected converter efficiency in worst case. The critical inductances are calculated by considering the inductor current ripples 4 A as follows:

$$L_{1,\text{crit}} = \frac{20 \times 0.64}{4 \times 50\,000} = 64\ \mu\text{H}$$

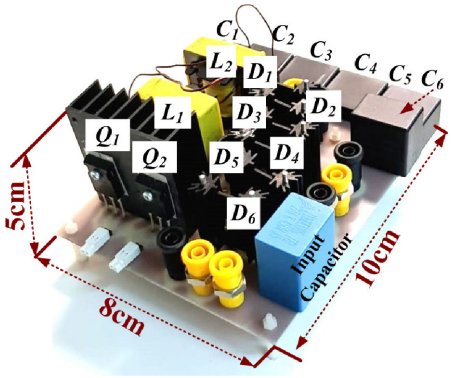

Fig. 13. Photograph of implemented proposed converter with six levels.

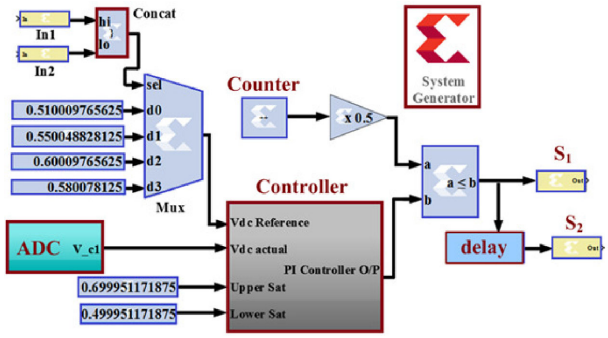

Fig. 14. Control scheme of the proposed converter.

TABLE III
SPECIFICATION OF THE PROPOSED CONVERTER

Parameters and Components	Values	Quantity
Input voltage	20 V	-
Output voltage	-300 V	-
Output Power	300 W	-
Number of level	6	-
Inductors	200 µH, 20A, R_L=80mΩ	2
Capacitors	15 µF, 160V, ESR=4mΩ	6
Input capacitor	22uF, 100V	1
Switching frequency	50 kHz	-
MOSFET	FQH44N10, (R_S = 0.039Ω)	2
Diodes	SDUR3020W, (V_{DF}= 0.95)	6
Sensor	LEM LV 20-P	1

$$L_{2,\text{crit}} = \frac{20 \times 0.64}{4 \times 50\,000} = 64\ \mu\text{H}. \tag{104}$$

The critical capacitances are calculated by considering the capacitor voltage ripple 1 V as follows:

$$C_k(k = 1to6) = \frac{(-V_o)\,TD}{R_o \Delta v_{Ck}} = \frac{-(-300) \times 0.64}{300 \times 1 \times 50\,000} = 12.8\ \mu\text{F}. \tag{105}$$

The voltage ratings of capacitors are calculated as follows:

$$V_{Ck} = \frac{2V_i}{1-D} = \frac{40}{1-0.64} = 111.1\,\text{V}, \quad k = 2, \ldots, 6. \tag{106}$$

The voltage ratings of diodes are calculated as follows:

$$VD_k = \frac{2V_i}{1-D} = \frac{2 \times 20}{1-0.64} = 111.1\,\text{V}, \quad k = 1, 2, \ldots, 6. \tag{107}$$

The voltage ratings of MOSFETs are calculated as follows:

$$V_{Q1} = \frac{V_i}{1-D} = \frac{20}{1-0.64} = 55.5\,\text{V}$$
$$V_{Q2} = \frac{V_i}{1-D} = \frac{20}{1-0.6} = 55.5\text{V}. \tag{108}$$

Two equal inductors of 200 μH are made with the ferrite E-type cores for the 20-A rms current rating. Flat-type heat sink and hook-type heat sink are used for MOSFET (FQH44N10) and diodes (SDUR3020W), respectively. Capacitors with rating 15 μF, 160 V are used to design six-level interleaved-MBC. The FPGA vertex-5 platform is utilized for the generation of the 50-kHz carrier signal with 100-ns sampling rate. The control block includes counter, ADC, PI controller, logic gates, multiplexer, constant, etc., as shown in Fig. 14. The multiplex (4:1) is used to select the output voltage reference. The required value of the output voltage is chosen through MUX. The actual output voltage is fed to PI controller using LEM LV 20-P and ADC. In PI controller, the actual output voltage is compared with required output voltages, and control signal is generated based on the difference between actual and required output voltage. The control signal is compared with sawtooth generated waveform to obtain pulses for switch Q_1. The delay block (180°) is used to generate pulse for switch Q_2. In the switching pulse generation logic, the lower duty limit is set as 52% and the upper saturation is set at 80%. The length, breadth, and height of the designed converter are 10, 8, and 5 cm, respectively. The power density of the designed converter prototype is calculated as follows:

$$\rho_{\text{Power}} = \frac{\text{Power}}{\text{Volume}} = \frac{300}{10 \times 8 \times 5} = 0.75\ \text{W/cm}^3. \tag{109}$$

Fig. 15(a) depicts the waveform of the output voltage, output current, input voltage, and input current. The average values of output voltage are -299.88 V and output current of -0.99 A is flowing through the load. The input voltage is 20.1 V and average value of the input current to feed load of 300 W is 15.83 A. It is clearly visible that the input current ripple frequency is 100 kHz i.e., twice the switching frequency (50 kHz) due to the interleaved operation of the converter. In Fig. 15(b), voltage and current of inductors L_1 and L_2 are shown. It is observed that Mode I is placed in between the Modes II and III in every switching cycle and is considered as a discharging state for the output capacitor of the multiplier circuit. In Mode I, the voltages across inductors L_1 and L_2 are 20 V each. In Mode II, the voltages across inductor L_1 and L_2 are 20 and -33.52 V, respectively. In Mode III, the voltages across inductors L_1 and L_2 are 20 and -32.4 V, respectively. Therefore, the average current through inductors voltage inductors L_1 and L_2 are 7.84 and 7.92 A, respectively. In Fig. 15(c), diodes D_1 and D_2 voltage waveforms are shown along with inductors L_1 and L_2 current waveforms for reference. It is observed that the voltages across diodes are in steps. The maximum voltage observed across diodes D_1 and D_2 are observed in Modes III and II, respectively. In Mode I, the voltage across diodes D_1 and D_2 are -53.1 V. In Mode II, diode

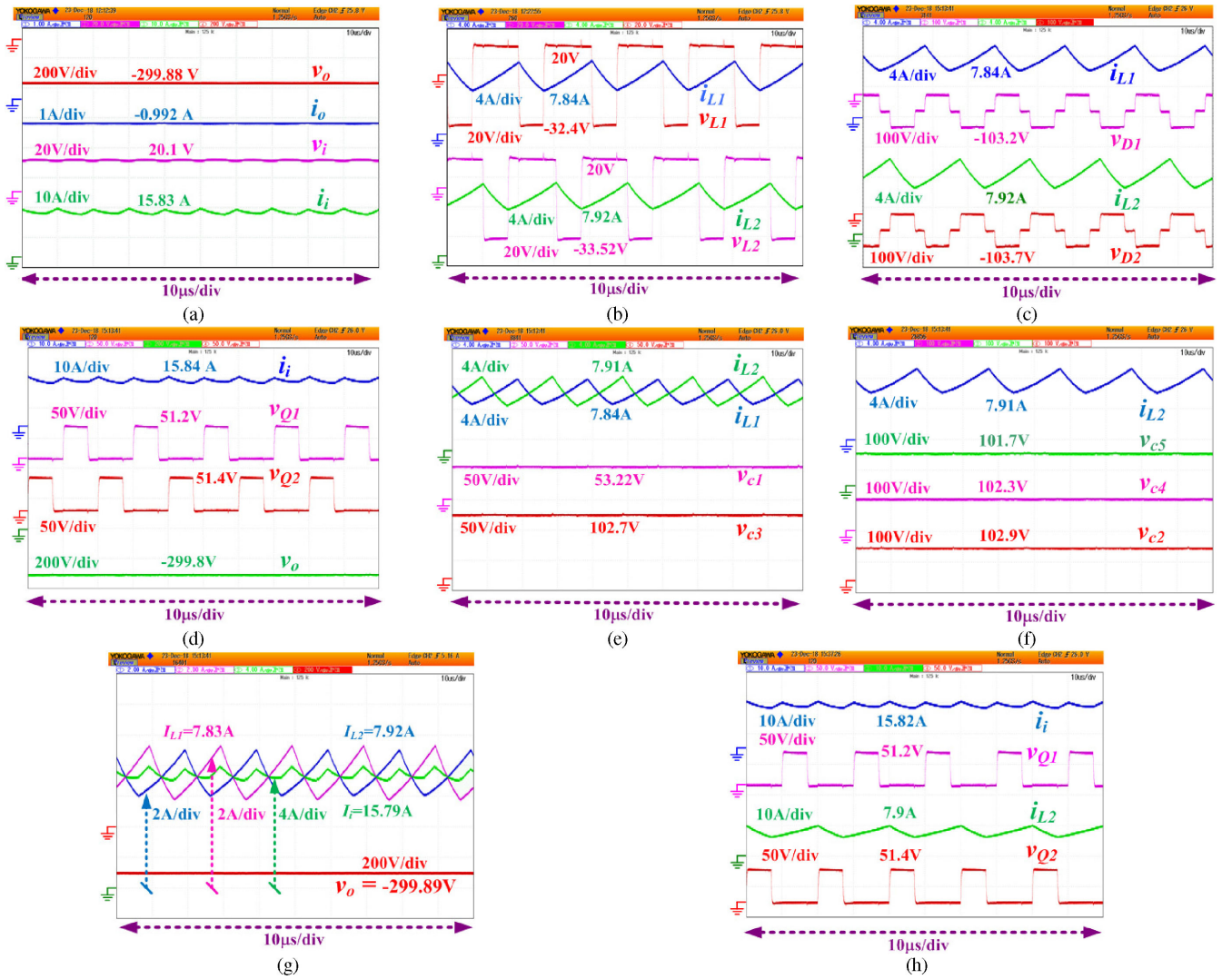

Fig. 15. Experimental results. (a) Input current, input voltage, output current, and output voltage. (b) Inductor L_2 voltage and current, and inductor L_1 voltage and current. (c) Diode D_2 voltage, inductor L_2 current, diode D_1 voltage, and inductor L_1 current. (d) Output voltage, switch Q_2 voltage, switch Q_1 voltage, and input current. (e) Capacitor C_3 voltage, capacitor C_1 voltage, and inductor L_1 and L_2 currents. (f) Capacitor C_2 voltage, capacitor C_4 voltage, capacitor C_5 voltage, and inductor L_2 current. (g) Output voltage, inductor L_1 and L_2 currents, and input current. (h) Switch Q_2 voltage, inductor L_2 current, switch Q_1 voltage, and input current.

D_2 blocks the voltage −103.2 V, and diode D_1 is forward biased. In Mode III, diode D_1 blocks the voltage −103.2 V, and diode D_2 is forward biased. The MOSFET Q_1 and Q_2 drain-to-source voltages along with the output voltage and input current are shown in Fig. 15(d). For MOSFET Q_1 and Q_2, the voltage stresses are 51.2 and 51.4 V, respectively. It is investigated that the voltage across the switch is one-sixth of the total output voltage, which is expected according to the theoretical analysis. It is visible that the input current is 15.84 A, and have reduced ripples due to the interleaved structure at the input side.

Fig. 15(e) shows the voltages across the capacitor C_1 and C_3 along with the inductor L_1 and L_2 currents, which cumulatively forms the very less ripples at the input side. The observed values of the voltages across capacitors C_1 and C_3 are 53.22 and 102.72 V, respectively. The voltages across capacitors C_2, C_4, and C_5 are shown in Fig. 15(f). It is investigated that the voltages across capacitor C_2, C_4, and C_5 are 102.9, 102.3, and 101.7 V, respectively. Hence, it is confirmed that the voltage across the capacitor is the same except for capacitor C_1. Thus, each capacitor except C_1 contributes $2/(1-D)$ times of the input voltage to the output voltage, whereas capacitor C_1 contributes $1/(1-D)$ time input voltage. The overlap-interleaved currents of the inductors are shown with input currents and output voltages in Fig. 15(g). It is observed that currents 7.92 and 7.83 A are flowing through the inductors L_2 and L_1, respectively, and the observed input current is 15.79 A while −299.89 V is achieved at the load. The requirement of the input capacitor is reduced due to a reduction in the higher frequency (twice the switching frequency) input current ripple. Fig. 15(h) shows the voltages across switches Q_1 and Q_2, current through inductor L_2, and input current. It is clearly observed that both the switches Q_1 and Q_2 are operated at 180° phase shift and inductor L_2 is charging when switch Q_2 is turned ON. The designed prototype is tested under perturbation of the output reference voltage $(v_{o,\mathrm{ref}})$

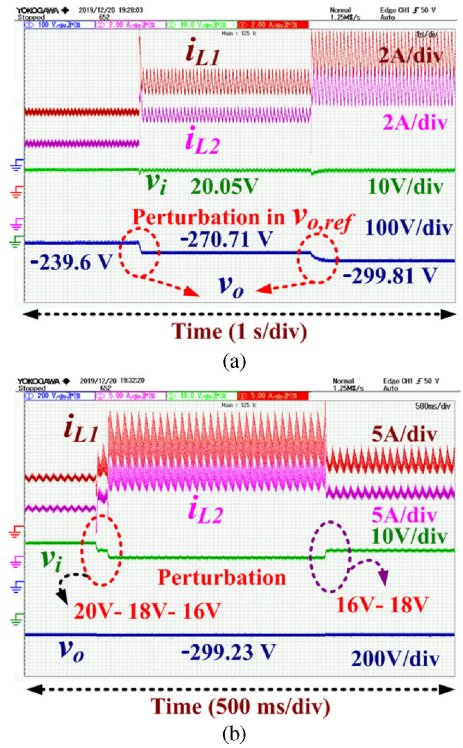

Fig. 16. Experimental results. (a) Output voltage, input voltage, and current through inductors L_2 and L_1 waveforms when reference of output voltage changed. (b) Output voltage, input voltage, and current through inductors L_2 and L_1 waveforms when input voltage changed.

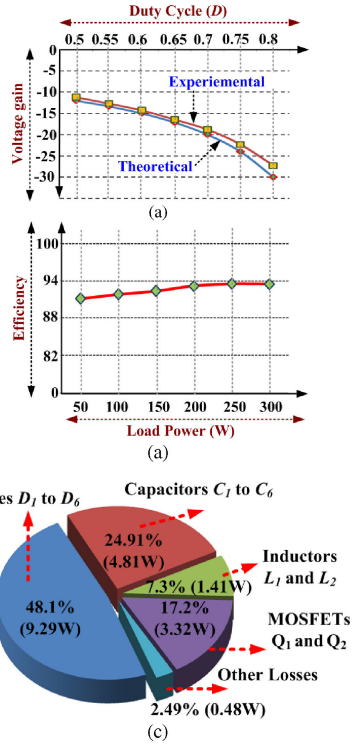

Fig. 17. (a) Voltage gain versus duty cycle. (b) Efficiency versus load power. (c) Loss distribution in percentage and in watt.

and input voltage (v_i) in order to test dynamics characteristics of converter and accuracy of the controller. Case I: the output reference voltage is changed from -240 V to -270 V to -300 V and input voltage is set at 20.5 V. The observed input voltage, output voltage, and inductor currents waveforms are shown in Fig. 16(a). It is clearly visible that the required voltage at the output port is achieved without change in the input voltage. The duty cycles for both the switches are adjusted automatically to achieve required output voltage. The input voltage is changed from 20 V to 18 V to 16 V and the output voltage reference is set at -300 V, and the observed input voltage, output voltage, and inductor currents waveforms are shown in Fig. 16(b). It is observed that the value of output voltage, i.e., -299.23 V is constant, even the input voltage is changed from 20 V to 18 V to 16 V and from 16 V to 20 V. The inductor currents are changed according to the variation to maintain power equality at input and output ports. The experimental work is conducted for the different load power to test the performance and efficiency. Fig. 17(a) and (b) shows the plot of voltage gain versus duty cycle, and efficiency versus load power, respectively. It is observed that 93.56% efficiency is achieved when load power is 300 W. Fig. 17(c) shows the loss distribution and it is observed that the most of the losses occurs due to diodes (48.1% of the total loss, i.e., 9.29 W).

VIII. Conclusion

Interleaved-MBC configuration is presented for high-voltage step-up applications. The circuit is derived from the combination of front-end structure of the interleaved converter and VM cells. Unlike the standard MBC, only one capacitor and one diode are needed to increase the level by one. The benefits of the proposed converter include reduced ripple at the input side, higher voltage gain using less number of components, the circuitry that is easily extendable to any higher number of levels, modular structure and feasible to use low-voltage rating components, and the voltage across capacitors after first level of VM cell are equal. The detailed analysis using nonidealities, operation modes, and the boundary conditions for CCM and DCM are explained in detail. Additionally, the proposed converter is compared with the recently proposed converters to reflect the novelty of the proposed circuit. The experimental results of the six-level proposed converter are provided, which validates the operation and practicability of the converter. Furthermore, the previous investigation shows that the proposed converter is a potential solution to achieve high voltage gain and reduce input current ripple.

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