Hybrid Alternate-Common Arm Converter With High Power Capability: Potential and Limitations

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***Abstract*—This article studies a new hybrid converter that utilizes thyristors and full-bridge (FB) arms for achieving high-power capability with reduced semiconductor power rating compared to the FB modular multilevel converter. The study covers the theoretical analysis of the energy balancing, the dimensioning principles, the maximum power capability, and the limitations imposed by the discontinuous operation of the converter. Based on the analysis of these aspects, the theoretical analysis is concluded by identifying the operational constraints that need to be fulfilled for maximizing the power capability of the converter. It is concluded that the maximum power capability can be achieved for a certain range of modulation indices and is limited by both the commutation time of the thyristors and the power angle. Moreover, the *P*–*Q* capability of the hybrid converter is presented and discussed. Finally, simulation and experimental results that confirm the theoretical analysis and the feasibility of the studied converter are presented and discussed.**

***Index Terms*—DC–AC power conversion, high-voltage dc (HVdc) transmission, static VAr compensators, thyristors.**

I. INTRODUCTION

THE thyristor-based line-commutated converter (LCC) has been employed, since the 1960s for enabling high-voltage dc (HVdc) transmission. The main advantages of the LCC is high efficiency, high surge-current capability, and dc-fault ride-through capability. However, the LCC suffers from sensitivity to ac-grid disturbances, lack of independent active–reactive power control, high reactive-power consumption, and low-order harmonics in the ac-side currents [1]. The two-level voltage-source converter (VSC) solves many of the shortcomings of the LCC, but suffers from relatively low efficiency, high cost, and lack of dc-fault blocking capability. Since the LCC and VSC technologies feature complementary characteristics, research has been performed on how to combine them either for compensating the harmonics [2]–[4] or the reactive power of the LCC [5], [6], while improving the efficiency of the combined system.

The modular multilevel converter (MMC) [7] is a recently proposed VSC technology that remedies some of the shortcomings of the two-level VSC and opens new possibilities for the combination of the LCC and VSC technologies. Research has been performed on utilizing the half-bridge (HB)-MMC for eliminating the risk of commutation failures of the LCC, while the LCC is utilized for achieving dc-fault blocking [8], [9] that is required in overhead line applications. The utilization of the FB-MMC has been proposed for enabling the independent active–reactive power control of the LCC [10]. Even though the MMC is very well suited for HVdc applications, it suffers from high semiconductor ratings [11] and high energy storage requirements [12]. Therefore, an interesting research direction that has been addressed extensively in the literature is the combination of MMC arms with series-connected switches for reducing the energy storage requirements, the rating of the semiconductor devices, the conduction losses, or a combination of these [13]–[15]. An extensive review of such concepts was presented in [16].

Recently, the use of thyristors in VSCs has gained research attention. For example, in [17], a variant of the alternate-arm converter with thyristor-based director switches is proposed for reducing the conduction losses. Furthermore, variants of a thyristor-based two-level VSC that employs a modular STATCOM for turning-OFF the thyristor switches and controlling the ac-side currents are proposed in [3], [18], [19]. Both circuits reduce the total rating of the semiconductors and the energy storage elements compared to the MMC. The variations of an FB-MMC proposed in [18] and [20]–[22], utilize thyristor (or diode) switches for bypassing a converter arm or small groups of series-connected FB submodules (SMs), which leads to a significant loss reduction. Moreover, a thyristor-based HB SM was proposed in [23] and [24] for constructing a thyristor-based MMC with reduced conduction losses. This SM is complemented with series-connected FB-SMs for turning-OFF the thyristors. Finally, the circuit proposed in [25] and [26] utilizes the thyristors not only for reducing the conduction losses, but also for reconfiguring the circuit in such a way that the energy storage requirements are reduced compared to the MMC. One main challenge in all the proposed circuits is the turn-OFF process of the thyristors, which cannot be turned OFF by gate control.

In this article, the converter that has been proposed in [27] and [28] is studied in depth. This converter employs thyristor

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switches for connecting arms in parallel, in order to double the ac-terminal current of the converter. Therefore, the power capability of the studied converter can be doubled without doubling the total power rating of the semiconductors compared to an FB-MMC, under certain operating conditions. However, the discontinuous operation of the converter and the thyristor turn-OFF process impose limitations on the converter's power capability, as shown in this article. The contributions of this article are summarized as follows.

1) In-depth theoretical analysis of the operating principles and the energy balancing of the converter.
2) Investigation of the operational and design limitations imposed by the discontinuous operation and the thyristor turn-OFF process.
3) Identification of the operating conditions for which the power capability of the studied converter is maximized.
4) Derivation of the *P–Q* capability curve of the studied converter, verification of the *P–Q* curve by simulations, and comparison with an FB-MMC.
5) Demonstration of the feasibility of the studied converter by both simulations and experiments.

Note that this article focuses on steady-state analysis and hence it does not cover the evaluation of the transient and fault ride-through performance of the discussed converter.

The rest of this article is organized as follows. Section II presents the main circuit and the operating principles of the converter. Section III provides the analytical derivation of the current required for the energy balancing of all arms and discusses the impact of this current on the peak arm currents. In Section IV, the operational conditions that maximize or limit the power capability of the converter are identified. Section V presents the operating and design conditions that need to be fulfilled for achieving maximum power capability. Section VI briefly describes the control and commutation scheme that was employed for controlling the studied converter. Section VII presents simulation results that confirm the theoretical analysis and the derived *P–Q* capability curve, while VIII shows experimental results that confirm the feasibility of the studied converter. Finally, Section IX presents a comparison of the studied converter with the FB-MMC and discusses circuit design and dynamic performance considerations. Finally, Section X concludes this article.

II. MAIN CIRCUIT AND OPERATING PRINCIPLES

A. Main Circuit

The single-phase circuit of the studied hybrid converter was initially presented in [27] and is illustrated in Fig. 1. The hybrid converter studied in this article consists of the following:

1) two main arms, i.e., upper and lower, which form an MMC leg;
2) two director switches, i.e., upper and lower, which are thyristors in this article, but could also be any self-commutated device;
3) one common arm that is connected between the midpoints of the MMC leg and the director switches;
4) two main inductors (L_u, L_l) that are utilized for current-control and current-filtering purposes;

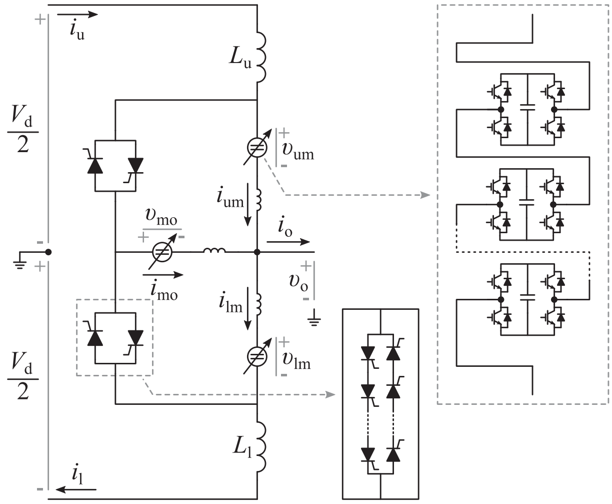


Fig. 1. Single-phase circuit of the HACC with the symbols of the important quantities (currents, voltages). Arms of series-connected FB-SMs are illustrated as variable voltage sources, while series-connected thyristors are illustrated as single thyristor switches.

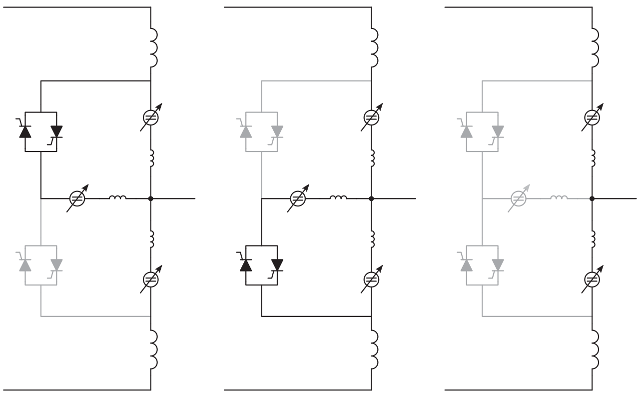

(csu) (csl) (trn)

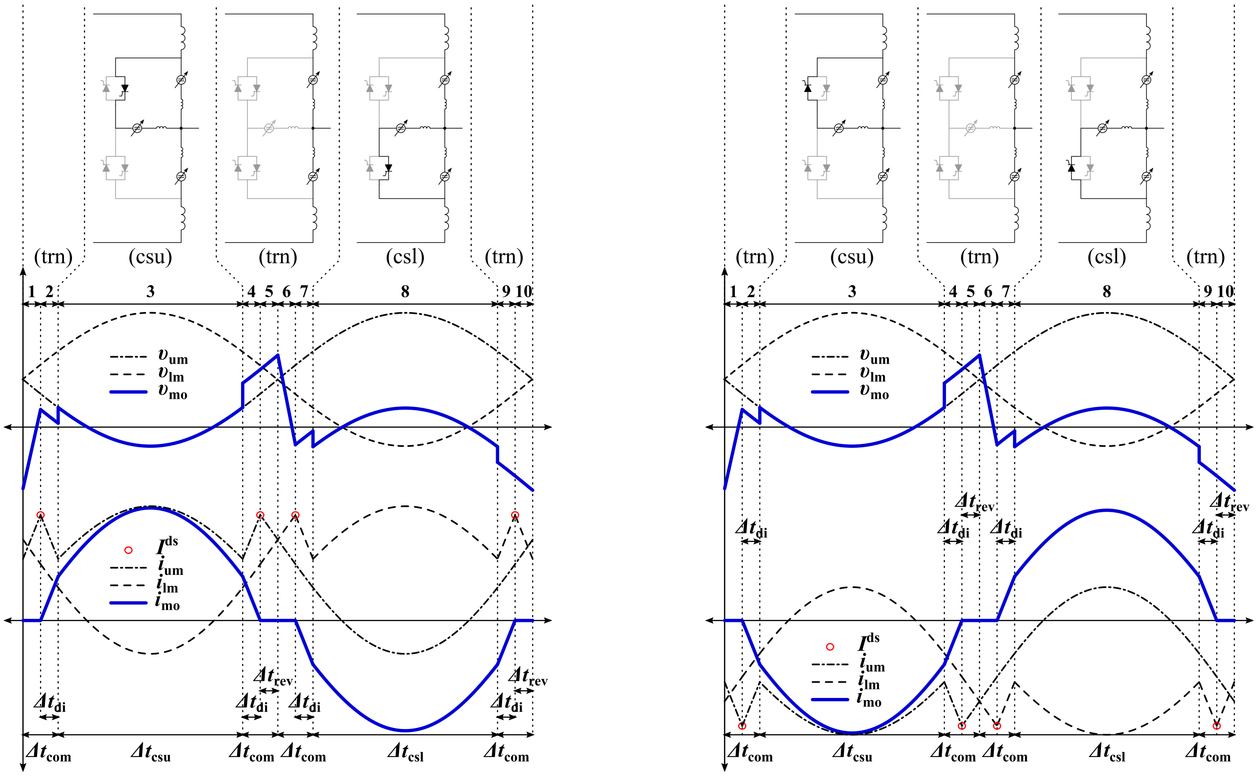
Fig. 2. Switching states of the proposed hybrid topology: (csu) common arm in parallel with the main-upper arm; (csl) common arm in parallel with the main-lower arm; (trn) common arm in transition between the two other states.

5) three inductors inside the loops formed by the main and common arms (termed *current-sharing loops*) that are much smaller than the main inductors (in the range of 10–20%) and are employed for limiting the di/dt during thyristor switchings as well as for current-sharing control.

Note that the director switches consist of series-connected thyristors and all arms consist of series-connected FB SMs. The main arms are operated similarly to an MMC, while the common arm is alternately connected in parallel to either the upper or the lower arm, depending on the switching state of the converter. Due to this alternation of the common arm, the proposed converter is termed hybrid alternate-common arm converter (HACC).

B. Switching States

The three switching states of the HACC are depicted in Fig. 2 and are namely: 1) current-sharing-upper state (csu) during which the common arm is connected in parallel to the



(a) (b)

Fig. 3. Timing diagram depicting the state intervals (1–10) of the HACC in relation to the voltage and current waveforms of the main (v_{um}-i_{um}, v_{lm}-i_{lm}) and common arms (v_{mo}-i_{mo}) over one fundamental cycle, for (a) inverter and (b) rectifier mode. Observe the definition of the discontinuity current I^{ds} that should be considered for the dimensioning of the converter.

upper arm; 2) current-sharing-lower state (csl) during which the common arm is connected in parallel to the lower arm; and 3) transition state (trn) during which the common arm transits among the previous two states and the current through this arm is zero. Moreover, the timing diagram that illustrates the transition between these different states is depicted in Fig. 3 for both inverter and rectifier mode. Observe that Fig. 3 shows that only the downward-facing and the upward-facing thyristors are conducting during inverter and rectifier mode, respectively. Even though it is possible to utilize both downward- and upward-facing thyristors during each mode, this is not considered in this study, as it adds complexity without significant benefits. The intervals shown in Fig. 3 are briefly described as follows.

1) Interval 1: The HACC is in the (trn) state and transits towards the (csu) state under a limited dv/dt rate.
2) Interval 2: the common arm enters the (csu) state by forward biasing one of the upper thyristors and increasing the current under a limited di/dt rate.
3) Interval 3 (Δt_{csu}): the common arm is in the (csu) state and shares the terminal current i_{u} with the upper arm.
4) Interval 4: the common arm starts exiting the (csu) state by applying a certain reverse voltage for turning OFF the conducting thyristor at a limited di/dt rate.
5) Interval 5: the common arm is in the (trn) state but continues to apply the reverse voltage on the turned-OFF thyristor for the time interval Δt_{rev}.
6) Interval 6: the common arm transits toward the (csl) state under a limited dv/dt rate.
7) Interval 7: the common arm enters the (csl) state by forward biasing one of the lower thyristors and increasing the current under a limited di/dt rate, as for interval 2.
8) Interval 8 (Δt_{csl}): the common arm is in the (csl) state and shares the terminal current i_{l} with the lower arm.
9) Interval 9: the common arm starts exiting the (csl) state by applying a reverse voltage for turning OFF the conducting thyristor at a limited di/dt rate, as for interval 4.
10) Interval 10: the common arm is in the (trn) state but continues to apply the reverse voltage on the turned-OFF thyristor for the time interval Δt_{rev}, as for interval 5.

As shown in Fig. 3, the thyristor turn-OFF process does not impact the voltage waveform of the main arms; thus, it does not distort the ac-terminal voltage. Furthermore, in Fig. 3, a certain current peak is highlighted in red circle and denoted by the superscript "ds," this is termed the discontinuity current and is important for deriving the dimensioning limitations of the HACC, as will be shown in the next sections of this article.

The thyristor turn-OFF process is characterized by the time interval Δt_{com}, which is shown in Fig. 3, is termed commutation time and includes: 1) the time interval of limited di/dt (i.e., intervals 4, 9), represented by Δt_{di}; and 2) the reverse-biasing interval Δt_{rev} (i.e., intervals 5, 10), which should be longer than the extinction time t_{q} required for reliable thyristor turn-OFF. The intervals of transition between states (i.e., 6, 7 and 1, 2) have been assumed to last also for Δt_{com}, in order to have a certain symmetry that simplifies the theoretical analysis. Another assumption that was made for simplifying the analytical expressions of the converter currents was that the interval Δt_{di} is very small, i.e., the current through the thyristors becomes zero instantaneously. This is assumed because the current-sharing inductors are small enough to allow di/dt rates in the range of 10–15 A/μs during thyristor turn ON/OFF and because the turn-ON/OFF current is below 1000 A; thus, $\Delta t_{\mathrm{di}} < 100\ \mu$s.

C. Operating Principles

The ac-side voltage and current of the HACC are assumed to be sinusoids with fundamental frequency $f_1 = 50$ Hz and are given by

$$v_{\mathrm{o}}(t) = \hat{V}_{\mathrm{o}} \sin(\omega_1 t) \tag{1}$$

$$i_{\mathrm{o}}(t) = \hat{I}_{\mathrm{o}} \sin(\omega_1 t - \varphi) \tag{2}$$

where $\omega_1 = 2\pi f_1$ is the fundamental angular frequency, $\hat{V}_{\mathrm{o}}$ and $\hat{I}_{\mathrm{o}}$ are the amplitudes of the ac-side voltage and current, respectively, while φ is the power angle of the converter arms; that is, $\varphi = 0^\circ$ means that the alternating components of the arm voltage and arm current are in phase. Observe that the ac-side quantities are termed as output quantities for the rest of this article.

The HACC exploits the inherent asymmetry of the terminal currents i_{u}, i_{l}, the waveforms of which are identical to an MMC and are given by

$$i_{\mathrm{u}}(t) = \frac{I_{\mathrm{d}}}{3} + \frac{i_{\mathrm{o}}(t)}{2} \tag{3}$$

$$i_{l}(t) = \frac{I_{\mathrm{d}}}{3} - \frac{i_{\mathrm{o}}(t)}{2} \tag{4}$$

where i_{o} is the output current given by (2), while I_{d} is the dc-link current, given by

$$I_{\mathrm{d}} = \frac{3}{4} M \hat{I}_{\mathrm{o}} \cos\varphi. \tag{5}$$

The asymmetry of the terminal currents becomes evident by inspecting (3) and (4), which reveal that the peak of the upper terminal current (i_{u}) is occurs during one half-cycle, while the peak of the lower terminal current (i_{l}) occurs during the other half-cycle. Therefore, the common arm is connected in parallel to the upper arm for the half-cycle during which the peak of the upper terminal current occurs, and in parallel to the lower arm for the half-cycle during which the peak of the lower terminal current occurs.

The voltages generated by the main arms are given by

$$v_{\mathrm{um}}(t) = \frac{V_{\mathrm{d}}}{2} - v_{\mathrm{o}}(t) = \frac{V_{\mathrm{d}}}{2} - M\frac{V_{\mathrm{d}}}{2}\sin(\omega_1 t) \tag{6}$$

$$v_{\mathrm{lm}}(t) = \frac{V_{\mathrm{d}}}{2} + v_{\mathrm{o}}(t) = \frac{V_{\mathrm{d}}}{2} + M\frac{V_{\mathrm{d}}}{2}\sin(\omega_1 t) \tag{7}$$

where v_{o} is the converter output voltage given by (1), V_{d} is the dc-link voltage, and M is the modulation index, i.e., the ratio between the amplitude of the output voltage and half of the dc-link voltage or $M = 2\hat{V}_{\mathrm{o}}/V_{\mathrm{d}}$. By considering the current-sharing intervals illustrated in Fig. 3 and assuming that $\Delta t_{\mathrm{di}} = 0$, the currents through the main arms are given by

$$i_{\mathrm{um}}(t) = \begin{cases} i_{\mathrm{u}}(t), & 0 \le \omega_1 t < \Delta\theta_{\mathrm{com}} \\ p i_{\mathrm{u}}(t) + I_{\mathrm{dx}}, & \Delta\theta_{\mathrm{com}} \le \omega_1 t < \pi - \Delta\theta_{\mathrm{com}} \\ i_{\mathrm{u}}(t), & \pi - \Delta\theta_{\mathrm{com}} \le \omega_1 t < 2\pi \end{cases} \tag{8}$$

$$i_{\mathrm{lm}}(t) = \begin{cases} i_{l}(t), & 0 \le \omega_1 t < \pi + \Delta\theta_{\mathrm{com}} \\ p i_{l}(t) + I_{\mathrm{dx}}, & \pi + \Delta\theta_{\mathrm{com}} \le \omega_1 t < 2\pi - \Delta\theta_{\mathrm{com}} \\ i_{l}(t), & 2\pi - \Delta\theta_{\mathrm{com}} \le \omega_1 t < 2\pi \end{cases} \tag{9}$$

where p is the current-sharing factor that defines the portion of the terminal current that flows through the main arms, while I_{dx} is a direct current that circulates in the current-sharing loops and ensures the energy balancing of the parallel-connected arms. Note that the current-sharing factor takes values in the range $p = [0, 1]$, with $p = 1$ meaning that no current sharing occurs and the terminal currents flow exclusively through the main arms, and $p = 0$ meaning that the terminal currents flow only through the common arm during the respective current-sharing interval (yet, the current through the main arms is not zero, as a balancing current I_{dx} is required to balance the energy of all arms). Since the waveforms of the upper and lower arms are symmetrical, only those of the upper arm are considered for the rest of this article.

The current through the common arm is derived by the difference of the corresponding terminal current and the balancing current for each half-period and is expressed by

$$i_{\mathrm{mo}}(t) = \begin{cases} 0, & 0 \le \omega_1 t < \Delta\theta_{\mathrm{com}} \\ x i_{\mathrm{u}}(t) - I_{\mathrm{dx}}, & \Delta\theta_{\mathrm{com}} \le \omega_1 t < \pi - \Delta\theta_{\mathrm{com}} \\ 0, & \pi - \Delta\theta_{\mathrm{com}} \le \omega_1 t < \pi + \Delta\theta_{\mathrm{com}} \\ I_{\mathrm{dx}} - x i_{l}(t), & \pi + \Delta\theta_{\mathrm{com}} \le \omega_1 t < 2\pi - \Delta\theta_{\mathrm{com}} \\ 0, & 2\pi - \Delta\theta_{\mathrm{com}} \le \omega_1 t < 2\pi \end{cases} \tag{10}$$

where $x = (1 - p)$, with p being the current-sharing factor. By inspecting (8)–(10) it can be observed that during the current-sharing intervals ($\Delta t_{\mathrm{csu}} = [\Delta\theta_{\mathrm{com}}, \pi - \Delta\theta_{\mathrm{com}}]$, $\Delta t_{\mathrm{csl}} = [\pi + \Delta\theta_{\mathrm{com}}, 2\pi - \Delta\theta_{\mathrm{com}}]$) the sum of the currents of the main and common arms is equal to the terminal current (i_{u}, i_{l} that is being shared.

III. ENERGY BALANCING AND PEAK ARM CURRENTS

A. Circulating Current for Arm Energy Balancing

As shown in [27] and introduced in (8)–(10), a balancing current I_{dx} is required for ensuring that the net energy within a fundamental cycle is zero through all arms. Note that in this article, in contrast to [27], I_{dx} is derived by considering a nonzero commutation time Δt_{com}. This derivation is performed by equating the upper-arm energy E_{um} over one fundamental cycle with zero and solving for I_{dx}, i.e.,

$$E_{\mathrm{um}} = \int_0^{2\pi} v_{\mathrm{um}}(t) i_{\mathrm{um}}(t) dt = 0 \tag{11}$$

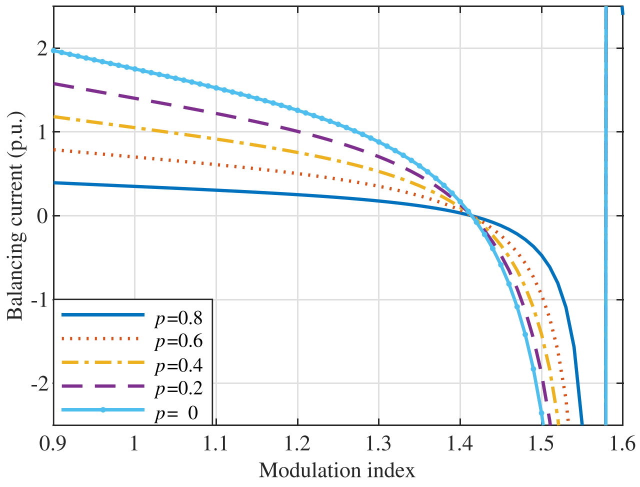


Fig. 4. Balancing current I_{dx} (normalized with respect to $I_{\mathrm{d}}/3$) versus M for different values of p, but for $\Delta t_{\mathrm{com}}=0$ μs and $\varphi=0°$. Note that I_{dx} becomes zero for $M=\sqrt{2}$ and infinite for $M\approx 1.57$.

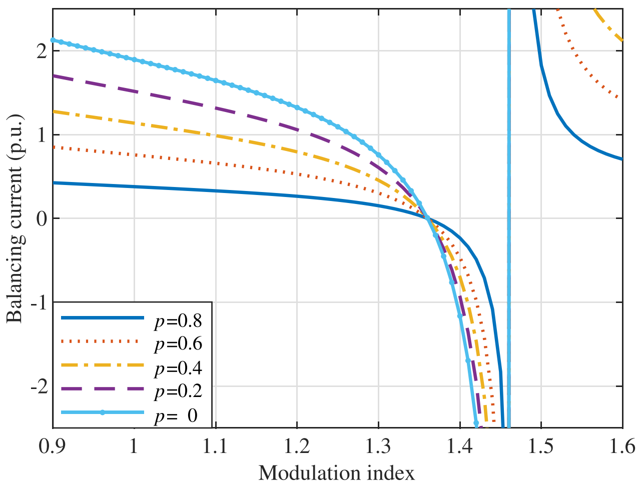


Fig. 5. Balancing current I_{dx} (normalized with respect to $I_{\mathrm{d}}/3$) versus M for different values of p, but for $\Delta t_{\mathrm{com}}=350$ μs and $\varphi=0°$. Note that I_{dx} becomes zero for $M=1.36$ and infinite for $M\approx 1.45$.

where v_{um} and i_{um} are given by (6) and (8), respectively. By solving (11) for I_{dx}, the balancing current is derived as

$$I_{\mathrm{dx}}=\frac{1-p}{4}C_{\mathrm{dx}}\hat{I}_{\mathrm{o}}. \tag{12}$$

The coefficient C_{dx} is given by

$$C_{\mathrm{dx}}=\frac{2(2-M^2)\cos\Delta\theta_{\mathrm{com}}-M\sin(2\Delta\theta_{\mathrm{com}})}{\pi-2\Delta\theta_{\mathrm{com}}-2M\cos\Delta\theta_{\mathrm{com}}}\cos\varphi \tag{13}$$

where $\Delta\theta_{\mathrm{com}}=\omega_1\Delta t_{\mathrm{com}}$ is the angle that corresponds to the commutation time. It is possible to prove that the balancing current given by (12) ensures that the net energy is zero through the lower and common arms during one fundamental cycle. This can be done by substituting (12) in (9) and (10) and calculating the integral of the products $v_{\mathrm{lm}}(t)i_{\mathrm{lm}}(t)$ and $v_{\mathrm{mo}}(t)i_{\mathrm{mo}}(t)$ over one fundamental period. By straightforward algebraic manipulations it can be shown that these definite integrals, which represent the energy of the lower and common arms, are equal to zero.

B. Balancing Current With Zero Commutation Time

For the special case of zero commutation time $\Delta\theta_{\mathrm{com}}=0$, (12) becomes equal to the expression presented in [27] and repeated as follows:

$$I_{\mathrm{dx}}=\frac{(1-p)}{2}\frac{2-M^2}{\pi-2M}\hat{I}_{\mathrm{o}}\cos\varphi. \tag{14}$$

Equation (14) is rewritten in this article because it is less complex than (12) and reveals the following important points:

1) I_{dx} is directly dependent on the current-sharing factor;
2) I_{dx} becomes zero for $M=\sqrt{2}$;
3) I_{dx} becomes infinite for $M=\pi/2$.

These observations are illustrated in Fig. 4, where I_{dx} is plotted versus the modulation index for various current-sharing factors. In Fig. 4, I_{dx} is normalized with respect to the per-phase dc-link current, i.e., 1/3rd of I_{d} given by (5). Fig. 4 shows that I_{dx} increases with decreasing current-sharing factor, which is expected from the definition of the latter. That is, for $p=1$, the terminal currents flow exclusively through the main arms. Hence, the common arm current is zero, which means that the balancing current I_{dx} is also zero. In other words, $p=1$ represents the case where only the MMC part of the HACC conducts current, i.e., the currents of the upper and lower arms are equal to (3) and (4), respectively. However, as the current-sharing factor is reduced, the portion of the terminal current that flows through the main arms is reduced accordingly, which disturbs the inherent energy balancing for $p=1$. Thus, it is expected that the more p moves away from the value 1, the higher balancing current is required for restoring the energy balancing of the main arms.

Moreover, Fig. 4 shows that for $M=\sqrt{2}$ the balancing current becomes zero, because for this modulation index the energy balancing of all arms occurs within a half-cycle. Finally, I_{dx} becomes infinite for $M=\pi/2$, because at this modulation index the integral of the main-arm voltages within half a cycle become zero. Hence, multiplying I_{dx} with the zero integrals of the main-arm voltages does not produce any net energy transfer, which means that energy balancing for $M=\pi/2$ is not possible with a direct current.

C. Balancing Current With Nonzero Commutation Time

If $\Delta\theta_{\mathrm{com}}\neq 0$ similar observations as for $\Delta\theta_{\mathrm{com}}=0$ apply, but the modulation indices for which the balancing current becomes zero and infinite are different. This is illustrated by calculating I_{dx} from (12) with $\Delta t_{\mathrm{com}}=350$ μs for the same modulation indices and current-sharing factors as for Fig. 4. The results of this calculation are plotted in Fig. 5, which is similar to Fig. 4 but the modulation indices for which I_{dx} becomes zero and infinite are shifted to lower values. The most important conclusion from Figs. 4 and 5 is that the maximum modulation index of the HACC should be lower than the value for which I_{dx} becomes infinite.

D. Impact of Current Sharing on Peak Arm Currents

In Section III-A, it was shown that the current-sharing factor p impacts the balancing current, which in turn impacts the peak arm currents. In order to evaluate the impact of p on the peak arm currents, the case of $p=1$ is considered as the reference case. This is because $p=1$ corresponds to the worst case for the peak currents of the main arms, which are equal to the peak terminal currents, i.e., $I_{\mathrm{um}}^{\mathrm{pk}}=I_{\mathrm{u}}^{\mathrm{pk}}$, $I_{\mathrm{lm}}^{\mathrm{pk}}=I_{\mathrm{l}}^{\mathrm{pk}}$. Hence, for the reference case the following holds:

$$I_{\mathrm{um}}^{\mathrm{pk,ref}}=I_{\mathrm{u}}^{\mathrm{pk,ref}}=\left(\frac{1}{4}M\cos\varphi+\frac{1}{2}\right)\hat{I}_{\mathrm{o}}^{\mathrm{ref}}=A_{\mathrm{pk}}\hat{I}_{\mathrm{o}}^{\mathrm{ref}} \quad (15)$$

$$I_{\mathrm{mo}}^{\mathrm{pk,ref}}=0 \quad (16)$$

where $\hat{I}_{\mathrm{u}}^{\mathrm{pk,ref}}$ is the peak terminal current (i_{u}), $\hat{I}_{\mathrm{o}}^{\mathrm{ref}}$ is the amplitude of the output current for the reference case, while A_{pk} is the coefficient that relates the peak arm current with the output current in (15) and is given by

$$A_{\mathrm{pk}}=\frac{1}{4}M\cos\varphi+\frac{1}{2}. \quad (17)$$

Note that only the current of the upper arm is considered from now on, as that of the lower arm differs only in phase; hence, the peak currents are equal for both arms. The peak currents of the upper and the common arms for $p=[0,1)$ are derived, respectively, by (8) and (10) and are given by

$$\begin{aligned}I_{\mathrm{um}}^{\mathrm{pk}}&=pI_{\mathrm{u}}^{\mathrm{pk}}+I_{\mathrm{dx}}\Rightarrow\\ I_{\mathrm{um}}^{\mathrm{pk}}&=\left(pA_{\mathrm{pk}}+\frac{1-p}{4}C_{\mathrm{dx}}\right)\hat{I}_{\mathrm{o}}=K_{\mathrm{um}}\hat{I}_{\mathrm{o}}\end{aligned} \quad (18)$$

$$\begin{aligned}I_{\mathrm{mo}}^{\mathrm{pk}}&=(1-p)I_{\mathrm{u}}^{\mathrm{pk}}-I_{\mathrm{dx}}\Rightarrow\\ I_{\mathrm{mo}}^{\mathrm{pk}}&=\left[(1-p)A_{\mathrm{pk}}-\frac{1-p}{4}C_{\mathrm{dx}}\right]\hat{I}_{\mathrm{o}}=K_{\mathrm{mo}}\hat{I}_{\mathrm{o}}\end{aligned} \quad (19)$$

where $\hat{I}_{\mathrm{o}}$ is the amplitude of the output current when $p=[0,1)$, while K_{um} and K_{mo} represent the coefficients that are multiplied with $\hat{I}_{\mathrm{o}}$. These coefficients are a combination of the coefficients C_{dx} and A_{pk}, which are given by (13) and (17), respectively. Note that (18) indicates that the peak current of the upper arm is not equal to the peak terminal current ($I_{\mathrm{um}}^{\mathrm{pk}}\neq I_{\mathrm{u}}^{\mathrm{pk}}$), as for the reference case (15). Moreover, for a certain modulation index and commutation time, the peak currents of the upper and common arms can be varied, compared to the reference case, by changing the current-sharing factor. This is illustrated in Fig. 6 for commutation time $\Delta t_{\mathrm{com}}=350\ \mu$s and for modulation indices $M=1.25$, $M=1.35$. Fig. 6 shows the peak currents of the upper and common arms normalized with respect to the reference peak current ($I_{\mathrm{um}}^{\mathrm{pk,ref}}=I_{\mathrm{u}}^{\mathrm{pk,ref}}$) versus the current-sharing factor.

Fig. 6 shows that by decreasing the current-sharing factor, the peak current of the upper arm is decreased while the peak current of the common arm is increased compared to the reference case. Thus, the current-sharing factor impacts oppositely the peak currents through the upper and common arms, which is because the balancing current I_{dx} appears with opposite signs in (18) and (19). Most importantly, for a certain current-sharing factor (i.e., $p=0.14$ for $M=1.25$ and $p=0.46$ for $M=1.35$ in Fig. 6), the peak currents of the upper and common arms become equal to half of the reference peak current $I_{\mathrm{um}}^{\mathrm{pk,ref}}$, as also shown in [28].

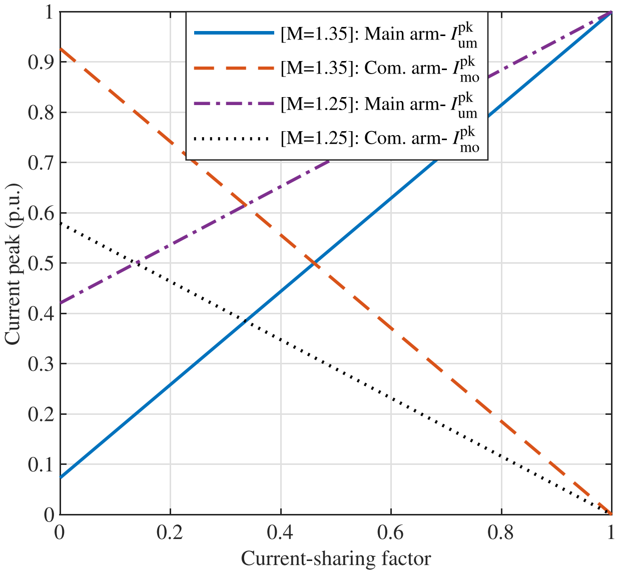


Fig. 6. Impact of the current-sharing factor on the peak arm currents for $\Delta t_{\mathrm{com}}=350\ \mu$s, $\varphi=0°$, and modulation indices $M=1.25$, $M=1.35$. Currents are normalized to the peak current of the reference case $I_{\mathrm{um}}^{\mathrm{pk,ref}}$ for the corresponding modulation index. Peak arm currents of both the main and common arms are equal to half the reference peak current $I_{\mathrm{um}}^{\mathrm{pk,ref}}$ for [$p=0.14$, $M=1.25$] and for [$p=0.46$, $M=1.35$] [28].

IV. POWER CAPABILITY AND SELECTION OF CURRENT-SHARING FACTOR

A. Maximum Power Capability

The analysis of Section III-D reveals that by sharing the terminal current between the main and common arms, the peak current of the main arms can be reduced compared to the reference case. This means that the converter transfers the same output current as the reference case but with reduced peak current through the main/common arms (i.e., $\hat{I}_{\mathrm{o}}=\hat{I}_{\mathrm{o}}^{\mathrm{ref}}$ while $I_{\mathrm{um}}^{\mathrm{pk}}<I_{\mathrm{um}}^{\mathrm{pk,ref}}$). However, the feature of current sharing can be utilized to enable the converter to transfer higher output current than the reference case but with peak-arm currents equal to the reference case (i.e., $\hat{I}_{\mathrm{o}}>\hat{I}_{\mathrm{o}}^{\mathrm{ref}}$ while $I_{\mathrm{um}}^{\mathrm{pk}}=I_{\mathrm{um}}^{\mathrm{pk,ref}}$). This increase of the output current implies a proportional increase of the output power (both apparent S and active P power) of the converter at the same output voltage (modulation index) and the same power angle (φ) as the reference case.

This section examines the extent to which the power-transfer capability of the converter can be increased compared to the reference case, under the condition that the rated current of the converter for $p=[0,1)$ is equal to the reference case. This increase of the power-transfer capability is quantified by the parameter *power ratio*, which is defined as the ratio

$$R_{\mathrm{h}}:=\frac{\hat{I}_{\mathrm{o}}}{\hat{I}_{\mathrm{o}}^{\mathrm{ref}}} \quad (20)$$

where $\hat{I}_\text{o}^\text{ref}$ is the output current at the reference case (i.e., for $p = 1$), while $\hat{I}_\text{o}$ is the output current when the converter is operated at current-sharing factors in the interval $p = [0, 1)$.

The power ratio can be derived by equating the rated current of the converter for $p = [0, 1)$ with the peak terminal current of the reference case for $p = 1$, and then solving for the ratio of output currents as defined by (20). However, since the peak current of the main and common arms differ depending on the value of the current-sharing factor, as shown in Fig. 6, the rated current of the converter I_rated is defined as

$$I_\text{rated} = \max(I_\text{um}^\text{pk}, I_\text{mo}^\text{pk}). \tag{21}$$

Based on this, the power ratio is derived by

$$\begin{aligned}&\frac{I_\text{rated}}{\hat{I}_\text{u}^\text{pk,ref}} = 1 \Rightarrow \frac{\max(I_\text{um}^\text{pk}, I_\text{mo}^\text{pk})}{\hat{I}_\text{u}^\text{pk,ref}} = 1 \Rightarrow\\ &\frac{\max(K_\text{um}, K_\text{mo})\hat{I}_\text{o}}{A_\text{pk}\hat{I}_\text{o}^\text{ref}} = 1 \Rightarrow \frac{\hat{I}_\text{o}}{\hat{I}_\text{o}^\text{ref}} = \frac{A_\text{pk}}{\max(K_\text{um}, K_\text{mo})},\end{aligned} \tag{22}$$

where A_pk is given by (17), while K_um and K_mo are the coefficients shown in (18) and (19), respectively. Finally, by combining the definition (20) with (22), the power ratio of the converter can be expressed as

$$\begin{aligned}&R_\text{h} = \frac{A_\text{pk}}{\max(K_\text{um}, K_\text{mo})} = \min\left(\frac{A_\text{pk}}{K_\text{um}}, \frac{A_\text{pk}}{K_\text{mo}}\right) \Rightarrow\\ &R_\text{h} = \min(R_\text{ulm}, R_\text{mo})\end{aligned} \tag{23}$$

where R_ulm and R_mo are, respectively, defined as follows:

1) *main-arm power ratio* (R_ulm) that represents the power ratio calculated by considering only the peak current of the main arms, i.e., if $I_\text{rated} = I_\text{um}^\text{pk}$;
2) *common-arm power ratio* (R_mo) that represents the power ratio calculated by considering only the peak current of the common arm, i.e., if $I_\text{rated} = I_\text{mo}^\text{pk}$.

The main-arm power ratio (R_ulm) is derived by substituting A_pk from (17) and K_um from (18) and is given by

$$R_\text{ulm} = \frac{A_\text{pk}}{K_\text{um}} \Rightarrow R_\text{ulm} = \frac{1}{p + \dfrac{1-p}{4}\dfrac{C_\text{dx}}{A_\text{pk}}}. \tag{24}$$

Similarly, the common-arm power ratio (R_mo) is derived by substituting A_pk from (17) and K_mo from (19), which yields

$$R_\text{mo} = \frac{A_\text{pk}}{K_\text{mo}} \Rightarrow R_\text{mo} = \frac{1}{(1-p)\left(1 + \dfrac{1}{4}\dfrac{C_\text{dx}}{A_\text{pk}}\right)}. \tag{25}$$

In order to clarify the meaning of the various power ratios, the latter have been calculated for the example of Fig. 6 for $M = 1.35$ and are plotted versus the current-sharing factor in Fig. 7. By comparing Figs. 6 and 7, it can be observed that the main-arm power ratio (R_ulm) is lower than the common-arm power ratio (R_mo) when the peak current of the main arms is higher than the peak current of the common arm, and vice versa. Eventually, the converter power ratio (R_h), which takes into account the peak current of both the main and common arms, is decided based on the minimum of the main- and common-arm power ratios, as expressed by (23). Thus, the usefulness of the main- and common-arm power ratios is that they indicate, whereas the final power ratio (R_h) is limited by the peak current of the main or common arms. That is, for the lower range of current-sharing factors the final power ratio (R_h) is equal to the common-arm power ratio (R_mo); hence, it is limited by the peak common-arm current (I_mo^pk). Conversely, for the higher range of current-sharing factors the final power ratio (R_h) is equal to the main-arm power ratio (R_ulm); hence, it is limited by the peak main-arm current (I_um^pk).

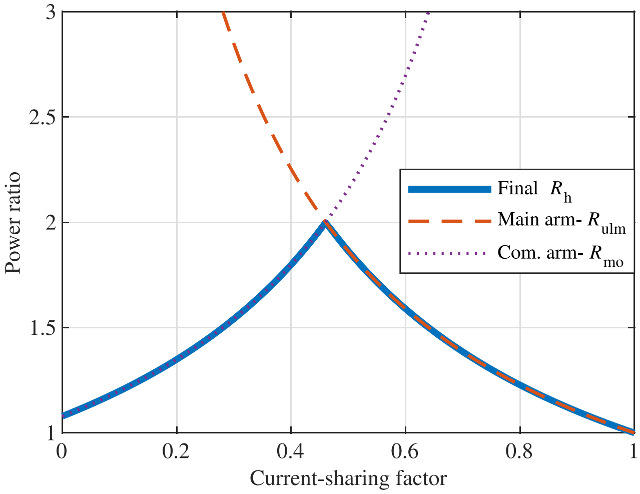


Fig. 7. Final power ratio R_h (solid line) versus p for $M = 1.35$, $\Delta t_\text{com} = 350$ μs, and $\varphi = 0°$. For $p = 0.46$ the power ratio is maximized and is equal to the main-arm (dashed red) and common-arm (dotted purple) power ratios. For $p < 0.46$ and $p > 0.46$ the power ratio is limited by the peak current of the common and upper arm, respectively.

The most interesting point of Fig. 7 is the intersection of the main- and common-arm power ratios, where the final power ratio is maximized to $R_\text{h} = 2$; thus, the following holds:

$$\begin{aligned}&R_\text{um} = R_\text{mo} \Rightarrow \frac{A_\text{pk}}{K_\text{um}} = \frac{A_\text{pk}}{K_\text{mo}} \Rightarrow K_\text{um} = K_\text{mo} \Rightarrow\\ &K_\text{um}\hat{I}_\text{o} = K_\text{mo}\hat{I}_\text{o} \Rightarrow I_\text{um}^\text{pk} = I_\text{mo}^\text{pk}.\end{aligned} \tag{26}$$

Notably, the maximum power ratio $R_\text{h} = 2$ occurs when the peak currents of the main and common arms are equal. Thus, the intersection point of the main-arm and common arm power ratios in Fig. 7 coincides with the intersection point of the peak currents of the main and common arms in Fig. 6. In other words, the maximum power ratio is achieved at the point where the rated current of the converter, as given by (21), is minimized.

To illustrate the impact of both the current-sharing factor and the modulation index, the power ratio was calculated for two current-sharing factors and for a range of modulation indices. The results are plotted in Fig. 8, which shows that the power ratio is maximized for a specific pair of modulation index and current-sharing factor. Therefore, a method is needed for estimating the optimal current-sharing factor that maximizes the power ratio for a given modulation index.

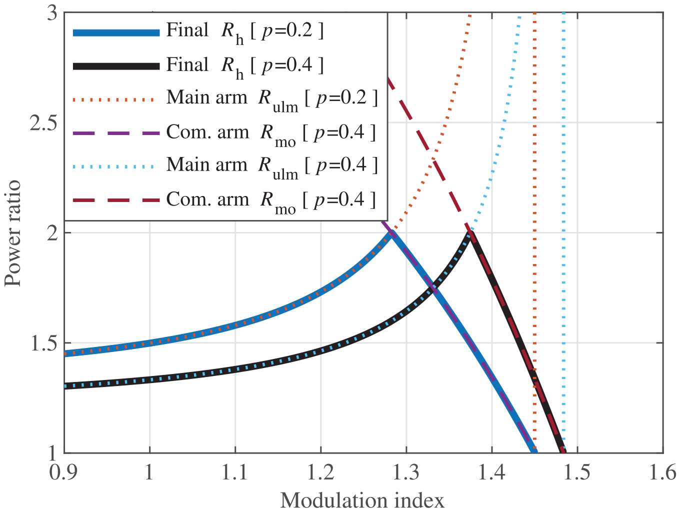


Fig. 8. Final power ratio R_h versus M for $p = 0.2$ (solid blue) and $p = 0.4$ (solid black). R_h is maximized for a specific pair of M and p, for which the main-arm (dashed) and common-arm (dotted) power ratios are equal. Alternatively, M changes the value of p for which R_h is maximized.

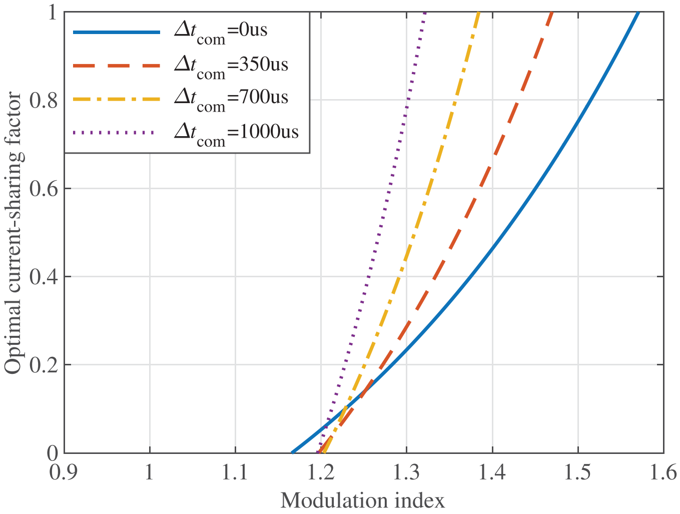


Fig. 9. Optimal current-sharing factor p_opt at which the power ratio is maximized, versus M for different values of Δt_com. Increasing Δt_com limits the range of modulation indices for which the power ratio can be maximized.

B. Selection of Optimal Current-Sharing Factor

In Section IV-A, it was shown that the power capability (power ratio) of the converter is maximized for a very specific value of the current-sharing factor p that changes for different modulation index M and commutation time Δt_com. This value of p at which the power ratio is maximized is termed *optimal current-sharing factor* and represented by the symbol p_opt. This section presents a method for estimating the optimal current-sharing factor for a given modulation index and commutation time. This method reveals that the maximum power ratio can be achieved in a limited range of modulation indices, which differs depending on the commutation time.

In Section IV-A, it was shown that the maximum power ratio $R_\mathrm{h} = 2$ achieved when the peak currents through all arms is equal, or equivalently when $R_\mathrm{ulm} = R_\mathrm{mo} = R_\mathrm{h} = 2$. Therefore, for given values of M and Δt_com, the optimal current-sharing factor p_opt can be derived by setting either (24) or (25) equal to $R_\mathrm{h} = 2$ and solving for p. For simplifying the solution process, p_opt is derived by equating (24) with $R_\mathrm{h} = 2$ and solving for p_opt, which yields

$$p_\mathrm{opt} + \frac{1 - p_\mathrm{opt}}{4}\frac{C_\mathrm{dx}}{A_\mathrm{pk}} = \frac{1}{2} \Rightarrow p_\mathrm{opt} = \frac{2 - C_\mathrm{dx}/A_\mathrm{pk}}{4 - C_\mathrm{dx}/A_\mathrm{pk}}. \quad (27)$$

Note that for some modulation indices, (27) might yield solutions outside the interval [0,1). Such solutions should be rejected, as they mean that for the specific modulation indices, there is no value of the current-sharing factor for which the power ratio R_h can be equal to 2.

Equation (27) is used to calculate the optimal current-sharing factor for various modulation indices and commutation times, while the power angle is set to $\varphi = 0^\circ$; the results are illustrated in Fig. 9. Given that only the current-sharing factors within the interval $p_\mathrm{opt} = [0, 1)$ are shown in Fig. 9, three important observations can be made and are listed as follows.

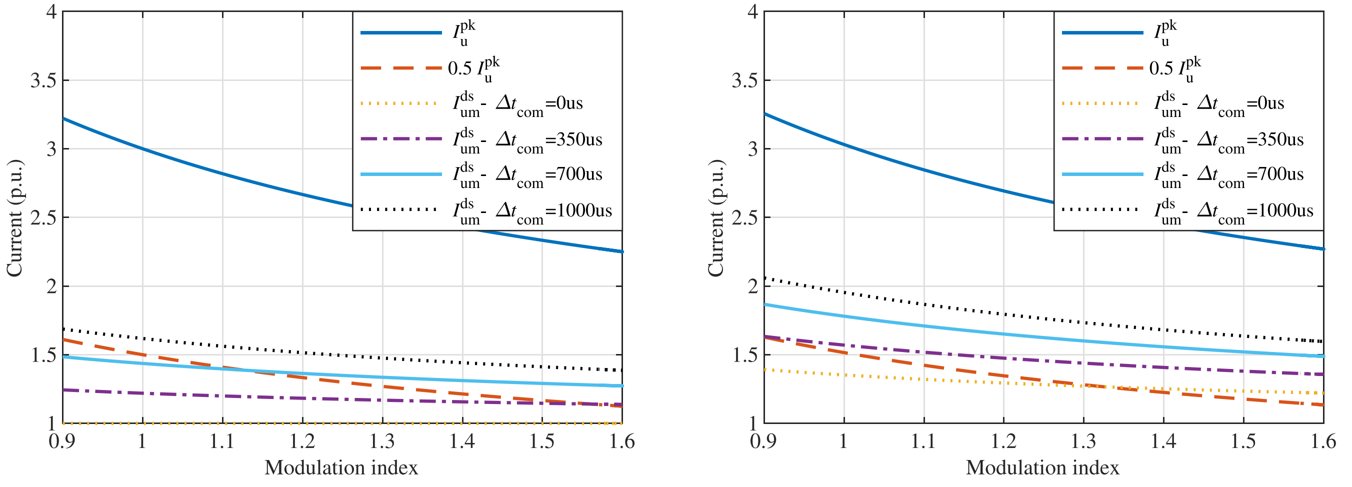
1) For a certain commutation time, there is a limited range of modulation indices for which the power ratio can be maximized.
2) If the commutation time is increased, the range of modulation indices for which the power ratio can be maximized becomes narrower.
3) The power ratio is maximized for modulation indices higher than 1.1, regardless of the commutation time.

These observations reveal that the maximum power ratio cannot be achieved for any modulation index. The third observation is important because it reveals that the ac-side voltage of the converter must be higher than the dc-link voltage in order to achieve the maximum power ratio.

At this point, it should be mentioned that the impact of the power angle on the optimal current-sharing factor is not significant as long as $\varphi \leq 10^\circ$. Moreover, in the next sections, it is shown that for higher power angles the power ratio is not limited by the peak currents of the main and common arms, which are dependent on the optimal current-sharing factor. Hence, the impact of the power angle on the optimal current-sharing factor is not studied further. Finally, for current-sharing factors higher than 0.8 the common arm is mainly employed for balancing the energy of the main arms and transfers very low active power. Thus, 0.8 is considered as the maximum value of the current-sharing factor from now on.

C. Power Capability Limitation Due to Discontinuity Currents

Thus far, it has been shown that a proper selection of the current-sharing factor leads to the reduction of the peak arm currents to half of the peak terminal currents. Hence,the converter arms can be designed for half of the peak terminal currents. Yet, the discontinuity current (I_ds in Fig. 3) might become higher than half of the peak terminal current under the conditions of high commutation time, high power angle, or both. Depending on the power angle, the peak discontinuity current occurs at



(a) (b)

Fig. 10. Discontinuity current I^{ds} (normalized to $I_\text{d}/3$) versus M for different values of Δt_com and φ. I^{ds} limits the power capability of the converter if it exceeds the peak arm currents achieved for p_opt (dashed red), for which the power ratio is maximized. (a) $\varphi = 0°$. (b) $\varphi = 10°$ capacitive.

either of two instants: 1) $\omega t = \Delta\theta_\text{com}$; and 2) $\omega t = \pi - \Delta\theta_\text{com}$; thus, it can be calculated by substituting these instants in (3) [after substituting I_d with (5)], which yields

$$I_\text{um}^\text{ds,1} = \left[\frac{M}{4}\cos\varphi + \frac{1}{2}\sin(\Delta\theta_\text{com} - \varphi)\right]\hat{I}_\text{o} = K_\text{ds,1}\hat{I}_\text{o}, \tag{28}$$

$$\begin{aligned} I_\text{um}^\text{ds,2} &= \left[\frac{M}{4}\cos\varphi + \frac{1}{2}\sin(\pi - \Delta\theta_\text{com} - \varphi)\right]\hat{I}_\text{o} \\ &= K_\text{ds,2}\hat{I}_\text{o} \end{aligned} \tag{29}$$

where $K_\text{ds,1}$ and $K_\text{ds,2}$ represent the coefficients that are multiplied with $\hat{I}_\text{o}$. Equations (28) and (29) clearly show that the discontinuity current is independent of the current-sharing factor and thus cannot be controlled in the same manner as the peak arm currents. Hence, (21) should be revised as follows:

$$I_\text{rated}^\text{ds} = \max(I_\text{um}^\text{pk}, I_\text{mo}^\text{pk}, I_\text{um}^\text{ds,1}, I_\text{um}^\text{ds,2}) \tag{30}$$

where I_rated^ds is the rated converter current with consideration of the discontinuity currents. Similarly as the derivation of (22), the power ratio with consideration of the discontinuity currents R_h^ds is derived as follows:

$$\frac{I_\text{rated}^\text{ds}}{\hat{I}_\text{u}^\text{pk,ref}} = 1 \Rightarrow R_\text{h}^\text{ds} = \frac{A_\text{pk}}{\max(K_\text{um}, K_\text{mo}, K_\text{ds,1}, K_\text{ds,2})}. \tag{31}$$

In order to illustrate the impact of the discontinuity current on the design of the converter, (29) was utilized to calculate the discontinuity current $I_\text{um}^\text{ds,2}$ for different modulation indices, commutation times, and power angles. The results are plotted in Fig. 10(a) and (b) for $\varphi = 0°$ and $\varphi = 10°$, respectively, along with the peak terminal current (I_u^pk) and the peak upper-arm current (0.5 I_u^pk) for the optimal current-sharing factor given by (27). Fig. 10(a) clearly shows that as the commutation time increases the discontinuity current becomes higher than the peak upper-arm current beyond certain modulation indices. This means that the converter should be dimensioned for the discontinuity current instead of the peak arm currents; thus, the power capability of the converter is reduced and given by (31). For example, for $\Delta t_\text{com} = 700\ \mu$s, the discontinuity current $I_\text{um}^\text{ds,2}$ becomes higher than the peak upper-arm current for modulation indices higher than 1.12 and thus the converter arms should be dimensioned for $I_\text{um}^\text{ds,2}$. Therefore, the power capability is defined by the discontinuity current $I_\text{um}^\text{ds,2}$ and cannot be maximized, i.e., $R_\text{h}^\text{ds} < 2$.

Moreover, Fig. 10(b) shows that the impact of the discontinuity current is more significant when the power angle is non zero. For example, for $\Delta t_\text{com} = 700\ \mu$s the discontinuity current becomes the dimensioning factor of the arms for the whole range of modulation indices. Therefore, it can be concluded that the discontinuity current limits the power capability of the converter when it becomes higher than the optimal peak arm current (0.5 I_u^pk). More specifically, the discontinuity current defines a maximum modulation index for which power capability is maximum, i.e., $R_\text{h}^\text{ds} = 2$.

V. MODULATION INDEX RANGE FOR MAXIMUM POWER

From the theoretical analysis so far and from thyristor turn-OFF considerations, it was found that the modulation index should not exceed certain limits, which are listed as follows.

1) The modulation index should be lower than the one for which the balancing current I_dx becomes infinite, which is represented by the symbol M_max^dx.
2) The modulation index should be lower than the one for which the discontinuity current I_ds becomes higher than the peak arm current given by (21), which is represented by the symbol M_max^ds.
3) The modulation index should be lower than the one for which the optimal current-sharing factor is equal to 0.8, which is represented by the symbol M_max^p.

4) The modulation index should be higher than the one for which the optimal current-sharing factor approximates 0, which is represented by the symbol $M^{\mathrm{p}}_{\min}$.
5) The modulation index should be higher than that for which the common-arm current becomes bidirectional within one half-cycle (the reason is for avoiding triggering antiparallel thyristors and thus two turn-OFF processes within a half-cycle), which is represented by the symbol $M^{\mathrm{zc}}_{\min}$.

Since all the mentioned limits define the range of modulation indices for which the power ratio is maximized (i.e., $R^{\mathrm{ds}}_{\mathrm{h}} = 2$), they have to be estimated and considered during the design process of the HACC. Moreover, since all these limits are impacted by the commutation time Δt_{com}, it is useful to derive a method that yields the range of modulation indices that maximizes the power ratio for a given Δt_{com} and power angle φ. The first step of this method is to derive each of the modulation index limits as follows.

1) $M^{\mathrm{dx}}_{\max}$ can be derived by setting the denominator of C_{dx} from (13) equal to zero (i.e., equivalent to $I_{\mathrm{dx}} = \infty$) and solving for M.
2) $M^{\mathrm{ds}}_{\max}$ can be derived by setting the discontinuity current I_{ds} equal to half of the peak terminal current $I^{\mathrm{pk}}_{\mathrm{u}}$ and solving for M.
3) $M^{\mathrm{p}}_{\max}$ can be derived by setting the optimal current-sharing factor in (27) equal to 0.8 (for the reason mentioned previously and for having a margin from the modulation index for which the balancing current I_{dx} becomes infinite), and solving for M.
4) $M^{\mathrm{p}}_{\min}$ can be derived by setting the optimal current-sharing factor in (27) equal to 0 and solving for M.
5) $M^{\mathrm{zc}}_{\min}$ can be derived graphically by iteratively plotting the current of the common arm and is not discussed further.

After calculating all these limits, it is clear that the minimum modulation index for which the power ratio is maximized is defined by $M^{\mathrm{p}}_{\min}$, while the maximum modulation index is defined by the minimum value of the other three limits, i.e.,

$$M_{\min} = M^{\mathrm{p0}}_{\min} \tag{32}$$

$$M_{\max} = \min(M^{\mathrm{dx}}_{\max}, M^{\mathrm{ds}}_{\max}, M^{\mathrm{p1}}_{\max}). \tag{33}$$

Finally, $M_{\min}$ and $M_{\max}$ define the range of modulation indices for which the power ratio of the converter is maximized, which is termed *optimal range of modulation indices*. By iterating this method for different commutation times, an optimal region of modulation indices can be derived as a function of the commutation time. This optimal region of modulation indices can be employed for easily evaluating the design limitations that are imposed by the commutation time.

In order to demonstrate the usefulness of the described method, the optimal region of modulation indices was derived for commutation times ranging from 0 up to 800 μs and for power angles $\varphi = 0°, 3°, 10°$. The resulting optimal region of modulation indices is plotted versus the commutation time in Fig. 11 and it is bounded by the calculated $M_{\min}$, $M_{\max}$, and $M^{\mathrm{ds}}_{\max}$. The former two, which are represented by the dashed red and dashed blue curves, respectively, do not change significantly for the specified power angles. The latter limit $M^{\mathrm{ds}}_{\max}$ is represented by the dotted black, dashed-dotted black, and solid black lines for power angles $\varphi = 0°$, $3°$, and $10°$, respectively. Thus, it becomes evident that the limit $M^{\mathrm{ds}}_{\max}$ due to the discontinuity current is the one that impacts most significantly the optimal region of modulation indices.

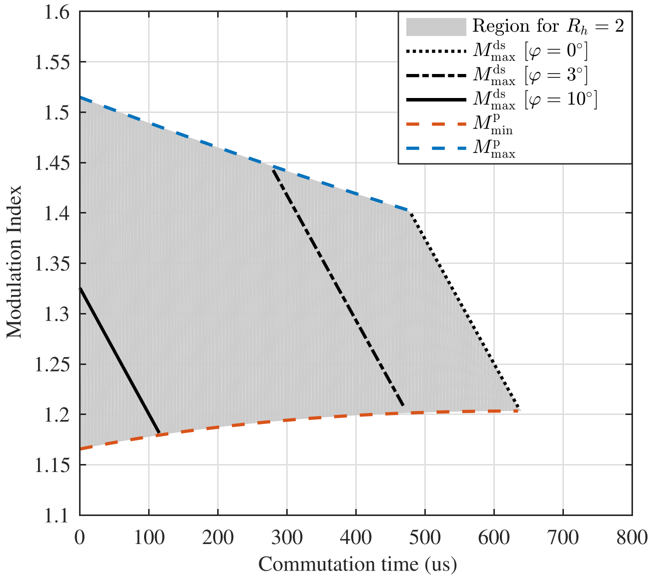


Fig. 11. Optimal regions of modulation indices at which maximum power ratio can be achieved versus the commutation time Δt_{com}, for different values of the power angle: (grey area bounded by black dotted line) $\varphi = 0°$; (grey area bounded by black dashed-dotted line) $\varphi = 3°$ capacitive; (grey area bounded by black solid line) $\varphi = 10°$ capacitive. The region bounds defined by dotted, dashed-dotted, solid black lines are defined by the respective I^{ds}.

Fig. 11 reveals that for power angle $\varphi = 0°$ the maximum power ratio $R^{\mathrm{ds}}_{\mathrm{h}} = 2$ cannot be achieved if the commutation time is $\Delta t_{\mathrm{com}} \geq 620$ μs. Yet, for $\Delta t_{\mathrm{com}} = 500$ μs a reasonable optimal range of modulation indices [1.2,1.4] can be obtained. Moreover, for higher power angles the commutation time needs to be even lower for achieving the maximum power ratio in a reasonable range of modulation indices. For example, if the converter is designed for a power angle of $\varphi = 10°$, the commutation time should be close to zero. Remember that the commutation time Δt_{com} is not the same as the thyristor extinction time t_{q}. For example, if $\Delta t_{\mathrm{di}} = 100$ μs and $\Delta t_{\mathrm{com}} = 500$ μs, the reverse-biasing interval is $\Delta t_{\mathrm{rev}} = \Delta t_{\mathrm{com}} - \Delta t_{\mathrm{di}} = 400$ μs; hence, the thyristor extinction time should be in the range of $t_{\mathrm{q}} \leq 0.5\Delta t_{\mathrm{rev}} = 200$ μs. This is much lower than the extinction time of the thyristors that are typically used in HVdc applications, which is in the range of 500–800 μs. In summary, Fig. 11 reveals that it is necessary to utilize thyristors with low t_{q} times and operate at low power angles, in order to exploit the maximum power capability of the HACC; otherwise, the converter's power has to be derated.

VI. CURRENT-SHARING CONTROL AND THYRISTOR COMMUTATION

This section briefly describes the control of the HACC by focusing particularly on the control scheme of phase a, which is depicted in Fig. 12. First, the main arms are controlled by the output-current controller (OCC), which is a proportional-resonant controller with the resonant term tuned at the

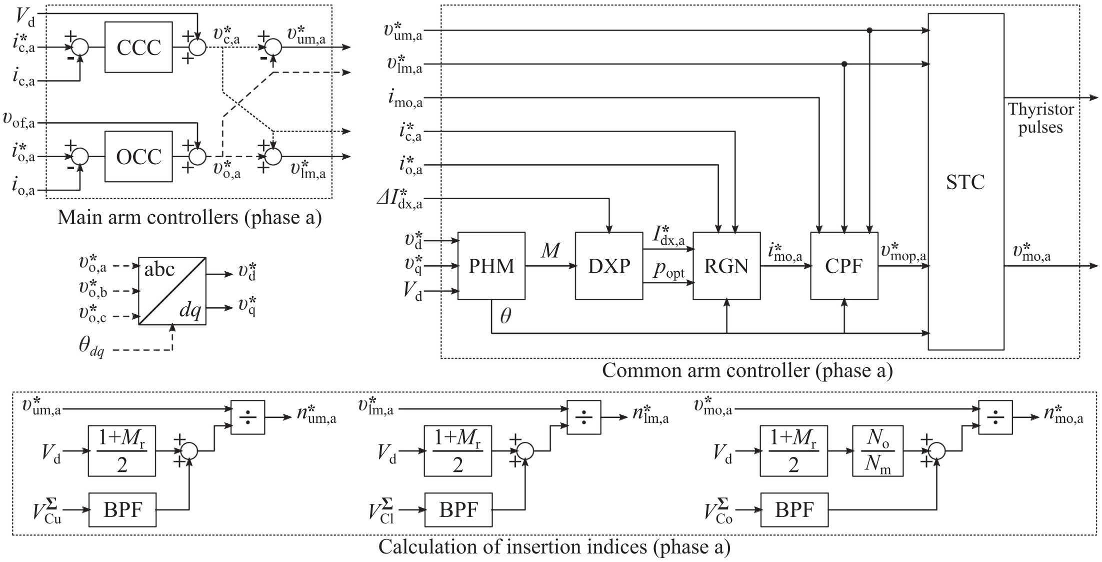


Fig. 12. Control diagram of main and common arms for phase a of the HACC. The control of the main arms consists of the blocks: circulating current controller (CCC); output current controller (OCC). The control of the common arm consists of the blocks: phase and modulation index calculation block (PHM); balancing current and optimal current-sharing factor calculation block (DXP); reference generation block (RGN); common-arm current controller (CPF); and converter-state control block (STC). The calculation of insertion indices employs the band-pass filter blocks (BPF), while $M_r = 1.5$, $N_m = 25$ is the number of SMs of each main arm, and $N_o = 15$ is the number of SMs of each common arm.

fundamental frequency (ω_1), and the circulating-current controller (CCC), which is a proportional-resonant controller with the resonant term tuned at the 2nd harmonic ($2\omega_1$) to suppress circulating currents at this frequency. Note that the OCC and the CCC are supplemented by the feed-forward terms $v^*_{of,a}$ and V_d, respectively, and were implemented as described in [11, Ch. 3]. Moreover, the circulating-current reference $i^*_{c,a}$ is the direct component of the terminal currents of phase a, represented by $I_d/3$ in (3) and (4). The outputs of the CCC and the OCC are used to generate the voltage reference $v^*_{um,a}$ and $v^*_{lm,a}$ for the upper and lower arm, respectively.

The output-voltage references ($v^*_{o,a}$, $v^*_{o,b}$, $v^*_{o,c}$), generated by the OCCs of the three phases, are transformed from the abc to the dq frame based on the dq-reference angle θ_{dq}. The resulting dq components (v^*_d, v^*_q) and the dc-link voltage V_d are utilized by the phase and modulation index calculation block (PHM) that calculates the phase θ of the output-voltage reference $v^*_{o,a}$ and the modulation index M. The modulation index is required by the balancing current and optimal current-sharing factor calculation block (DXP) for the estimation of the balancing current according to (12) and the optimal current-sharing factor according to (27). Note that the DXP block gets as input a small adjustment for the balancing current ($\Delta I^*_{dx,a}$), which comes from the energy controller of the common arm (not shown in Fig. 12). This is a simple proportional controller that acts on the difference between the reference energy and the available energy of the common arm and yields $\Delta I^*_{dx,a}$. The reference balancing current $I^*_{dx,a}$ is then calculated by summing the result of (12) with the adjustment $\Delta I^*_{dx,a}$.

The reference generation block (RGN) is generating the reference current $i^*_{o,a}$ for the common-arm current controller (CPF). Notably, the RGN block generates $i^*_{mo,a}$ by substituting the values of the output-current $i^*_{o,a}$, the circulating-current $i^*_{c,a}$, and the balancing-current $I^*_{dx,a}$ references, as well as the optimal current-sharing factor p_{opt}, and the phase of the output-voltage reference θ in (10). The generated current reference $i^*_{mo,a}$ is compared with the measured common-arm current $i_{mo,a}$ by the CPF block, which comprises a proportional controller with feed-forward terms of the arm-voltage references $v^*_{um,a}$, $v^*_{lm,a}$. The CPF block decides which arm-voltage reference to use as feed-forward by checking the phase of the output-voltage reference θ and finally generates the common arm-voltage reference $v^*_{mop,a}$.

The final common-arm voltage reference $v^*_{mo,a}$ is decided by the state-control block (STC), which receives the following inputs: 1) the output of the CPF block $v^*_{mop,a}$; 2) the phase of the output-voltage references θ; and 3) the arm-voltage references $v^*_{um,a}$, $v^*_{lm,a}$. The STC block uses the phase θ to decide the state in which the HACC should be, based on the ten intervals shown in Fig. 3. If the HACC should be in the current-sharing intervals (i.e., 3, 8), the STC block sets its output $v^*_{mo,a}$ equal to that of the CPF block $v^*_{mop,a}$. For the thyristor turn-OFF intervals (i.e., 4, 5 and 9, 10), the STC block sets its output equal to the sum of the suitable arm-voltage reference and the commutation voltage, which is required for turning OFF the conducting thyristor, as described in [28]. Moreover, during the voltage-transition intervals (i.e., 1, 6) the STC block varies its output with a certain dv/dt rate [28].

Finally, the sum-capacitor voltage ripple is considered for calculating the insertion indices of the main and common arms ($n^*_{um,a}$, $n^*_{lm,a}$, $n^*_{mo,a}$), in order to minimize its impact on the tracking of the controlled currents. This is performed by employing the band-pass filters (BPF) of Fig. 12, which are different for the main and common arms. Namely, two BPFs are employed for the insertion indices of the main arms, one tuned at the fundamental and one at the second harmonic. For the insertion

TABLE I
DESIGN PARAMETERS OF THE SIMULATED CONVERTERS (PWM STANDS FOR PULSEWIDTH MODULATION)

	HACC	FB-MMC
Rated power	198 MVA	99 MVA
DC-link voltage	55 kV	55 kV
Arm voltage reference for avoiding overmodulation ($M_{\mathrm{r}} = 1.5$)	68.8 kV	68.8 kV
RMS phase voltage at $M = 1.35$	26.3 kV	26.3 kV
RMS phase current at $M = 1.35$	2.52 kA	1.26 kA
Arm inductance	3.2 mH (0.094 p.u.)	6.6 mH (0.1 p.u.)
Current-sharing inductance (per arm)	0.2 mH (0.006 p.u.)	-
Num.of SMs per main/common arm	25/15	25/-
SM nominal voltage	2.75 kV	2.75 kV
SM capacitance	10.7 mF (40 kJ/MVA)	7 mF (40 kJ/MVA)
Combined power rating of semiconductors	4450.1 MVA	2557.5 MVA
Commutation time (Δt_{com})	350 μs	-
Thyristor extinction time (t_{q})	125 μs	-
Change rate of current (di/dt) during commutation	12 A/μs	-
PWM carrier frequency of main/common arms	159 Hz/265 Hz	159 Hz/-
Sampling frequency for control loops, filters	20 kHz	20 kHz

indices of the common arms, one BPF is tuned at the second and the other at the fourth harmonic.

VII. SIMULATION RESULTS

In order to verify the theoretical analysis of the HACC, a three-phase simulation model has been implemented based on the control scheme described in Section VI. The phase-shifted carrier modulation scheme without sorting has been employed for the main arms of both converters as described in [29], but sorting at 2.5 kHz was required for the common arm of the HACC. The three-phase HACC model was connected to a stiff voltage source at the dc side, but to two different loads at the ac side for the following purposes.

1) For verifying that the power ratio of the HACC is maximized for the range of modulation indices defined in Fig. 11, the three-phase HACC was connected to a passive load at the ac side. For comparison purposes, a similar model of a three-phase FB-MMC was also constructed. The design parameters of both converter models are summarized in Table I.
2) In order to illustrate the *P–Q* capability of the HACC, the three-phase HACC model was connected to a stiff voltage source via an impedance at the ac side, which represent the grid and the transformer leakage impedance, respectively. The design parameters of the HACC model are the same as those mentioned in Table I.

A. Maximum Power Capability

The first simulation test was aimed at verifying that the HACC can achieve its maximum power at the range of modulation indices defined by Fig. 11 for a certain power angle. For this purpose, the HACC was connected to a resistive load of $R_{\mathrm{o}} = 10.3\ \Omega$, which, combined with the inductances specified in Table I, leads to a power angle $\varphi = 3^{\circ}$ capacitive for the converter arms, i.e., the arms are supplying the reactive power consumed by the converter inductances. Thus, the optimal range of modulation indices is $M = [1.25, 1.35]$, based on Fig. 11 and by deriving the modulation index ($M_{\min}^{\mathrm{zc}}$) for which the common-arm current is unidirectional per half-cycle. Moreover, the three-phase reference currents ($i_{\mathrm{o,a}}^{*}$, $i_{\mathrm{o,b}}^{*}$, $i_{\mathrm{o,c}}^{*}$) for the OCC were calculated based on the resistive load, the converter inductances, and the selected modulation index range. The three-phase feed-forward terms ($v_{\mathrm{of,a}}$, $v_{\mathrm{of,b}}$, $v_{\mathrm{of,c}}$) were calculated by multiplying the corresponding reference currents with the load resistance $R_{\mathrm{o}} = 10.3\,\Omega$, while the phase of $v_{\mathrm{of,a}}$ was used as the dq-reference angle θ_{dq}. Thus, the modulation index was varied indirectly by varying the current reference of the OCCs. The simulation test was performed by initially operating the HACC at the minimum modulation index (i.e., minimum current reference for the OCCs) and then ramping up to the maximum modulation index within four fundamental cycles. For comparison purposes, the same simulation test was performed with the model of an FB-MMC, for which the resistive load was doubled to 20.6 Ω, because the FB-MMC is rated for half the power of the HACC.

The design parameters of the two simulated converters are summarized in Table I, which shows that both converters have been designed with the same energy storage capability (i.e., 40 kJ/MVA). Moreover, the arms were designed so that they could reach a maximum average arm-voltage reference of 68.8 kV, which corresponds to a maximum modulation index of $M_{\mathrm{r}} = 1.5$. As the HACC is operated up to $M = 1.35$, dimensioning the arms for $M_{\mathrm{r}} = 1.5$ provides a margin for avoiding the situation, where the requested arm voltage is higher than the available arm voltage, in which case overmodulation would occur, as outlined in [12]. It should be noted that even if this margin might seem generous, it was applied because the aim was not to operate the converters at their limits, but rather to compare them as fairly as possible. Based on this, the nominal SM voltage was calculated for the modulation index $M_{\mathrm{r}} = 1.5$. Finally, the combined power rating of the semiconductor devices has been calculated for both converters with the method employed in [30]. This calculation shows that, for the design parameters of Table I the HACC can transfer twice the power of the FB-MMC without doubling the power rating of semiconductor devices.

The simulation results are illustrated in Figs. 13 and 14 for the HACC and the FB-MMC, respectively. The first plot from the

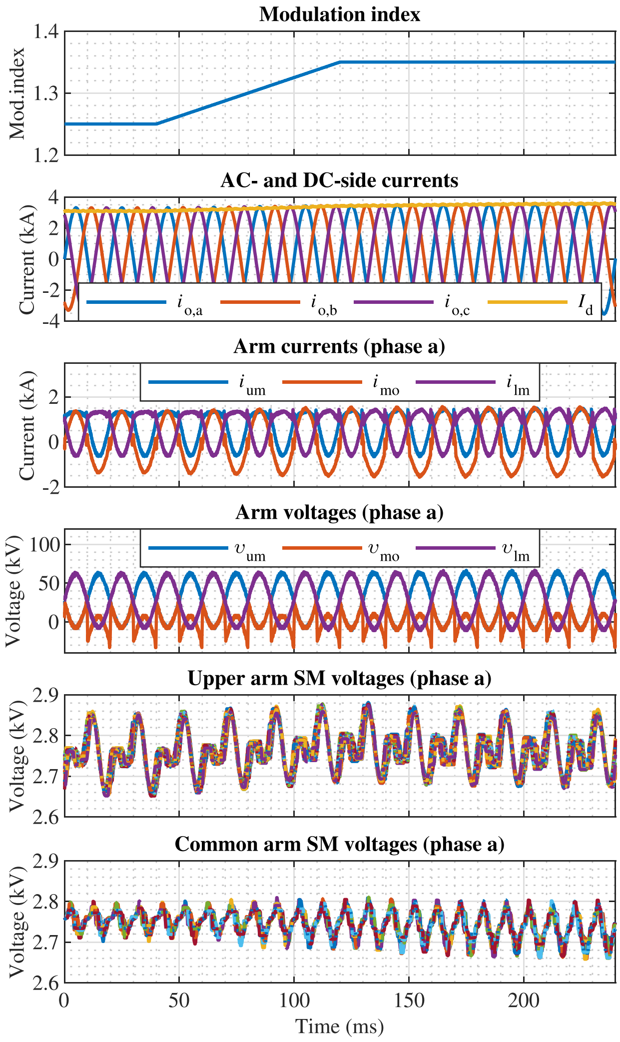


Fig. 13. Simulation results for a ramp change $M = 1.25 - 1.35$ of the HACC connected to a passive load $R_o = 10.3\ \Omega$, for $\Delta t_{\text{com}} = 350\ \mu\text{s}$ and $\varphi = 3°$ capacitive.

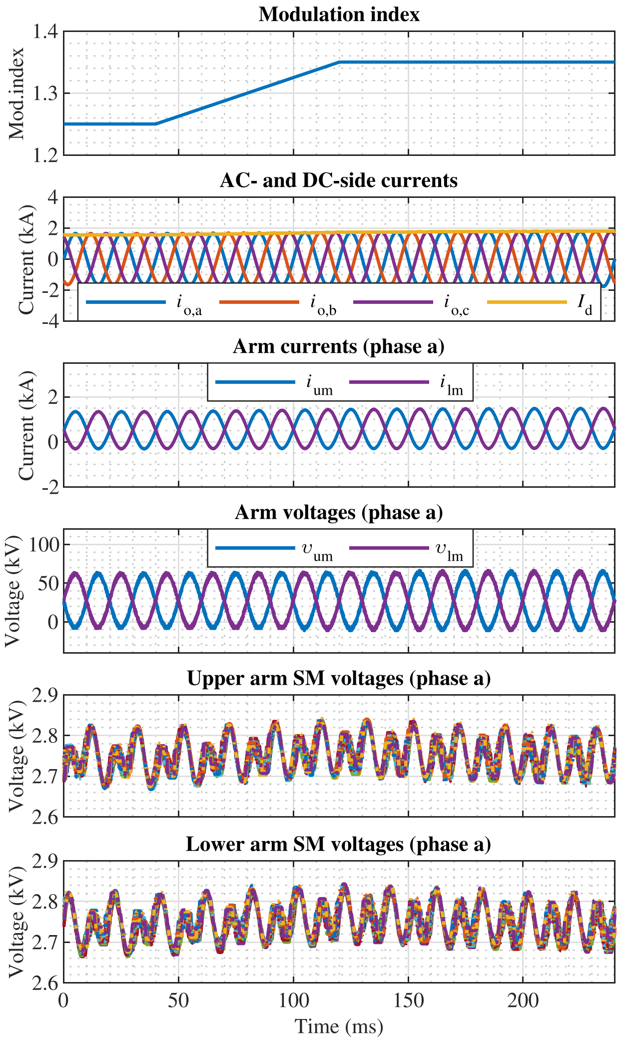


Fig. 14. Simulation results for a ramp change $M = 1.25 - 1.35$ of the FB-MMC connected to a passive load $R_o = 20.6\ \Omega$, for $\varphi = 3°$ capacitive.

top of Fig. 13 shows the variation of the modulation index, while the second plot from the top shows the corresponding variation of the phase and the dc-link currents. The fourth plot from the top illustrates the voltages generated by the arms of phase a; it can be seen that the voltage of the common arm (v_{mo}) is roughly half that of the main arms. However, the most interesting plot is the third from the top of Fig. 13, which shows that the peak currents of all arms of the HACC are equal throughout the defined range of modulation indices. Hence, it can be concluded that selecting the current-sharing factor according to (27) leads to equal sharing of the peak terminal currents among the main and common arms.

The two bottom plots of Fig. 13 show that the average SM voltages of the main and the common arm remain around the nominal SM voltage of 2.75 kV, even though they are slightly distrurbed during the ramp of the modulation index. Moreover, the ripple of the SM voltages of the main and common arms at the maximum modulation index $M = 1.35$ is 6.6% and 5.4%, respectively. These ripple figures represent the maximum ripples among all SMs of the main and common arms, and were derived by measuring the SM voltage variations at steady state. The ripple of each SM was derived by subtracting the minimum and the maximum voltage within ten fundamental cycles. Then, the maximum ripple among all SMs of the main arms was extracted and found to be 6.6%. The same process was followed for the extracting the maximum ripple of the SMs of the common arm, which was found to be 5.4%.

By comparing the second and third plots from the top of Figs. 13 and 14, it can be directly observed that the output current of the HACC is double that of the MMC, while the peak arm currents are equal for both converters. This result verifies that the HACC can transfer double power by using SMs rated for the same peak current as those of the MMC. However, the SM-voltage ripple of the HACC at the maximum modulation index $M = 1.35$ is higher than that of the MMC, which was found to be 5.1%.

The most important results from the simulations of the two converters are summarized in Table II. All results were extracted

TABLE II
COMPARISON OF THE HACC AND THE MMC FOR $M = 1.35$ BASED ON SIMULATION RESULTS

	HACC	FB-MMC
RMS phase current	2.51 kA	1.26 kA
Peak currents of main/common arms	1.52/1.55 kA	1.50/- kA
RMS current of main/common arms	0.96 kA/1.18 kA	0.87 kA/-
SM voltage ripple of main/common arms	6.7%/5.4%	5.1%/-

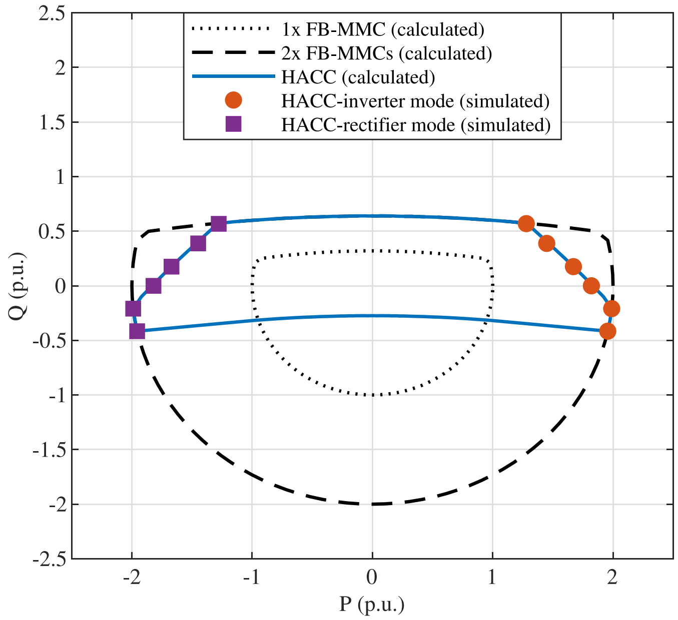


Fig. 15. Calculated *P–Q* capability curves of a single FB-MMC (dotted black line), two parallel FB-MMCs representing the power ratio two (dashed black line), and the HACC (solid blue line), as well as simulated *P–Q* points of the HACC for inverter (red circles) and rectifier (purple squares) modes. Note that positive and negative *Q* represent the converters' reactive power generation and consumption, respectively.

at steady state after the end of the ramp of the modulation index M; thus, the results correspond to $M = 1.35$. The phase current of the HACC is double than that of the MMC at the same modulation index, while the peak arm currents of the HACC are slightly higher, i.e., 2.5%. The reason is that the arm currents of the HACC have higher ripple, due to the low inductance in the current-sharing loops. Therefore, the simulation results confirm that the HACC can transfer twice the power of the MMC for equal peak arm currents.

Table II shows that the rms current of the main arms of the HACC is increased by 12% compared to that of the MMC, which implies that the conduction losses are also increased. Moreover, the rms current of the common arm is even higher than that of the main arms for the given modulation index. Yet, it was found that the conduction losses of the HACC are in the same range as that of the FB-MMC, as the number of devices in the conduction path of the common arm and the thyristor switch are lower than that of the main arms. It should be noted that the current through the common arm approximates a sinusoid with amplitude roughly equal to the peak arm current, as shown in the third plot from the top of Fig. 13. Based on this observation, the rms current of the common arms is expected to be 1086 A, which is almost equal to the value of Table II. Moreover, the voltage ripple of the SM capacitors is higher for the HACC. This is because the energy variations of the main arms are roughly doubled compared to the MMC, but the SM capacitance is not double, as shown in Table I. The reason for this is that both converters were designed for the same energy storage capability (i.e,. 40 kJ/MVA), but the energy storage in the HACC is distributed among the main and common arms. Therefore, it can be concluded that the HACC designed for the same modulation index (within the optimal range), peak arm current, and energy storage capability as the FB-MMC can transfer twice the power of the MMC without doubling the semiconductor power rating, but at the expense of higher SM voltage ripple and rms arm currents.

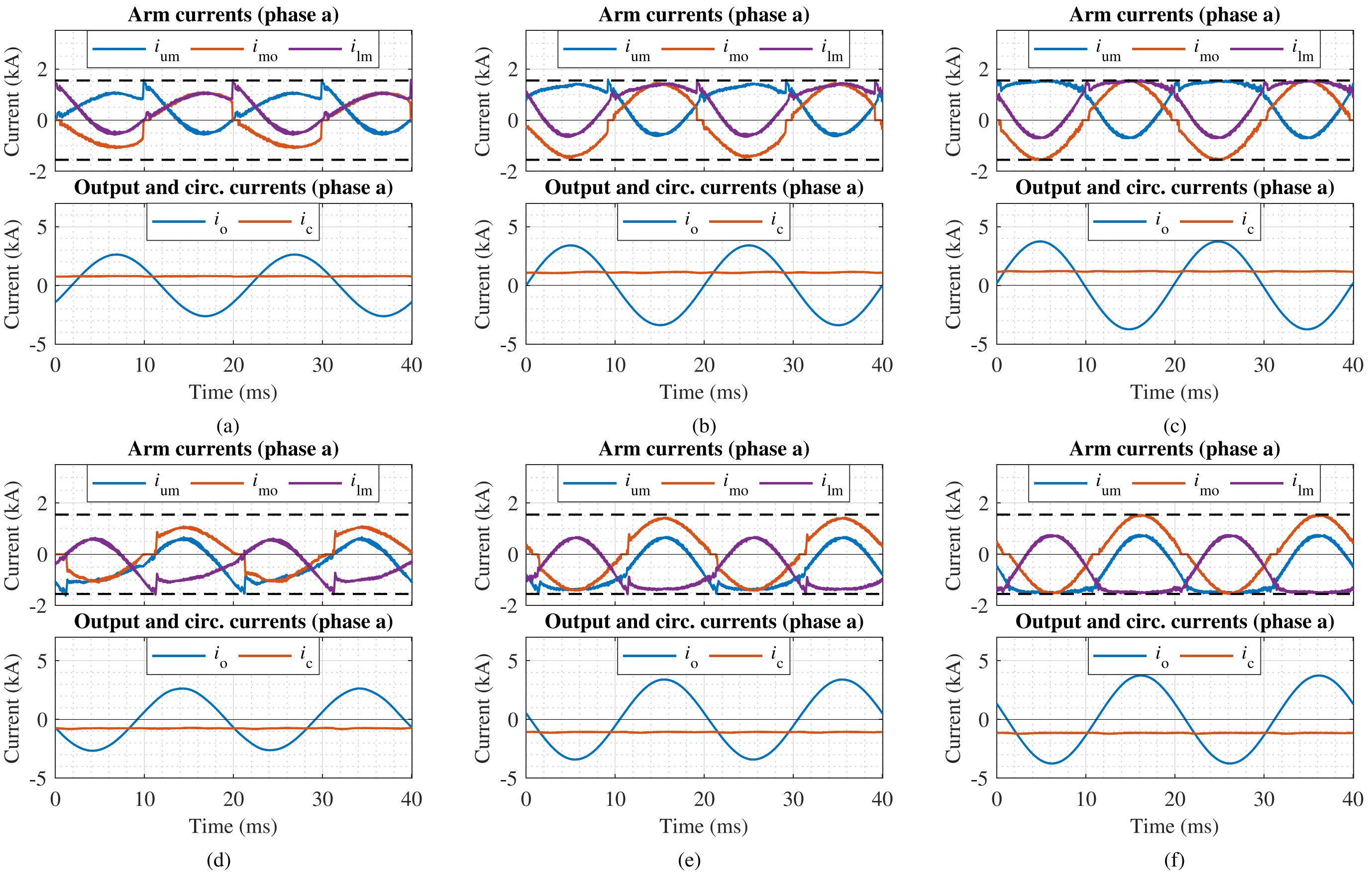
B. *P–Q* Capability

The second simulation test was aimed at verifying the *P–Q* capability of the HACC. For this purpose, the simulation model was modified by connecting the HACC to a grid, with rms phase voltage $V_{\mathrm{g,ph}} = 24.9$ kV (i.e., line voltage $V_{\mathrm{g,ll}} = 43.1$ kV), via a transformer with leakage inductance 3.4 mH (i.e., 0.1 p.u. and roughly equal to the arm inductance). In this case, the three-phase feed-forward terms of the OCC ($v_{\mathrm{of,a}}$, $v_{\mathrm{of,b}}$, $v_{\mathrm{of,c}}$) were set equal to the grid voltages and the phase of the grid voltage, which can be retrieved by a phase-locked loop, was used as the dq-reference angle θ_{dq}.

Thus far, the analysis revealed that the discontinuity currents is an important limiting factor of the power ratio. As shown in Fig. 11, the power ratio of the HACC can be a achieved for a specific range of modulation indices, which depends on the power angle and the commutation time. In order to illustrate these limitations, the *P–Q* capability of the HACC, with commutation time $\Delta t_{\mathrm{com}} = 350\ \mu$s, has been calculated by considering the following conditions.

1) The HACC is connected to a grid via the transformer leakage inductance, as described previously.
2) The arm resistances were disregarded.
3) The peak current through all arms must not exceed ± 1.55 kA. Therefore, the output current of the HACC is adjusted so that the peak current limit is respected.
4) The HACC is operated at the modulation index range $M = [1.25, 1.35]$ (corresponding to a range of rms output voltages $V_{\mathrm{o}} = [48.6, 52.5]$ kV). As the maximum and minimum modulation index limit the maximum reactive power that the HACC generates and consumes, respectively, the output current is adjusted accordingly.
5) The SM-voltage ripple was not considered for estimating the minimum reactive-power consumption.

For comparison purposes, the *P–Q* curves of a single FB-MMC and two parallel FB-MMCs were calculated by



(a) (b) (c)

(d) (e) (f)

Fig. 16. Arm currents of phase a to show that peak and discontinuity currents are below the maximum of 1550 A that has been defined for the calculation of the *P*–*Q* curve. φ_g is the angle between the grid voltage and current. (a) Inverter mode, $\varphi_\mathrm{g} = 24^\circ$, $R_\mathrm{h} = 1.41$. (b) Inverter mode, $\varphi_\mathrm{g} = 0^\circ$, $R_\mathrm{h} = 1.82$. (c) Inverter mode, $\varphi_\mathrm{g} = -12^\circ$, $R_\mathrm{h} = 2$. (d) Rectifier mode, $\varphi_\mathrm{g} = 156^\circ$, $R_\mathrm{h} = 1.41$. (e) Rectifier mode, $\varphi_\mathrm{g} = 180^\circ$, $R_\mathrm{h} = 1.82$. (f) Rectifier mode, $\varphi_\mathrm{g} = 192^\circ$, $R_\mathrm{h} = 2$.

considering the same conditions. Since the FB-MMCs can operate down to modulation index zero, their reactive power consumption is not limited by the minimum modulation index. Note that the two parallel FB-MMCs represent the power ratio of two for any *P*–*Q* operating point.

The calculated *P*–*Q* capability curves of all converters are depicted in Fig. 15, which shows that the *P*–*Q* capability of the HACC is narrower than that of the two parallel FB-MMCs. This is because of two limits: 1) the minimum modulation index $M = 1.25$ that causes the flattening of the bottom part of the *P*–*Q* curve; and 2) the discontinuity current that causes the tilting of the sides of the *P*–*Q* curve. Yet, the flattening of the upper part of the *P*–*Q* curve is the same for both converters due to the maximum modulation index $M = 1.35$. Note that the HACC achieves the maximum power ratio $R_\mathrm{h}^\mathrm{ds} = 2$ at the points where its *P*–*Q* curve is equal to that of the two parallel FB-MMCs. Clearly, the range of points where the power ratio of the HACC is equal to 2 is limited. Furthermore, for increased reactive-power generation, the power ratio of the HACC is reduced. For example, for zero reactive-power, the power ratio of the HACC is 1.82, while for 0.57 p.u. reactive-power generation (i.e., grid power angle $\varphi_\mathrm{g} = 24^\circ$), the power ratio of the HACC is 1.41. Conversely, for increased reactive-power consumption, the power ratio of the HACC is increased, e.g., for -0.21 p.u. reactive-power generation (i.e., grid power angle $\varphi_\mathrm{g} = -12^\circ$), the power ratio of the HACC is maximum. Hence, it can be concluded that the HACC can achieve its maximum power capability when it consumes reactive power.

Moreover, Fig. 15 includes 12 *P*–*Q* points of the HACC that were acquired from the simulation model described in the beginning of this section. Note that six of the *P*–*Q* points correspond to inverter mode (red dots) while the other six correspond to rectifier mode (purple squares). As mentioned previously, the output current for each of these points has been adjusted so that the peak current of all arms not exceeding ±1.55 kA. This is clearly shown in Fig. 16, where the arm-, output-, and circulating-current waveforms of phase a are illustrated for three inverter-mode *P*–*Q* points [see Fig. 16(a)–(c)] and for three rectifier-mode *P*–*Q* points [see Fig. 16(d)–(e)]. From the arm-current waveforms, which are illustrated in the top plot of each subfigure in Fig. 16, it can be observed that all arm currents are within the defined limits of ±1.55 kA, which are represented by the dashed black lines. Moreover, the bottom plots of each subfigure in Fig. 16 show that the output current is different for each case, which reflects the fact that the output current was scaled so that the peak arm currents do not exceed ±1.55 kA. The same can be observed for the dc circulating current, which reflects that the power transferred between the dc and ac sides is modified according to the scaling of the output current.

TABLE III
DESIGN PARAMETERS OF THE HACC PROTOTYPE

Rated power	1.26 kVA
DC-link voltage	200 V
Output voltage ($M = 1.35$)	95.4 V (rms)
Output Current	13.3 A (rms)
DC-link capacitance (per arm)	2.2 mF
Arm inductance	5.0 mH
Current-sharing inductance (per arm)	0.2 mH
Num.of SMs per main arm	5
Num.of SMs per common arm	5
SM nominal voltage	50 V
SM capacitance	2.7 mF (40 kJ/MVA)
Thyristor snubber capacitance	0.1 μF
Thyristor snubber resistance	40 Ω
Commutation time (Δt_{com})	350 μs
Thyristor extinction time (t_{q})	150 μs
Change rate of current during commutation	0.25 A/μs
PWM carrier frequency of main/common arms	1.14 kHz / 1.14 kHz
Sampling frequency for control loops, filters	11.4 kHz

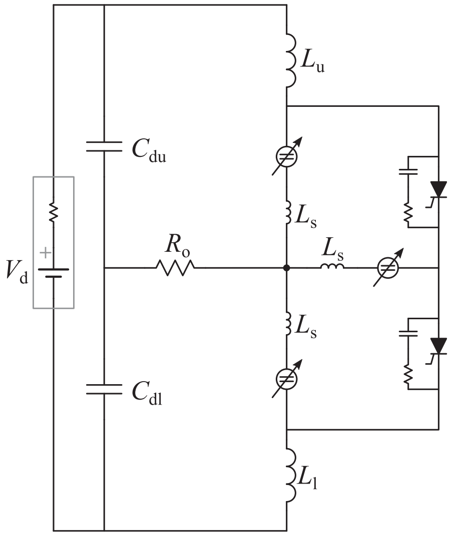


Fig. 17. Test setup of the single-phase HACC prototype.

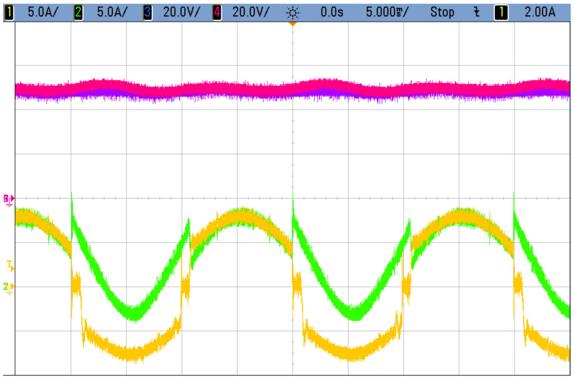


Fig. 18. Steady-state waveforms of voltage of SM1 of upper (magenta) and common (blue) arm and of current of the upper (green) and common arm (yellow). Note that the selection of p_{opt} leads to equal peak arm currents.

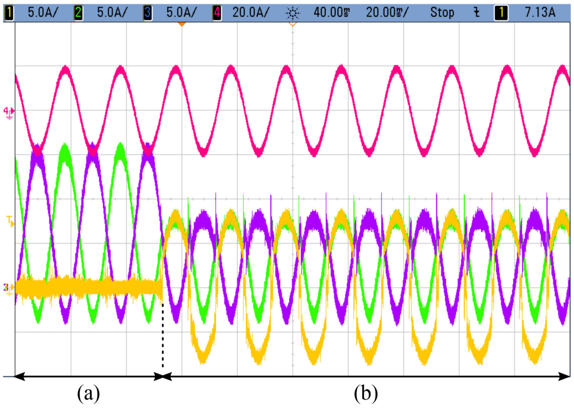


Fig. 19. Waveforms of the load current (magenta) and the current through all arms of the single-phase HACC prototype during a step change of the control mode: (a) no current-sharing before 50 ms; and (b) current-sharing with p_{opt} after 50 ms. Note that the selection of p_{opt} leads to equal peak arm currents without affecting the load current. The current spikes observed at the thyristor turn-OFF instants are caused by the reverse recovery current of the related thyristor.

VIII. EXPERIMENTAL RESULTS

In order to verify the feasibility of the HACC and the theoretical analysis, a single-phase laboratory prototype has been built with the specifications summarized in Table III. Note that the common arm has the same number of SMs as the main arms. This design choice was made because it did not impact the validity of the tests and it simplified the start-up process and the implementation of the modulation scheme. The latter is the phase-shifted carrier scheme without phase-shift among the carriers of the different arms; that is the same five carriers have been used for all arms. The control structure is similar to the one shown in Fig. 12, but the output-voltage reference (i.e., modulation index and phase) and the optimal current-sharing factor are supplied in an open-loop fashion.

The test setup of the prototype is illustrated in Fig. 17, which shows that the prototype was connected to a resistive load (R_{o}) and to a dc power supply via two dc-link capacitors (C_{du}, C_{dl}). The dc-link capacitors were used for two purposes, namely: 1) for creating a midpoint where the load could be connected; and 2) for compensating the reactive power of the relatively large arm inductors (L_{u}, L_{l}), as the fundamental components of the terminal currents flow through these capacitors. Therefore, the arms of the prototype were operated at a power angle close to zero. Note that only the thyristors required for inverter mode were utilized. These were complemented with simple RC snubbers for limiting the rate of change of the voltage during the turn-OFF process and during the OFF-state when SMs are inserted and bypassed. The current-sharing inductors (L_{s}) were selected in order to limit the current ripple, as the number of SMs is small, i.e., 5. Hence, the di/dt during the turn-OFF process of the thyristors is fairly low.

The current and the voltage of one SM of both the upper and common arms were recorded during steady-state operation at the modulation index $M = 1.352$ and the optimal current-sharing factor $p_{\mathrm{opt}} = 0.47$. The results are shown in Fig. 18, which shows that the SM voltages and the peak currents are equal for both the upper and common arms. Note that the spikes observed in the main-arm current at the times when the common-arm current becomes zero are due to the fairly high reverse recovery current of the employed thyristors. Despite this spike, the observation

TABLE IV
CONVERTER COMPARISON

Converter	2x HB-MMCs	2x FB-MMCs	HACC
DC-fault ride through	No	Yes	Yes
DC-link voltage	55 kV	55 kV	55 kV
Grid line voltage	28.0 kV (rms)	43.1 kV (rms)	43.1 kV (rms)
Main arm: rated current	2.05 kA	1.55 kA	1.55 kA
Main arm: nominal SMs voltage	2.75 kV	2.75 kV	2.75 kV
Main arm: number of SMs	20	25	25
Main arm: number of IGBTs	40	100	100
Common arm: rated current	-	-	1.55 kA
Common arm: nominal SMs voltage	-	-	2.75 kV
Common arm: number of SMs	-	-	17
Common arm: number of IGBTs	-	-	68
Thyristor switch: rated current	-	-	1.55 kA
Thyristor switch: rated voltage	-	-	60.5 kV$^{(*)}$
Thyristor switch: number of thyristors	-	-	2
Semiconductor power of all main arms	2x 1353 MVA	2x 2557.5 MVA	2557.5 MVA
Semiconductor power of all common arms	-	-	767.3 MVA
Semiconductor power of all thyristors	-	-	1125.3 MVA
Total Semiconductor power rating	2574 MVA	5115.0 MVA	4450.1 MVA
Apparent power at $\varphi_{\mathrm{g}} = -24°$	198.0 MVA	198.0 MVA	71.3 MVA
Apparent power at $\varphi_{\mathrm{g}} = -12°$	198.0 MVA	198.0 MVA	198.0 MVA
Apparent power at $\varphi_{\mathrm{g}} = 0°$	198.0 MVA	198.0 MVA	180.2 MVA
Apparent power at $\varphi_{\mathrm{g}} = 15°$	173.3 MVA	191.1 MVA	148.5 MVA
Apparent power at $\varphi_{\mathrm{g}} = 24°$	137.8 MVA	139.6 MVA	139.6 MVA

(*): Thyristor rated for the dc-link voltage plus the nominal voltage of two SMs that is used for the thyristor turn-OFF process.

of equal peak currents demonstrates that the selection of the current-sharing factor, as defined by (27), is in line with the theoretical analysis and the simulation results.

In order to demonstrate more clearly the effectiveness of the current-sharing concept, a second measurement was performed. In this measurement, the converter was initially operated without current-sharing and then current-sharing was activated. The currents of all arms and the load current were recorded and are presented in Fig. 19. This figure shows that for the first 50 ms the current through the common arm is zero, while the main arms carry the terminal currents. After the first 50 ms, when the current-sharing control is activated, the peak currents through the main arms are roughly halved, while the output current remains at the same level as during the first 50 ms. Therefore, it can be concluded that the experimental results confirm the theoretical analysis of the converter operation and particularly the selection of the current-sharing factor according to (27).

IX. DISCUSSION

A. Converter Comparison

In this section, the HACC is compared with two parallel FB-MMCs and two parallel HB-MMCs for the same dc-link voltage, based on the former's *P–Q* capability curve, shown and verified in Section VII-B. It should be highlighted that the comparison is presented only for demonstrating the potential of the HACC, as none of the converters is optimized in terms of arm-voltage rating, stored energy, or efficiency. Such a comparison would require a thorough design process and is beyond the scope of this article. The comparison of the HACC, the two parallel FB-MMCs, and the two parallel HB-MMCs is summarized in Table IV, which includes the ratings and number of the main semiconductor devices, the total semiconductor power rating, and the apparent power supplied to the grid for different grid power angles φ_{g} corresponding to inverter mode.

Table IV shows that the HB-MMCs requires the lower semiconductor power rating, but its arm current rating is higher due to its lower output voltage and it does not feature dc-fault ride through capability, as the other two converters. Apart from this, the total semiconductor power rating of the HACC is 13% lower than that of the FB-MMCs and 64% higher than that of the HB-MMCs, while all converters supply the same apparent power to the grid for $\varphi_{\mathrm{g}} = -12°$, i.e., the converter consumes reactive power. Yet, the apparent power supplied by the HACC is lower than that of the FB-MMCs and the HB-MMCs for $\varphi_{\mathrm{g}} = 0°$ and likewise for $\varphi_{\mathrm{g}} = 15°$, i.e., when the converter generates reactive power. This reduction is attributed to the discontinuity current and indicates the tradeoff between power capability and semiconductor power rating. However, for $\varphi_{\mathrm{g}} = 24°$ all converters supply the same apparent power to the grid, because at this power angle the power capability is limited by the maximum modulation index, which is $M = 1.35$ for the HACC and the FB-MMCs and $M = 0.95$ for the HB-MMCs. Moreover, note that for $\varphi_{\mathrm{g}} = -24°$, the power capability of the HACC is severely limited due to the minimum modulation index of $M = 1.25$.

The comparison of Table IV clearly shows that the power capability of the HACC is limited for increasing reactive-power demand. The limits are imposed by the discontinuity current, for reactive-power generation, and the minimum modulation index, for reactive-power consumption. Yet, these shortcomings could be potentially alleviated by the following techniques.

1) Addition of capacitor banks at the ac terminals of the HACC to generate some of the reactive power required by the grid. In this way, the power angle at the arms of the

HACC would be closer to zero and thus, the limitation due to the discontinuity current could be decreased or eliminated, as shown in Fig. 10(a). Hence, the *P*–*Q* capability could be extended for reactive-power generation.

2) Employing transformers with tap-changing capability so that the HACC can operate at modulation indices higher than $M = 1.25$ even when the converter needs to consume reactive power, i.e., its output voltage needs to be much lower than the grid voltage. Alternatively, the reactive-power consumption of the HACC can be equal to that of a single FB-MMC (i.e., dotted black line in Fig. 15) by operating only the main arms.

B. Circuit Design and Dynamic Performance Considerations

This section briefly discusses considerations that were taken into account during the study of the HACC, but are not addressed in great detail in this article. First, note that the main inductors L_u and L_l are placed outside the current-sharing loops because they are fairly large. Thus, if they were placed within these loops, very high voltages would be required for switching the thyristors at di/dt rates in the range of 10–15 A/μs. Achieving these di/dt rates is important for minimizing the interval Δt_di, and thus the commutation time Δt_com, without exceeding the di/dt-rate limitation of the thyristors. Thus, the inductances within the current-sharing loops need to be much smaller than the main inductances, which has implications on the selection of the effective switching frequency of the converter ams. Notably, this frequency should be high enough so that: 1) the current ripple during current sharing is acceptable; and 2) the bandwidth of the current-sharing control loop is sufficiently high.

In this article, the main arms of the HACC consist only of FB SMs. However, it is also possible to construct the main arms by combining FB and HB SMs. For ensuring the dc-fault blocking of such design, the number of FB SMs of the main and common arms should be equal and sufficient to provide an alternate voltage with amplitude equal or higher than the grid voltage. Yet, the modulation and SM sorting needs to be modified to address the SM-voltage balancing problem of the mixed HB-FB arms [31].

Finally, this article focused on the operating principles and dimensioning of the HACC under balanced steady-state conditions. Yet, it is important to study the operation of the HACC under unbalanced grid conditions. For example, when large amounts of negative sequence voltage are present in the grid voltage, the legs of the HACC will need to operate at very different modulation indices (assuming that the converter does not inject negative sequence currents). As such a situation might complicate the operation of the HACC, due to the modulation index limitations, a simple solution could be to reduce the power of the converter up to a point where all power can be handled by the main arms. Then, the thyristor part of the converter could be completely turned OFF, so that only the main arms remain active and the HACC is operated as an FB-MMC. As soon as the grid voltage becomes balanced, the thyristor part of the converter can be activated again and the power can be ramped up. Moreover, it is equally important to study the dynamic performance of the HACC under ac and dc faults. Such studies are out of the scope of this article, but would be interesting topics for future research.

X. CONCLUSION

In this article, the energy balancing and the dimensioning principles of the HACC have been studied. It has been shown that the power capability of the converter is maximized when the peak currents of all arms are equal. In order to achieve this condition, the current-sharing factor needs to be carefully selected by employing the method suggested in this article. However, it was shown that the power capability is significantly impacted by the discontinuous operation of the converter, i.e., by the discontinuity currents. A method that compiles all the factors that impact the power capability was presented and used for identifying the range of modulation indices and commutation times for which the power capability is maximized. The results indicate that the power capability of the HACC is maximized in a limited range of modulation indices and commutation times. The simulation results confirm that, if operated within the optimal range of modulation indices, the HACC can transfer double the power of the FB-MMC, without doubling the total semiconductor power rating, provided that thyristors with low t_q time are employed. However, this benefit comes at the cost of increased SM voltage ripple and rms currents through all the arms. Moreover, the power capability of the grid-connected HACC was demonstrated by the calculated *P*–*Q* curve, which was verified by simulations. Finally, the feasibility of the HACC, the energy balancing, and the method of selecting the optimal current-sharing factor were confirmed by experimental results acquired from a single-phase lab prototype of the HACC.

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