Hold-Up Time Compensation Circuit of Half-Bridge LLC Resonant Converter for High Light-Load Efficiency

Yeonho Jeong, *Member, IEEE*, Min-Su Lee, *Student Member, IEEE*, Jae-Do Park, *Senior Member, IEEE*, Jae-Kuk Kim, *Member, IEEE*, and Ronald. A. L. Rorrer, *Member, IEEE*

***Abstract*—This article proposes a half-bridge *LLC* resonant converter applying a simple circuit with a variable magnetizing inductance scheme for hold-up time requirement. By changing the magnetizing inductance of the main transformer, the proposed converter can satisfy the hold-up time requirement without sacrificing efficiency, featuring small conduction, and turn-OFF switching losses of the primary switches in the nominal status. In addition, the proposed converter can relieve the burden of the additional components by positioning them on the signal path, and the proposed circuit is self-powered by adding only one additional winding instead of the isolated power supply. Therefore, those of the size and cost of the proposed circuit can be reduced compared to the previous studies. The feasibility of the proposed method was verified with a 350 W prototype converter (56 V/6.25 A), and the improved circuit for the transient mode was also presented. The experimental results validated the theoretical analysis and showed the effectiveness of the proposed converter for high-efficiency applications, especially in light-load conditions.**

***Index Terms*—High voltage gain, hold-up time compensation, *LLC* resonant converter, server power supply, variable inductance.**

I. Introduction

FOR the server power supplies that strongly require high efficiency, some standards have been developed for their power consumption, especially in the efficiency guideline set by climate savers computing initiative for computing and server systems [1]–[3]. Although the highest efficiency is still required at the half-load conditions, a standard efficiency at 20% load conditions has been reinforced. Moreover, the efficiency guideline at 10% load conditions is newly added [3]. This trend shows that the light-load efficiency is becoming more important and emphasized, where a server system mostly operates [4]–[6]. In addition, power systems can operate under light-load conditions when the system load is shared by multiple power systems in parallel [7]–[9].

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The authors are with the Department of Electrical/Mechanical Engineering, University of Colorado Denver, Denver, CO 80204 USA (e-mail: yeonho.jeong@ucdenver.edu; trevin6248@kaist.ac.kr; jaedo.park@ucdenver.edu; jkkim99@inha.ac.kr; ronald.rorrer@ucdenver.edu).

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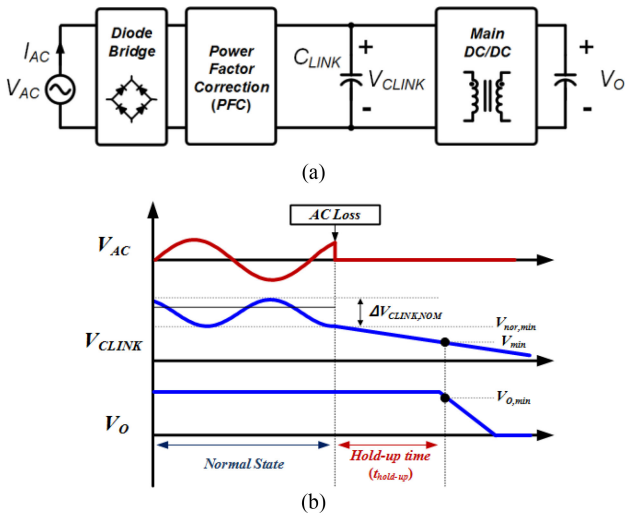


Fig. 1. Various requirements of Server Power Systems. (a) General server power structure. (b) Hold-up time requirement.

A server and network power supply mostly consists of three stages, as shown in Fig. 1(a). The first stage has a diode bridge rectifier converting ac input voltage to dc voltage. In the second stage, a power factor correction (PFC) circuit provides near unity power factor and low total harmonic distortion. The third is a dc/dc converter stage to regulate the output voltage tightly and achieve a galvanic isolation [5]–[9], where the half-bridge (HB) *LLC* resonant converter is widely used for the medium power applications because of the simple structure, zero-voltage-switching (ZVS) operation for primary switches over the entire load range, and zero-current-switching for secondary-side rectifiers. Moreover, the HB *LLC* resonant converter inherently shows high light-load efficiency because there is no output inductor core loss.

Meanwhile, one of the most important specifications for a server power supply is the hold-up time [10]–[15], where the output voltage should be regulated after ac line is lost to save the data in the server system as shown in Fig. 1(b). To maintain the output voltage during the hold-up time, a large link capacitor CLINK is inserted between the PFC and dc/dc stage, as shown in Fig. 1(a) to supply the power after ac line drops, but it reduces the input voltage range for the following dc/dc stage. Since

the size of link capacitor is limited due to the required power density, the HB *LLC* resonant converter in the dc/dc converter stage should be designed to cover a wide input voltage range to satisfy the hold-up time requirement; however, the efficiency of the dc/dc converter is degraded because of the small magnetizing inductance for high voltage gain that increases the conduction and turn-OFF switching losses at the nominal input operations, especially at the light-load conditions.

To achieve high efficiency at nominal input voltage and meet the hold-up time requirement, hold-up time compensation circuits have been proposed [10]–[19]. The first approach uses an additional power stage, which is supplying power for regulating the output voltage during the hold-up time [10]. In [11]–[13], methods with additional transformer windings and semiconductor devices are presented. By increasing the secondary turns of the transformer during the hold-up time, a large voltage conversion ratio can be achieved for hold-up time requirement. Approaches with an additional power switch are proposed in [14]–[17] changing the operation mode of the *LLC* resonant converter into pulsewidth modulation (PWM) control mode to get a high voltage gain during the hold-up time. Although these methods in [10]–[17] show a high efficiency in nominal conditions by optimized design for the narrow input voltage range, they require many additional power devices. In [18], the asymmetric PWM (APWM) control method is very attractive because high voltage gain can be obtained without power switches; however, it causes the dc offset current in the transformer that may increase the transformer size, which lowers the power density. In addition, the methods in [13]–[18] require an additional controller IC for the PWM and APWM control, and the increased complexity and cost of the control circuit can be burdensome. Finally, in [19], an auxiliary *LC* tank is additionally connected to the magnetizing inductance in parallel to change the equivalent inductance, and it achieves high voltage gain without additional control. However, the large size of the *LC* tanks can deteriorate the power density, although there is no additional active switch. Moreover, the switching should be controlled with high resolution due to the steep voltage gain.

In this article, a novel hold-up compensation scheme is proposed to eliminate the abovementioned limitations of previous studies. The proposed converter changes the transformer magnetizing inductance in response to the input status in the HB *LLC* resonant converter. In nominal status, it can achieve high efficiency with small conduction and turn-OFF losses of the primary switches because the HB *LLC* resonant converter operates with large transformer magnetizing inductance. Meanwhile, during the hold-up time, high voltage gain can be obtained because of the reduced transformer magnetizing inductance. In addition, the proposed method is implemented by adding three auxiliary transformer windings and a simple self-powered control circuit without any additional switch ON the power path and an isolated power supply, so that it can achieve a high power density. The comparison with previous studies is also discussed in view of the power density and cost. Moreover, a practical design example for the proposed scheme is presented in detail, and the feasibility is experimentally verified with a 350-W prototype.

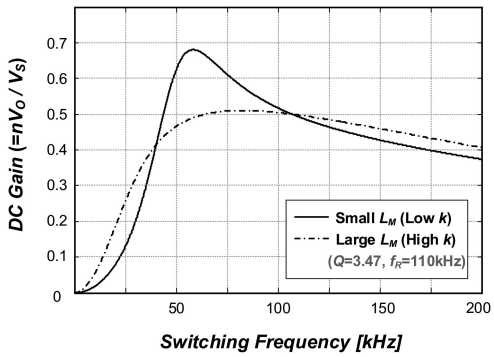


Fig. 2. Design examples with different L_M and k factor.

II. Description of Proposed Converter

A. Concept of Proposed Method

Based on the fundamental harmonic approximation [10], [11], the voltage gain of the HB *LLC* resonant converter can be obtained as follows:

$$M = \frac{nV_O}{V_S} = \frac{1}{2\sqrt{\left[1+\frac{1}{k}\left\{1-\left(\frac{f_R}{f_{sw}}\right)^2\right\}\right]^2 + \left\{\frac{\pi^2}{8n^2}Q\left(\frac{f_R}{f_{sw}}-\frac{f_{sw}}{f_R}\right)\right\}^2}}, \quad (1)$$

where $k = L_M/L_R$, $Q = (L_R/C_R)^{0.5}/R_O$, $f_R = 1/(2\pi \cdot (L_R C_R)^{0.5})$, $n\,(= N_P/N_S)$ is the transformer turns-ratio, and f_{sw} is the switching frequency.

Fig. 2 shows the voltage gain curves of the HB *LLC* resonant converter in accordance with the different value of magnetizing inductance L_M and k factors, which is the ratio between L_M and resonant inductance L_R. To meet the hold-up time specification, the HB *LLC* resonant converter should be designed with low k factor, i.e., small L_M as shown in solid line in Fig. 2. However, it causes high peak magnetizing current, which lowers efficiency due to the large conduction and turn-OFF losses on the primary switches. On the other hand, to achieve a high efficiency at nominal input, the HB *LLC* resonant converter should be designed with high k factor indicating large L_M to reduce conduction and switch turn-OFF losses in the primary side. However, the maximum gain is not high enough to satisfy hold-up time requirement in this case as shown with the dotted line in Fig. 2; desired k factor would substantially vary depending on the input mode, nominal input voltage and hold-up time. A high k factor with large L_M is necessary in the nominal status for high efficiency, while low k factor with small L_M is required during hold-up time for high voltage gain. The proposed method can have high efficiency with large L_M in nominal status and obtain high voltage gain by decreasing L_M during the hold-up time. In addition, the voltage gain can be smoothly changed in the proposed converter, since only L_M is changed and there is no change of other resonant design factors such as L_R and C_R that are related with f_R and Q. The dynamic change of the voltage

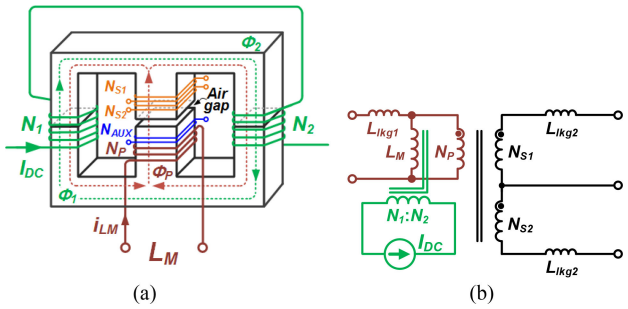


Fig. 3. Concept of variable inductance by using E-E type core. (a) Implementation for the proposed scheme. (b) Equivalent circuit.

gain can be advantageous for the transient performance, and the design of the proposed method is very straightforward.

B. Variable Magnetizing Inductance for Proposed Scheme

The variable inductor in this article is based on the one in [20]–[23] due to its easy implementation and low dc bias current $I_{\rm DC}$ by using *E-E* type core as shown in Fig. 3(a). The main powering windings on primary and secondary, which are defined as N_P, N_{S1}, and N_{S2}, are same with those on the conventional *LLC* resonant converter. For the variable L_M, two additional windings in the side-legs N_1 and N_2 are employed, and the inductance is controlled by $I_{\rm DC}$. The proposed transformer includes one auxiliary winding N_{AUX}, which is supplying power to the auxiliary circuit. The equivalent circuit including L_M and leakage inductances L_{lkg1} on primary side and L_{lkg2} on the secondary side is shown in Fig. 3(b).

When $I_{\rm DC}$ is not flowing, the inductance of L_M is the designed value by N_P, N_{S1}, and N_{S2} in the center leg. The voltage across N_1 and N_2 by the reflected flux of Φ_P can be canceled due to the opposite connection of them. Namely, there is no change in the nominal operation. On the other hand, when $I_{\rm DC}$ is flowing through N_1 and N_2, the dc magnetic flux on the side-legs Φ_1 and Φ_2 flow through outer legs as a dotted line due to the considerable reluctance of the center-leg by the air gap. Therefore, $\tilde{\Phi}_P$, which flows through the entire core, is overlapped with Φ_2 and canceled by Φ_1. When the voltage across the transformer is opposite, Φ_P is overlapped with Φ_1. Thus, the partial saturation is accomplished so that the total permeability of the main transformer and L_M can be reduced.

C. Implementation and Operation of Proposed Method

To implement the proposed converter, two parts are changed from the conventional converter. First, the auxiliary windings N_1 and N_2 for varying L_M, and second, a control circuit including D_{AUX}, C_{AUX}, R_{AUX}, and N_{AUX} in the main transformer T_1 are added. The proposed circuit can be very simple because it is supported by internal power from N_{AUX} winding without any additional power stage. The auxiliary winding current $I_{\rm DC}$ is controlled, as shown in Fig. 4, for nominal operation and in Fig. 5 during hold-up time operation. In addition, a very small and inexpensive switch Q_{AUX} is used to control $I_{\rm DC}$ flow through windings in side-legs.

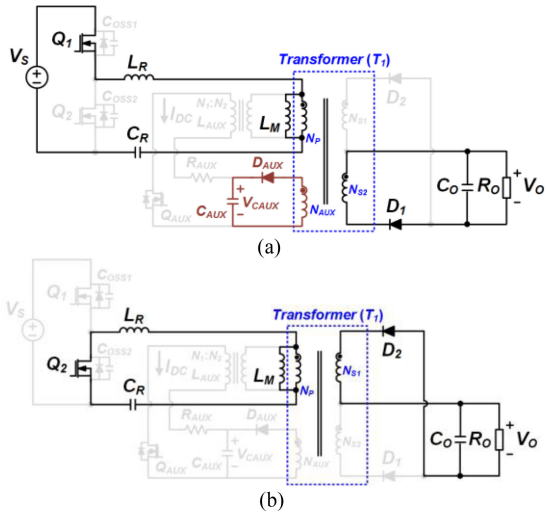


Fig. 4. Operating circuits of proposed method in nominal operation. (a) Q_1 is turned ON. (b) Q_2 is turned ON.

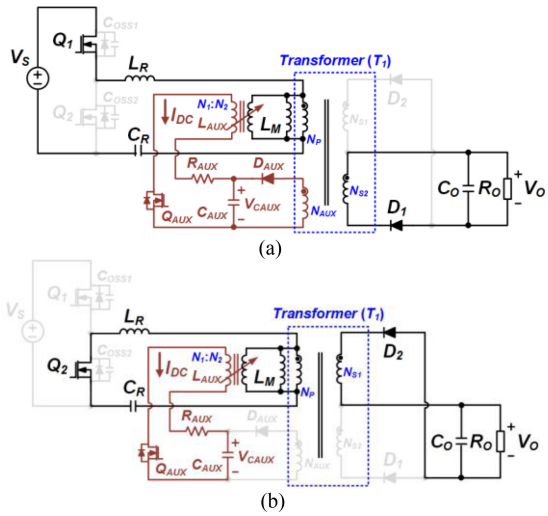


Fig. 5. Operating circuits of proposed method during hold-up time. (a) Q_1 is turned ON. (b) Q_2 is turned ON.

To simplify the mode operation analysis of the proposed converter, the followings are assumed: the dead time is negligible, the capacitance of C_O is large enough and its equivalent series resistance is very small, hence V_O is constant, $I_{\rm DC}$ is considered as dc current without any ripple, and the primary and secondary side leakage inductances are negligible.

The operating circuit in the nominal status is shown in Fig. 4. When Q_1 is turned-ON [see Fig. 4(a)], the positive voltage is applied across the magnetizing inductance of transformer. In the secondary side, the power is transferred to the output stage through D_1. In the auxiliary circuit, V_{CAUX} is clamped to the reflected voltage, $N_{AUX}V_O/N_{N2}$. On the other hand, the negative voltage is applied across the transformer when Q_2 is turned on after Q_1 is turned OFF, as shown in Fig. 4(b). The power is transferred through D_2 in the secondary side. The auxiliary circuit does not operate because D_{AUX} and Q_{AUX}

are turned OFF. In the auxiliary circuit, V_{CAUX} is maintained without the voltage ripple after charging C_{AUX}, as shown in Fig. 4(a), because there is no $I_{\rm DC}$. Moreover, there is no pulsating voltage and efficiency degradation by the eddy current because of the compensated winding connection of N_1 and N_2. As a result, the compensating circuit does not affect the operation and performance of the HB *LLC* resonant converter at the nominal input voltage.

Fig. 5 shows the operation of the proposed converter during the hold-up time. The operation for the power stage is the same with the nominal operation, except that the auxiliary circuit changes L_M by turning on $Q_{\rm AUX}$. In Fig. 5(a), the power is supported through D_1 when Q_1 is turned-on. In the auxiliary circuit, $I_{\rm DC}$ flows through $D_{\rm AUX}$, $Q_{\rm AUX}$, and $R_{\rm AUX}$. In Fig. 5(b), Q_2 is turned-ON and the power is transferred through D_2. In the auxiliary circuit, $C_{\rm AUX}$ is discharged in order to supply $I_{\rm DC}$ to the auxiliary circuit because $D_{\rm AUX}$ is turned OFF by the reflected negative voltage. Therefore, $V_{C\rm AUX}$ in the auxiliary circuit should be carefully designed to retain a constant value of $I_{\rm DC}$. During the hold-up time, $Q_{\rm AUX}$ is turned ON and it allows the dc bias current to flow through N_1 and N_2, which decreases L_M, so that the high voltage gain can be obtained.

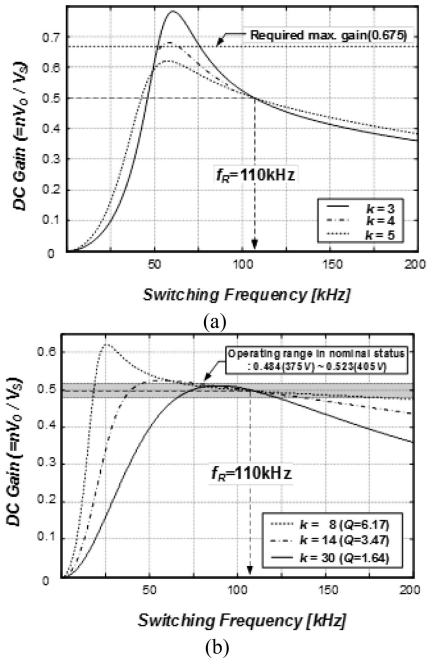


Fig. 6. Design examples with different k factor. (a) Conventional HB LLC resonant converter. (b) Proposed method in the nominal status.

III. Design Guidelines and Analysis of Proposed Converter

In order to prove the effectiveness of the proposed method, a dc/dc stage of server and network power systems is designed, which has the output voltage of 56 V, the maximum average load current of 6.25 A, and the maximum power rating $P_{O,\rm MAX}$ is 350 W. Its input voltage comes from the output of the PFC stage, and it is normally 390 V with 120 Hz ripple voltage, which is 375–405 V in this case with 270 μF of $C_{\rm LINK}$. To satisfy the required hold-up time $t_{\rm holdup}$ of 16 ms, the minimum input voltage $V_{S,\rm MIN}$ can be expressed as follows:

$$V_{S,\rm MIN}=\sqrt{V_{S,\rm NOM(MIN)}^2-\frac{2P_{O,\rm MAX}t_{\rm holdup}}{C_{\rm LINK,MIN}}}. \quad (2)$$

where $V_{\rm S,NOM(MIN)}$ is the minimum input voltage at the nominal input voltage by considering the ripple voltage of $V_{\rm LINK}$ and $C_{\rm LINK,MIN}$ is the minimum capacitance of $C_{\rm LINK}$ with the tolerance.

The required maximum voltage gain $M_{\rm MAX}$ should be considered as follows to satisfy the required hold-up time:

$$M_{\rm MAX}=\frac{nV_O}{V_{S,\rm MIN}\,(1-V_{\rm gain,margin})}=\frac{3.5\times 56}{305(1-0.05)}\cong 0.675, \quad (3)$$

where $V_{\rm gain,margin}$ is the voltage gain margin of 5% in this case by considering the magnetizing inductance's tolerance.

A. Design for Magnetizing Inductance and Resonant Tank

First of all, to operate with the resonant frequency f_R in the nominal input voltage $V_{S,\rm NOM}$ for higher efficiency compared with other operating modes in below and above f_R [10], [11], the turns ratio of transformer n can be calculated as $V_{S,\rm NOM}/(2V_O)$, and it can be 3.5 in this article.

To meet $M_{\rm MAX}$ from (3), the resonant tank, especially the k factor, is selected based on the peak voltage gain. In this article, the magnetizing inductance of the conventional method $L_{M,\rm conv}$ is selected as 180 μH for the maximum load condition that has the lowest voltage gain and high Q factor, and the k factor is set to 4, as shown in Fig. 6(a).

In the proposed converter, the resonant tank design can focus on achieving high efficiency at the nominal operation because $M_{\rm MAX}$ for the hold-up time requirement can be satisfied by varying the magnetizing inductance. To minimize the circulating current and peak value of magnetizing inductor, L_M should be maximized. However, it is hard to achieve ZVS of the primary switches if L_M is too large. Therefore, L_M in the nominal input conditions $L_{M,\rm nominal}$ is determined as follows considering the ZVS of the primary switches at nominal input:

$$\frac{1}{2}L_M I_{LM\_pk}^2=\frac{1}{2}L_M\left(\frac{nV_O}{4L_M f_{SW}}\right)^2<\frac{1}{2}C_{\rm Total}(\frac{1}{2}V_S)^2, \quad (4)$$

$$L_{M,\rm nominal}<\frac{n^2V_O^2}{4C_{\rm Total}V_S^2f_{sw}^2}=640\ [\mu H], \quad (5)$$

where I_{LM_pk} and $C_{\rm Total}$ are the peak value of the magnetizing inductance current and the total equivalent capacitance in primary switches, i.e., $C_{\rm Total}=C_{OSS1}+C_{OSS2}$, respectively.

From (5), L_M of the proposed approach is chosen as 640 μH, as large as possible to minimize conduction and switch turn-OFF losses in the primary side within the full ZVS range. Moreover, due to large L_M, the proposed converter can have narrower air-gap compared to that in the conventional converter having

a small inductance, i.e., 180 μH. It results in the proposed converter's small core loss by weakening the fringing flux effect from the air gap. On the other hand, L_M during hold-up time $L_{M,\mathrm{hold-up}}$ in the proposed converter is designed as same as that of the conventional converter.

For the design of resonant tank, three design examples with $k = 8$, 14, and 30, are discussed, as shown in Fig. 6(b). To cover the 120 Hz ripple voltage of C_{LINK}, the peak voltage gain should be larger than required in the operating range. Therefore, in the case of large k (= 30), it is hard to tightly regulate the output voltage because of the small M_{MAX}. In the case of $k = 8$, although the required voltage gain in the operating range can be satisfied with enough margin, core loss of the 80 μH resonant inductor will be large. In addition, the frequency variation is large because of the large Q factor. Therefore, the k factor is selected as 14 in the proposed converter to minimize the core loss while satisfying the required voltage gain in nominal operation. Based on the selected k factor, L_M (= 640 μH), L_R (= 45 μH), and R_O (= 8.96 Ω) for the worst case, which is the maximum load conditions having the smallest voltage gain, the resonant capacitor C_R is determined as 47 nF with $f_R = 110$ kHz and Q factor = 3.475.

Based on the value of L_R, the maximum current of the resonant inductor $I_{LR,\mathrm{PEAK}}$ and the saturated flux density of CS172 core (Changsung, sendust) $B_{\mathrm{sat,core}}$ with enough margin, the minimum turns ratio of the resonant inductor $N_{LR,\mathrm{min}}$ can be determined as

$$N_{LR,\mathrm{min}} = \frac{L_R I_{LR,\mathrm{PEAK}}}{A_{e,LR} B_{\mathrm{sat,core}}} = \frac{45 \cdot 4.62}{23.2 \cdot 0.3} = 31 \tag{6}$$

where A_e is the effective area of CS172. In addition, the maximum flux density of the resonant inductor $B_{\mathrm{max},LR}$ can be applied as follows using the $N_{LR,\mathrm{min}}$ and CS172060, which has $A_L = 43\,\mathrm{nH}/n^2$ and $\mu = 60$ in CS172 series

$$B_{\mathrm{max,LR}} = \frac{L_R I_{LR,\mathrm{PEAK}}}{A_e N_{LR}} = \frac{45 \cdot 4.62}{23.2 \cdot 33} = 0.283\,[T]. \tag{7}$$

From (6), (7), and the design example of the resonant tank in the previous paragraph, L_R with the selected inductance (=45 μH) and the core (=CS172060) can be finally confirmed.

B. Design of Main Transformer and DC Bias Current

From the design for L_M in Section III-A, $L_{M,\mathrm{nominal}}$ is determined as 640 μH based on (5), which is the same with that of the conventional converter, whereas $L_{M,\mathrm{hold-up}}$ is at 180 μH to satisfy the hold-up time. In the proposed approach, the ratio of permeability μ_{ratio} is defined between two different L_M values as follows to design the transformer with variable inductance characteristics

$$\mu_{\mathrm{ratio}} = \frac{L_{M,\mathrm{hold-}up}}{L_{M,\mathrm{nominal}}} = \frac{\mu_{\mathrm{hold-up}}}{\mu_{\mathrm{nominal}}} = 0.143. \tag{8}$$

From (8) and the core's material datasheet [24], the magnetic field H is set, which is 140 A/m in this case, for the low permeability. For the required H, I_{DC} can be calculated by Ampere's law as follows:

$$I_{\mathrm{DC}} = \frac{(l_1 + l_2)H}{N_1 + N_2} \tag{9}$$

where l_1 and l_2 are the effective lengths in the side-legs of the magnetic field. It can be seen that I_{DC} is selected based on the number of turns, core size, and field intensity, which are related to the ratio of permeability and the required L_M. We can simplify (9) to $I_{\mathrm{DC}} = l_1 H/N_1$ assuming that the flux lengths and the turns-ratios in side legs are identical.

Two side-leg windings and one center-leg winding for I_{DC} are additionally employed with the conventional main transformer's three windings on primary- and secondary-side in the proposed converter, which requires larger window area A_W. Therefore, the turn ratio on side-legs should be carefully selected to optimize the size of the main transformer. With l_1 and l_2 described in the core datasheets (=38.981 mm), N_1 and N_2 are selected as 19 in this article. The diameter of windings is selected as 0.2 mm to consider high solidity. Based on the selected diameter with the typical current density of auxiliary windings 10 A/mm^2, I_{DC} can finally be calculated as 0.3 A by considering the tolerances of l_1 and l_2 based on the core datasheet, which is $+2.764/-3.8106\%$ in the case of EF25, and one turn for N_1 and N_2. By considering A_W of the transformer, an EF25 core that has wider A_W compared to that of conventional converter's PQ2620 is selected in this article.

C. Loss Analysis

The proposed method with large L_M shows high efficiency at the nominal input voltage by reducing the conduction and turn-OFF switching loss. Hence, the relationship between L_M and the power losses is derived in this section to compare the conventional and proposed methods.

For the conduction loss, the root-mean-square (rms) current of L_M and L_R in the HB *LLC* resonant converter, which are same in both of the conventional and proposed method, can be derived as follows:

$$I_{LM,\mathrm{RMS}} = \frac{nV_O}{4\sqrt{3}L_M f_{SW}} \tag{10}$$

$$I_{LR,RMS} = \sqrt{I_{LM}^2 + \left(\frac{\pi I_O}{2\sqrt{2}n}\right)^2} = \frac{nV_O}{2\sqrt{2}}\sqrt{\frac{1}{6L_M^2 f_{SW}^2} + \frac{\pi^2}{n^4 R_O^2}}. \tag{11}$$

From (10) and (11), the conduction loss of primary switches P_{Cond} is given as

$$P_{\mathrm{Cond}} = \frac{n^2 V_O^2 R_{\mathrm{DS(ON)}}}{8}\left(\frac{1}{6L_M^2 f_{SW}^2} + \frac{\pi^2}{n^4 R_O^2}\right) \tag{12}$$

where $I_{Q1,\mathrm{RMS}}$, $I_{Q2,\mathrm{RMS}}$, and $R_{\mathrm{DS(ON)}}$ are the rms current of Q_1 and Q_2, and the ON-resistance of primary switches, respectively. Fig. 7 shows that P_{Cond} in the dotted line is inversely proportional to L_M, as derived in (12).

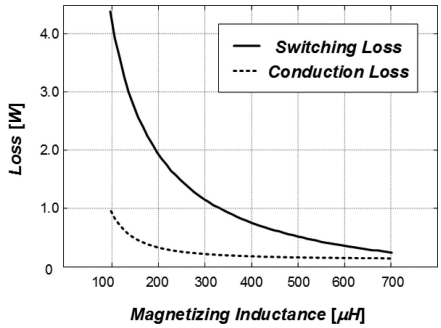


Fig. 7. Loss analysis in accordance with L_M at 390 V input and 50% load conditions. (a) Conduction loss. (b) Turn-OFF switching loss.

The turn-OFF switching loss $P_{\text{turn-off}}$ of the primary switches in the HB *LLC* resonant converter is presented as follows [25]:

$$P_{\text{turn-off}} = \frac{V_S}{3}\left[\frac{nV_O DT_S}{L_M} - C_{OSS}\frac{V_S}{T_{\text{off}}}\right]T_{\text{off}} f_{SW} \quad (13)$$

where C_{OSS} is the drain-source capacitance of the primary switches, which has the same value on the primary switches, i.e., $C_{OSS} = C_{OSS1} = C_{OSS2}$, and T_{off} is the turn-OFF time. The relationship between L_M and $P_{\text{turn-off}}$ of the primary switches is shown in the solid line in Fig. 7 under 390 V input and 50% load condition, which requires the highest efficiency in 80PLUS standards, and it shows that $P_{\text{turn-off}}$ is also inversely proportional to L_M under the same conditions. Therefore, it can be easily seen that the proposed method with large L_M can reduce the conduction and switching loss compared with the conventional *LLC* resonant converter with small L_M. The maximum value of L_M based on the ZVS operation should be determined from (5).

D. Design of Auxiliary Circuits

The voltage across C_{AUX}, $V_{C\text{AUX}}$, is important because it is proportional to the wattage of R_{AUX}, which takes the largest volume of the auxiliary circuits. To minimize $V_{C\text{AUX}}$ and additional loss of R_{AUX}, the auxiliary turns of transformer for dc bias current N_{AUX} is set as 1 turn in this article. Assuming all diodes are ideal, $V_{C\text{AUX}}$ can be expressed as

$$V_{C\text{AUX}} = \frac{N_{\text{AUX}} V_O}{N_{S2}} = 7\,[V]. \quad (14)$$

The auxiliary capacitance C_{AUX} should be large enough to supply I_{DC} during half-cycle of the switching period T_S with small variation of $V_{C\text{AUX}}$, which is set as 1% in this article, i.e., $\Delta V_{C\text{AUX}} < 0.07\text{V}$. Therefore, a capacitance of C_{AUX} can be obtained as

$$C_{\text{AUX}} > \frac{I_{\text{DC}} T_S}{2\Delta V_{C\text{AUX}}} = 19.5\,[\mu F]. \quad (15)$$

From (15), a 22 μF multilayer ceramic capacitor is applied for C_{AUX}, and R_{AUX} and its power consumption, $W_{R\text{AUX}}$, can be determined by Ohm's law as follows:

$$R_{\text{AUX}} = \frac{V_{C\text{AUX}}}{I_{\text{DC}}} = 23.33\,[\Omega] \quad (16)$$

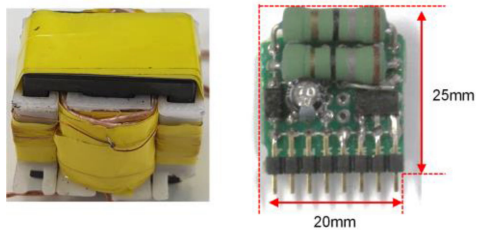


Fig. 8. Pictures of the constructed transformer and the auxiliary circuit.

$$W_{R\text{AUX}} = I_{\text{DC}}^2 R_{\text{AUX}} = 2.16\,[W]. \quad (17)$$

From (16) and (17), R_{AUX} is decided as two resistors having 47 ohm and maximum 2 W power rating with 50% stress margin.

For Q_{AUX} and D_{AUX}, the voltage and current stress should be considered. First, the maximum voltage and current stress of Q_{AUX} are $V_{C\text{AUX}}$, and I_{DC}, respectively. Therefore, the small and low cost power switch, NTF3055 (60 V/3 A/88 mΩ/SOT-223), can be selected. Secondly, the maximum voltage rating of D_{AUX} should be more than the sum of $V_{C\text{AUX}}$ and the voltage across N_{AUX}, and it can be as high as twice of the maximum $V_{C\text{AUX}}$. The maximum current rating can be same I_{DC}. Therefore, an ES1D (200 V/1 A/1.3 V/SMA) diode can be employed. The design in this section guarantees that the control circuit can be implemented in a very small footprint with low cost because the additional switch is very small in size due to the low voltage and current stress. The auxiliary circuit in the proposed converter can be implemented in 25 $\times$ 20 $\times$ 5mm, as shown in Fig. 8. The cost of R_{AUX}, C_{AUX}, D_{AUX}, and Q_{AUX} are \$ 0.107, \$0.053, \$ 0.078, and \$ 0.246, and the total cost is \$ 0.485, which is based on 1000 units from Digi-key website.

E. Comparison With Previous Studies

Although the previous hold-up time compensation circuits in [10]–[19] and proposed converter can get high efficiency through the optimal design in the nominal status, the additional components are employed, as given in Table I. There are three comparison factors to compare the power density. The position of the additional components, control method during the hold-up time, and dc offset current of the transformer. The position of additional components is crucial because it affects the power density and cost. When the additional components are located in the power path, the cost can be increased, and power density can be lower compared to the case where the components are on the signal path because high voltage and current ratings are required for the parts in power path. In [10]–[17] and [19], the power switches, diodes, passive components, or transformer windings in the power path are required. Moreover, a gate driver circuit is also employed when switches are added in [10]–[17]. The proposed method uses additional parts and windings on signal path; hence the proposed converter has better than [10]–[17] and [19]. On the other hand, [18] does not require any additional part. The second factor is the control method for the hold-up time. The previous studies in [10] and [13]–[18] should change the control scheme to the PWM or APWM. It can be a burden on the

TABLE I
COMPARISON WITH PREVIOUS STUDIES

Items			[10]	[11]	[12]	[13]	[14]-[15]	[16]-[17]	[18]	[19]	Proposed
Additional parts	Power	Diodes/switches	3	4	3	4	1	2	-	-	-
		Passive components	1	-	-	-	-	-	-	2	-
		Windings	-	2	2	2	-	-	-	1	-
	Signal	Signal diodes/switches	-	-	-	-	-	-	-	-	2
		Passive components	-	-	-	-	-	-	-	-	3
		Windings	-	-	-	-	-	-	-	-	3
Control scheme			PWM	on/off	on/off	PWM	PWM	PWM	APWM	-	on/off
DC offset current of main transformer			X	X	X	O	O	O	O	O	X

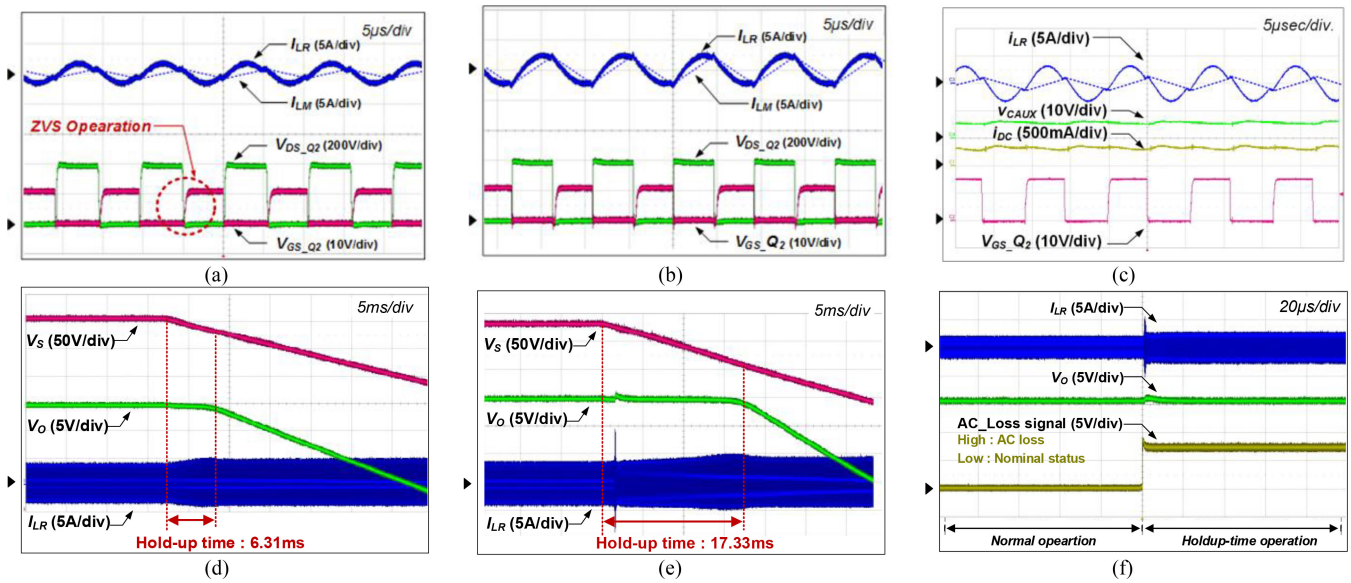


Fig. 9. Key operational waveforms. (a) Nominal operation. (b) Hold-up status. (c) Key waveforms of auxiliary circuit during hold-up status and measured hold-up time at 100% load (d) without proposed method ($L_M = 640\ \mu$H) and (e) with proposed method for the variation of L_M from 640 to 180 μH. (f) Transient response of the proposed method.

controller, especially the analog one, because the new controller for PWM or APWM should be applied. In [11] and [12], and the proposed converter, the ON/OFF control to detect ac loss is necessary, which can be easily implemented. In [19], although an additional *LC* resonant tank should be carefully designed due to the steep slope of the voltage gain, there is no additional control. Finally, the dc offset current of the main transformer directly affects the size of the main transformer. Therefore, it is also a critical factor for power density and cost. The previous circuits in [13]–[19] have the dc offset current during the hold-up time. In order to avoid the saturation of the main transformer, a large sized core is required. On the other hand, [11], [12], and the proposed method require the additional windings without dc offset current. The additional windings in the proposed method are in the signal path, but [11], [12] require thicker wires and cause significant conduction loss because of the large current of additional windings.

Consequently, [10], [18] and [19] have a strong point for each factor, respectively. However, the proposed method has overall good performance for all factors compared with other previous methods. Namely, the proposed method has a simple circuit on the signal path and simple control, which has only ON/OFF operation. Furthermore, the transformer size is slightly increased by the additional windings because there is no dc offset current. Therefore, high power density can be achieved inexpensively in the proposed method.

IV. EXPERIMENTAL RESULTS

In order to verify the performance of the proposed converter, a prototype power supply with following specification is implemented: input voltage 290–405 V, output voltage 56 V, rated power 350 W, and required hold-up time 16 ms. The list of components is given in Table II. The pictures of the transformer and the auxiliary circuit are presented in Fig. 8, and two additional wingdings N_1 and N_2 are implemented on custom bobbins for easy utilization, and they can be used as the nonisolated wire because the three isolation wire (TIW) is applied to the primary side in general use.

TABLE II
COMPONENTS LIST OF PROTOTYPE

Items		Conventional	Proposed
Main switches (Q_1 and Q_2)		IPP60R125C6. (650 V/$R_{DS(ON)}$=0.125 Ω/C_{OSS}=125 pF)	
Diodes in secondary (D_1 and D_2)		STPS30150. (150 V/I_F=30 A/V_F=0.75 V)	
Transformer (T_1)	Core	PQ2620. (A_e=119 mm^2, A_w=60 mm^2, and V_e=5470 mm^3)	EF25 x2. (A_e=104 mm^2, A_w=75 mm^2, and V_e=6040 mm^3)
		L_M=180μH.	$L_{M,nominal}$=640 μH and $L_{M,hold-up}$=180 μH.
	Wire	N_P : 0.4 mm x 2 (TIW). N_{S1} and N_{S2} : 0.1 mm x60 Litz.	
		-	N_1, N_2, and N_{AUX} : 0.2 mm.
		Turns-ratio (N_P:N_{S1}:N_{S2}) = 28:8:8.	Turns-ratio (N_P:N_{S1}:N_{S2}:N_1:N_2:N_{AUX}) = 28:8:8:19:19:1.
Resonant inductor (L_R)		L_R=45 μH, Core : CS172060, Wire :0.5 mm x2, Turns ratio: 33.	
Resonant capacitor (C_R)		47 nF/450 V.	
Resonant frequency (f_R)		110 kHz	

Fig. 9(a) shows key operational waveforms of the proposed method in nominal condition. It can be seen that the ZVS operation of the primary switches is well achieved with the designed large L_M. Moreover, the estimated current slope of L_M is gentle due to the large L_M ($= 640\,\mu$H), which decreases the conduction loss and turn-OFF loss in the primary side. Fig. 9(b) shows the hold-up time operation when $Q_{\rm AUX}$ is turned ON, and the inductance of L_M is reduced as 180 μH. The estimated slope of I_{LM} is steep compared to that of the normal operation, as shown in Fig. 9(a), so that a high voltage gain can be achieved. Moreover, as can be seen in the waveform in Fig. 9(b), the proposed converter has no concern of transformer saturation. For the auxiliary circuit operation during the hold-up time, $I_{\rm DC}$ starts to flow through the auxiliary circuit presented in Fig. 9(c).

Fig. 9(d) and (e) shows the measured hold-up time waveforms without and with the proposed method respectively under the 100% load conditions, which is the worst condition for hold-up time requirement. When a large L_M for the high efficiency, 640 μH, is applied without the change of L_M, the measured hold-up time is only 6.31 ms because the maximum voltage gain is very low, and it does not meet the given hold-up time specification. On the other hand, by applying the proposed method, the hold-up time is extended to 17.33 ms due to the reduced L_M from 640 to 180 μH and low k factor, and it satisfies the hold-up time requirement.

Fig. 9(f) shows a transient from the nominal to the hold-up operation. When ac loss signal is detected, $Q_{\rm AUX}$ is turned-ON to change L_M. In this case, the overshoot of the output voltage and resonant current can be seen because of sudden change of the voltage gain of HB *LLC* resonant converter. However, the maximum value of the output voltage is not out of the required range, which is typically maximum 2% in this application, and

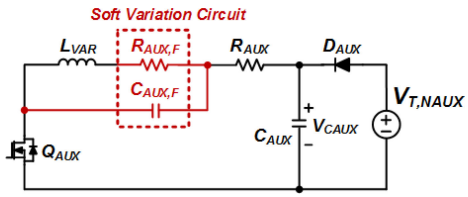


Fig. 10. Soft variation circuit during the transient. (a) Circuit diagram. (b) Mode transient waveform at 100% load conditions.

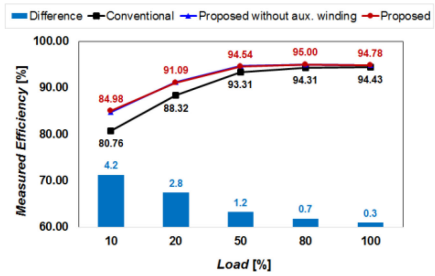


Fig. 11. Measured efficiencies of the conventional and the proposed converters under the nominal input voltage (=390 V).

the resonant current does not exceed the maximum current rating of all components. In addition, to relieve the transient stress, the voltage source of the auxiliary turn $V_{T,\rm AUX}$ should be smoothly applied to the variable inductance $L_{\rm VAR}$. A simple circuit is presented in Fig. 10(a). There are two changes; $R_{\rm AUX}$ is separated as two parts evenly as $R_{\rm AUX}$ and $R_{\rm AUX,F}$, and one capacitor $C_{\rm AUC,F}$ is added. Due to the time delay to charge $C_{\rm AUX,F}$, the voltage across $L_{\rm VAR}$ is slowly increased, so that the overshoot of V_O and I_{LR} can be reduced. To prove the presented soft variation circuit, Fig. 10(b) shows that the voltage peak of V_O and current stress of I_{LR} can be mitigated under the same conditions of Fig. 9(e).

Fig. 11 shows the measured efficiencies of the conventional and proposed converters at nominal input voltage (=390 V). The proposed converter improves the conversion efficiency over the entire load range. Especially, the light-load efficiency is significantly increased about 4.2% at 10%, as well as 2.8% increase at 20% load conditions. Moreover, the measured efficiency when $L_M = 640\,\mu$H is also presented with and without auxiliary windings, and it can be noted that there is no effect of the auxiliary windings for the efficiency at the nominal input status.

The proposed method can achieve higher efficiency with slightly increased volume and cost for the auxiliary circuit and windings compared with the conventional method. The design in this article focused on the efficiency, which the efficiency and the transformer design can be a tradeoff in the proposed method. However, the proposed converter can be guaranteed to have lower cost and higher power density compared with the previous studies as discussed.

V. CONCLUSION

In this article, a HB *LLC* resonant converter with the hold-up time extension circuit using the variable inductance is proposed.

In the nominal state, the proposed converter operates with large L_M and high k factor, so that the conduction and turn-OFF switching loss of the primary switches can be significantly reduced, and high light-load efficiency over the entire load range can be obtained. During the hold-up time, because of the small L_M and low k factor by the variable inductance, the proposed converter can achieve high voltage gain to satisfy the hold-up time requirement. Moreover, the power density is almost same with that of the conventional method, because the additional control circuit and auxiliary windings are in small size. Practical design guidelines and circuits are presented in this article, and the improved circuit for the transient mode was also discussed. Consequently, the proposed method is expected to be attractive for high power density and high-efficiency applications, such as server and network power supplies to meet the hold-up time specification. Moreover, the simple proposed method can have high availability to the other applications and all-type transformers.

REFERENCES

[1] 80Plus Program, Mar. 2012, [Online]. Available: http://www.80plus. org/index.html

[2] Energy Start Program, Washington, DC, USA, 2012, [Online]. Available: http://www.energystar. gov

[3] Climate Savers Computing Initiative, Portland , OR, USA, 2012. [Online]. Available: http://www.climatesaverscomputing.org/

[4] "Power and cooling technology symposium," IBM, Yorktown Heights, NY, USA, Oct. 1, 2008.

[5] Y. S. Lai, Z. J. Su, and W. S. Chen, "New hybrid control technique to improve light load efficiency while meeting the hold-up time requirement for two-stage server power," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4763–4775, Sep. 2014.

[6] J. H. Kim, C. E. Kim, J. K. Kim, J. B. Lee, and G. W. Moon, "Analysis on load-adaptive phase-shift control for high efficiency full-bridge LLC resonant converter under light-load conditions," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4763–4775, Jul. 2016.

[7] H. S. Kim, J. K. Kim, K. B. Park, H. W. Seong, G. W. Moon, and M. J. Youn, "On/off control of boost PFC converters to improve light-load efficiency in paralleled power supply units for servers," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1235–1242, Mar. 2014.

[8] J. W. Kim, D. Y. Kim, C. E. Kim, and G. W. Moon, "A simple switching control technique for improving light load efficiency in a phase-shifted full-bridge converter with a server power system," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1562–1566, Apr. 2014.

[9] Y. Jeong, S. Y. Cho, D. Y. Kim, C. E. Kim, and G. W. Moon, "Unexpected bi-directional operation of phase-shift full-bridge converter in parallel operation system," in *Proc. IEEE ECCE Asia Downunder*, 2013, pp. 999–1004.

[10] Y. Jang, M. M. Jovanovic, and D. L. Dillman, "Hold-up time extension circuit with integrated magnetics," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 394–400, Mar. 2006.

[11] B.-C. Kim, K.-B. Park, S.-W. Choi, and G.-W. Moon, "LLC series resonant converter with auxiliary circuit for hold-up time," in *Proc. IEEE Int. Telecommun. Energy Conf.*, Oct. 2009. pp. 1–4.

[12] B. Yang, P. Xu, and F. C. Lee, "Range winding for wide input range front end DC/DC converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2001, pp. 476–479.

[13] B. Lin, Y. Du, B. Lin, and Y. Du, "LLC resonant converter with additional secondary winding to extend hold-up time LLC resonant converter with additional secondary winding to extend hold-up time," *Elect. Power Compon. Syst.*, vol. 45, no. 6, pp. 672–680, 2017.

[14] H. Wang, Y. Chen, P. Fang, Y.-F. Liu, J. Afsharian, and Z. Yang, "An LLC converter family with auxiliary switch for hold-up mode operation," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4291–4306, Jun. 2017.

[15] I.-H. Cho, Y.-D. Kim, and G.-W. Moon, "A half-bridge LLC resonant converter adopting boost PWM control scheme for hold-up state operation," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 841–850, Feb. 2014.

[16] W. Sun, H. Wu, H. Hu, and Y. Xing, "Modified LLC resonant converter with secondary paralleled bidirectional switch for applications with hold-up time requirement," *IET Power Electron.*, vol. 10, pp. 398–404, 2017.

[17] J. -W. Kim and G. Moon, "A new LLC series resonant converter with a narrow switching frequency variation and reduced conduction losses," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4278–4287, Aug. 2014.

[18] B. -C. Kim, K. -B. Park, and G.-W. Moon, "Asymmetric PWM control scheme during hold-up time for LLC resonant converter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 7, pp. 2992–2997, Jul. 2012.

[19] D. -K. Kim, S. C. Moon, C. -O. Yeon, and G. –W. Moon, "High-efficiency LLC resonant converter with high voltage gain using an auxiliary LC resonant circuit," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 6901–6909, Oct. 2016.

[20] G. Martinez, J. M. Alonso, and R. Osorio Sanchez, "Analysis and design of a unidirectional resonant switched capacitor step-up converter for OLED lamp driving based on variable inductor," in *Proc. IEEE Ind. Appl. Soc. Annu. Meeting*, Oct. 2017, pp. 1–8.

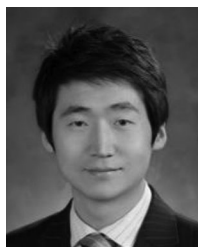
[21] Y. Hu, L. Huber, and M. Jovanovic, "Single-stage, universal-Input AC/DC LED driver with current-controlled variable PFC boost inductor," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1579–1588, Mar. 2012.

[22] V. S. Costa, M. S. Perdigao, A. S. Mendes, D. Abbes, and A. Aitouche, "Analysis and simulation of a LLC-VI resonant converter for solar applications," in *Proc. 52nd Int. Univ. Power Eng. Conf.*, Jan. 2017, pp. 1–6.

[23] J. M. Alonso, M. Perdigao, M. A. Dalla Costa, S. Zhang, and Y. Wang, "Variable inductor modeling revisited: The analytical approach," in *Proc. IEEE Energy Conves. Congr. Expo.*, Oct. 2017.

[24] Ferroxcube Corp., Sao Paulo, Brazil. 3C90 material data sheet.

[25] J. -Y. Lee, Y. -S. Jeong, and B.-M. Han, "An isolated DC/DC converter using high-frequency unregulated LLC resonant converter for fuel cell applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2926–2934, Jul. 2011.



Yeonho Jeong (Member, IEEE) received the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2014 and 2018, respectively.

From 2008 to 2015, he was a Research and Development Engineer with Power Advanced Group in Samsung Electro-Mechanics Co. Ltd., Suwon, South Korea. From 2015 to 2018, he was a Senior Research Engineer for developing server power systems in Solu-M, Yong-In, South Korea. From 2018, he was a Postdoctoral Fellow with the Department of Electical/Mechanical Engineering, University of Colorado, Denver, CO, USA. His main research interests include dc/dc converters, ac/dc power-factor-correction converters, the sever power supplies, hybrid power systems and energy managements for transportation, and digital control approach for power converters.

Min-Su Lee (Student Member, IEEE) received the B.S. degree in electrical engineering, in 2017, from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, where he is currently working toward the Ph.D. degree.

His research interests include high-efficiency dc/dc converter topology, electric vehicle charger system, server power system, converter topologies, and magnetics.

Jae-Do Park (Senior Member, IEEE) received the Ph.D. degree from the Pennsylvania State University, University Park, State College, PA, USA in 2007.

He is currently an Associate Professor in electrical engineering with the University of Colorado, Denver, CO, USA. Prior to his arrival at the University of Colorado Denver, he worked for Pentadyne Power Corporation in California as the Manager of Software and Controls, where he took charge of control algorithm design and firmware development for the high-speed flywheel energy storage system. His research interests include energy system applications such as renewable energy sources, energy harvesting, energy storage, and dc microgrids.

Dr. Park research has been sponsored by the National Science Foundation (NSF), Office of Naval Research (ONR), and Defense Advanced Research Projects Agency (DARPA), including an NSF CAREER Award in 2016.

Jae-Kuk Kim (Member, IEEE) received the B.S. degree in the electrical engineering from Inha University, Incheon, South Korea, in 2004, and the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2007 and 2011, respectively.

From 2011 to 2015, he was a Senior Engineer in Samsung Electro-Mechanics, Suwon, South Korea. He is currently an Assistant Professor with the Department of Electrical Engineering, Inha University, Incheon, South Korea. His research interests include converter topology designs, soft-switching techniques, display driving systems, server power systems, and battery charger systems.

Ronald A. L. Rorrer, Jr. (Member, IEEE) was born in Heidelberg, West Germany, in 1962. He received the B.S., M.S., and Ph.D. degrees in mechanical engineering from Virginia Polytechnic Institute and State University, Blacksburg, VA, USA in 1984, 1985 and 1991.

From 1985 to 1986, he was a Precision Mechanical Design Engineer with Martin Marietta, Orlando, FL, USA. From 1992 to 1997, he was an Advanced Materials Project Leader with the Gates Rubber Company, Denver, CO, USA. Since 1997, he has been a Professor of mechanical engineering with the University of Colorado, Denver, CO, USA. His research interests include tribology, composite materials and alternative power systems.