Development and Verification Test of the 6.6-kV 200-kVA Transformerless SDBC-Based STATCOM Using SiC-MOSFET Modules

Laxman Maharjan, *Senior Member, IEEE*, Toshihisa Tajyuta, *Member, IEEE*, Koji Maruyama, Akio Suzuki, and Akio Toba, *Senior Member, IEEE*

***Abstract*—This article discusses development and verification test results of the 6.6-kV 200-kVA transformerless static synchronous compensator (STATCOM). This STATCOM is characterized by the use of a modular multilevel single-delta bridge-cell (SDBC) converter and silicon carbide metal-oxide-semiconductor field-effect transistor (MOSFET) modules. The article discusses a control method for the 6.6-kV system with focus on dc-capacitor voltage control. The voltage control presented in this article is different from the ones presented earlier. It consists of intercluster balancing control and intracluster balancing control. The former, also known as cluster balancing control, eliminates the requirement of the separate overall dc-voltage control present in conventional methods, whereas the latter, also known as individual balancing control, is replaced with a new technique based on the control of a dead time of each bridge cell. The article makes a detailed description of the latter. Experimental results obtained from the 6.6-kV 200-kVA verification test equipment validate the effectiveness of the control method. Moreover, successful test results confirm the efficacy of the system for grid-voltage regulation and load compensation.**

***Index Terms*—DC-capacitor voltage control, grid-voltage regulation, load compensation, modular multilevel single-delta bridge-cell (SDBC) converter, static synchronous compensator (STATCOM).**

I. Introduction

In RECENT years, the family of modular multilevel cascade converters has gained significant interest for grid applications [1], [3]–[12], [14]–[25]. Modular topology of these converters allows direct connection to medium- and high-voltage grids without using step-up line-frequency transformers. Fundamentally different circuit configurations or members exist in the family [15]. As for static synchronous compensator (STATCOM) applications, however, the most investigated configurations are as follows:

1) single-star bridge-cell (SSBC) converters [1];
2) single-delta bridge-cell (SDBC) converters [5], [16].

The basic circuit unit of both SSBC and SDBC converters is a single-phase H-bridge converter equipped with a dc capacitor, which is referred to as a bridge cell. For the same voltage rating, the SSBC converter, or shortly, SSBC requires fewer bridge cells than the SDBC converter, or shortly, SDBC. Hence, the SSBC is the first choice as long as the STATCOM is installed for controlling only the positive-sequence reactive power. Many STATCOMs for voltage regulation in utility applications fall into this category. However, when a STATCOM is required to control both positive-sequence and negative-sequence reactive powers, the SDBC is preferred over the SSBC. Some STATCOMs for flicker compensation in industry applications, for example, electric arc furnaces [2], [13], fall into this category.

Fuji Electric has developed the 6.6-kV 200-kVA transformerless STATCOM based on the SDBC. The STATCOM has been designed, constructed, and tested as part of a national project in Japan to demonstrate the feasibility of high-efficiency medium-voltage transformerless grid converters using silicon carbide (SiC) devices. The aim of the article is to develop and demonstrate the 6.6-kV system with focus on dc-capacitor voltage control.

The dc-capacitor voltage control presented in this article consists of intercluster balancing control and intracluster balancing control. The intercluster balancing control, also known as cluster balancing control, is different in structure from conventional ones [9], [16], [20], [25]. This intercluster balancing control allows a line frequency zero-sequence current to circulate in the delta loop of the converter. In addition, it allows an exchange of an active power with the grid. This capability results in eliminating the requirement of the separate overall dc-voltage control. The intracluster balancing control, also known as individual balancing control, is different in principle from conventional ones [9]–[11], [20], [25]. It is characterized by a new technique based on the control of a dead time of each bridge cell [23]. This article provides a detailed explanation of the technique.

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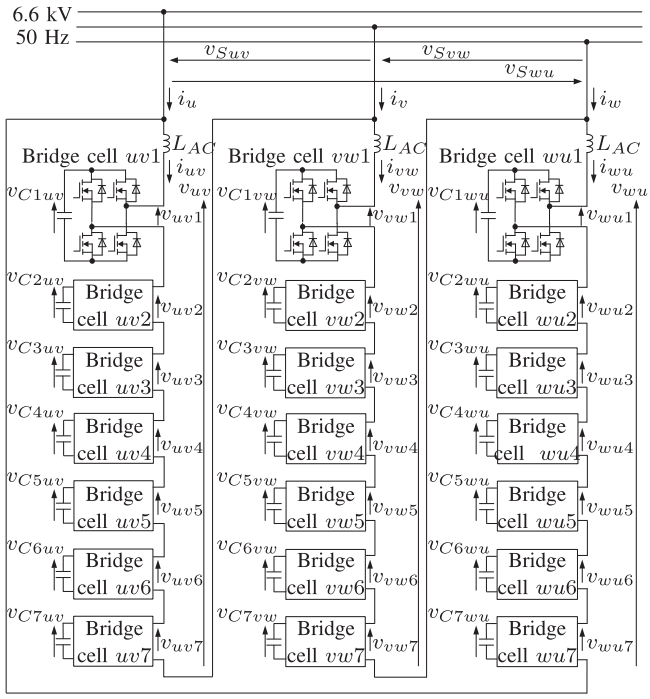

Fig. 1. Circuit configuration of the 6.6-kV 200-kVA transformerless STATCOM based on the SDBC converter using SiC-MOSFET modules.

TABLE I
CIRCUIT PARAMETERS OF THE 6.6-KV SYSTEM

Nominal line-to-line rms voltage		V_S	6.6 kV
Capacity rating		S	200 kVA
Line frequency		f	50 Hz
Carrier frequency		f_C	5 kHz
Equivalent carrier frequency			70 kHz
AC inductor		L_{AC}	104 mH (5%)[a]
Number of bridge cells per phase		N	7
Bridge cell	DC capacitor	C	100 μF
	Unit capacitance constant	H	15 ms
	Nominal dc voltage	V_C	1.7 kV
	Nominal output voltage		942 V
	Nominal output current		10 A
	Capacity rating		9.5 kVA

[a]Calculated on a three phase, 6.6-kV, 200-kVA, and 50-Hz base.

Experimental results based on the 6.6-kV system are presented to validate the dc-capacitor voltage control. Moreover, successful test results demonstrate that the system has the capability of controlling both positive-sequence and negative-sequence reactive powers in utility and industry applications.

II. 6.6-kV 200-kVA STATCOM

A. Circuit Configuration

Fig. 1 shows the circuit configuration of the 6.6-kV 200-kVA STATCOM based on the SDBC converter. Each phase-to-phase converter consists of a series connection of an ac inductor L_{AC} and a cluster of seven series-connected bridge cells. Thus, the three phase-to-phase converters result in being connected in delta. This configuration allows a zero-sequence current to be circulated in the delta loop, thus enabling the control of negative-sequence reactive power [7], [15]–[24]. The STATCOM is connected to the 6.6-kV grid without using a line-frequency transformer.

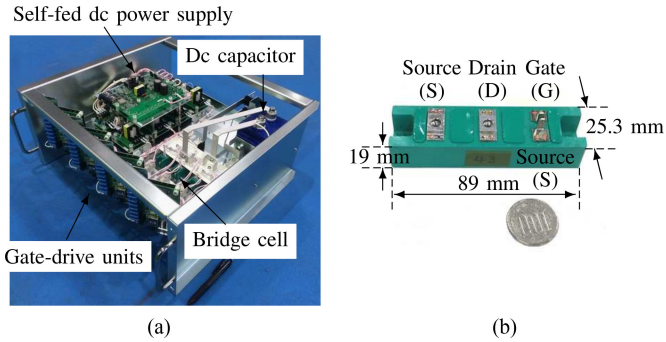

Fig. 2. General view of a power converter unit in the 6.6-kV system. (a) the power converter unit, and (b) the 3.3-kV SiC-MOSFET module used in a bridge-cell arm of the power converter unit.

B. Circuit Parameters

Table I shows the circuit parameters of the 6.6-kV 200-kVA system. It consists of 21 bridge cells, each of which is rated at 942 V and 9.5 kVA. Each bridge cell is controlled by phase-shifted unipolar sinusoidal pulsewidth modulation (PWM) with a carrier frequency f_C of 5 kHz. The equivalent carrier frequency is 70 kHz. As a result, the SDBC converter has a 15-level phase-to-phase voltage at the ac side. The nominal dc voltage V_C is 1.7 kV. The dc capacitors and ac inductors are rated at 100 μF and 104 mH, respectively.

C. Power Converter Unit

Fig. 2 shows a general view of one of the 21 power converter units. Each unit consists of:

1) a bridge cell;
2) a self-fed dc power supply board; and
3) four gate-drive units.

The bridge cell employs four 3.3-kV SiC-MOSFET (metal-oxide-semiconductor field-effect transistor) modules from Fuji Electric. The self-fed dc power supply board supplies electric power from the dc terminals of each bridge cell to four gate-drive units. The board also includes a dc-voltage detection circuit.

Although silicon (Si) devices with lower switching frequencies are generally used in modular multilevel cascade converters, the use of high-voltage SiC devices enables to reach a higher grid voltage with a lower number of bridge cells per phase. Since the SiC devices can be switched at high frequencies, the harmonic performance is not sacrificed. Moreover, the lower switching loss of SiC devices allows to achieve a higher efficiency. The lower number of bridge cells also results in lower complexity (for example, in terms of communication), higher reliability, and potentially lower cost of the system.

D. Verification Test Equipment

Fig. 3 shows a general view of the verification test equipment rated at 6.6 kV and 200 kVA. Each phase-to-phase cabinet

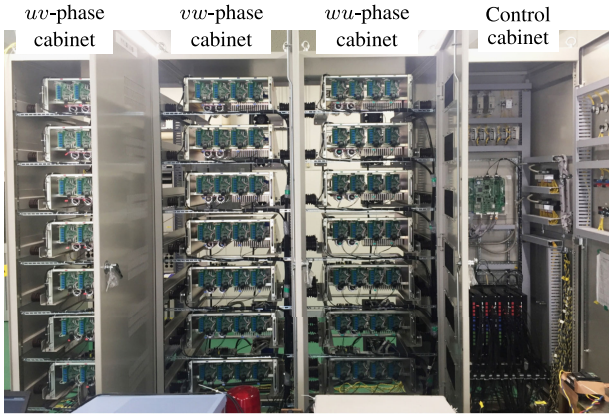

Fig. 3. General view of the 6.6-kV 200-kVA verification test equipment.

is mounted with the seven power converter units. The control cabinet contains control hardware and sequence circuits.

The control system of the verification test equipment is comprised of one main (master) control board and four local (slave) control boards. The main control board consists of a digital signal processor (DSP), a microcontroller, and multiple field-programmable gate arrays (FPGAs). Most of the control programs including a current control, a grid-voltage control, and the intercluster balancing control as well as the sequence programs are implemented on it. The local control boards consist of a DSP and multiple FPGAs each. The proposed intracluster balancing control and the PWM are implemented on them. Each of the first three local control boards controls a group of six power converter units containing two from each cluster, while the fourth local control board controls a group of the remaining three power converter units. Assigning one local control board to a small group of power converter units containing one or two from each cluster in this way enables easy extension of the system for building a higher voltage system.

In order to ensure isolation between the main circuit and the control circuit, optical communication is used between the local control boards and the dc-voltage detection circuits of the power converter units. Furthermore, the local control boards send the PWM signals to the gate-drive units of the power converter units using optical fiber.

III. Control System

Fig. 4 shows the block diagram of the control system of the verification test equipment. The control system is divided into:

1) current control;
2) grid-voltage control;
3) dc-capacitor voltage control.

A. Current Control

The control system employs a conventional ac current control. The output signals from the current control are the following three converter voltage references:

$$v^*_{uv} = K_1(i^*_{uv} - i_{uv}) + v_{Suv} \tag{1}$$

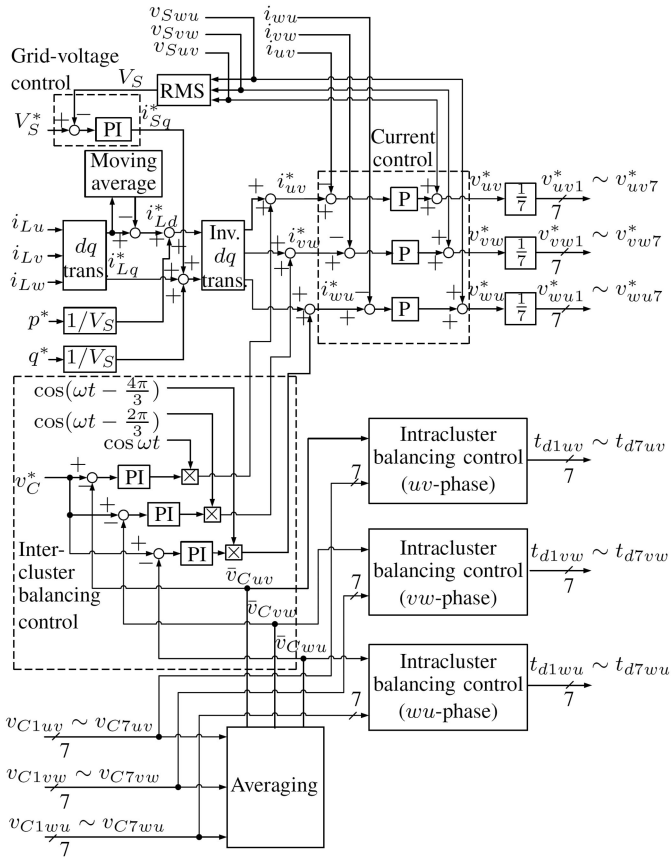

Fig. 4. Block diagram of the control system. Note that $\cos\omega t$ is synchronized to v_{Suv} in Fig. 1.

$$v^*_{vw} = K_1(i^*_{vw} - i_{vw}) + v_{Svw} \tag{2}$$

$$v^*_{wu} = K_1(i^*_{wu} - i_{wu}) + v_{Swu} \tag{3}$$

where K_1 is the gain of proportional (P) controllers, and i^*_{uv}, i^*_{vw}, and i^*_{wu} are the converter phase current references. Here, the voltage and current signals correspond to those in Fig. 1.

B. Grid-Voltage Control

The grid-voltage control regulates the grid voltage V_S to its nominal voltage. It is based on a proportional-integral (PI) controller. The output signal from this controller is an instantaneous reactive-current reference given by

$$i^*_{Sq} = K_2(V^*_S - V_S) + \frac{K_2}{T}\int (V^*_S - V_S) \tag{4}$$

where K_2 is a proportional gain and T is an integral time constant of the PI controller, and V^*_S is the grid-voltage reference. The control has the function of adjusting three-phase reactive currents drawn from the grid to regulate the grid voltage to V^*_S.

C. DC-Capacitor Voltage Control

In contrast to a two-level voltage-source converter, a SDBC-based STATCOM has no common dc capacitor, but multiple floating dc capacitors, as shown in Fig. 1. The dc-capacitor voltage control is, therefore, indispensable for stable operation.

The dc-capacitor voltage control included in the control system in Fig. 4 is different from the ones presented earlier, and is comprised of intercluster balancing control and intracluster balancing control.

The intercluster balancing control regulates the mean dc voltages in the uv-, vw-, and wu-phase clusters ($\bar{v}_{Cuv}$, $\bar{v}_{Cvw,}$ and $\bar{v}_{Cwu}$) at the dc voltage command v_C^*. Here, $\bar{v}_{Cuv}$, $\bar{v}_{Cvw}$, and $\bar{v}_{Cwu}$ are given by

$$\bar{v}_{Cuv} = \frac{1}{7}\sum_{j=1}^{7} v_{Cjuv} \tag{5}$$

$$\bar{v}_{Cvw} = \frac{1}{7}\sum_{j=1}^{7} v_{Cjvw} \tag{6}$$

$$\bar{v}_{Cwu} = \frac{1}{7}\sum_{j=1}^{7} v_{Cjwu} \tag{7}$$

The intercluster balancing control presented in this article combines the functions of cluster balancing control and overall dc-voltage control of conventional dc-capacitor voltage control methods [9], [16], [20], [25]. Besides being able to circulate a line frequency zero-sequence current i_Z in the delta loop of the converter, it is capable of exchanging an active power with the grid, thus eliminating the requirement of the separate overall dc-voltage control. The circulating current is given by

$$i_Z = \frac{1}{3}(i_{uv} + i_{vw} + i_{wu}) \tag{8}$$

The intracluster balancing control, on the other hand, regulates the dc voltages of the bridge cells in a cluster (e.g., $v_{C1uv} \sim v_{C7uv}$ in uv-phase cluster) at the mean dc voltage in the cluster ($\bar{v}_{Cuv}$ in this case). This article presents a new technique for intracluster balancing that is based on the control of a dead time of each bridge cell [23]. It is explained in detail in the following section.

IV. Intracluster Balancing Control

Conventional methods of intracluster balancing have been reported in literatures [9], [10], [16], [25]. They all have one major problem. They require sign information of the converter phase currents in order to produce balancing voltage references which are in phase or 180° out of phase of the converter phase currents, and as such, are sensitive to current detection error. As a result, they may not work properly at no-load and light-load conditions. Additional measures may be required to maintain the balancing at no-load and light-load conditions. Furthermore, it is reported in [18] that, when using a phase-shifted PWM, the interaction between voltage and current harmonics results in an uneven power distribution among the bridge cells. This may lead to drifting of the dc-capacitor voltages, again especially at no-load and light-load conditions where the conventional method of intracluster balancing is not effective.

In contrast, the intracluster balancing control presented in this article, which is based on the control a dead time of each bridge cell in a cluster, does not require sign information of the converter phase currents. As such, it is not sensitive to current detection error and works excellently even at no-load and light-load conditions.

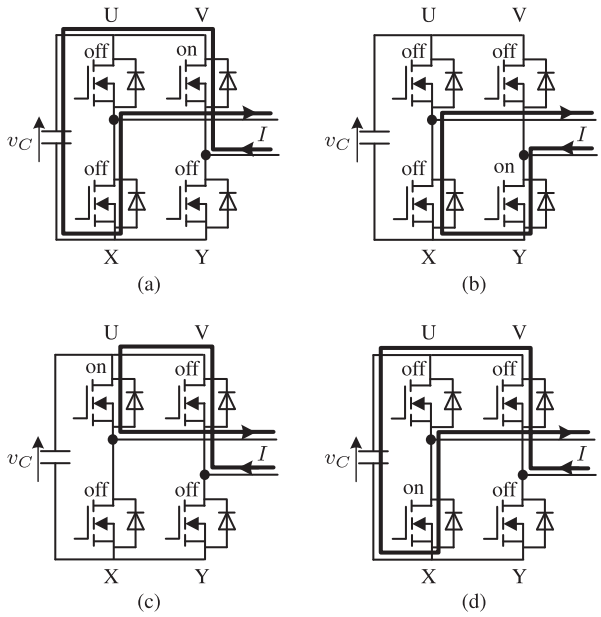

Fig. 5. Four modes of operation that occur in dead times of a bridge cell. (a) Mode A. (b) Mode B. (c) Mode C. (d) Mode D.

A. Basic Principle

The basic principle of the intracluster balancing control presented here is based on the fact that increasing the dead time of a bridge cell results in rise in dc-capacitor voltage of the bridge cell. Fig. 5 shows four modes of operation that occur during dead times of a bridge cell: (a) mode A, (b) mode B, (c) mode C, and (d) mode D. Modes A and B occur during the dead time of leg UX, whereas modes C and D occur during the dead time of leg VY. For a current direction from leg VY to leg UX,

1) modes A and D charge the dc capacitor, whereas
2) modes B and C are zero-voltage modes and do not charge or discharge the dc capacitor.

Fig. 6 shows four main modes of operation each of which follow a dead time: (a) mode 1, (b) mode 2, (c) mode 3, and (d) mode 4. For a current direction from leg VY to leg UX:

1) mode 1 charges the dc capacitor;
2) mode 2 discharges the dc capacitor; and
3) modes 3 and 4 are zero-voltage modes and do not charge or discharge the dc capacitor.

When the dead time of a bridge cell is increased, the durations of dead-time modes A through D of Fig. 5 are elongated, whereas the durations of main modes 1 through 4 of Fig. 6 are shortened.

Table II summarizes the effects of elongated dead-time modes and their shortened subsequent main modes on dc-capacitor voltage. It is seen that the effect, as compared to the one without dead-time control, is either rise or no change in dc-capacitor voltage. However, when all the dead-time modes and their subsequent main modes are considered, the net effect is always rise in dc-capacitor voltage. That means, the dc-capacitor voltage of a bridge cell rises with increase in dead time of the bridge cell.

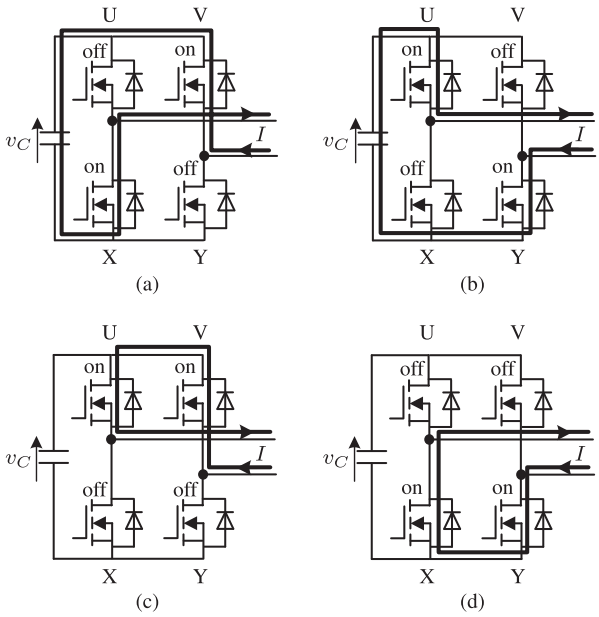

Fig. 6. Four main modes of operation of a bridge cell. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

TABLE II
EFFECTS OF ELONGATED DEAD-TIME MODES AND THEIR SHORTENED SUBSEQUENT MAIN MODES ON DC-CAPACITOR VOLTAGE

Dead-time mode[a]	Subsequent main mode[a]	Effect in dc-capacitor voltage[b]
Mode A (Charge)	Mode 1 (Charge)	No change
	Mode 3 (Zero-voltage)	Rise
Mode B (Zero-voltage)	Mode 2 (Discharge)	Rise
	Mode 4 (Zero-voltage)	No change
Mode C (Zero-voltage)	Mode 2 (Discharge)	Rise
	Mode 3 (Zero-voltage)	No change
Mode D (Charge)	Mode 1 (Charge)	No change
	Mode 4 (Zero-voltage)	Rise

[a]Indications in () assume current direction from leg VY to leg UX.
[b]Effect is as compared to the one without dead-time control.

For opposite current direction, the indications in parenthesis (charge, discharge, or zero voltage) as well as the effect in dc-capacitor voltage (rise or no change) for a set of a dead-time mode and its subsequent main mode in Table II may vary. However, for an increase in dead time, the net effect of all the sets of dead-time modes and their subsequent main modes will always be rise in dc-capacitor voltage. Note that the rise in dc-capacitor voltage here is as compared to the one without the control of dead time.

B. Balancing Mechanism

If the dc-capacitor voltage of a bridge cell in a cluster is, for example, lower than the mean dc voltage of the cluster, the dead time of the bridge cell is increased, which in turn increases the dc-capacitor voltage. On the other hand, if the dc-capacitor voltage of the bridge cell is higher than the mean dc voltage of the cluster, the dead time of the bridge cell is decreased, which in turn decreases the dc-capacitor voltage. In this way, the dc-capacitor voltage of a bridge cell is increased or decreased by increasing or decreasing the dead time of the bridge cell, resulting in the balancing of dc-capacitor voltages of the bridge cells within a cluster.

However, there is one major limitation. The dead time of a bridge cell cannot be less than zero. In fact, in practical application, the dead time is always some positive value. The balancing mechanism under this limitation is explained below, taking uv-phase cluster in Fig. 1 as an example.

Suppose the dc-capacitor voltage of bridge cell $uv1$ in uv-phase cluster (v_{C1uv}) is higher than the mean dc voltage of the cluster, $\bar{v}_{Cuv}$. The aforementioned limitation means that if the dead time of the bridge cell (t_{d1uv}) is already at its minimum value, $t_{d(\min)}$, it is not possible to decrease it further. However, in such case, there will at least be one bridge cell in the cluster with dc-capacitor voltage lower than $\bar{v}_{Cuv}$. Suppose there is only one bridge cell, which has a lower dc-capacitor voltage than $\bar{v}_{Cuv}$ and it is bridge cell $uv2$. The intracluster balancing control will then increase the dead time t_{d2uv} of the bridge cell to increase its dc-capacitor voltage, v_{C2uv}. This will result in a higher mean dc voltage of the cluster. The intercluster balancing control will then act immediately to bring down $\bar{v}_{Cuv}$ to the dc voltage command v_C^*. This will, in effect, bring down all the dc-capacitor voltages ($v_{C1uv} \sim v_{C7uv}$) in the cluster. The result is that v_{C1uv} will now be less higher than $\bar{v}_{Cuv}$. At the same time, other dc-capacitor voltages ($v_{C3uv} \sim v_{C7uv}$ and possibly v_{C2uv}) in the cluster will be lower than $\bar{v}_{Cuv}$. The intracluster balancing control will then increase the dead times ($t_{d2uv} \sim t_{d7uv}$) of these bridge cells to increase their dc-capacitor voltages ($v_{C2uv} \sim v_{C7uv}$). The process is repeated until all the dc-capacitor voltages in the uv-phase cluster are balanced at $\bar{v}_{Cuv}$, which itself is regulated at v_C^*.

From the abovementioned discussion, it is clear that the presented intracluster balancing control is dependent on the functioning of the intercluster balancing control and may exchange an amount of active power with the grid to perform the balancing function. This is one big difference with the conventional method, where the intracluster balancing control exchanges no active power with the grid and can perform the balancing function within a cluster independent of the intercluster balancing control.

C. Block Diagram

Fig. 7 shows the block diagram of intracluster balancing control, taking bridge cell $uv1$ of uv-phase cluster as an example. It is clear from Fig. 7 that the presented method, as explained earlier, requires no sign information of the converter phase current which is in contrast to conventional methods. Moreover, the output of the control is the dead time of the bridge cell. In the case of conventional methods, the output of the control is a balancing voltage reference which is added to the bridge-cell

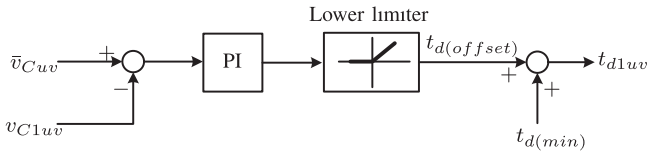

Fig. 7. Block diagram of the intracluster balancing control, taking bridge cell $uv1$ of uv-phase cluster as an example.

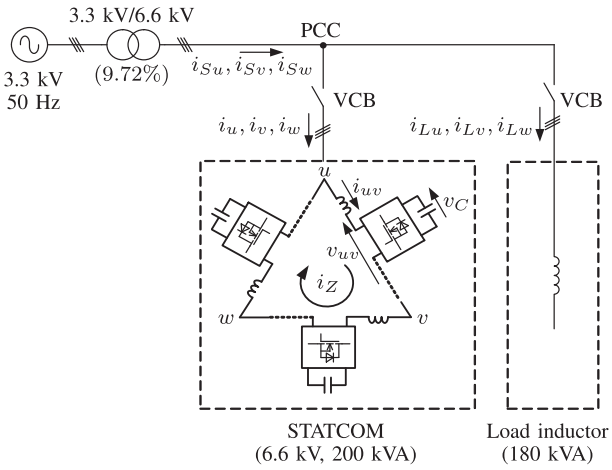

Fig. 8. Test circuit of the 6.6-kV STATCOM.

voltage reference. Detailed explanation of conventional methods together with block diagrams could be found in [9], [10], and [16].

For a particular bridge cell, the PI control calculates the dead-time offset $t_{d(\text{offset})}$ based on the difference between the dc voltage in that cell (v_{C1uv}) and the mean dc-voltage of the cluster which the cell belongs to ($\bar{v}_{Cuv}$). The dead-time offset is then added to the minimum dead-time $t_{d(\min)}$ to generate the dead time t_{d1uv} to be used in that bridge cell. Note that the minimum value of $t_{d(\text{offset})}$ is limited to zero using a lower limiter, because t_{d1uv} is not supposed to be less than $t_{d(\min)}$.

D. Influence on Converter Performance

The dc-voltage imbalance among bridge cells within a cluster is caused mainly by the differences in power losses among the bridge cells. Therefore, a narrow variation in dead time is sufficient to achieve the dc-voltage balancing within the cluster. Consequently, the influence on the converter performance, for example in terms of voltage and current total harmonic distortion (THD), is not significant.

V. Test Circuit

Fig. 8 shows the test circuit used to verify the performance of the 6.6-kV STATCOM. Since the industrial system voltage at the test site was 3.3 kV, a 50-Hz transformer was used to step up the voltage to 6.6 kV. The leakage impedance of the transformer was 9.72%.[1] It can be considered as the background impedance upstream of the 6.6-kV STATCOM, neglecting the real background impedance upstream of the primary of the 50-Hz transformer.

The verification test equipment was connected to the test grid at the point of common coupling (PCC). A three-phase inductor rated at 180 kVA was also connected at the PCC. A vacuum circuit breaker made it possible to switch ON or OFF the inductor during a real test for load compensation.

[1]Calculated on a three phase, 6.6 kV, 200 kVA, and 50-Hz base.

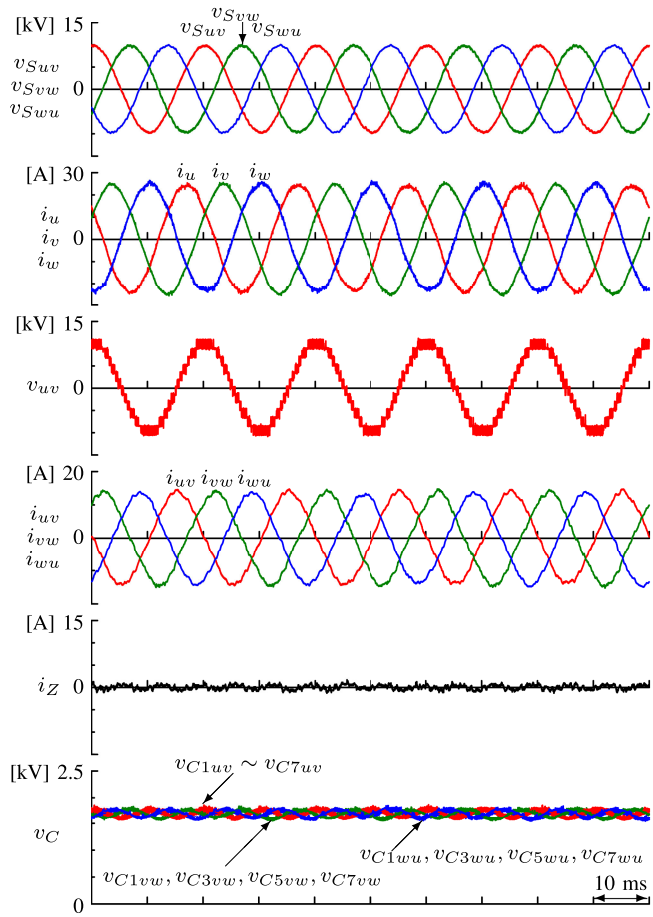

Fig. 9. Experimental waveforms when the rated positive-sequence reactive power of 200 kvar was controlled in capacitive operation.

VI. Test Results

Figs. 9 to 14 show test results obtained from the 6.6-kV 200-kVA STATCOM. The voltage and current waveforms correspond to those in Figs. 1 and 8.

A. Steady-State Performance

Fig. 9 shows experimental waveforms when the rated positive-sequence reactive power of 200 kvar was controlled in capacitive operation. For this test, the grid-voltage control was disabled, and the load inductor was also switched off. The instantaneous active- and reactive-power commands, p^* and q^*, were given as the input commands in Fig. 4. The waveforms of i_u, i_v and i_w lead those of v_{Suv}, v_{Svw} and v_{Swu} by 60°, thus indicating capacitive operation. The THD value of each line current is as low as 2.5%. The waveform of v_{uv} exhibits a multilevel PWM

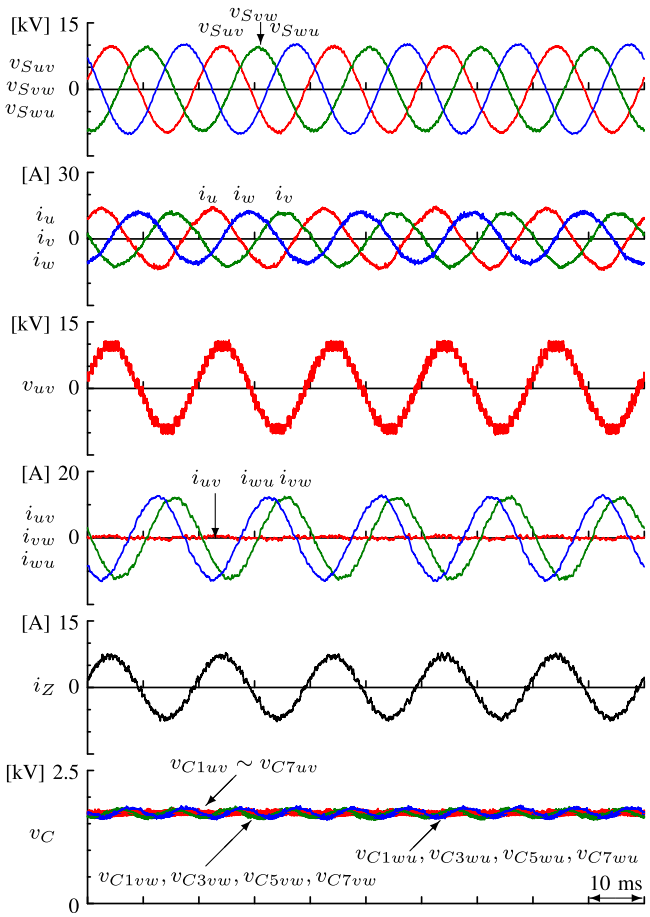

Fig. 10. Experimental waveforms when a negative-sequence reactive power of 100 kvar was controlled.

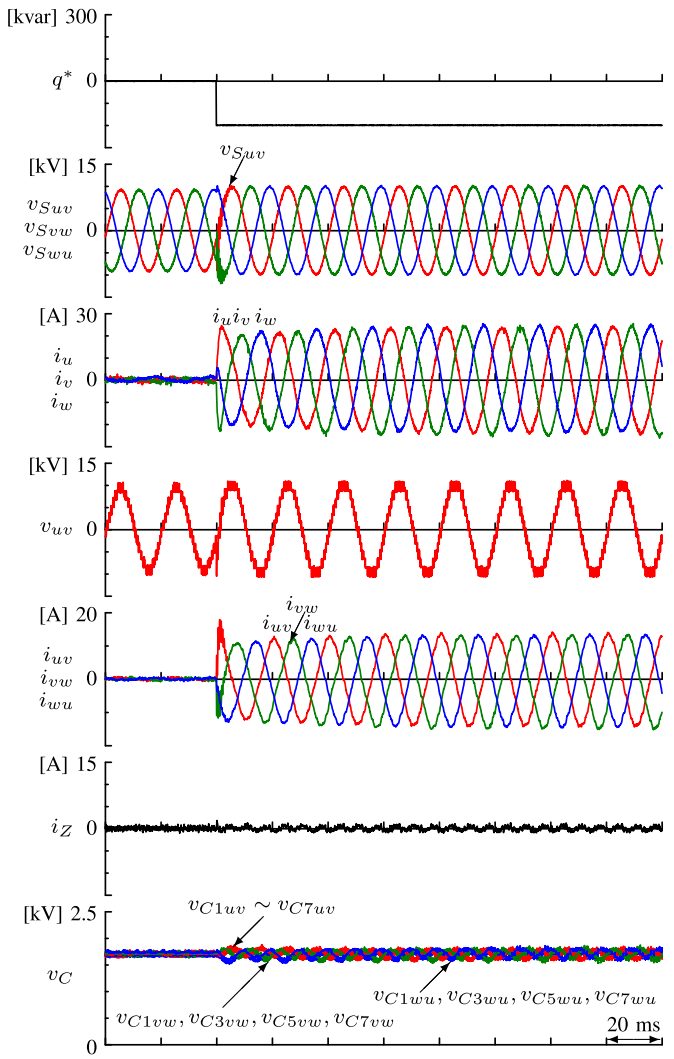

Fig. 11. Experimental waveforms with a step-change in positive-sequence reactive power from 0 to 200 kvar in capacitive operation.

waveform with a voltage step of 1.7 kV. The dc-voltage control succeeded in regulating the 21 dc-capacitor voltages to 1.7 kV without any steady-state error.

Fig. 10 shows experimental waveforms when a negative-sequence reactive power of 100 kvar was controlled. Although the waveforms of i_u, i_v and i_w have a phase difference of 120°, they come, not in order of i_u, i_v, and i_w, but in order of i_u, i_w, and i_v. This fact results in drawing of the negative-sequence reactive power from the grid. The waveform of i_Z looks a single-phase 50-Hz sinusoidal one with 5.5 A in rms. This zero-sequence current was circulating through the delta loop of the SDBC converter, which made a significant contribution to capacitor-voltage balancing among the three clusters in negative-sequence reactive-power control. The uv-phase cluster dc-capacitor voltages ($v_{C1uv} \sim v_{C7uv}$) contained no 100-Hz ripple because the waveform of i_{uv} concludes that no current flowed in the uv-phase cluster during this experiment.

B. Transient-State Performance

Fig. 11 shows experimental waveforms with a step change in positive-sequence reactive-power command from 0 to 200 kvar in capacitive operation. Due to the excellent current control performance that relies on an equivalent carrier frequency of 70 kHz, the STATCOM experienced an overcurrent of only 120% of the rated current in the transient state. The waveforms of dc-capacitor voltages showed that the dc voltage fluctuation was limited to ±10% even in the transient state. Since the dc capacitors were designed to have a dc voltage ripple of ±5% at the rated power in the steady state, the experimental waveforms shown in Fig. 11 conclude that the STATCOM has satisfactory transient-state performance.

C. Performance of Intracluster Balancing Control

Fig. 12 shows experimental waveforms demonstrating the performance of intracluster balancing control. It plays a part in achieving capacitor-voltage balancing inside each cluster. Therefore, attention was paid to only the dc-capacitor voltages of the uv-phase cluster in Fig. 12. Initially, the STATCOM in inductive operation was controlling a positive-sequence reactive power of 100 kvar with the intracluster balancing control enabled. At the time of 1.2 s, the intracluster balancing control was intentionally disabled. This was leading the dc capacitor

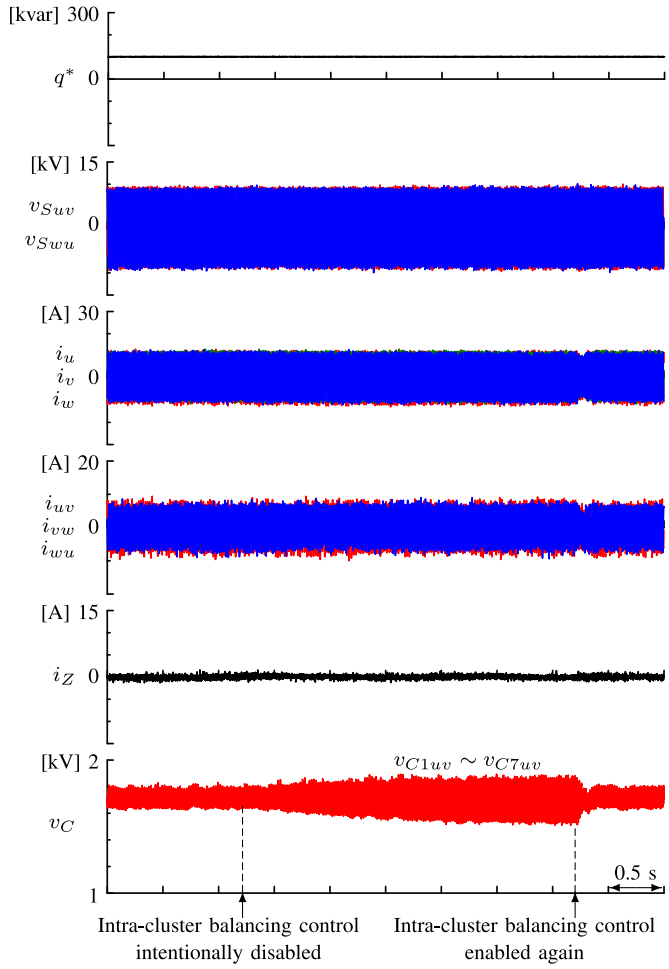

Fig. 12. Experimental waveforms when the intracluster balancing control was intentionally disabled and enabled again during the control of a positive-sequence reactive power of 100 kvar in inductive operation.

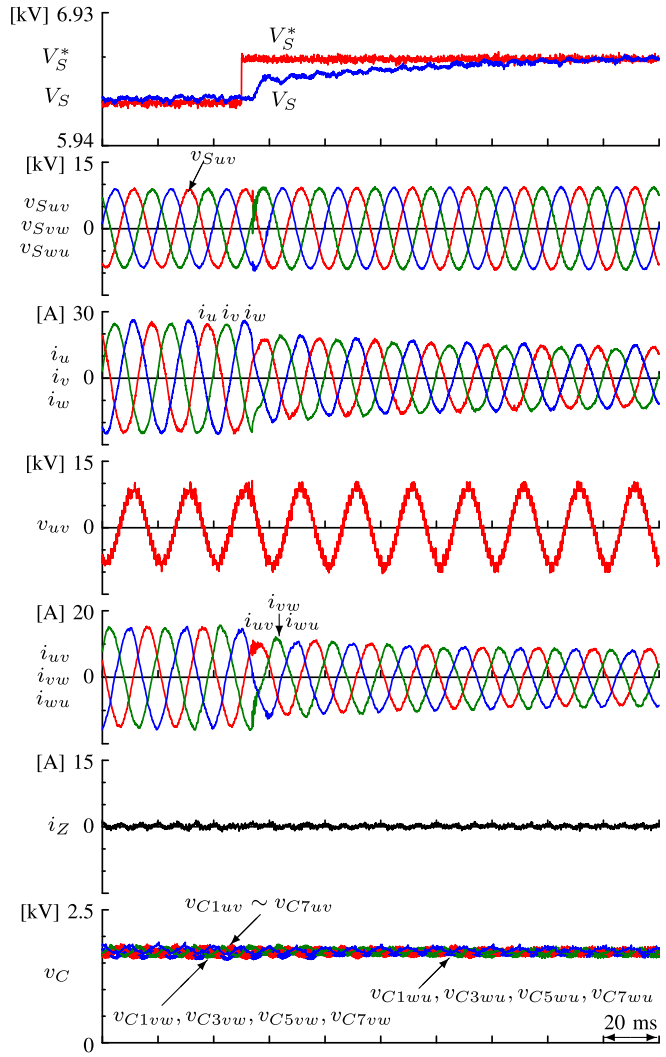

Fig. 13. Experimental waveforms with a step-change in grid-voltage command from 95% to 100%.

voltages in the uv-phase cluster to deviate from its reference of 1.7 kV. In other words, the dc-capacitor voltage fluctuation in peak-to-peak was being increased from $\pm 5\%$ to $\pm 10\%$. At the time of 4.2 s, the intracluster balancing control was enabled again. Immediately, it started regulating the seven dc-capacitor voltages to 1.7 kV. The waveforms of Fig. 12 conclude that the proposed intracluster balancing control, that is characterized by the control of a dead time of each bridge cell, is effective in capacitor-voltage balancing in each of the three clusters.

The waveforms of i_u, i_v, i_w as well as that of i_{uv}, i_{vw}, and i_{wu} in Fig. 12 showed a small glitch when the intracluster balancing control was enabled again. As explained earlier, the proposed method, in contrast to the conventional method, may cause an exchange of active power with the grid in order to achieve the balancing of dc-capacitor voltages in a cluster. The glitch is due to this exchange of active power with the grid.

D. Grid-Voltage Regulation

Fig. 13 shows experimental waveforms demonstrating voltage-regulating performance of the STATCOM. Note that the background system impedance of the test grid was 9.72%. Before this experiment was started, the voltage at the PCC in the test grid was higher by almost 5% than the nominal voltage of 6.6 kV. Since a voltage command of 95% of the nominal voltage was given to the STATCOM from the time of 0 to 50 ms, the STATCOM was in inductive operation at the rated power to regulate the voltage at the PCC to 6.27 kV (95% of 6.6 kV) during that period. At the time of 50 ms, the command was step changed from 95% to 100%. Then, the STATCOM was gradually adjusting the inductive reactive current from 100% to 50% to regulate the voltage at the PCC to 6.6 kV in about 100 ms. The maximum capacitor voltage fluctuation was $\pm 5\%$ throughout this experiment. The experimental waveforms showed that an appropriate adjustment of an inductive or capacitive reactive current allows the STATCOM to regulate the grid voltage in a certain range.

E. Load Compensation

Fig. 14 shows experimental waveforms demonstrating load-compensating performance of the STATCOM. For this test, the

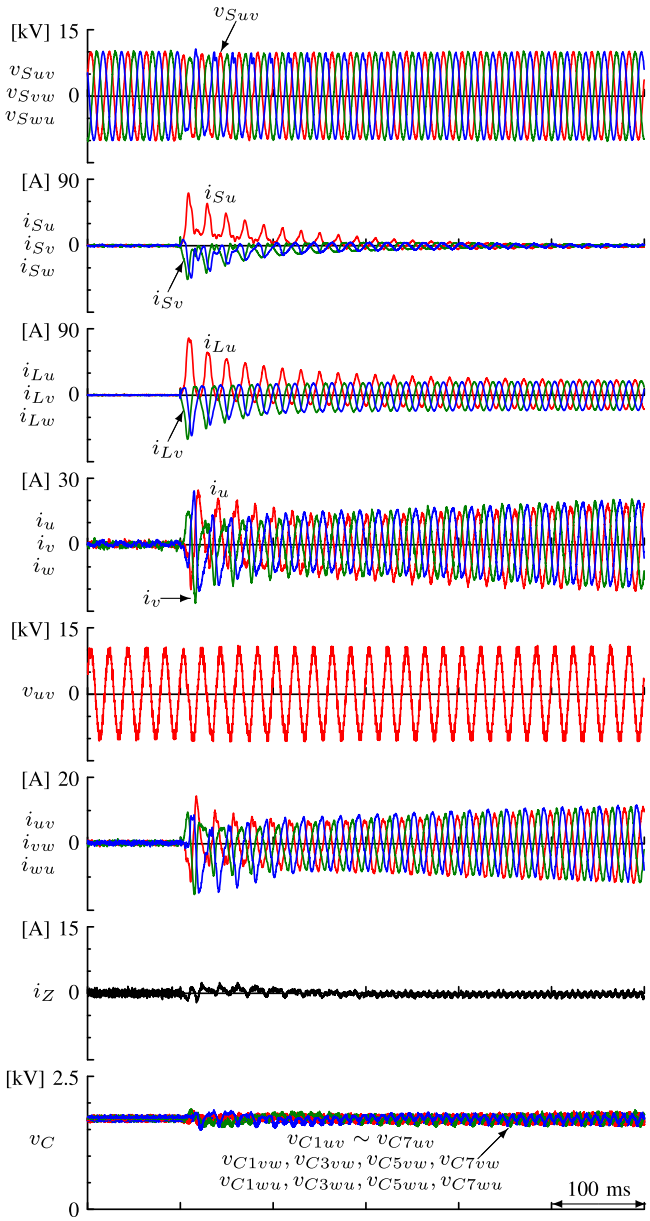

Fig. 14. Experimental waveforms when a three-phase inductive load rated at 180 kVA was switched on during load compensation mode of the STATCOM.

grid-voltage control was disabled. Initially, the load inductor was disconnected from the test grid, so that the STATCOM produced no reactive current. However, when the three-phase inductor was switched ON at the time of 100 ms, the STATCOM immediately started producing a capacitive reactive current. With the passage of time, the inrush current caused by the load settled down, and the STATCOM was able to fully compensate for the inductive reactive power resulting from the load. Note that the inrush current forced the grid voltage to drop for a moment, for example, by about 25% in case of v_{Swu}. However, the waveforms of dc-capacitor voltages showed no strong oscillation, thus demonstrating that the STATCOM can perform load compensation in a stable manner. Also note that the waveforms of i_u, i_v, and i_w were unbalanced for a period of time after the load was switched ON. This is because the waveforms of i_{Lu}, i_{Lv}, and i_{Lw}, which the load was drawing and the converter was compensating for, were unbalanced for that period of time.

VII. Conclusion

This article has discussed a 6.6-kV 200-kVA transformerless STATCOM based on the modular multilevel SDBC converter using SiC-MOSFET modules. The STATCOM has been developed as a verification test equipment for a medium-voltage transformerless grid converter under a national project in Japan. This article has discussed a new dc-capacitor voltage control, consisting of intercluster balancing control, which is different in structure, and intracluster balancing control, which is different in principle, from earlier methods. This article has provided a detailed description of the latter, which is based on the control of a dead time of each bridge cell. Experimental results obtained from the verification test equipment have validated the effectiveness of the control method. Moreover, successful test results have confirmed the capability of the system for the control of both positive-sequence and negative-sequence reactive powers in utility and industry applications.

References

[1] F. Z. Peng, J. S. Lai, J. W. McKeever, and J. VanCoevering, "A multilevel voltage-source inverter with separate dc sources for static VAR generation," *IEEE Trans. Ind. Appl.*, vol. 32, no. 5, pp. 1130–1138, Sep./Oct. 1996.

[2] C. Schauder, "STATCOM for compensation of large electric arc furnace installations," in *Proc. IEEE PES Summer Meeting*, Jul. 1999, pp. 1109–1112.

[3] Y. Liang and C. O. Nwankpa, "A new type of STATCOM based on cascading voltage-source inverters with phase-shifted unipolar SPWM," *IEEE Trans. Ind. Appl.*, vol. 35, no. 5, pp. 1118–1123, Sep./Oct. 1999.

[4] A. Lesnicar and R. Marquardt, "A new modular voltage source inverter topology," in *Proc. Eur. Conf. Power Electron. Appl*, Sep. 2003, pp. 1–10.

[5] F. Z. Peng and J. Wang, "A universal STATCOM with delta-connected cascade multilevel inverter," in *Proc. IEEE Power Electron. Specialists Conf.*, Jun. 2004, pp. 3529–3533.

[6] K. Fujii, U. Schwarzer, and R. W. De Doncker, "Comparison of hard-switched multi-level inverter topologies for STATCOM by loss-implemented simulation and cost estimation," in *Proc. IEEE Power Electron. Specialists Conf.*, 2005, pp. 340–346.

[7] R. E. Betz, T. Summers, and T. Furney, "Symmetry compensation using a H-bridge multilevel STATCOM with zero sequence injection," *in Proc. Conf. Rec. IEEE IAS Annu. Meeting*, Oct. 2006, pp. 1724–1731.

[8] C. Han *et al.*, "Evaluation of cascade-multilevel converter-based STATCOM for arc furnace flicker mitigation," *IEEE Trans. Ind. Appl.*, vol. 43, no. 2, pp. 748–755, Mar./Apr. 2007.

[9] H. Akagi, S. Inoue, and T. Yoshii, "Control and performance of a transformerless cascade PWM STATCOM with star configuration," *IEEE Trans. Ind. Appl.*, vol. 43, no. 4, pp. 1041–1049, Jul./Aug. 2007.

[10] L. Maharjan, S. Inoue, and H. Akagi, "A transformerless energy storage system based on a cascade PWM converter with star configuration," *IEEE Trans. Ind. Appl.*, vol. 44, no. 5, pp. 1621–1630, Sep./Oct. 2008.

[11] L. Maharjan, S. Inoue, H. Akagi, and J. Asakura, "SOC (state-of-charge)-balancing control of a battery energy storage system based on a cascade PWM converter," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1628–1636, Jun. 2009.

[12] B. Gultekin *et al.*, "Design and implementation of a 154-kV ±50-mvar transmission STATCOM based on 21-level cascaded multilevel converter," *IEEE Trans. Ind. Appl.*, vol. 48, no. 3, pp. 1030–1045, May/Jun. 2012.

[13] K. Usuki, F. Aoyama, and M. Hanamatsu, "Development of SVC control for suppressing voltage fluctuations," in *Proc. IEEE 8th Int. Conf. Power Electron Asia*, May/Jun. 2011, pp. 2073–2080.

[14] H. J. Knaak, "Modular multilevel converters and HVDC/FACTS: A success story," in *Proc. 14th Eur. Conf. Power Electron. Appl.*, Aug./Sep. 2011, pp. 1–6.

[15] H. Akagi, "Classification, terminology, and application of the modular multilevel casdcade converter (MMCC)," *IEEE Trans. Power Eletron*, vol. 26, no. 11, pp. 3119–3130, Nov. 2011.
[16] M. Hagiwara, R. Maeda and H. Akagi, "Negative-sequence reactive-power control by a PWM STATCOM based on a modular multilevel cascade converter (MMCC-SDBC)," *IEEE Trans. Ind. Appl.*, vol. 48, no. 2, pp. 720–729, Mar./Apr. 2012.
[17] P. Sochor, and H. Akagi, "Theoretical comparison in energy-balancing capability between star- and delta-configured modular multilevel cascade inverters for utility-scale photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1980–1992, Mar. 2016.
[18] E. Behrouzian, M. Bongiorno, and R. Teodorescu, "Impact of switching harmonics on capacitor cells balancing in phase-shifted PWM-based cascaded H-bridge STATCOM," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 815–824, Jan. 2017.
[19] E. Behrouzian, and M. Bongiorno, "Investigation of negative-sequence injection capability of cascaded H-bridge converters in star and delta configuration," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1675–1683, Feb. 2017.
[20] P. H. Wu, H. C. Chen, and P. T. Cheng, "Delta-connected cascaded H-bridge converter application in unbalanced load compensation," *IEEE Trans. Ind. Appl.*, vol. 53, no. 2, pp. 1254–1262, Mar./Apr. 2017.
[21] H. Akagi, "Multilevel converters: Fundamental circuits and systems," *Proc. IEEE*, vol. 105, no. 11, pp. 2048–2065, Nov. 2017.
[22] L. Maharjan, T. Tajyuta, A. Suzuki, A. Toba, Y. Matsumoto, and H. Akagi, "Control of a transformerless STATCOM based on the MMCC-SDBC (modular multilevel cascade converter single-delta bridge-cells)," in *Proc. Eur. Conf. Power Electron. Appl.*, Sep. 2017, pp. 1–9.
[23] L. Maharjan, T. Tajyuta, H. Shinohara, A. Suzuki, and A. Toba, "Control of a 6.6-kV transformerless STATCOM based on the MMCC-SDBC using SiC MOSFETs," in *Proc. Int. Power Electron. Conf.*, May 2018, pp. 1840–1846.
[24] J. J. Jung, J. H. Lee, S. K. Sul, G. T. Son, and Y. H. Chung, "DC capacitor voltage balancing control for delta-connected cascaded H-bridge STATCOM considering unbalanced grid and load conditions," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 4726–4735, Jun. 2018.
[25] Y. Koyama, Y. Nakazawa, H. Mochikawa, A. Kuzumaki, K. Sano, and N. Okada, "A transformerless 6.6-kV STATCOM based on hybrid cascade multilevel converter using SiC devices," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7411–7423, Sep. 2018.

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