Control Conflict Suppressing and Stability Improving for an MMC Distributed Control System

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***Abstract*—Compared with traditional centralized control strategies, the distributed control systems significantly improve the flexibility and expandability of an modular multilevel converter (MMC). However, the stability issue in the MMC distributed control system with the presence of control loop coupling interactions is rarely discussed in existing research works. This article is to improve the stability of an MMC distributed control system by inhibiting the control conflict due to the coupling interactions among control loops with incomplete control information. By modeling the MMC distributed control system, the control loop coupling interactions are analyzed and the essential cause of control conflict is revealed. Accordingly, a control parameter design principle is proposed to effectively suppress the disturbances from the targeted control conflict and improve the MMC system stability. The rationality of the theoretical analysis and the effectiveness of the control parameter design principle are confirmed by simulation and experimental results.**

***Index Terms*—Control conflict, coupling interaction, distributed control system, modular multilevel converter.**

I. Introduction

MODULAR multilevel converter (MMC) is one of the most promising topologies in recent years for medium- or high-voltage industrial applications, such as high-voltage dc transmission (HVdc) [1], [2], medium voltage microgrids [3], [4], and variable speed drives [5]–[7]. The wide adoption of MMCs in the industry is mainly due to its modularity, flexible expandability, transformerless configuration, common dc bus, high reliability from redundancy, etc., [8]–[10]. However, the traditional centralized control strategies [11]–[15] are not applicable to the MMC with numerous submodules (SMs) to limit the modularity and expandability of the overall system [16]. In the practical MMC-based HVdc projects [17]–[19], the nearest level modulation and capacitor voltage sorting are the dominating schemes. In addition, as a promising solution for managing the MMC systems with numerous SMs, the distributed control strategies [16], [20]–[28], which can improve the modularity, flexibility, and expandability of MMC systems, also attract increasing attention from researchers in recent years.

Two different Ethernet-based protocols, communication delay, PWM generation, and voltage balancing control of an MMC distributed control are discussed in [21]. A hierarchical control scheme characterized by modular design and excellent expansibility, where the different control tasks are assigned in the central control unit and valve-group control units, is presented and practiced in an MMC prototype containing 264 SMs [22]. A distributed control system with reduced data transmission from the central controller to local controllers is discussed in [23]. A distributed control method for an MMC based on CAN bus communication is proposed in [24], which needs capacitor voltages measured by local controllers to be sent to the central controller and the communication burden is heavy. An improved distributed control architecture, which assigns the current controls and capacitor voltage balancing control to a central controller and local controllers, respectively, is proposed and confirmed by experimental results in [26]. A decentralized control architecture for the SM capacitor voltage and switching frequency balancing is presented in [25], where the arm controllers are used to reduce the communication burden between the central controller and valve-group controllers. It is worth noting that the phase-shifted PWM scheme is also applied in MMC distributed control strategies [16], [20], [23], [24], [26]–[28].

There are a few works [16], [20] discussing the stability issues of the distributed control systems. The individual control loop stability is separately analyzed based on the distributed control architecture for a modular multilevel matrix converter (M3C) in [20]. A distributed control architecture that assigns the internal dynamic controls to local controllers is proposed in [16], and the control conflict issue in the system stability is briefly discussed. However, the root cause of such control conflict is not studied in [16], which makes it difficult to effectively inhibit the control conflict in a targeted way. In the MMC distributed control structures, the average voltage control is distributed into local controllers and only the corresponding SM capacitor voltage is collected as the feedback of the control loop for each local controller. The control information of the average control is incomplete compared with that in conventional MMC control systems. The outputs of all control loops in central and local controllers eventually couple together to manage all the control objectives. As a result, the control conflicts may be introduced

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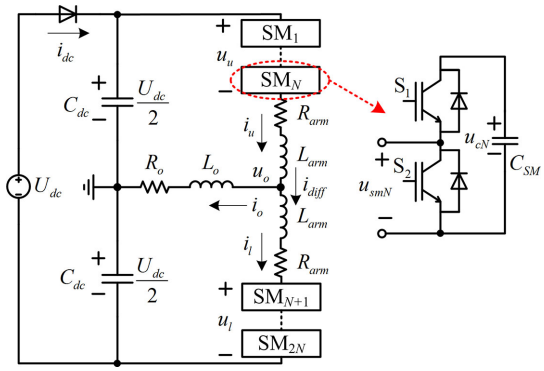

Fig. 1. Structure of a single-phase MMC-based inverter.

due to the coupling interaction among the control loops with incomplete control information, which deteriorates the control performance and even makes the MMC system unstable.

This article aims to reveal the root cause of the control conflicts in the MMC distributed control system by analyzing the coupling interactions among all control loops, and effectively inhibit the targeted control conflicts to ensure the system stability. A detailed model of the MMC distributed control system is established and simplified in this article. The coupling interactions among all control loops are elaborately studied based on the proposed MMC distributed control system model. It is found that the energy stored in the upper and lower arms can be automatically balanced with the help of the capacitor voltage averaging and balancing controls. The output current control loop and capacitor voltage balancing loops also interfere with each other. With the presence of such interference, the SM capacitor voltages are actually balanced to the phase average capacitor voltage, while the output current regulating is scarcely influenced. Due to incomplete control information, the distributed average voltage controls introduce different net dc power to SMs trying to diverge the capacitor voltage, which is deemed as the root cause of control conflict between the average voltage control and voltage balancing control loops. Such a net dc power exceeding the balancing capability of the capacitor voltage controllers will lead to the MMC system instability. Therefore, a control parameter design principle, which yields the parameter selection range for capacitor voltage control loops in the MMC distributed control system, is proposed. Besides sufficient phase margins, such a principle also has to be always satisfied to suppress the control conflict and guarantee the stable operation of the MMC. Finally, the correctness and effectiveness of the control loop coupling interactions, control conflict root cause analysis, and the parameter design principle are verified by simulation and experiment on a single-phase MMC structure shown in Fig. 1.

II. MMC Distributed Control System Modeling

A. Mathematical Model of the MMC

The basic structure and operation principles of an MMC have been extensively explained in the literature [11], [29] and will not be discussed. A single-phase MMC-based inverter system shown in Fig. 1 is adopted for the analysis in this article. There are N half-bridge SMs connected in series in the upper and lower arms, respectively. Each arm is equipped with an arm inductor $L_{\rm arm}$. An equivalent resistor $R_{\rm arm}$ is employed in each arm to represent the losses in that arm. Based on circuit theory, the following expressions can be obtained from Fig. 1

$$\begin{cases} i_o = i_u - i_l \\ i_{\rm diff} = 0.5\left(i_u + i_l\right) \end{cases} \tag{1}$$

$$\begin{cases} \frac{U_{\rm dc}}{2} - \frac{(u_u+u_l)}{2} - \left(R_{\rm arm} i_{\rm diff} + L_{\rm arm}\frac{di_{\rm diff}}{dt}\right) = 0 \\ \frac{u_l-u_u}{2} - \left(R_{\rm eq} i_o + L_{\rm eq}\frac{di_o}{dt}\right) = 0 \end{cases} \tag{2}$$

where i_u and i_l are the upper and lower arm currents, respectively, $U_{\rm dc}$ is the dc-side voltage, u_u and u_l are the upper and lower arm voltages, respectively, and i_o and $i_{\rm diff}$ refer to the output current and differential current, respectively. $R_{\rm eq}$ and $L_{\rm eq}$ can be expressed as

$$\begin{cases} R_{\rm eq} = R_o + 0.5R_{\rm arm} \\ L_{\rm eq} = L_o + 0.5L_{\rm arm}. \end{cases} \tag{3}$$

Based on (2), the inner electromotive force (EMF) e and the differential voltage $u_{\rm diff}$, which generate the output current i_o and the differential current $i_{\rm diff}$, respectively, are defined as follows:

$$\begin{cases} e = R_{\rm eq} i_o + L_{\rm eq}\frac{di_o}{dt} = \frac{u_l-u_u}{2} \\ \quad = \frac{1}{2}\left(\sum_{j=N+1}^{2N} u_{{\rm sm}j} - \sum_{j=1}^{N} u_{{\rm sm}j}\right) \\ u_{\rm diff} = R_{\rm arm} i_{\rm diff} + L_{\rm arm}\frac{di_{\rm diff}}{dt} \\ \quad = \frac{U_{\rm dc}-u_u-u_l}{2} = \frac{U_{\rm dc}}{2} - \frac{1}{2}\sum_{j=1}^{2N} u_{{\rm sm}j} \end{cases} \tag{4}$$

where $u_{{\rm sm}j}$ is the jth SM output voltage.

If the output voltage and current of the MMC are well regulated [12], [30], [31], they can be expressed as

$$\begin{cases} u_o = U_o \sin\left(\omega_o t\right) \\ i_o = I_o \sin\left(\omega_o t + \phi_o\right) \end{cases} \tag{5}$$

where U_o and I_o are the amplitudes of u_o and i_o, respectively, ω_o refers to the fundamental angular frequency in radian per second, and ϕ_o stands for the phase displacement between the output voltage and current.

B. MMC Distributed Control Structure

The MMC distributed control structure proposed in [16] is adopted in this article and shown in Fig. 2, where the control tasks are assigned to different controllers, i.e., a central controller and local controllers located in SMs. The output power control is implemented in the central controller, while the capacitor average voltage control and capacitor voltage balancing control are distributed in local controllers. In addition, necessary information is transmitted between the central and local controllers through a communication network [16].

In the central controller, the MMC output power control is realized by controlling the output current and the output current

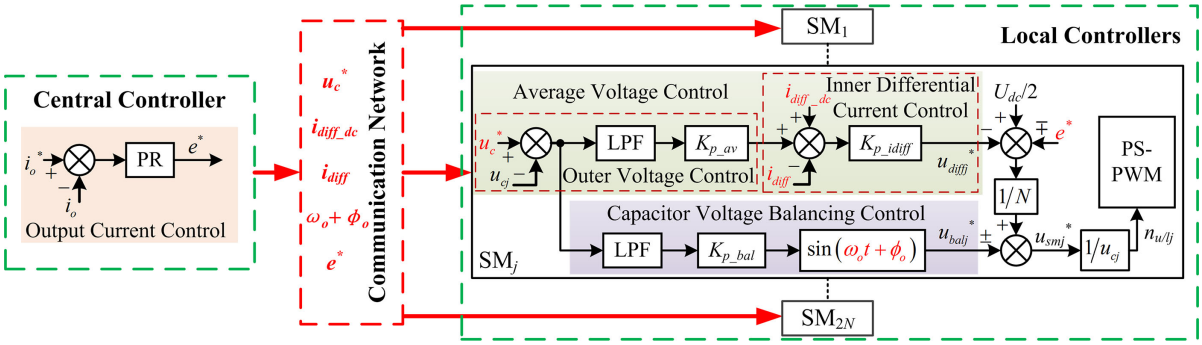

Fig. 2. MMC distributed control structure.

reference is given as $i_o^* = I_o \sin(\omega_o t + \phi_o)$. A proportional-resonant (PR) controller is employed to make the output current accurately track its sinusoidal reference i_o^*.

Taking the *j*th local controller as an example, only the *j*th SM capacitor voltage is captured in real time to perform the distributed capacitor voltage averaging and balancing controls due to the distributed structure. In the distributed average voltage control loop, the reference of the inner differential current $i_{\mathrm{diff}j}^*$ is obtained from the output of the outer capacitor voltage control and the dc-side current reference $i_{\mathrm{diff\_dc}}^*$ as

$$i_{\mathrm{diff}j}^* = i_{\mathrm{diff\_dc}}^* + K_{\mathrm{p\_av}}\left(u_c^* - \bar{u}_{cj}\right) \ (j = 1 \sim 2N) \quad (6)$$

where $i_{\mathrm{diff\_dc}}^* = U_o I_o \cos\phi_o / (2U_{\mathrm{dc}})$ is calculated according to the power balance between the dc- and ac-sides, u_c^* is the capacitor voltage reference, and $\bar{u}_{cj}$ is the dc component of the *j*th SM capacitor voltage after a low-pass filter (LPF). The feedback control of i_{diff} simultaneously contributes to the active power balance between the dc- and ac-sides and capacitor average voltage control with the help of a slightly adjusted dc-side power. Perfectly balanced capacitor voltage is rarely achievable in the practical operation of an MMC, since the SM capacitance tolerance, the MMC operating state change, or even the modulation scheme [32], [33] might introduce disturbances that deteriorate the consistency of capacitor voltages. Therefore, it is necessary to employ a capacitor voltage balancing control to avoid the voltage diverging due to the disturbances and the side-effect of the average voltage control. The output of the capacitor voltage balancing control loop $u_{\mathrm{bal}j}^*$ is a fundamental component in phase with the output current i_o. It introduces a corresponding sine component in the SM output voltage $u_{\mathrm{sm}j}$. Such a sine component in $u_{\mathrm{sm}j}$ will couple with i_{o} and consequently generates a controllable SM output power to balance the *j*th SM capacitor voltage [34].

Proportional controls are used in local controllers. The MMC distributed system could be easily unstable under severe disturbances if PI controls are employed to regulate the capacitor voltages. Since the capacitor voltage errors fed into the PI controllers are actually different, the outputs of the distributed average voltage control loops become unpredictable due to the unknown and various "histories" of the integrators [35], [36].

In the conventional MMC centralized control structure [11]–[13], [31], [37], the capacitor voltages of all SMs in one phase are collected in each control cycle, and the phase average capacitor voltage is calculated as the feedback for the average voltage control loop. In the adopted MMC distributed control structure, the internal dynamic controls, i.e., the average voltage control and capacitor voltage balancing control are assigned to different local controllers, and the control information is not exchanged among local controllers in real time. Each local controller can only collect the corresponding SM capacitor voltage to perform the average voltage control. Therefore, the acquired control information is "incomplete" compared with that of average voltage control loops in the MMC centralized control structures. With the presence of the incomplete control information, the coupling interaction among all distributed control loops is inevitable to cause control conflicts and even leads to system instability.

C. Modeling of the MMC Distributed Control System

In order to analyze the effect of the control loop coupling interaction on the control objectives and reveal the essential causes of control conflicts, the MMC distributed control system is elaborately modeled. As shown in Fig. 3(a), the MMC system is divided into two parts, i.e., control part and circuit model part. The *j*th SM output voltage is taken as a point of penetration to analyze the model as follows.

In the control part, the reference of the *j*th SM output voltage $u_{\mathrm{sm}j}^*$ is formed by the outputs of all control loops, and can be written as

$$\begin{cases} u_{\mathrm{sm}j}^* = \frac{U_{\mathrm{dc}}}{2N} - \frac{u_{\mathrm{diff}j}^*}{N} - \left(\frac{e^*}{N} - u_{\mathrm{bal}j}^*\right) & (j = 1 \sim N) \\ u_{\mathrm{sm}j}^* = \frac{U_{\mathrm{dc}}}{2N} - \frac{u_{\mathrm{diff}j}^*}{N} + \left(\frac{e^*}{N} - u_{\mathrm{bal}j}^*\right) & (j = N+1 \sim 2N) \end{cases} \quad (7)$$

where e^* $u_{\mathrm{diff}j}^*$ and $u_{\mathrm{bal}j}^*$ are the outputs of the output current loop, the *j*th distributed average voltage control loop, and the *j*th capacitor voltage balancing loop, respectively. Then, $u_{\mathrm{sm}j}^*$ is normalized by the *j*th SM capacitor voltage u_{cj}, and compared with a phase-shifted triangular waveform having a carrier frequency of f_c in the PWM modulation unit [16], [27], [38].

The circuit model part is composed of the current models and SM capacitor voltage models. The *j*th SM output voltage $u_{\mathrm{sm}j}$ is obtained by multiplying the modulated PWM signal with the capacitor voltage u_{cj}. On the one hand, the differential voltage u_{diff} and the EMF e in the current models, which generate i_{diff} and i_o, respectively, are determined by the output voltages of all SMs in the same phase. On the other hand, in the *j*th SM capacitor voltage model, the *j*th SM output voltage is multiplied

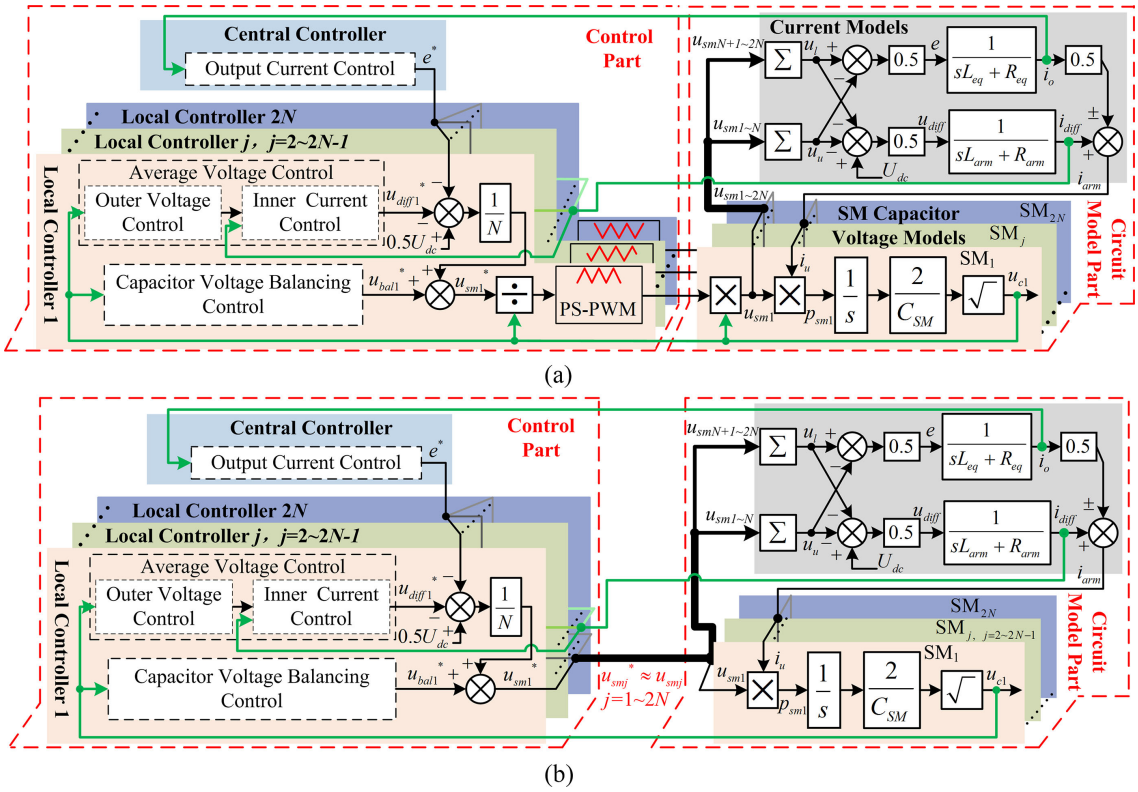

Fig. 3. Models of the MMC distributed control system. (a) Detailed model. (b) Simplified model.

by the arm current to generate the jth SM power $p_{\mathrm{sm}j}$, whose dc component adjusts the corresponding capacitor voltage u_{cj}.

Ignoring the influence of the modulation, $1/u_{cj}$ and u_{cj} before and after the PWM modulation unit can cancel out, and the output voltage of individual SM is approximately equal to its reference. Therefore, the model of the MMC distributed control system is simplified as shown in Fig. 3(b). The jth SM output voltage can be expressed as

$$u_{\mathrm{sm}j} \approx u^*_{\mathrm{sm}j}\,(j = 1 \sim 2N)\,. \tag{8}$$

In the simplified model, the outputs of all control loops are directly connected to the circuit model to conveniently analyze the coupling interaction effects among the control loops on the control objectives (i_o, i_{diff}, u_c).

According to (7) and (8), the individual SM power $p_{\mathrm{sm}j}$, which determines the individual SM capacitor voltage u_{cj}, can be expressed as

$$\begin{cases} p_{\mathrm{sm}j} & \approx u^*_{\mathrm{sm}j} \times i_u \quad (j = 1 \sim N) \\ & = p_{\mathrm{sm}j\_\mathrm{dc}} - p_{\mathrm{sm}j\_\mathrm{ac}} + p_{\mathrm{sm}\_(3)} + p_{\mathrm{sm}j\_(4)} \\ p_{\mathrm{sm}j} & \approx u^*_{\mathrm{sm}j} \times i_l \quad (j = N+1 \sim 2N) \\ & = p_{\mathrm{sm}j\_\mathrm{dc}} - p_{\mathrm{sm}j\_\mathrm{ac}} - p_{\mathrm{sm}\_(3)} - p_{\mathrm{sm}j\_(4)} \end{cases} \tag{9}$$

where

$$p_{\mathrm{sm}j\_\mathrm{dc}} = \left(\frac{U_{\mathrm{dc}}}{2N} - \frac{u^*_{\mathrm{diff}j}}{N}\right) i_{\mathrm{diff}}, p_{\mathrm{sm}j\_\mathrm{ac}} = \left(\frac{e^*}{N} - u^*_{\mathrm{bal}j}\right) \frac{i_o}{2}$$

$$p_{\mathrm{sm}\_(3)} = \frac{U_{\mathrm{dc}}}{2N}\frac{i_o}{2} - \frac{e^*}{N} i_{\mathrm{diff}}$$

$$p_{\mathrm{sm}j\_(4)} = -\frac{u^*_{\mathrm{diff}j}}{N}\frac{i_o}{2} + u^*_{\mathrm{bal}j} i_{\mathrm{diff}}.$$

In (9), $p_{\mathrm{sm}j\_\mathrm{dc}}$ represents the power transferred from the dc side to SM; $p_{\mathrm{sm}j\_\mathrm{ac}}$ represents the power transferred from SM to the ac side; and $p_{\mathrm{sm}\_(3)}$ and $p_{\mathrm{sm}j\_(4)}$ represent the power flowing between the upper and lower arms in a phase leg. $p_{sm\_(3)}$ is the same for all SMs in one phase and is independent of j. And, $p_{\mathrm{sm}j\_(4)}$ is small compared to the other three terms and is not discussed in this article.

According to (4) and (8), first, the EMF e is expressed as follows:

$$\begin{aligned} e &\approx \frac{1}{2}\left(\sum_{j=N+1}^{2N} u^*_{\mathrm{sm}j} - \sum_{j=1}^{N} u^*_{\mathrm{sm}j}\right) \\ &= e^* - \frac{1}{2}\sum_{j=1}^{2N} u^*_{\mathrm{bal}j} + \frac{1}{2N}\left(\sum_{j=1}^{N} u^*_{\mathrm{diff}j} - \sum_{j=N+1}^{2N} u^*_{\mathrm{diff}j}\right) \\ &= e^* - \frac{K_{p\_\mathrm{bal}}}{2}\left(2U_{\mathrm{dc}} - \sum_{j=1}^{2N} \bar{u}_{cj}\right)\sin\left(\omega_o t + \phi_o\right) \\ &\quad + \underbrace{\frac{K_{p\_\mathrm{av}} K_{p\_i\mathrm{diff}}}{2N}\left(\sum_{j=N+1}^{2N} \bar{u}_{cj} - \sum_{j=1}^{N} \bar{u}_{cj}\right)}_{e_{\mathrm{dc}}} \end{aligned} \tag{10}$$

where e_{dc} represents the dc component in e when the upper and lower arm voltages are unbalanced; K_{p_bal}, K_{p_av}, and $K_{p\_i\mathrm{diff}}$ are the proportional gains of the capacitor voltage balancing loop, the outer and inner loops of the average voltage control,

respectively. Second, $u_{\rm diff}$ can be expressed as

$$\begin{aligned} u_{\rm diff} &\approx \frac{1}{2}\left(U_{\rm dc} - \sum_{j=1}^{2N} u^*_{{\rm sm}j}\right) \\ &= \frac{1}{2N}\sum_{j=1}^{2N} u^*_{{\rm diff}j} + \frac{1}{2}\left(\sum_{j=N+1}^{2N} u^*_{{\rm bal}j} - \sum_{j=1}^{N} u^*_{{\rm bal}j}\right) \\ &= \frac{1}{2N}\sum_{j=1}^{2N} u^*_{{\rm diff}j} \\ &\quad + \underbrace{\frac{K_{p\_{\rm bal}}\sin(\omega_o t+\phi_o)}{2}\left(\sum_{j=1}^{N}\bar{u}_{cj} - \sum_{j=N+1}^{2N}\bar{u}_{cj}\right)}_{u_{\rm diff\_ac}} \end{aligned} \tag{11}$$

where $u_{\rm diff\_ac}$ represents the ac component in $u_{\rm diff}$ when the arm voltages are unbalanced.

Based on (9)–(11), the control loop coupling effects on u_c, i_o, and $i_{\rm diff}$ can be briefly expressed as follows.

1) In (9), the output current, the average voltage, and the capacitor voltage balancing control loops are coupled in $p_{{\rm sm}j}$ to adjust the SM capacitor voltage u_{cj}. Specifically, $p_{{\rm sm}j\_{\rm dc}}$ can be adjusted by $u^*_{{\rm diff}j}$, and $p_{{\rm sm}j\_{\rm ac}}$ is adjusted by both e^* and $u^*_{{\rm bal}j}$. In addition, the dc component in i_o and the fundamental component in $i_{\rm diff}$ can be used to change u_{cj} through $p_{\rm sm\_(3)}$.
2) In (10), the output current control loop, all the capacitor voltage balancing control loops, and all the average voltage control loops are coupled in e to generate the output current i_o. The fundamental component in i_o is mainly determined by both e^* and $u^*_{{\rm bal}j}$, and a dc component would be injected into i_o by $e_{\rm dc}$ (average voltage control) only when the upper and lower arm voltages are unbalanced. It should be noted that $e_{\rm dc}$ does not exist in steady state nor in most operating modes of the MMC, since the MMC arm voltages are naturally balanced if a direct modulation scheme is adopted [39], [40]. Even if the arm voltages are unbalanced due to transient disturbances, the voltage difference between the two arms will rapidly vanish with the help of $e_{\rm dc}$ and $u_{\rm diff\_ac}$ in (10) and (11). Therefore, the average voltage and inner differential current controls scarcely interfere with the output current control.
3) In (11), all the distributed average voltage and capacitor voltage balancing control loops are coupled together in $u_{\rm diff}$ to generate the differential current $i_{\rm diff}$. In particular, $i_{\rm diff}$ is mainly determined by $u^*_{{\rm diff}j}$, and a fundamental component is compulsorily injected into $i_{\rm diff}$ by $u_{\rm diff\_ac}$ (capacitor voltage balancing control) when the upper and lower arm voltages are unbalanced.

In this section, the complex control loop coupling relation in the MMC distributed control system is briefly described. In order to reveal the essential cause of control conflicts, it is necessary to study the interaction among control loops in depth.

III. Coupling Interaction Analysis and Control Conflict Suppression

A. Control Loop Coupling Interaction for Arm Voltage Balance

According to (10) and (11), when the upper and lower arm voltages are unbalanced, a dc component $e_{\rm dc}$ and an dc fundamental component $u_{\rm diff\_ac}$ would be injected into e and $u_{\rm diff}$ with the help of the average voltage and capacitor voltage balancing controls, respectively. Consequently, an ac fundamental component in $i_{\rm diff}$ is generated by $u_{\rm diff\_ac}$ and a dc component in i_o is generated by $e_{\rm dc}$, which will further generate extra dc components in the SM power $p_{{\rm sm}j}$ of (9) to adjust the arm voltage balancing. It is noted that only the additionally generated $p_{\rm sm\_(3)}$ in $p_{{\rm sm}j}$ is taken into account since other extra dc power terms in $p_{{\rm sm}j\_{\rm dc}}$, $p_{{\rm sm}j\_{\rm ac}}$, and $p_{{\rm sm}j\_(4)}$ are small and neglectable compared with that of $p_{\rm sm\_(3)}$. And $p_{\rm sm\_(3)}$ can be rewritten as

$$\begin{aligned} p_{\rm sm\_(3)} &= \frac{U_{\rm dc}}{2N}\frac{i_o}{2} - \frac{e^*}{N}i_{\rm diff} \\ &= \underbrace{k_{io}\left(\sum_{j=N+1}^{2N}\bar{u}_{cj} - \sum_{j=1}^{N}\bar{u}_{cj}\right)}_{1} \\ &\quad + \underbrace{k_{i{\rm diff}}\left(\sum_{j=N+1}^{2N}\bar{u}_{cj} - \sum_{j=1}^{N}\bar{u}_{cj}\right)}_{2} \\ &\quad + \text{ac components} \end{aligned} \tag{12}$$

where k_{io} and $k_{\rm idiff}$ refer to the positive coefficients of the dc power directly introduced by the dc component in i_o and the ac fundamental component in $i_{\rm diff}$, respectively. The terms 1 and 2 are two dc powers generated by existing control loops when the arm voltages are unbalanced. The effect of the two dc powers is to eliminate the voltage difference between the upper and lower arms. For instance, when the average capacitor voltage of the upper arm is less than that of the lower arm, two positive dc components are added into $p_{\rm sm\_arm}$ to charge all the capacitors in the upper arm. Meanwhile, all capacitors in the lower arm are discharged since $p_{\rm sm\_(3)}$ is subtracted from $p_{{\rm sm}j}$ of the lower arm. Therefore, the coupling interaction of the control loops naturally forces the energy stored in two arms to reach equilibrium. Accordingly, the arm voltages are assumed the same in subsequent analysis.

B. Coupling Interaction Between the Output Current Control and Capacitor Voltage Balancing Control Loops

According to (9) and (10), the output current control loop (e^*) and all capacitor voltage balancing control loops ($u^*_{{\rm bal}j}$) are coupled to determine i_o through e and to balance the SM capacitor voltages through $p_{{\rm sm}j\_{\rm ac}}$. Assuming the upper and

lower arm voltages are the same, e can be rewritten as

$$e \approx e^* - \frac{1}{2N}\sum_{j=1}^{2N} u^*_{\mathrm{bal}j} = e^* - \frac{K_{p\_\mathrm{bal}}}{2}\left(2U_{\mathrm{dc}} - \sum_{j=1}^{2N}\bar{u}_{cj}\right)\sin\left(\omega_o t + \phi_o\right). \quad (13)$$

Normally, the current control loops react much faster than the capacitor voltage control loops in an MMC control system. Once i_o is affected by the capacitor voltage balancing control, the output current control will rapidly adjust its output e^* to cancel out the influence and maintain i_o constant. Therefore, the effect of the capacitor voltage balancing loop on i_o is minor.

The power $p_{\mathrm{sm}j\_\mathrm{ac}}$ in (9) is used to maintain the output power and balance the SM capacitor voltages, which can be rewritten as follows:

$$p_{\mathrm{sm}j\_\mathrm{ac}} = \frac{e^* i_o}{2N} - \frac{u^*_{\mathrm{bal}j} i_o}{2} = p_{\mathrm{sm}\_(1)} - p_{\mathrm{sm}j\_(2)}\,(j = 1 \sim 2N) \quad (14)$$

where $p_{\mathrm{sm}\_(1)}$ represents the power regulated by the output current loop and $p_{\mathrm{sm}j\_(2)}$ stands for the power adjusted by the balancing control loops. In the process of balancing the SM capacitor voltages, e can be reasonably considered constant due to the fast dynamic response of the output current loop. Substituting e^* in (13) into (14), one can obtain

$$\begin{aligned} p_{\mathrm{sm}j\_\mathrm{ac}} &= \left[\left(e + \tfrac{1}{2}\sum_{i=1}^{2N} u^*_{\mathrm{bal}i}\right)\tfrac{1}{N} - u^*_{\mathrm{bal}j}\right]\tfrac{i_o}{2} \\ &= \tfrac{e i_o}{2N} + \left(\tfrac{1}{2N}\sum_{i=1}^{2N} u^*_{\mathrm{bal}i} - u^*_{\mathrm{bal}j}\right)\tfrac{i_o}{2} \\ &= \underbrace{\frac{e i_o}{2N}}_{1} - \underbrace{\frac{K_{p\_\mathrm{bal}} I_o}{4}\left(\frac{1}{2N}\sum_{i=1}^{2N}\bar{u}_{ci} - \bar{u}_{cj}\right)}_{2} \\ &\quad -\text{ac components} \end{aligned} \quad (j = 1 \sim 2N) \quad (15)$$

where term 1 represents the constant ac-side power strongly maintained by the output current control, and term 2 represents the active power actually used to balance the SM capacitor voltages while the output current control maintaining the output power unaffected. In other words, the coupling interaction among the output current and capacitor voltage balancing control loops makes each SM capacitor voltage approaching the phase average capacitor voltage without influencing the output power.

Based on the above analysis, the actual active power $p_{\mathrm{sm}j\_\mathrm{bal}}$ obtained by the MMC distributed control system that balances the SM capacitor voltages, which is also deemed as the capacitor voltage balancing capability, can be expressed as

$$p_{\mathrm{sm}j\_\mathrm{bal}} = \frac{K_{p\_\mathrm{bal}} I_o}{4}\left(\frac{1}{2N}\sum_{i=1}^{2N}\bar{u}_{ci} - \bar{u}_{cj}\right)(j = 1 \sim 2N). \quad (16)$$

C. Coupling Interaction Among Average Voltage Control Loops

As described by (9) and (11), all average voltage control loops are coupled to determine i_{diff} through u_{diff} and to regulate SM capacitor voltages through $p_{\mathrm{sm}j\_\mathrm{dc}}$. According to (11) and assuming the upper and lower arm voltages are balanced, u_{diff} can be rewritten as

$$\begin{aligned} u_{\mathrm{diff}} &\approx \frac{1}{2N}\sum_{j=1}^{2N} u^*_{\mathrm{diff}j} = K_{p\_i\mathrm{diff}}\left(\frac{1}{2N}\sum_{j=1}^{2N} i^*_{\mathrm{diff}j} - i_{\mathrm{diff}}\right) \\ &= K_{p\_i\mathrm{diff}}\left\{\underbrace{\left[i^*_{\mathrm{diff\_dc}} + K_{p\_\mathrm{av}}\left(u^*_c - \frac{1}{2N}\sum_{j=1}^{2N}\bar{u}_{cj}\right)\right]}_{i^*_{\mathrm{diff}}} - i_{\mathrm{diff}}\right\} \end{aligned} \quad (17)$$

where i^*_{diff} is the actual differential current reference in the MMC distributed control system. As shown in (17), with the coupling interaction of all distributed average voltage control loops, i^*_{diff} is equal to the average value of all distributed differential current references and can be expressed as

$$i^*_{\mathrm{diff}} = \frac{1}{2N}\sum_{j=1}^{2N} i^*_{\mathrm{diff}j} = i^*_{\mathrm{diff\_dc}} + \underbrace{K_{p\_\mathrm{av}}\left(u^*_c - \frac{1}{2N}\sum_{j=1}^{2N}\bar{u}_{cj}\right)}_{i^*_{\mathrm{diff\_av}}} \quad (18)$$

where $i^*_{\mathrm{diff\_av}}$ is a component of differential current reference that is related to the phase average capacitor voltage control. Although the individual average voltage control loop only collects the corresponding SM capacitor voltage, the phase average capacitor voltage can still follow its reference u^*_c by adjusting $i^*_{\mathrm{diff\_av}}$ thanks to the coupling interaction of all average voltage controls, which has the same effect of that in centralized control systems.

It is normally assumed that i_{diff} is equal to its actual reference i^*_{diff} when analyzing the average voltage control loops, due to the much faster response of the internal current control compared with that of the external voltage control

$$i_{\mathrm{diff}} \approx i^*_{\mathrm{diff}}. \quad (19)$$

Based on (6), (18), and (19), the outputs of the distributed average voltage control loops can be expressed as

$$\begin{aligned} u^*_{\mathrm{diff}j} &= K_{p\_i\mathrm{diff}}\left(i^*_{\mathrm{diff}j} - i_{\mathrm{diff}}\right) \approx K_{p\_i\mathrm{diff}}\left(i^*_{\mathrm{diff}j} - i^*_{\mathrm{diff}}\right) \\ &= K_{p\_i\mathrm{diff}} K_{p\_\mathrm{av}}\left(\tfrac{1}{2N}\sum_{i=1}^{2N}\bar{u}_{ci} - \bar{u}_{cj}\right) \end{aligned} \quad (j = 1 \sim 2N). \quad (20)$$

As shown in (20), the distributed average voltage control outputs are different for SMs due to the difference between $i^*_{\mathrm{diff}j}$ and i^*_{diff}, which results in various $p_{\mathrm{sm}j\_\mathrm{dc}}$ in (9). Substituting

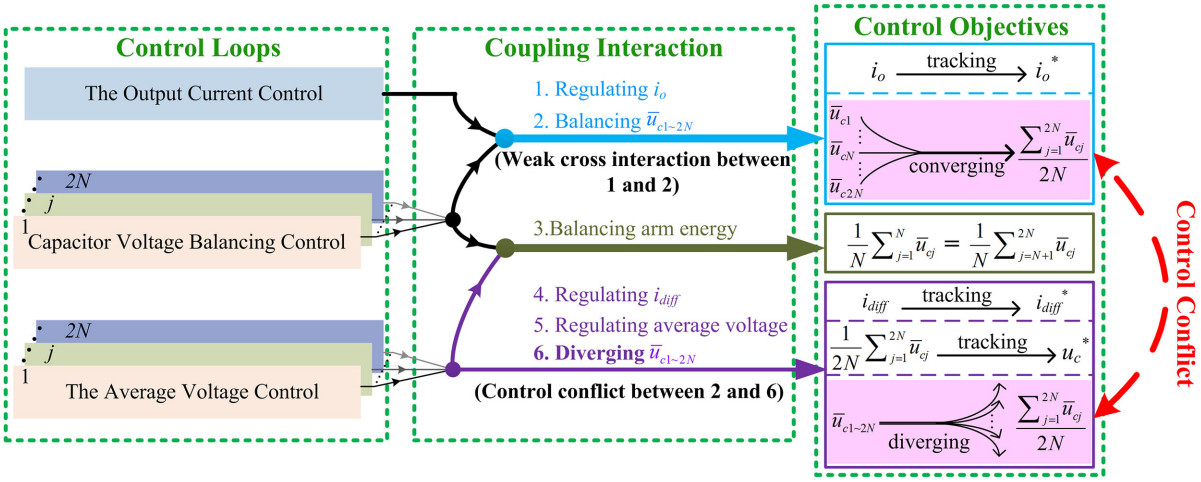

Fig. 4. Effects of the coupling interaction in the control loops on the control objectives.

(18)–(20) into $p_{\mathrm{sm}j\_\mathrm{dc}}$, it can be rewritten as

$$\begin{aligned} &p_{\mathrm{sm}j\_\mathrm{dc}} \\ &\approx \left(\frac{U_{\mathrm{dc}}}{2N}-\frac{u^*_{\mathrm{diff}j}}{N}\right)\left[i^*_{\mathrm{diff\_dc}}+K_{p\_\mathrm{av}}\left(u_c^*-\frac{1}{2N}\sum_{j=1}^{2N}\bar{u}_{cj}\right)\right] \\ &=\underbrace{\frac{U_{\mathrm{dc}}i^*_{\mathrm{diff\_dc}}}{2N}}_{1}+\underbrace{\frac{U_{\mathrm{dc}}K_{p\_\mathrm{av}}}{2N}\left(u_c^*-\frac{1}{2N}\sum_{j=1}^{2N}\bar{u}_{cj}\right)}_{2} \\ &+\underbrace{\frac{K_{p\_i\mathrm{diff}}K_{p\_\mathrm{av}}i^*_{\mathrm{diff}}}{N}\left(\bar{u}_{cj}-\frac{1}{2N}\sum_{i=1}^{2N}\bar{u}_{ci}\right)}_{3}\ (j=1\sim2N) \end{aligned} \tag{21}$$

where term 1, which represents the dc-side power, is used to maintain the ac and dc power balance; term 2, which represents a controllable dc-side power, makes the phase average capacitor voltage to follow u_c^*; and term 3, whose value is different for different SMs represents the power determined by the individual average voltage control loop.

Considering that $i^*_{\mathrm{diff\_av}}$ in (18) is generally much smaller than $i^*_{\mathrm{diff\_dc}}$ in the normal operation of the MMC, i.e., $i^*_{\mathrm{diff\_dc}} \gg i^*_{\mathrm{diff\_av}}$, term 3 in (21) can be rewritten as

$$\begin{aligned} \text{term 3} &= \frac{K_{p\_i\mathrm{diff}}K_{p\_\mathrm{av}}i^*_{\mathrm{diff}}}{N}\left(\bar{u}_{cj}-\frac{1}{2N}\sum_{i=1}^{2N}\bar{u}_{ci}\right) \\ &\approx \underbrace{\frac{K_{p\_i\mathrm{diff}}K_{p\_\mathrm{av}}i^*_{\mathrm{diff\_dc}}}{N}\left(\bar{u}_{cj}-\frac{1}{2N}\sum_{i=1}^{2N}\bar{u}_{ci}\right)}_{p_{\mathrm{sm}j\_\mathrm{av}}}. \\ &\qquad (j=1\sim2N) \end{aligned} \tag{22}$$

Attention paid to $p_{\mathrm{sm}j\_\mathrm{av}}$ in (22) actually makes the SM capacitor voltages diverge from the phase average capacitor voltage. For instance, considering the jth SM whose capacitor voltage is higher than the average capacitor voltage, $p_{\mathrm{sm}j\_\mathrm{av}}$ in (22) is greater than zero, which theoretically further increases the capacitor voltage of the SM to infinite, and vice versa. Although the phase average capacitor voltage can still track its reference u_c^* with the help of term 2 in (21), the consistency of SM capacitor voltages is deteriorated by $p_{\mathrm{sm}j\_\mathrm{av}}$, which is in conflict with the effect of capacitor voltage balancing control loop. More severely, if not suppressed, the control conflict might exceed the capacitor voltage balancing capability, diverge capacitor voltages, and even destabilize the MMC system. As a consequence, it is an instability risk in the MMC distributed system.

D. Interaction Summary and Control Conflict Suppression

The control loop coupling interactions are summarized in this section, and the effects of the coupling interaction in the control loops on the control objectives are shown in Fig. 4.

1) The upper and lower arm voltages can be naturally forced to reach equilibrium by the coupling interaction of all the average voltage control loops and capacitor voltage balancing control loops.
2) The coupling interaction between the output current control loop and all capacitor voltage balancing control loops makes each SM capacitor voltage approach to the phase average capacitor voltage without influencing i_o, and the SM capacitor voltage balancing capability is expressed in (16).
3) The coupling interaction of average voltage control loops has three effects: first, the differential current actually tracks the average reference i^*_{diff}; second, the phase average capacitor voltage is forced to reach its reference u_c^*; third, the consistency of SM capacitor voltages is deteriorated and SM capacitor voltages diverge from each other. And, $p_{\mathrm{sm}j\_\mathrm{av}}$ in (22) is defined as the disturbance of average voltage control loops on the SM capacitor voltage balancing.

It is concluded that there are control conflicts between the average voltage control and the SM capacitor voltage balancing

TABLE I
PARAMETERS OF THE MMC SYSTEM

Parameters	Values
DC bus voltage: U_{dc}	160 V
DC bus capacitance: C_{dc}	4.7 mF
Load Resistance: R_o	15 Ω
Rated output frequency: f_o	50 Hz
No. of SM in each arm: N	4
Arm inductance: L_{arm}	5 mH
Arm resistance: R_{arm}	0.05 Ω
SM capacitance: C_{SM}	940 μF
Carrier frequency: f_c	1 kHz
Deadtime	2 μs
Amplitude of output current reference: I_o	4 A
SM Capacitor voltage reference: u_c^*	40 V

TABLE II
CONTROLLER PARAMETERS OF THE CURRENT LOOPS

Control loop	Controller parameter	Phase margin
Output current	K_{p_io}=13.5; K_{r_io}=500	52.9°
Differential current	K_{p_idiff}=12	47.3°

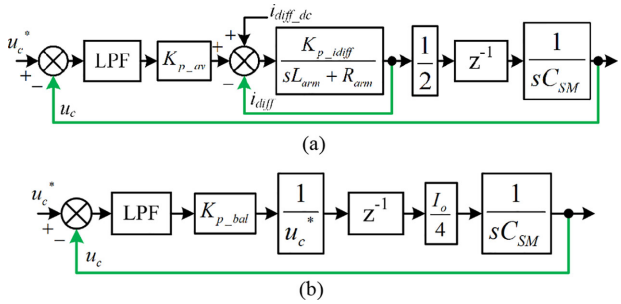

Fig. 5. Simplified block diagrams for capacitor voltage control loops. (a) Average voltage control loop. (b) Capacitor voltage balancing control loop.

loops in the MMC distributed control system, which might lead to the system instability. The capability of the voltage balancing control must be greater than the disturbance introduced by the average voltage control to inhibit the control conflict. Thus, combining (16) and (22), one can obtain

$$\frac{K_{p\_\mathrm{bal}} I_o}{4} > \frac{K_{p\_i\mathrm{diff}} K_{p\_\mathrm{av}} i^*_{\mathrm{diff\_dc}}}{N}. \tag{23}$$

Considering the active power balance of the dc- and ac-sides so that $i^*_{\mathrm{diff\_dc}} = U_o I_o \cos\phi_o/(2U_{\mathrm{dc}})$, (23) can be simplified as

$$K_{p\_\mathrm{bal}} > \frac{2K_{p\_\mathrm{av}} K_{p\_i\mathrm{diff}} U_o \cos\phi_o}{N U_{\mathrm{dc}}}. \tag{24}$$

The inequality (24) is determined by the number of SM in one arm, the MMC system parameters, and the control parameters. The SM number, the system parameters, and the control parameter vary for different MMC systems, so that the change of the relevant parameters has to be comprehensively considered to obtain the inequality (24) for different MMCs. Since the control parameters can be designed more flexibly and conveniently compared with the number of SM and system parameters, the inequality (24) can be regarded as a design principle of control parameters to inhibit control conflict and improve the stability of the MMC distributed control system.

IV. CASE STUDY

A single-phase MMC-based inverter shown in Fig. 1, whose key parameters are listed in Table I, is studied to verify the effectiveness of the proposed control conflict analysis for the distributed control system.

As the equivalent switching frequency of the MMC is $4f_c =$ 4 kHz, the sampling frequency is designed to be $f_s = 4$ kHz and the period of the control system is selected to be $T_s = 1/f_s$. According to the analysis method of digital control system delay in [41] and [42], a $1.5T_s$ delay exists in the current control loops and a $3T_s$ delay exists in the capacitor voltage control loops. Table II gives the control parameters and phase margins of the current control loops. According to (24) and the parameters in Tables I and II, the following inequality must be satisfied to guarantee the stable operation of the MMC system

$$K_{p\_\mathrm{bal}} > 2.25 K_{p\_\mathrm{av}}. \tag{25}$$

The control parameter relation in (25) is derived from the perspective of the disturbance introduced by the average voltage control loop [$p_{\mathrm{sm}j\_\mathrm{av}}$ in (22)] and the control conflict suppression capability of the balancing loop [$p_{\mathrm{sm}j\_\mathrm{bal}}$ in (16)].

The simplified block diagrams for the distributed average voltage control and capacitor voltage balancing control, which are used to design the controller parameters K_{p_av} and K_{p_bal}, are shown in Fig. 5. According to Fig. 5(a) and (b), the open-loop transfer functions of the average voltage control loop and the capacitor voltage balancing loop, i.e., $G_{\mathrm{av\_op}}(s)$ and $G_{\mathrm{bal\_op}}(s)$, are respectively derived as

$$G_{\mathrm{av\_op}}(s) = \frac{\pi K_{p\_\mathrm{av}} K_{p\_i\mathrm{diff}} f_{\mathrm{LPF\_av}} e^{-3s/f_s}}{C_{\mathrm{SM}} s (s + 2\pi f_{\mathrm{LPF\_av}}) (L_{\mathrm{arm}} s + K_{p\_i\mathrm{diff}} + R_{\mathrm{arm}})} \tag{26}$$

$$G_{\mathrm{bal\_op}}(s) = \frac{\pi K_{p\_\mathrm{bal}} f_{\mathrm{LPF\_bal}} I_o e^{-3s/f_s}}{2C_{\mathrm{SM}} u_c^* s (s + 2\pi f_{\mathrm{LPF\_bal}})} \tag{27}$$

where $f_{\mathrm{LPF\_av}}$ and $f_{\mathrm{LPF\_bal}}$ are the cutoff frequencies of the LPFs for the average voltage control loop and the capacitor voltage balancing loop, respectively. In this case, $f_{\mathrm{LPF\_av}}$ is 10 Hz and $f_{\mathrm{LPF\_bal}}$ is 5 Hz.

Based on (26) and (27), the open-loop Bode diagrams of the average voltage and capacitor voltage balancing controls are shown in Fig. 6, in which the ranges of K_{p_av} and K_{p_bal} with sufficient phase margins that supposed to ensure the control stability are marked. Six groups of controller parameters for capacitor voltage control loops, as listed in Table III, are selected to verify the correctness and effectiveness of the control parameter design principle expressed in (25).

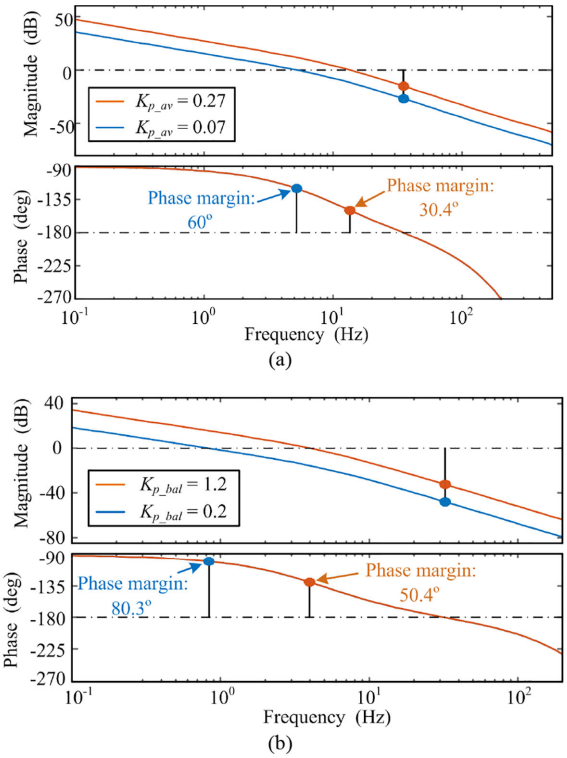

Fig. 6. Bode diagrams for capacitor voltage control loops. (a) Average voltage control loop. (b) Capacitor voltage balancing control loop.

V. Simulation and Experimental Results

A. Simulation Results

1) Control Parameter Design Principle Verification: A simulation of the single-phase MMC distributed control system in the piecewise linear electrical circuit simulation (PLECS) software, whose parameters are listed in Tables I–III, is conducted to verify the correctness and effectiveness of the proposed control parameter design principle in (25).

The simulation waveforms with control parameters listed in Table III are illustrated in Fig. 7. It can be seen in Fig. 7 that the MMC operates stably with the control parameters of group 1, 3, 4, and 6, where the control parameter design principle in (25) is satisfied. The SM capacitor voltages become divergent and the MMC system might become unstable with the control parameter of groups 2 and 5, where the phase margins of the control loops are theoretically still sufficient, but the inequality (25) is not satisfied. Moreover, as shown in Fig. 7, the output current regulating are rarely affected by the SM capacitor voltage diverging under the control parameters of groups 2 and 5, as long as the arm average capacitor voltages are not severely deteriorated and the capacitor voltages do not exceed the safe operating area (SOA) of the capacitor and switching devices. The MMC system has to shut down if the capacitor voltages approach the SOA of these devices to avoid catastrophic damages. In this case, the MMC is not able to operate normally and stably.

2) Eeffectiveness of Parameter Design Principle for Capacitor Voltage Control Loops With Different Control Delays: The effectiveness of (25) when the control delays of the average voltage loop and the balancing loop are different is verified by simulation results in this section.

TABLE III
Six Groups of Controller Parameters of Capacitor Voltage Loops

Group	Parameters	Phase margin	Is (25) satisfied?
1	K_{p_av}=0.09, K_{p_bal}=0.3	54.5°, 75.8°	yes
2	K_{p_av}=0.14, K_{p_bal}=0.3	44.6°, 71.7°	no
3	K_{p_av}=0.14, K_{p_bal}=0.48	44.6°, 68.7°	yes
4	K_{p_av}=0.19, K_{p_bal}=0.5	37.8°, 68°	yes
5	K_{p_av}=0.23, K_{p_bal}=0.5	33.7°, 68°	no
6	K_{p_av}=0.23, K_{p_bal}=0.8	33.7°, 58.9°	yes

TABLE IV
Three Groups of Control Parameters in Capacitor Voltage Control Loops

Group	Parameters	Is (25) satisfied?
1	K_{p_av}=0.07, K_{p_bal}=0.2	yes
2	K_{p_av}=0.12, K_{p_bal}=0.2	no
3	K_{p_av}=0.12, K_{p_bal}=0.3	yes

A time delay of 20 control cycles (i.e., $20T_s = 0.005$ s) is intentionally introduced into the average voltage control and balancing loops. The introduced control delay will reduce the stability margin of the two control loops. Therefore, the corresponding control parameters, i.e., K_{p_av} and K_{p_bal} have to be reselected. Three groups of capacitor voltage control parameters are listed in Table IV, which ensure adequate stability margin of the two capacitor voltage loops even with the additional 0.005 s control delay.

The simulation waveforms of SM capacitor voltages with three groups of control parameters in Table IV are shown in Fig. 8. Four different cases are considered in the simulation: **Case "00"**: no additional control delay is introduced in the two capacitor voltage loops; **Case "01"**: a 0.005 s control delay is introduced in the balancing loop; **Case "10"**: a 0.005 s control delay is introduced in the average voltage loop; **Case "11"**: a 0.005 s control delay is introduced in both capacitor voltage loops. It can be observed in Fig. 8 that the SM capacitor voltages in the four different cases are all stable with the control parameters of groups 1 and 3. The SM capacitor voltages are unbalanced with the control parameters of group 2, while (25) is not satisfied. Therefore, the control parameter design principle in (25) is still valid to effectively suppress the control conflicts in the distributed control system when different control delays exist in the two capacitor control loops.

B. Experimental Results

The experimental setup of an MMC shown in Fig. 9 is built in the laboratory. Due to the limited number of digital controllers, only one phase, whose structure is shown in Fig. 1 and parameters are listed in Tables I–III, is used to verify the correctness and effectiveness of the proposed control parameter

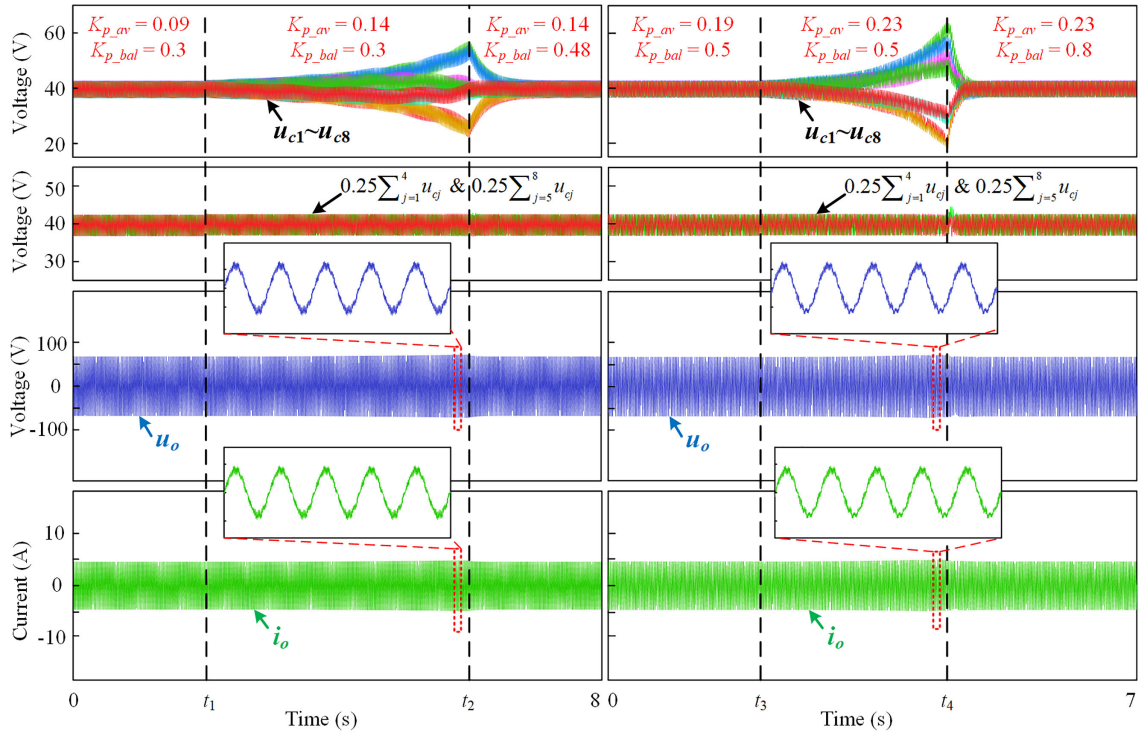

Fig. 7. Simulation waveforms of eight SM capacitor voltages, arm average capacitor voltages, output voltage, and current under six groups of control parameters.

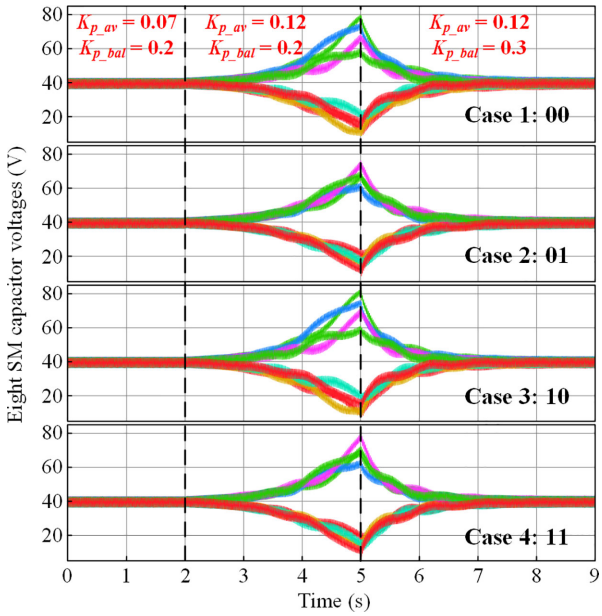

Fig. 8. Simulation waveforms of eight SM capacitor voltages with control parameters listed in Table IV.

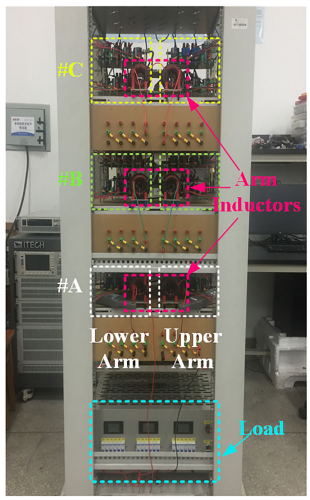

Fig. 9. Experimental setup of an MMC.

design principle in (25). A TMS320F28346 DSP is adopted as the central controller to perform the output current control. Two TMS320F28335 DSPs are employed as the local controllers to manage the four SMs in the upper and lower arms, respectively. The average voltage and capacitor voltage balancing control loops in local controllers are strictly implemented according to Fig. 2. An ITECH DC Power Supply IT6526D and a 15-Ω resistive load are adopted in this setup.

1) Steady-State Performance: The steady-state performance of the MMC distributed control system under the control parameters of group 3 ($K_{p\_\mathrm{av}}=0.14$, $K_{p\_\mathrm{bal}}=0.48$) is presented in Fig. 10. It can be seen from Fig. 10(a) that the output current tracks its reference accurately and its amplitude is stable at 4 A. Meanwhile, i_{diff} is regulated as almost a dc current with the help of the differential current control and the ripples in i_{diff} are effectively suppressed while normalizing the modulation signal by individual SM capacitor voltage. Moreover, the eight SM capacitor voltages are well balanced and are stable around 40 V, as shown in Fig. 10(b).

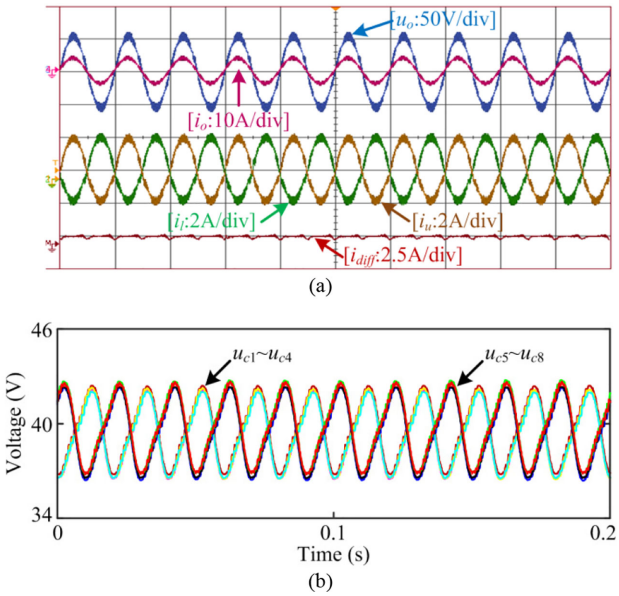

Fig. 10. Voltage and current waveforms of the MMC during the steady-state operation. (a) Output voltage and current, arm currents, differential current. (b) Capacitor voltages.

2) Control Parameter Design Principle and Arm Voltage Balancing Verification: The correctness of the parameter design principle expressed in (25) and effectiveness of balancing arm energy under the capacitor voltage control are illustrated in this set of experiments. The experimental waveforms of eight SM capacitor voltages and arm average capacitor voltages are shown in Fig. 11 with six groups of control parameters in Table III.

It can be seen from Fig. 11(a) that the system initially operates stably with the controller parameter of group 1. And the eight SM capacitor voltages start to differ from each other at t_1 when the controller parameters are switched from group 1 to group 2, while the phase margins of the control loops are theoretically still sufficient but the inequality in (25) is not satisfied. The MMC system resumes stable operation after t_2 when the controller parameters are switched from groups 2 to 3 with an even smaller phase margin. Similarly, it is clear in Fig. 11(b) that the SM capacitor voltages are stable under the controller parameters of groups 4 and 6. The MMC system cannot remain stable during the period of t_3–t_4 when the controller parameters of group 5 are utilized.

According to the theoretical analysis, the average voltage control and capacitor voltage balancing control contribute to balance the arm energy. As illustrated in Fig. 11, the upper and lower arm average capacitor voltages are well balanced with the controller parameters of groups 1, 3, 4, and 6 and are still basically balanced under the controller parameters of groups 2, 5 while the SM capacitor voltages are unbalanced and the MMC system turns to unstable.

VI. Conclusion

In this article, the control conflicts in an MMC distributed control system are analyzed and tackled to improve the system stability. The detailed model of the MMC distributed control system is proposed to cope with the complex coupling relation among control loops. The root cause of control conflict is presented by analyzing the coupling interactions among all control loops in the MMC distributed control system. It is revealed that the distributed average voltage controls essentially deteriorate the consistency of SM capacitor voltages. The caused control disturbances, if not suppressed by the capacitor voltage balancing controllers, might eventually lead to system instability. A control parameter design principle for capacitor voltage loops, which is obtained based on findings in this article, is proposed to inhibit the control conflicts. The correctness and effectiveness of the control loop coupling interactions, control conflict root cause analysis, and the parameter design principle is confirmed by the simulation and experimental results. The simulation and experimental results show that the system stability is guaranteed with sufficient capacitor voltage balancing capability against the control conflicts and adequate control loop phase margins.

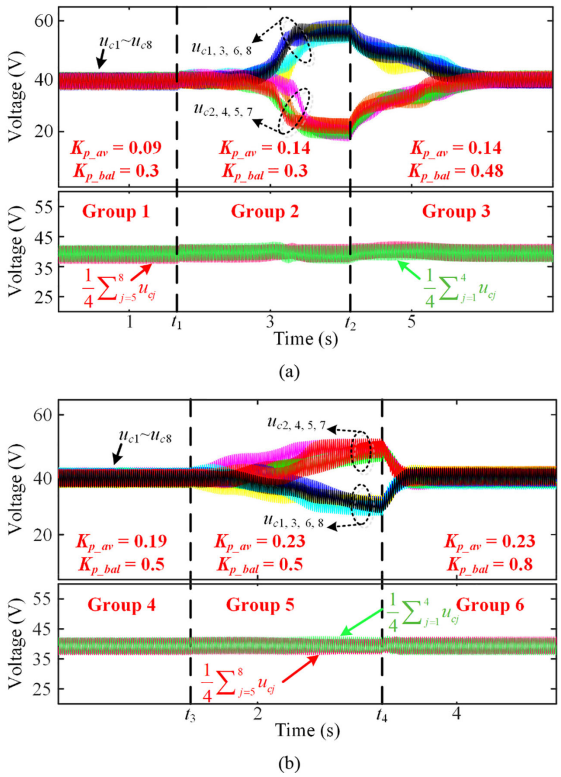

Fig. 11. Experimental waveforms of eight SM capacitor voltages and arm average capacitor voltages under six groups of control parameters. (a) Groups 1, 2, and 3. (b) Groups 4, 5, and 6.

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