Comprehensive Analysis and Experimental Validation of 240°-Clamped Space Vector PWM Technique Eliminating Zero States for EV Traction Inverters With Dynamic DC Link

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***Abstract*—A bus-clamping space vector pulsewidth modulation (PWM) called 240°-clamped PWM (240CPWM) is analyzed for three-phase converters that have a cascaded connection of a dc–dc stage and a dc–ac stage. A direct application of the proposed concept is electric vehicle (EV) traction inverters that employ a dc–dc stage to interface a relatively low-voltage battery to a high-voltage motor. The 240CPWM method has the major advantages of clamping a phase to the positive or negative rail for 240° in a fundamental period, clamping of two phases simultaneously at any given instant, and use of only active states, completely eliminating the use of zero states. These characteristics lead to more than seven times reduction in switching losses of the inverter at unity power factor compared to CSVPWM, comparable or better total harmonic distortion (THD) performance, significant reduction in common-mode voltage and high efficiency. The THD of the line current is analyzed using the notion of stator flux ripple and compared with conventional and discontinuous PWM methods. The switching loss characteristics under different power factor conditions are discussed. Experimental results from a 10-kW hardware prototype are presented. The full load efficiency with the proposed 240CPWM for the dc–ac stage exceeds 99% even with Si insulated-gate bipolar transistors (IGBTs).**

***Index Terms*—240°-clamped pulsewidth modulation (PWM) (240CPWM), discontinuous PWM, dynamic dc link, electric vehicle (EV), PWM, space vector, switching loss, total harmonic distortion (THD), traction drive, voltage source inverter (VSI).**

I. Introduction

EXTENSIVE research and development in the area of electric vehicle (EV) traction systems has established the significant advantages of a cascaded architecture for the traction drive comprising of a dc–dc stage followed by a dc–ac stage [1]–[7]. Employing a dc–dc converter enables to adjust the voltage of the battery pack and electric machine individually, leading to design flexibility that may improve power density and efficiency and reduce cost of the drivetrain [8]–[11].

Fig. 1(a) shows the EV powertrain architecture with a dc–dc converter that interfaces a relatively low-voltage battery to the inverter and the high-voltage motor. This cascaded topology in EV drivetrain supports higher dc-link voltages due to which the motor speed has increased from 6000 to 17 000 r/min over the years; reducing the size of motor and inverter thereby increasing the power density [12]. Commercial EVs particularly hybrid EVs (HEVs) have developed mature architecture to interface battery and inverter dc bus via bidirectional dc–dc converter [13]–[16]. This cascaded topology is used in various commercial vehicles such as Toyota Prius [13], Lexus LS 600h [14], Toyota Camry [15], and Honda Accord Hybrid [16].

Such a system with dc–dc converter already in place lends itself very well to the implementation of the 240°-clamped space vector pulsewidth modulation (PWM) (240CPWM). The dc-link voltage at the output of the dc–dc stage is controlled dynamically both in magnitude and in waveshape corresponding to the motor speed. The required dc-link voltage for 240CPWM for three different speeds is also shown in Fig. 1(b)–(d), as an example. This particular shape of the dc-link voltage for 240CPWM is explained and derived in Section II.

The dc–ac stage is a three-phase voltage source inverter (VSI), switched suitably to generate variable magnitude, and variable frequency sinusoidal output voltages. The control is achieved by various PWM techniques discussed in the literature [17]. The specific PWM technique used impacts the THD in the line current, switching losses, and common mode voltage (CMV). A two-level, three-phase VSI has eight switching states as shown in Fig. 2. The reference voltage vector $\boldsymbol{V}_{\mathrm{REF}}$ is sampled once in every subcycle, T_s. Conventionally, for $\boldsymbol{V}_{\mathrm{REF}}$ having angle α in Sector I, the active vectors 1, 2, and zero vectors are applied for durations T_1, T_2, and T_z, respectively.

Conventional space vector PWM (CSVPWM) uses both the zero states (0 and 7) and divides T_z equally between them. It employs the switching sequence of 0127 (or 7210) in a subcycle

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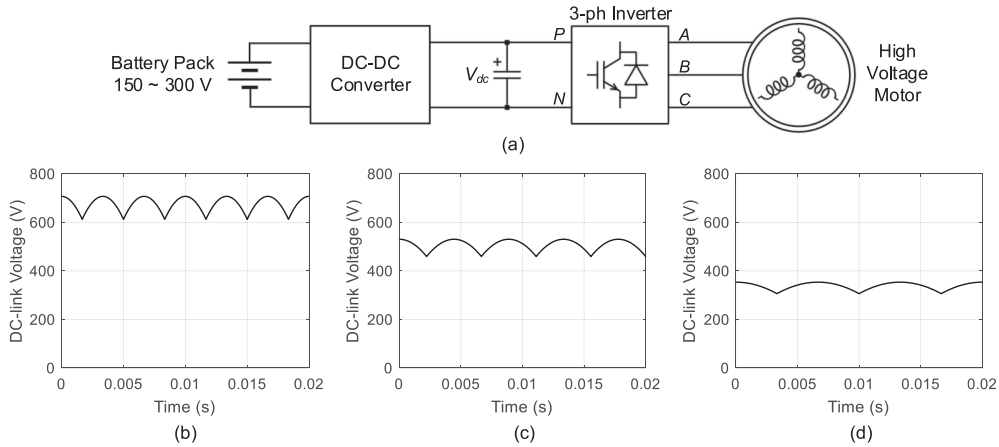

Fig. 1. EV powertrain architecture. (a) Block diagram; proposed dc-link voltage for (b) high speed, (c) medium speed, (d) low-speed operation.

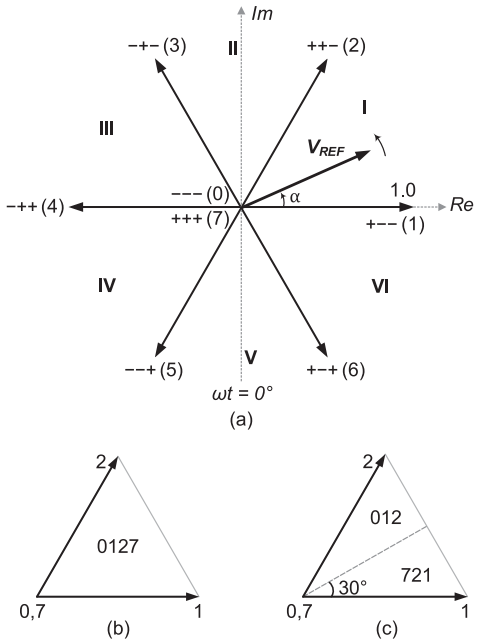

Fig. 2. (a) Voltage vectors produced by a two-level VSI. Switching sequence of (b) CSVPWM and (c) DPWM1 in Sector I. I–VI are sector numbers and ωt is angle of phase A fundamental voltage.

in Sector I. The total number of switchings in a subcycle with both the zero states applied is three. The discontinuous PWM (DPWM) methods employ only one zero state resulting in two switchings per subcycle. Several DPWM sequences have been discussed in the literature [17], [18]. CSVPWM results in lower distortion in line current whereas DPWM leads to a reduction in switching loss at the expense of increased switching frequency ripple and total harmonic distortion (THD) [18]–[20]. For the purpose of evaluation and comparison, we will consider the 120° clamping PWM and refer it as DPWM1, which employs sequences 721 (or 127) in the first 30° of Sector I and 012 (or 210) in the next 30° of Sector I. The switching sequence in a subcycle for CSVPWM and DPWM1 in Sector I are shown in Fig. 2.

CMV is an important metric in motor drives and other three-phase applications. An accepted CMV metric in a star-connected three-phase electric machine is defined as the voltage between the load star point to the center of dc bus which is given by $(v_{Ao} + v_{Bo} + v_{Co})/3$, where v_{Ao}, v_{Bo}, and v_{Co} are the three-phase voltages of inverter with respect to dc bus center point [21]. The use of zero vectors makes the maximum values of CMV to be $+V_{\rm dc}/2$ or $-V_{\rm dc}/2$ corresponding to vectors 7 and 0, respectively. If zero vectors are fully eliminated, the peak CMV can be reduced to $+V_{\rm dc}/6$ [22]. Several methods have been proposed to avoid the use of zero vectors; as stated in [22] only the active zero-state PWM (AZSPWM) [23] and near-state PWM (NSPWM) [24] are viable methods for practical applications. The AZSPWM uses two active vectors and two opposing active vectors over equal duration to create an effective zero state. The main drawbacks are that it results in bipolar line–line voltage and causes overvoltages at motor terminals. The NSPWM also causes bipolar line–line voltages and has also a restricted range of modulation index. Both the schemes result in higher number of switchings and higher distortion in line currents than conventional DPWM. The 240CPWM method eliminates zero states completely while having the minimum possible number of switchings of any PWM method, desirable unipolar voltage waveforms, and among the lowest THD (high-frequency ripple) in the line currents.

A double 120° flat-top modulation method has been proposed in [25] for a grid-connected photovoltaic (PV) inverter, in which a similar dc-link voltage waveform was established indirectly by regulating the dc-link current. Based on the same concept, a pulsewidth-amplitude-modulation method was proposed in [26] where comparison with SPWM was presented. A concept similar to the 240CPWM method with dynamically varying dc link corresponding to rectifier operation in battery chargers has been reported recently in [27] with only simulation results.

The major contributions of this article are summarized as follows:

1) space vector as well as carrier-based approach of the 240CPWM method;
2) derivation of the required dynamic dc-link voltage from the perspective of avoiding zero states;
3) comprehensive analysis on THD using the concept of stator flux ripple and switching loss and comparison with other PWM methods;

4) hardware results of the two-stage drive system at a power level of 10 kW with the highest dc-link voltage of 800 V covering a range of fundamental frequency from 25 to 150 Hz. The experimental results in terms of loss reduction, THD, and CMV reduction match very well with analysis.

This article is organized as follows. Section II discusses the modulation concept (240CPWM) and derivation of the unique dynamic dc-link voltage required for it. It also elaborates on the implementation of 240CPWM using space vectors as well as carrier based equivalent approach. Section III provides an in-depth analysis of THD based on stator flux ripple for 240CPWM and compares it with the performance of other PWM methods. The different PWM methods are analyzed in terms of switching loss characteristics at different power factors and the superiority of 240CPWM is shown in Section IV. The theoretical predictions are validated by using a hardware prototype presented in Section V. Section VI summarizes the conclusion and future work.

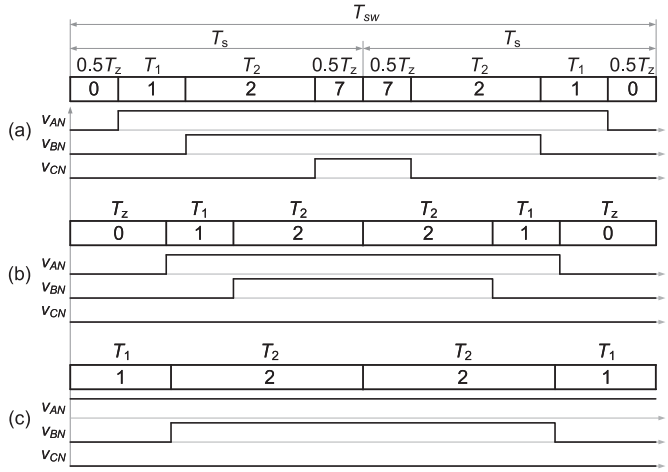

Fig. 3. Switching sequences in Sector I and the corresponding phase voltages in a switching cycle for (a) CSVPWM, (b) DPWM1, and (c) 240CPWM. Note that the durations T_1 and T_2 will be different for the 240CPWM compared to the other PWM methods due to the dynamically variable dc link.

II. The 240CPWM Concept

In order to synthesize a sinusoidal output voltage with a dc–ac inverter, one can control the modulating signal to be sinusoidal when the dc-link voltage is fixed, or control the dc-link voltage to be sinusoidal and the modulating signal to be constant. When the dc-link voltage is dynamically controlled to have a (piece-wise) sinusoidal waveshape, the modulating signal can be clamped at corresponding intervals to connect that dc-side sine-wave to the line-to-line output.

240CPWM is a space vector modulation concept that allows clamping of two-phase poles simultaneously. Each phase pole is clamped to positive or negative dc rails for a total of 240° covering four sectors, and switched only for 120° in each fundamental cycle. This is achieved by using only the two active vectors to synthesize the required reference vector in any sector. With the applied sequence of 12 in Sector I, 23 in Sector II, 34 in Sector III, and so on, phase A is clamped to positive dc rail in Sectors I and VI, it is clamped to negative dc rail in Sectors III and IV and switches only in Sectors II and V. Thus, phase A is clamped for 240° because it is fixed to either positive or negative dc rail in four sectors in a fundamental cycle. Similarly, phases B and C are also clamped for 240° and switched for only 120° in a line cycle.

Fig. 3 shows the switching sequences employed in Sector I for CSVPWM, DPWM1, and 240CPWM and their corresponding phase voltages, where T_s denotes the subcycle duration and $T_{\rm sw}$ corresponds to the switching cycle duration. The number of switchings for CSVPWM in a switching cycle is two per phase, or six for all three phases. For DPWM1, the number of switchings in phases A and B is also two each. However, clamping of phase C results in a total of four switching actions instead of six. The switching sequences 12–21 for 240CPWM are shown in Fig. 3(c). It can be seen that phase A is clamped to positive dc rail, phase C to negative dc rail, and switching of phase B results in only two switching actions in a switching cycle. Hence, 240CPWM achieves the least possible number of switchings.

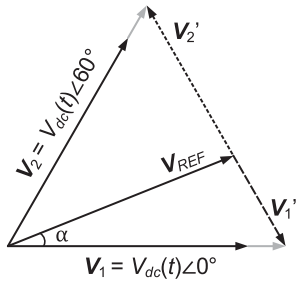

Fig. 4. Sector I of space vector plane for 240CPWM. $\boldsymbol{V}_{\rm REF}$: reference voltage vector. $\boldsymbol{V}_1$ and $\boldsymbol{V}_2$: applied voltage vectors with time-varying magnitude. $\boldsymbol{V}_1'$ and $\boldsymbol{V}_2'$: error voltage vectors.

A constant dc-link voltage is used in conventional inverter operation. However, the goal of complete elimination of zero states in 240CPWM cannot be achieved with a constant dc-link voltage. A unique and dynamic dc-link voltage varying both in average and instantaneous sense is required to achieve undistorted sinusoidal output voltages using only the active states, which is derived as follows.

Fig. 4 shows the Sector I of space vector plane for 240CPWM, where the regions corresponding to gray arrows represent the variable magnitudes of vectors $\boldsymbol{V}_1$ and $\boldsymbol{V}_2$. The main differences from that of other PWM shown in Fig. 2 are that the magnitude of the voltage vectors $\boldsymbol{V}_1$ and $\boldsymbol{V}_2$ are now functions of time corresponding to the dc link, and zero states 0 or 7 are not used. The magnitude of $\boldsymbol{V}_{\rm REF}$ is a constant corresponding to operation at maximum modulation index. The modulation index is defined as $M_i = V_{\rm REF}/V_{\rm dc}, 0 \le M_i \le M_{\max} = 0.866$ where $V_{\rm REF}$ is defined as $V_{\rm REF} = \sqrt{3}V_{\rm LL,pk}/2$, $V_{\rm dc}$ is the dc-link voltage, and $V_{\rm LL,pk}$ is the peak value of the reference line-to-line voltage. The angle α is given by $\alpha = [(\omega t - 90°) \bmod 60°]$, where $\omega = 2\pi f_1$ is the angular fundamental frequency. Similar

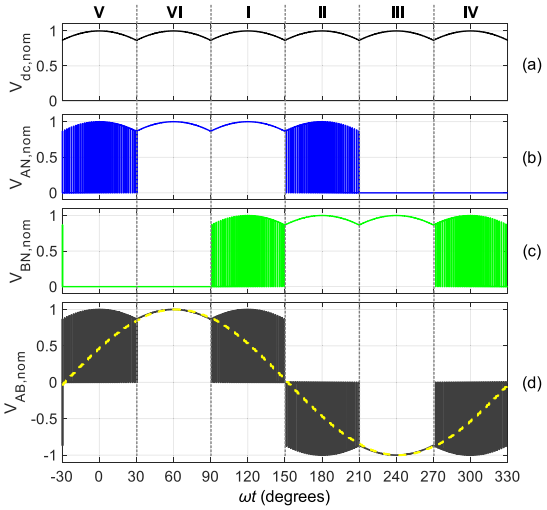

Fig. 5. (a) DC-link voltage, (b) phase A voltage, (c) phase B voltage, (d) instantaneous (solid) and average (dashed) line to line voltage with the 240CPWM technique, all normalized with respect to $V_{\mathrm{LL,pk}}$. The corresponding Sector numbers (I–VI) are also shown.

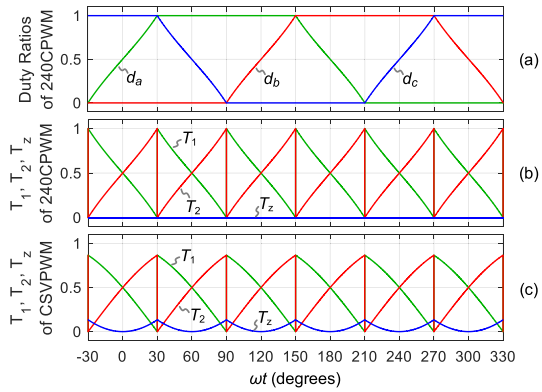

Fig. 6. (a) Duty ratios of individual phases with the 240CPWM technique. Normalized time durations of the voltage vectors (with respect to a subcycle T_s) of the (b) 240CPWM technique and (c) CSVPWM technique.

to the conventional PWM methods, the durations T_1 and T_2 over which the vectors $\boldsymbol{V}_1$ and $\boldsymbol{V}_2$ are, respectively, applied in each subcycle can be derived from Fig. 4 as given as follows. These equations are similar to the other PWM methods except that V_{dc} is varying for 240CPWM

$$T_1 = \frac{V_{\mathrm{REF}}}{V_{\mathrm{dc}}(t)} \frac{\sin(60^\circ - \alpha)}{\sin 60^\circ} T_s \tag{1}$$

$$T_2 = \frac{V_{\mathrm{REF}}}{V_{\mathrm{dc}}(t)} \frac{\sin \alpha}{\sin 60^\circ} T_s. \tag{2}$$

The condition for eliminating the zero states is given by

$$T_z = T_s - T_1 - T_2 = 0. \tag{3}$$

Using (1)–(3), we get

$$\frac{V_{\mathrm{REF}}}{V_{\mathrm{dc}}(t)} \left(\frac{\sin(60^\circ - \alpha)}{\sin 60^\circ} + \frac{\sin \alpha}{\sin 60^\circ} \right) = 1. \tag{4}$$

Using $V_{\mathrm{REF}} = \frac{\sqrt{3}}{2} V_{\mathrm{LL,pk}}$ in (4) and simplifying the trigonometric identities, we get expression for the required dynamic dc-link voltage

$$V_{\mathrm{dc}}(t) = V_{\mathrm{LL,pk}} \left(\tfrac{\sqrt{3}}{2} \cos \alpha + \tfrac{1}{2} \sin \alpha \right) = V_{\mathrm{LL,pk}} \cos(30^\circ - \alpha). \tag{5}$$

This dynamically varying dc-link voltage is a six pulse waveform in a line cycle that varies from $\sqrt{3} V_{\mathrm{LL,pk}}/2$ for $\alpha = 0^\circ$ to $V_{\mathrm{LL,pk}}$ for $\alpha = 30^\circ$ and back to $\sqrt{3} V_{\mathrm{LL,pk}}/2$ for $\alpha = 60^\circ$ in Sector I. Fig. 5 shows the dynamic dc-link voltage, phases A and B output voltages and output line to line voltage, all normalized with respect to $V_{\mathrm{LL,pk}}$, for 240CPWM. During the interval $30^\circ < \omega t < 90^\circ$, both phases A and B are clamped—phase A to the positive rail and phase B to the negative rail. Hence, v_{AB} is same as the dc-link voltage for this entire sector. Therefore, the dc link needs to follow exactly the required sinusoidal v_{AB} in this interval; and the same pattern repeats for the other sectors.

The dynamic dc-link voltage is generated by the front-end dc–dc stage. The expression for the dynamic dc-link voltage can be equivalently given as (6), which corresponds to the dc link requirement derived in (5) for Sector I

$$V_{\mathrm{dc}}(t) = \max\{v_a, v_b, v_c\} - \min\{v_a, v_b, v_c\} \tag{6}$$

where v_a, v_b, and v_c are the reference phase voltages.

The 240CPWM has an equivalence in carrier-based PWM approach as well, as long as the dc-link voltage is given by (5). In this case, the modulating signals that are compared with a triangle carrier to generate the PWM signals with required duty ratios are given as follows and are shown in Fig. 6(a)

$$d_a = [v_a - \min\{v_a, v_b, v_c\}]/V_{\mathrm{dc}}(t) \tag{7a}$$

$$d_b = [v_b - \min\{v_a, v_b, v_c\}]/V_{\mathrm{dc}}(t) \tag{7b}$$

$$d_c = [v_c - \min\{v_a, v_b, v_c\}]/V_{\mathrm{dc}}(t). \tag{7c}$$

Fig. 6(b) shows the time durations T_1, T_2, and T_z of the 240CPWM technique. It is evident that T_z is always zero, which means that the zero vector is not applied. For comparison, Fig. 6(c) shows the time durations of the CSVPWM technique, which has nonzero T_z values even at maximum modulation index.

III. Analytical Evaluation and Comparison of Harmonic Distortion Based on Stator Flux Ripple

Analytical evaluation of harmonic distortion for various space vector based PWM techniques including conventional [28], discontinuous [29], and hybrid PWM methods [19], [30], [31] using the notion of stator flux ripple has been elaborated in the literature.

In this section, we will analyze the harmonic distortion based on stator flux ripple for 240CPWM and compare with the existing techniques. The first step is to calculate the error voltage vector between applied and reference vector, which is then integrated to get stator flux ripple. Due to symmetry of the three-phase voltage waveforms, it is sufficient to perform the analysis only for Sector I. Typically, use of at least one zero state in switching sequences ensures that the magnitude of stator flux

ripple is zero at start and end of the subcycle. However, the zero states are entirely bypassed in 240CPWM due to which zero stator flux ripple at start and end of a sector is achieved only if the error vectors $\boldsymbol{V}_1'$ and $\boldsymbol{V}_2'$ corresponding to the applied vectors $\boldsymbol{V}_1$ and $\boldsymbol{V}_2$ are antiparallel to each other.

The magnitude of the reference vector $\boldsymbol{V}_{\rm REF}$ at any instant is constant given by $\sqrt{3}V_{\rm LL,pk}/2$ and its position changes with α. By definition, the amplitude of applied vectors $\boldsymbol{V}_1$ and $\boldsymbol{V}_2$ is equal to $V_{\rm dc}$, which for the 240CPWM method is dynamically controlled and varying from $\sqrt{3}V_{\rm LL,pk}/2$ at $\alpha = 0^\circ$ to $V_{\rm LL,pk}$ at $\alpha = 30^\circ$ and back to $\sqrt{3}V_{\rm LL,pk}/2$ for $\alpha = 60^\circ$ as described in previous section. Hence, amplitudes of $\boldsymbol{V}_1$ and $\boldsymbol{V}_2$ are taken as $V_{\rm dc} = V_{\rm LL,pk}\cos(30^\circ - \alpha)$ and their positions are fixed at 0° and 60°, respectively, as shown in Fig. 4 where the regions corresponding to gray arrows represent the variable magnitudes of $\boldsymbol{V}_1$ and $\boldsymbol{V}_2$ from $\sqrt{3}V_{\rm LL,pk}/2$ to $V_{\rm LL,pk}$. The expressions for the error voltage vectors $\boldsymbol{V}_1'$ and $\boldsymbol{V}_2'$ can be derived as shown in in the following equation, which confirm that the two error vectors are antiparallel to each other for any angle α in the proposed 240CPWM

$$\begin{aligned}\boldsymbol{V}_1' &= \boldsymbol{V}_1 - \boldsymbol{V}_{\rm REF}\\ &= V_{\rm dc}(t)\angle 0^\circ - \frac{\sqrt{3}}{2}V_{\rm LL,pk}\angle\alpha\\ &= V_{\rm LL,pk}\sin(\alpha)\angle -60^\circ \qquad (8)\\ \boldsymbol{V}_2' &= \boldsymbol{V}_2 - \boldsymbol{V}_{\rm REF}\\ &= V_{\rm dc}(t)\angle 60^\circ - \frac{\sqrt{3}}{2}V_{\rm LL,pk}\angle\alpha\\ &= V_{\rm LL,pk}\cos(\alpha+30^\circ)\angle 120^\circ. \qquad (9)\end{aligned}$$

The corresponding error volt–second quantities in the synchronously revolving dq reference frame are given by the following equations, and the two add up to zero satisfying the volt–second balance between applied vectors and reference in space vector PWM

$$\begin{aligned}\boldsymbol{V}_1'T_1 &= V_{\rm dc}(t)\sin(\alpha)T_1\\ &\quad + jV_{\rm dc}(t)[\cos(\alpha) - V_{\rm REF}]T_1\\ &\triangleq D + jQ_1 \qquad (10)\\ \boldsymbol{V}_2'T_2 &= -V_{\rm dc}(t)\sin(60^\circ - \alpha)T_2\\ &\quad + jV_{\rm dc}(t)[\cos(60^\circ - \alpha) - V_{\rm REF}]T_2\\ &= -D - jQ_1. \qquad (11)\end{aligned}$$

The time integral of error voltage vectors is called as "stator flux ripple" vector, which is a measure of ripple in line current. The stator flux ripple diagrams in a synchronously revolving dq reference frame for all three sequences under consideration for $\alpha = 10^\circ$ and $V_{\rm REF} = \sqrt{3}/2$ (i.e., normalized with respect to $V_{\rm LL,pk}$) are shown in Fig. 7. The use of at least one zero state in CSVPWM and DPWM1 results in a triangular trajectory of volt–second balanced quantities in the dq reference frame to ensure zero stator flux ripple at start and end of a subcycle. However, the volt–second vectors in 240CPWM are antiparallel

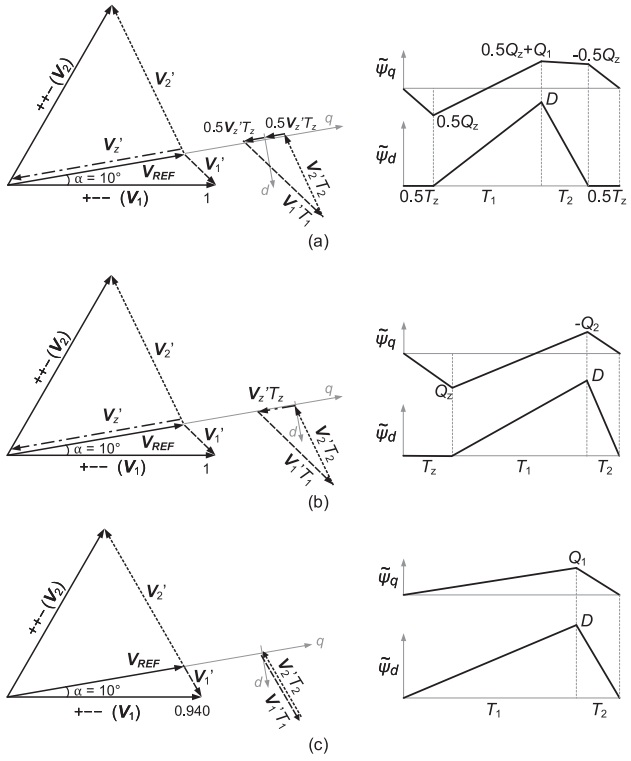

Fig. 7. Stator flux ripple over a subcycle and its components along d-axis and q-axis for $\alpha = 10^\circ$ for (a) CSVPWM, (b) DPWM1, and (c) 240CPWM.

with the same length, assuring zero stator flux at start and end of subcycle.

The d-axis ripple ($\widetilde{\psi}_{d,240C}$) and q-axis ripple ($\widetilde{\psi}_{q,240C}$) in different intervals are defined as follows:

$$\widetilde{\psi}_{d,240C} = \begin{cases}\frac{D}{T_1}t, & 0 \le t < T_1\\ D - \frac{D}{T_2}(t - T_1), & T_1 \le t \le T_1 + T_2\end{cases} \qquad (12)$$

$$\widetilde{\psi}_{q,240C} = \begin{cases}\frac{Q_1}{T_1}t, & 0 \le t < T_1\\ Q_1 - \frac{Q_1}{T_2}(t - T_1), & T_1 \le t \le T_1 + T_2.\end{cases} \qquad (13)$$

The root mean square (rms) stator flux ripple over a subcycle for 240CPWM ($\widetilde{\psi}_{240C,\rm rms}$) then becomes

$$\begin{aligned}\widetilde{\psi}_{240C,\rm rms} &= \sqrt{\frac{1}{T_s}\int_0^{T_s}\widetilde{\psi}_{d,240C}^2\,{\rm d}t + \frac{1}{T_s}\int_0^{T_s}\widetilde{\psi}_{q,240C}^2\,{\rm d}t}\\ &= \sqrt{\frac{D^2 + Q_1^2}{3}}. \qquad (14)\end{aligned}$$

Stator flux ripple and its components along d- and q-axis are drawn for 240CPWM with $\alpha = 30^\circ$ and $\alpha = 45^\circ$ to further validate that $\boldsymbol{V}_1'$ and $\boldsymbol{V}_2'$ remain antiparallel irrespective of α as shown in Fig. 8. For both the cases, magnitude of $\boldsymbol{V}_{\rm REF}$ remains constant but the magnitude of the applied vectors are varying, i.e., $V_1 = V_2 = 1$ for $\alpha = 30^\circ$ and $V_1 = V_2 = 0.966$ for $\alpha = 45^\circ$ all normalized to $V_{\rm LL,pk}$.

The rms stator flux ripple for CSVPWM and DPWM1 have been thoroughly discussed in [30] and [31] and we will use their well-established stator flux ripple expressions for the purpose

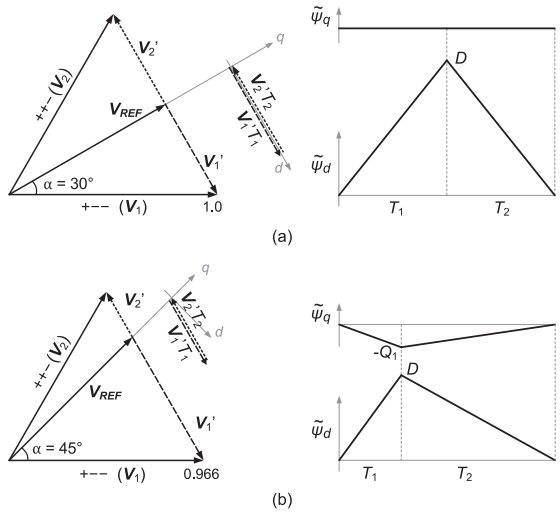

Fig. 8. Stator flux ripple over a subcycle and its components along d-axis and q-axis for 240CPWM for (a) $\alpha = 30°$, (b) $\alpha = 45°$. Note that the magnitude of $\boldsymbol{V}_1$ and $\boldsymbol{V}_2$ changes with α as given in (5).

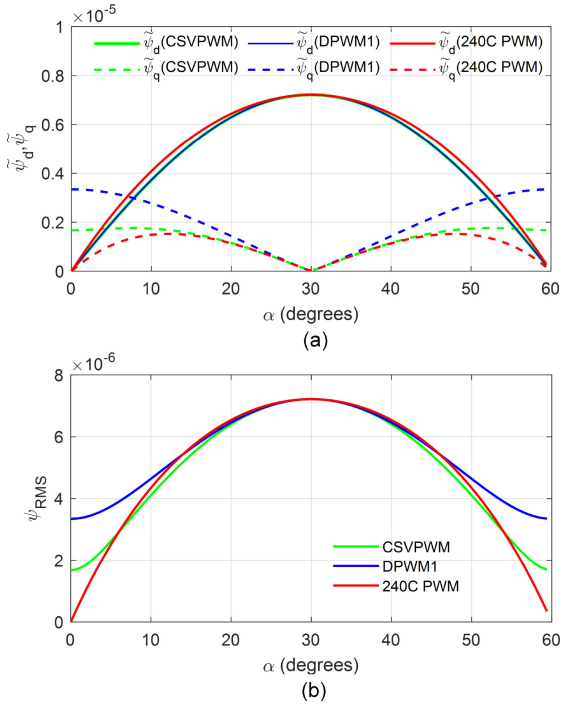

Fig. 9. Comparison of stator flux ripple over a sector for 240CPWM, CSVPWM, and DPWM1 assuming $f_{\rm sw} = 10$ kHz. (a) d- and q-axis ripple. (b) Total rms stator flux ripple.

of comparison. Based on the expressions, the dq axis ripple and total rms stator flux ripple of CSVPWM and DPWM1 are compared with those of 240CPWM for α $(0° < \alpha < 60°)$ considering the same instantaneous switching frequency of $f_{\rm sw}$. Thus, the average switching frequency of DPWM1 becomes $2f_{\rm sw}/3$ and for 240CPWM, it is $f_{\rm sw}/3$. It can be seen from Fig. 9(a) that the d-axis ripple for all the three techniques is almost equal. However, the q-axis ripple for 240CPWM converges to zero at the start and end of sector while it has a diverging pattern for DPWM1 and CSVPWM. The total rms stator flux ripple for 240CPWM is less for $(0° < \alpha < 6°)$ and $(54° < \alpha < 60°)$ and it is comparable to CSVPWM for $(6° < \alpha < 54°)$, as shown in Fig. 9(b). Moreover, stator flux ripple for all the switching sequences is minimum for $\alpha = 0°$ and $\alpha = 60°$ because the reference vector is close to one of the applied vectors that reduces one of the error vectors.

The rms harmonic distortion factor based on stator flux ripple, $F_{\rm DIST}$ is calculated by normalizing rms stator flux ripple over a sector with respect to the fundamental flux, ψ_1 [30]. $F_{\rm DIST}$ is a measure of THD of the line current

$$F_{\rm DIST} = \frac{\widetilde{\psi}_{\rm SEQ,rms}}{\psi_1}, \psi_1 = \frac{V_{\rm REF}}{2\pi f_1} \tag{15}$$

$$F_{\rm DIST} = \frac{1}{\psi_1}\sqrt{\frac{3}{\pi}\int_0^{\frac{\pi}{3}} \widetilde{\psi}^2_{\rm SEQ,rms}(\alpha)\, {\rm d}\alpha} \tag{16}$$

where $\widetilde{\psi}_{\rm SEQ,rms}$ is the rms stator flux ripple for the sequence under consideration and f_1 is the fundamental frequency. The relation between $F_{\rm DIST}$ and THD in line current is given by

$$\text{THD}_i = \left(\frac{V_{\rm REF}}{\sqrt{6}LI_{1,\rm rms}2\pi f_1}\right) F_{\rm DIST}. \tag{17}$$

The factor $\sqrt{6}$ serves to convert the line-to-line peak value of $V_{\rm REF}$ to line-to-neutral rms value that is required for calculating THD in line current. L is the load inductance in our case. However, it will be the inductance of motor when three-phase motor is used as a load.

In the analysis below, typical constant V/f mode of variable speed drives with constant load current is used to compare the characteristics of different PWM methods, where the fundamental voltage is proportional to the fundamental frequency. The CSVPWM method with constant dc-link voltage will be used as benchmark. DPWM1 and CSVPWM will be analyzed both with constant and varying dc-link voltage and 240CPWM will be analyzed only for dynamic dc-link voltage, since the very concept of this technique holds true for varying dc-link voltage only. For the cases with constant $V_{\rm dc}$, the modulation index is adjusted proportionally for different fundamental frequencies, while the other three cases with varying $V_{\rm dc}$ are evaluated using maximum modulation index $M_{\rm max}$, in order to maintain the same load current at different fundamental frequencies. The harmonic distortion based on stator flux ripple $F_{\rm DIST}$ of different modulation methods is calculated as a function of fundamental frequency and normalized with respect to the stator flux ripple of CSVPWM at maximum fundamental frequency $f_{1,\rm max}$. The results are shown in Fig. 10. It can be observed from Fig. 10 that all the PWM methods with variable dc-link voltage have similar and lower $F_{\rm DIST}$ for the full range of fundamental frequency. It may be emphasized that 240CPWM achieves this with just one-third number of switchings compared to CSVPWM and half compared to DPWM1. The DPWM1 with constant dc link has the highest $F_{\rm DIST}$.

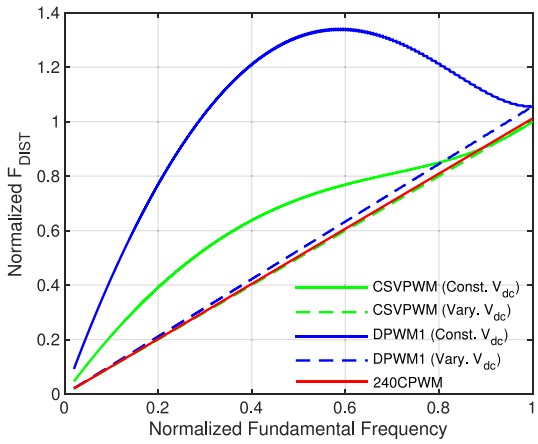

Fig. 10. Normalized F_{DIST} as a function of the normalized fundamental frequency. F_{DIST} is normalized with respect to the stator flux ripple distortion of CSVPWM at $f_{1,\max}$. The fundamental frequency is normalized with respect to $f_{1,\max}$.

TABLE I
NUMBER OF SWITCHINGS IN A PHASE IN SECTOR I

Technique		n_A	n_B	n_C
CSVPWM		1	1	1
DPWM1	721	0	1	1
	012	1	1	0
240CPWM		0	1	0

IV. ANALYTICAL EVALUATION AND COMPARISON OF SWITCHING LOSS

The total switching loss of the three-phase inverter over a line cycle can be reduced by minimizing the switching loss in every subcycle. Switching loss in a subcycle depends on dc-link voltage V_{dc}, number of switchings in a phase n_{PH} and the current flowing through the switch i_{PH}. The contribution of current ripple to switching loss is ignored since it is very small. To compare different PWM methods in terms of switching loss, the simplest way is to compare the product of number of switchings in a phase, the dc-link voltage and the instantaneous current flowing through the switch in each subcycle. Considering phase A, its fundamental current can be normalized with respect to its peak value I_m to produce normalized per phase switching loss $P_{\mathrm{SUB,PH}}$

$$P_{\mathrm{SUB,PH}} = V_{\mathrm{dc,nom}} \frac{n_{\mathrm{PH}} |i_{\mathrm{PH}}|}{I_m} = V_{\mathrm{dc,nom}} n_{\mathrm{PH}} |\sin(\omega t + \phi)| \tag{18}$$

where ϕ is the power factor angle and $V_{\mathrm{dc,nom}}$ is the dc-link voltage normalized to its peak value. The number of switchings in a phase depends on the specific PWM method used. For CSVPWM, each phase switches once in a subcycle while for DPWM1, a phase either switches once or does not switch at all in a subcycle. Table I shows the three modulation methods under consideration in terms of number of switchings in a phase in Sector I.

Detailed analysis of $P_{\mathrm{SUB,PH}}$ for various bus clamping techniques is carried out in [18]. Here, we present the variation of $P_{\mathrm{SUB,PH}}$ for CSVPWM, DPWM1, and 240CPWM at two

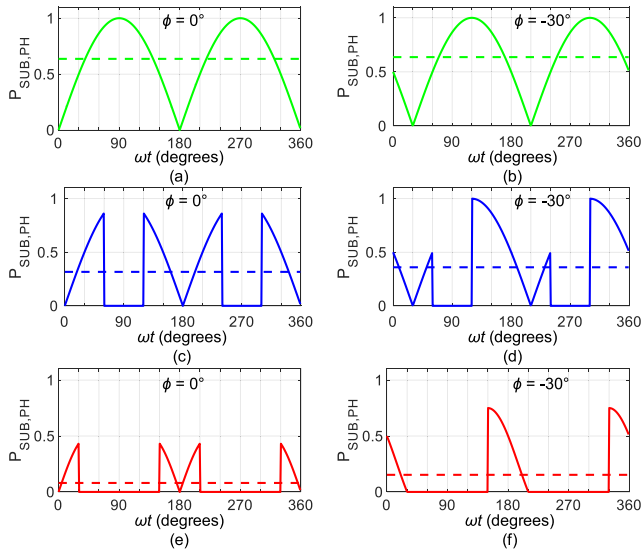

Fig. 11. Variation of normalized local switching loss in phase A over a line cycle $P_{\mathrm{SUB,PH}}$. (a) CSVPWM, $\phi = 0°$. (b) CSVPWM, $\phi = -30°$. (c) DPWM1, $\phi = 0°$. (d) DPWM1, $\phi = -30°$. (e) 240CPWM, $\phi = 0°$. (f) 240CPWM, $\phi = -30°$.

different power factor angles. $P_{\mathrm{SUB,PH}}$ for CSVPWM is just a rectified sine function of unit magnitude with average of $2/\pi$ (i.e., 0.637) in a line cycle [see Fig. 11(a)]. $P_{\mathrm{SUB,PH}}$ for CSVPWM only shifts depending on the power factor angle, but its average remains the same [see Fig. 11(b)]. For DPWM1, a phase is clamped for $\omega t \in [60°, 120°] \cup [240°, 300°]$, which is near the current peaks for a total of 120° in line cycle at unity power factor [see Fig. 11(c)]. Thus, average of $P_{\mathrm{SUB,PH}}$ for DPWM1 is lower than CSVPWM. At power factor angle of $-30°$ (30° lagging), averaged $P_{\mathrm{SUB,PH}}$ for DPWM1 is slightly higher than that for unity power factor due to nonideal positions of phase clamping, i.e., clamping near current peaks is not there anymore. In fact, some switching can be seen near current peaks in Fig. 11(d).

It can be observed from Fig. 11(e) that in 240CPWM, a phase switches only for $\omega t \in [0°, 30°] \cup [150°, 210°] \cup [330°, 360°]$, which is near the zero crossings of the phase current for a total of 120° and remains clamped for the remaining 240°, which happens to be the current peaks at unity power factor. This is an ideal scenario of switching to achieve minimum possible switching loss. That is why average of $P_{\mathrm{SUB,PH}}$ for 240CPWM is only 0.08, which is around eight times lower than that of CSVPWM. Now for nonunity power, 240CPWM still yields savings in switching loss as compared to CSVPWM but the extent of savings is a function of power factor angle. At power factor angle of 30° lagging, each phase still switches near zero crossing of current and remains clamped near current peaks with 240CPWM [see Fig. 11(f)]. 240CPWM outperforms CSVPWM and other clamped sequences too because it is effectively switching, in an average sense, only at one third of the switching frequency.

$P_{\mathrm{SUB,PH}}$ for all the three phases are added to give normalized total switching loss in a subcycle $P_{\mathrm{SUB,TOT}}$. $P_{\mathrm{SUB,TOT}}$ is in fact the product of the normalized dc-link voltage and the weighted sum of the absolute three-phase currents, where the

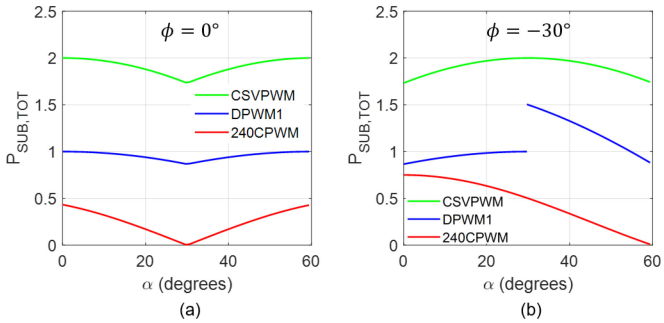

Fig. 12. Variation of normalized total switching loss in a subcycle over a sector $P_{\mathrm{SUB,TOT}}$ for different PWM methods. (a) $\phi = 0°$. (b) $\phi = -30°$.

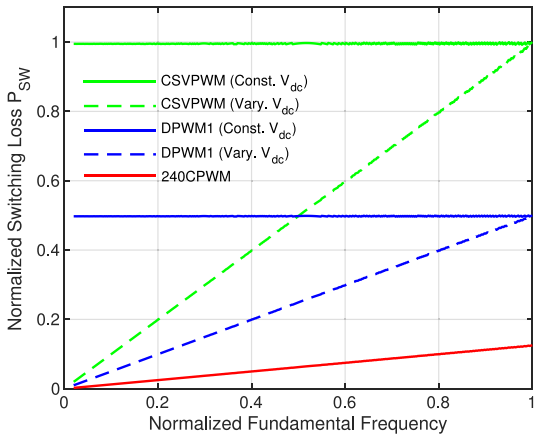

Fig. 13. Variation of normalized switching loss P_{SW} against normalized fundamental frequency for various PWM methods (normalized with respect to CSVPWM) at unity power factor. The fundamental frequency is normalized with respect to $f_{1,\max}$.

weights are the number of switching-transitions of each phase in a subcycle [19]

$$P_{\mathrm{SUB,TOT}} = V_{\mathrm{dc,nom}} \frac{n_A|i_A| + n_B|i_B| + n_C|i_C|}{I_m} \tag{19}$$

where $i_A = I_m \sin(\omega t + \phi)$, $i_B = I_m \sin(\omega t - 120° + \phi)$, $i_C = I_m \sin(\omega t - 240° + \phi)$. Variation of $P_{\mathrm{SUB,TOT}}$ for 240CPWM along with CSVPWM and DPWM1 in Sector I is shown for different power factor angles in Fig. 12. As discussed before, minimum switching losses can be observed for 240CPWM at unity power factor in Fig. 12(a). For CSVPWM all three absolute phase currents and for DPWM1 two absolute phase currents are added to yield $P_{\mathrm{SUB,TOT}}$ in Sector I. In 240CPWM, however, only one absolute phase current (phase B) gives $P_{\mathrm{SUB,TOT}}$ in Sector I because phases A and C are clamped to positive and negative dc bus, respectively. For nonunity power factors, weights in (19) remain the same as for unity power factor case, only sections of absolute currents that are being summed up shift accordingly, as shown in Fig. 12(b).

Average value of $P_{\mathrm{SUB,TOT}}$ for CSVPWM over a sector is $6/\pi$ at any power factor [18]. The normalized switching loss P_{SW} for a given PWM method is defined as the ratio of averaged $P_{\mathrm{SUB,TOT}}$ for the given PWM method over a sector to the averaged $P_{\mathrm{SUB,TOT}}$ for CSVPWM. P_{SW} facilitates the comparative evaluation of various techniques using power losses of all three phases at different power factor angles

$$P_{\mathrm{SW}} = \frac{1}{2} \int_0^{\pi/3} P_{\mathrm{SUB,TOT}} \, \mathrm{d}\alpha. \tag{20}$$

Now, the variation of switching loss for variable speed operation will be analyzed using the constant V/f control discussed in the previous section. Two scenarios of variable speed operation will be studied, one with constant V_{dc} and other with variable V_{dc}. For varying V_{dc} case, value of V_{dc} remains constant over a fundamental period but that constant value is different for different fundamental frequencies (or speeds) for CSVPWM and DPWM1. However, for 240CPWM, V_{dc} is variable both in average and instantaneous sense, i.e., V_{dc} is variable even within a fundamental period. For constant V_{dc} operation, switching losses are higher since switches are switching at fixed (high) V_{dc}, no matter how small the output voltage requirement is as governed by motor speed. Switching losses for varying V_{dc} cases are significantly lower than constant V_{dc} scenario since dc-link voltage is brought to the minimum value required to support the given line-to-line voltage using a dc–dc converter. This way the inverter switches do not have to switch at maximum V_{dc} at lower speeds, thereby reducing the switching loss considerably.

Fig. 13 shows the switching loss variation against fundamental frequency for CSVPWM (constant and varying V_{dc}), DPWM1 (constant and varying V_{dc}) and 240CPWM normalized with respect to the classical case of CSVPWM with constant V_{dc} at unity power factor. 240CPWM is the case of varying dc-link voltage by default. It can be observed that P_{SW} for 240CPWM is substantially lower than all the other cases. Switching loss for varying V_{dc} cases is always less than their corresponding constant V_{dc} cases. For the varying V_{dc} cases, switching loss is low at lower power and increases progressively for higher power levels. This is due to the fact that the magnitude of the line currents are kept the same while the dc-link voltage magnitude is increased linearly with fundamental frequency resulting in linear increase in the switching loss. From Fig. 13, it can be observed that switching loss for 240CPWM is 7.8 times lower than CSVPWM with constant dc-link voltage at the maximum fundamental frequency.

It is noted that the switch ratings with 240CPWM are identical to that of conventional two-level, three-phase inverters, since the dc-link voltage with 240CPWM is never more than that of an inverter with conventional PWM methods. The peak current rating is equal to the peak line current, which is similar to conventional PWM methods.

V. Experimental Validation

The experimental set-up is rated at 10 kW and is illustrated in Fig. 14. Fig. 15 shows a picture of the set-up. It is designed to test and compare the CSVPWM, DPWM1, and 240CPWM methods in terms of output current THD, conversion efficiency of the dc–ac stage and CMV. Test points at three different fundamental frequencies of 25, 37.5, and 50 Hz, respectively, are designed

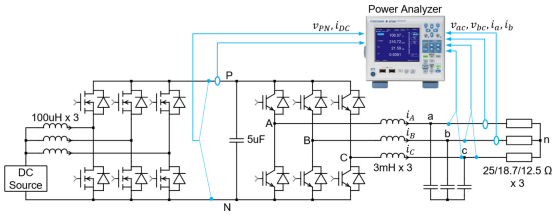

Fig. 14. Illustration of the experimental setup.

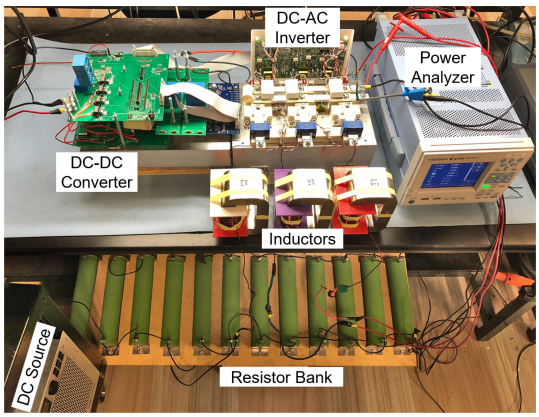

Fig. 15. Photograph of the experimental setup.

TABLE II
CONSTANT V/f OPERATING CONDITIONS AT THREE DIFFERENT FUNDAMENTAL FREQUENCIES

Parameters	Values		
Fundamental Frequency	50 Hz	37.5 Hz	25 Hz
Output Voltage (L-L RMS)	500 V	375 V	250 V
Load Resistance	25 Ω	18.7 Ω	12.5 Ω
Load Current (RMS)	11.5 A	11.5 A	11.5 A
Load Power	10 kW	7.5 kW	5 kW
Constant V_{dc}	800 V	800 V	800 V
Varying V_{dc}	800 V	600 V	400 V
Dynamic V_{dc}	707 V pk	530 V pk	353 V pk

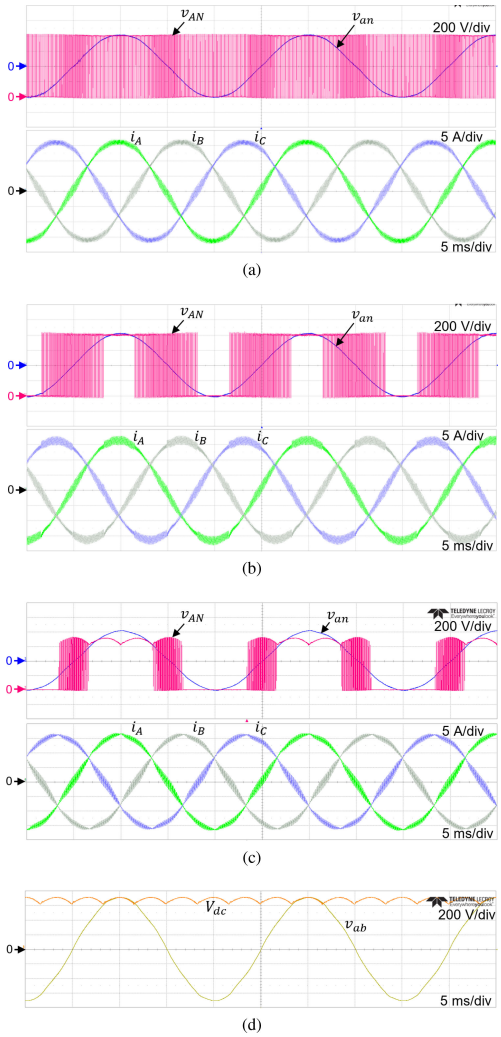

Fig. 16. Experimental waveforms of phase voltage v_{AN}, phase voltage after the filter v_{an}, and output currents at 10 kW, 50 Hz. (a) CSVPWM with $V_{\rm dc} = 800$ V. (b) DPWM1 with $V_{\rm dc} = 800$ V. (c) 240CPWM with dynamic dc link. (d) Experimental waveforms of dc-link voltage $V_{\rm dc}$ and line-to-line voltage after the filter v_{ab} with 240CPWM.

to test each modulation method with constant load current and constant fundamental V/f ratio. The operating conditions for different test points is summarized in Table II.

The CSVPWM and DPWM1 methods are tested for both constant and varying dc-link voltage conditions. For the constant dc-link voltage condition, the modulation index is adjusted for different fundamental frequencies in order to keep a constant V/f ratio. For the varying dc-link voltage condition, the modulation index is fixed at $0.9M_{\max}$ and the dc-link voltage is varied.

The dc–dc converter used in the experiment setup is a three-phase interleaved buck/boost converter. A common duty ratio is applied to all the three phases. The gate pulses of the three phases are shifted by 120° with respect to each other. The reference for the dc-link voltage is expressed by (6). Currently, open-loop control is used for the dc–dc converter and the duty ratio is calculated by $D = 1 - V_{\rm in}/(\max\{v_a, v_b, v_c\} - \min\{v_a, v_b, v_c\})$. Each phase leg of the boost converter is switching at 200 kHz, resulting in 600 kHz ripple in the dc-link voltage.

The dc–dc and dc–ac stages are controlled by using the same reference phase angle. When implementing the 240CPWM, the same reference phase angle is used for generating the dc-link voltage and the PWM, thus, synchronism between the generated six-pulse dc-link voltage and the modulation of the subsequent dc–ac stage is always secured by the control system. A series-connected inductive–resistive load bank is used to emulate a motor load with unity power factor. The switching frequency of the inverter is 10 kHz. A star-connected filter capacitor bank is connected after the inductors in order to extract the average phase voltage and line-to-line voltage waveforms.

The conversion efficiency of the inverter is measured by a Yokogawa WT500 power analyzer. The output current waveforms are captured by a LeCroy HDO8038 oscilloscope with 10 MHz sampling frequency with LeCroy CP030 30 A 50 MHz current probes. The current waveform data are postprocessed in MATLAB to compute the THD up to 1 MHz.

Fig. 16(a)–(c) shows the switching phase A voltage, line-neutral voltage, and the three line current waveforms with CSVPWM, DPWM1, and 240CPWM at 10 kW 50 Hz, respectively. Fig. 16(d) verifies that the dc-link voltage is exactly equal

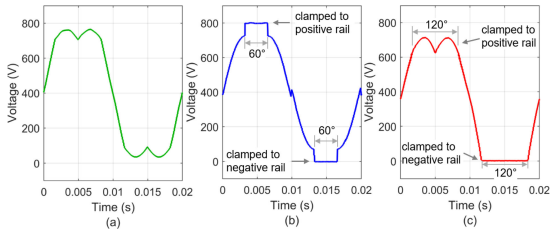

Fig. 17. Switching-cycle averaged phase voltage $\overline{v}_{AN}$ with (a) CSVPWM, (b) DPWM1, and (c) 240CPWM at 10 kW, 50 Hz, extracted from experimental phase voltage waveform.

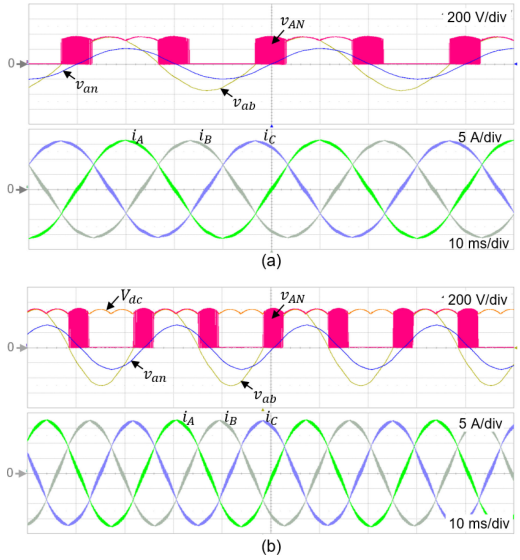

Fig. 18. Experimental waveforms of phase voltage v_{AN}, filtered phase voltage v_{an}, dc-link voltage $V_{\rm dc}$, filtered line-to-line voltage v_{ab} with 240CPWM at (a) 5 kW, 25 Hz, and (b) 7.5 kW, 37.5 Hz.

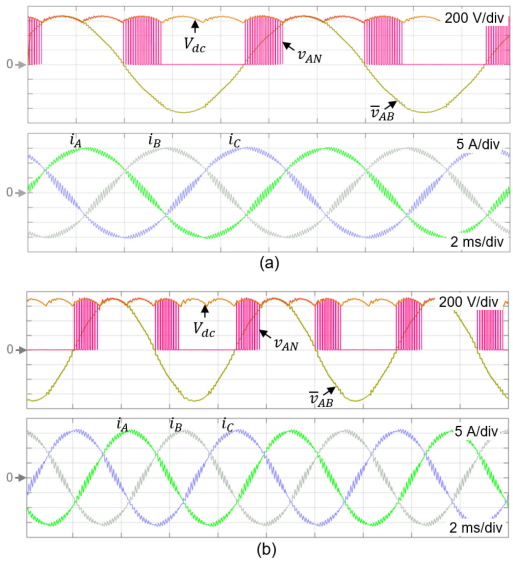

Fig. 19. Experimental waveforms with 240CPWM at 10 kW with fundamental frequency of (a) 100 Hz and (b) 150 Hz. $\overline{v}_{AB}$ denotes the switching cycle average of v_{AB}.

TABLE III
THD MEASUREMENT RESULTS OF THE CONSTANT V/f TEST POINTS WITH DIFFERENT PWM METHODS

Technique	f_1 = 25 Hz	f_1 = 37.5 Hz	f_1 = 50 Hz
CSVPWM (Constant V_{dc})	4.07%	4.29%	5.26%
CSVPWM (Varying V_{dc})	3.03%	3.65%	5.26%
DPWM1 (Constant V_{dc})	7.68%	7.11%	6.04%
DPWM1 (Varying V_{dc})	3.07%	4.69%	6.04%
240CPWM	3.07%	3.73%	5.24%

to the corresponding instantaneous line–line voltage of the two nonswitching phases in each sector to make the 240CPWM technique possible. Fig. 17(a)–(c) shows the corresponding average phase voltage $\overline{v}_{AN}$ waveforms. Fig. 18 shows the constant V/f operation waveforms with 240CPWM at 25 and 37.5 Hz fundamental frequencies, with the load current same as that with 50 Hz operation. Fig. 19 shows the operation waveforms with 240CPWM at 10 kW, 100 Hz, and 150 Hz, demonstrating the effectiveness of 240CPWM at higher fundamental frequency to better emulate actual EV drive performance.

The THD measurement results of the constant V/f test points with different PWM methods are summarized in Table III. Fig. 20 shows the harmonic spectrum of the load current at the 50 Hz 10 kW operation point. The 10 kHz side-band harmonics with 240CPWM is slightly higher than that with CSVPWM, while the DPWM1 method has the highest switching frequency harmonics. The same trend is verified from Fig. 21 where THD of CSVPWM and 240CPWM are comparable while THD of DPWM1 is quite high.

Fig. 21 shows the comparison of measured current THD with different modulation methods. The THD values for CSVPWM and DPWM1 at 50 Hz are obtained with a modulation index of $0.9M_{\rm max}$ because of limitation on the maximum allowable pulsewidth of the hardware prototype. The same trend is seen when comparing the measured THD values with theoretically predicted values of $F_{\rm DIST}$ recalculated with modulation index $0.9M_{\rm max}$.

It is evident from Figs. 16 and 17 that, with CSVPWM, the insulated-gate bipolar transistors (IGBTs) are constantly switching in a fundamental cycle.With DPWM1, the output is clamped to the positive dc link for 60° near the positive peak and to the negative dc link for 60° near the negative peak, resulting in less switching actions. With 240CPWM, tthe output is clamped to the positive dc link for 120° near the positive peak and to the negative dc link for 120° near the negative peak, resulting in the lowest number of switchings.

Fig. 22 shows the current in the Phase A top switch (through IGBT or the antiparallel diode) with 240CPWM, which is derived from the waveforms of the output current and the switch gate pulses. It can be seen that the IGBT only switches near the zero crossings of the output current and is kept ON during $\omega t \in [30^\circ, 150^\circ]$ and kept OFF during $\omega t \in [210^\circ, 330^\circ]$. Due to the near-unity power factor operation, this also corresponds to switching only near the zero-crossing of the line current. Therefore, with the combination of minimum number of switchings and low magnitude of currents at the instants of switching, the

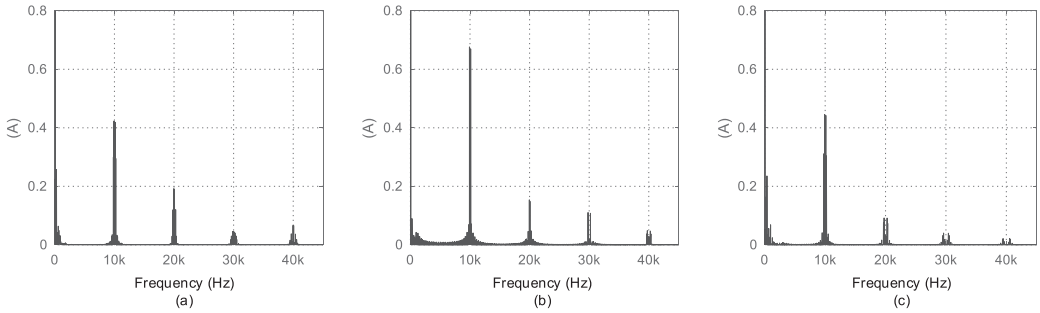

Fig. 20. Measured harmonic spectrum of the load current at 10 kW 50 Hz with (a) CSVPWM, (b) DPWM1, and (c) 240CPWM. (The magnitude of the fundamental current in each case is 16.3 A.)

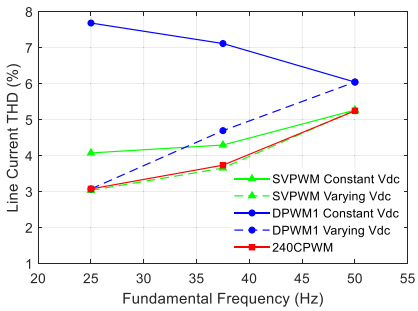

Fig. 21. Comparison of measured current THD with different modulation methods and dc-link voltage conditions

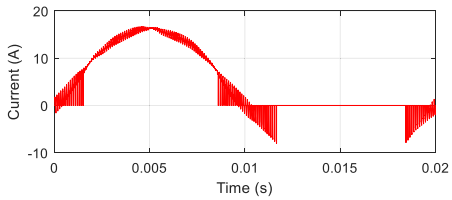

Fig. 22. Phase A top switch current waveform with 240CPWM, derived from measured switch gate pulse and inductor current waveforms.

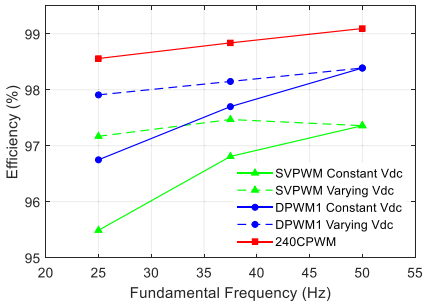

Fig. 23. Comparison of measured inverter (dc–ac stage) efficiency under different modulation methods and dc-link voltage conditions.

switching losses are significantly lower compared to even the DPWM1 and even more so compared to CSVPWM.

Fig. 23 shows the comparison of measured inverter efficiency with different modulation methods and dc-link voltage conditions. It is evident that the 240CPWM method has the highest

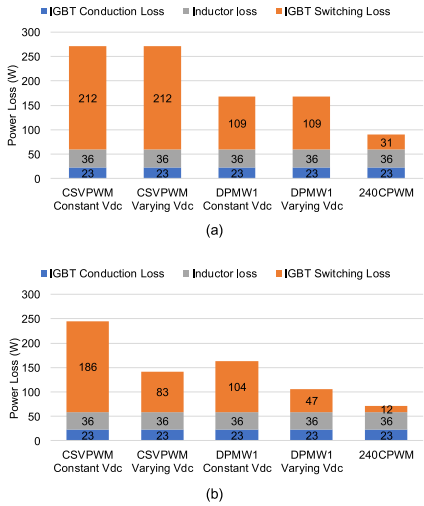

Fig. 24. Loss breakdown at (a) 50 Hz, 10 kW, and (b) 25 Hz, 5 kW.

efficiency over the tested operating range. At 10 kW, the inverter efficiency is 99.10% with 240CPWM while it is 98.39% with DPWM1 and 97.36% with CSVPWM. Loss breakdown of all PWM methods at high- and low-speed operations are presented in Fig. 24. Since the conduction loss is influenced only marginally by the modulation method [32], it is the switching loss associated with different PWM methods that dictates the total loss and, thus, the efficiency of the drive. Switching loss for 240CPWM is 31 W that is 6.8 times lower than CSVPWM with constant $V_{\rm dc}$ at 50 Hz operation. Likewise, switching loss for 240CPWM is 12 W that is 15.5 times lower than CSVPWM with constant $V_{\rm dc}$ at 25 Hz operation. This trend validates theoretically predicted switching loss given in Section IV.

CMV for all three PWM methods under consideration is measured by averaging the three switching pole voltages (with respect to dc link mid-point), as shown in Fig. 25. dc-link voltage of 800 V is maintained for 10 kW corresponding to high-speed (50 Hz) operation for CSVPWM and DPWM1. CSVPWM and DPWM1 use at least one zero state, thus, maximum CMV corresponding to both the cases is $\pm V_{\rm dc}/2$, which is verified from Fig. 25(a) and (b), respectively. With 240CPWM since no zero vector is used, significant reduction in CMV voltage is achieved as compared to CSVPWM and DPWM1. For 240CPWM,

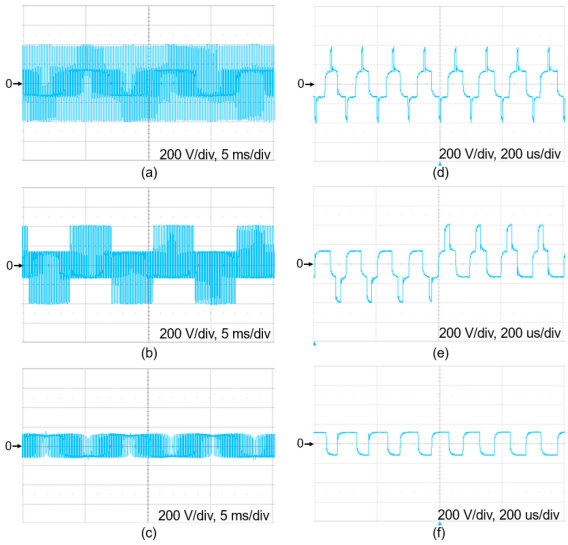

Fig. 25. Measured CMV at 10 kW 50 Hz with (a) CSVPWM, (b) DPWM1, (c) 240CPWM. (d), (e), and (f) are zoomed in version of (a), (b), and (c), respectively.

maximum CMV is only $\pm V_{\rm dc}/6$, as shown in Fig. 25(c), which is 67% lower than CSVPWM and DPWM1.

Zoomed-in versions of CMV voltage clearly show the CMV levels corresponding to each switching state. For example, in CSVPWM, CMV levels of $-V_{\rm dc}/2$, $-V_{\rm dc}/6$, $V_{\rm dc}/6$, and $V_{\rm dc}/2$ can be observed corresponding to the switching state 0 $(---)$, $1(+--)$, $2(++-)$, and $7(+++)$, respectively. However, CMV levels are reduced to $-V_{\rm dc}(t)/6$ and $V_{\rm dc}(t)/6$ in 240CPWM pertaining to the switching state $1(+--)$ and $2(++-)$, respectively.

VI. Conclusion and Future Work

A bus-clamping space vector PWM method called 240CPWM with several compelling advantages is introduced for two-level, three-phase converters. It is suitable for any power conversion system with a cascaded connection of a dc–dc stage and a dc–ac stage allowing the dc-link voltage to be dynamically variable. In this article, the potential application of the PWM method to EV and HEV traction drive systems where several production vehicles already have the needed bidirectional dc–dc converter is explored.

Comprehensive analysis of the space vector implementation, carrier-based modulation signals, harmonic distortion, and switching loss characteristics of the 240CPWM as well as comparison with CSVPWM and DPWM1 are presented. The 240CPWM method has the major advantages of clamping a phase to the positive or negative rail for 240° in a fundamental period, clamping of two phases simultaneously at any given instant, and use of only active states, completely eliminating the use of zero states. These characteristics lead to a significant reduction in switching losses of the inverter (reduction by more than seven times at unity power factor compared to CSVPWM), comparable or better THD performance compared to CSVPWM, and high efficiency even with Si IGBTs. Experimental results from a 10-kW hardware prototype with the maximum voltage of 500 $V_{\rm LL}$ and 10 kHz switching frequency validated the superior performance of the 240CPWM method. The full load efficiency with the proposed 240CPWM for the dc–ac stage even with Si IGBTs exceeds 99%. Significant reduction in CMV has also been experimentally verified.

Future work on the 240CPWM technique includes overall loss analysis that includes the dc–dc stage, the dc–ac stage and the motor, optimal dc-link capacitor sizing, more detailed analysis of CMV and leakage currents and dynamic performance of the cascaded system with the proposed PWM method.

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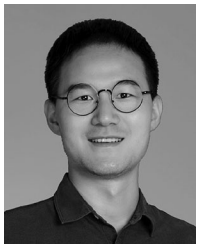

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