Charge Pump Gate Drive to Reduce Turn-ON Switching Loss of SiC MOSFETs

Handong Gui, *Student Member, IEEE*, Jingjing Sun, *Student Member, IEEE*, and Leon M. Tolbert, *Fellow, IEEE*

***Abstract*—Turn-ON loss is the dominant part of the switching loss for SiC MOSFETs in hard switching. Reducing turn-ON loss with conventional voltage source gate drives (VSGs) is difficult because of the limited gate voltage rating and large internal gate resistance of SiC MOSFETs. A charge pump gate drive (CPG) that can reduce the turn-ON loss is presented in this article. By precharging the charge-storage capacitor in the gate drive with a charge pump circuit, the gate drive output voltage is pumped up to provide higher gate current during the turn-ON transient. As a result, the turn-ON time and loss is decreased. Moreover, due to the charge transfer from the charge-storage capacitor to the MOSFET gate capacitance, the pumped output voltage can naturally drop back to a normal value that avoids gate overcharging. The structure of the gate drive is simple, and no additional control is needed. The operation of the proposed CPG is verified with double pulse tests based on SiC MOSFETs. The switching loss of the proposed CPG is reduced by up to 71.7% compared to the conventional VSG at full load condition.**

***Index Terms*—Double pulse test, gate drive, SiC MOSFET, switching loss, voltage source.**

I. Introduction

THE silicon carbide (SiC) MOSFET is regarded as a promising power semiconductor device for high frequency and high power applications [1], [2]. Compared with its counterparts like the Si insulated-gate bipolar transistor (IGBT), the SiC MOSFET has lower specific on-resistance, higher switching speed capability, and higher maximum junction temperature, which is beneficial for building converters with higher efficiency and power density. Despite the faster switching speed, the switching loss is still a main barrier that prevents the adoption of SiC MOSFETs in hard switching converters with switching frequency of hundreds of kHz. Device datasheets and the reported testing results indicate that the turn-ON loss is the dominant part in switching loss [3]–[7].

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The authors are with the Min H. Kao Department of Electrical Engineering and Computer Science, The University of Tennessee, Knoxville, TN 37996 USA (e-mail: hgui@vols.utk.edu; jsun30@vols.utk.edu; tolbert@utk.edu).

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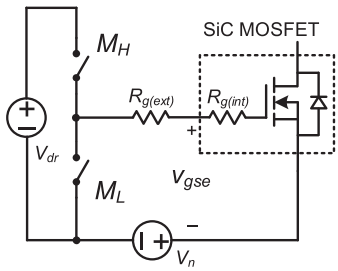

Fig. 1. Circuit of a typical VSG.

The gate drive is the interface between power devices and control signals, and it directly regulates the switching behavior of the power device. The basic requirements for a gate drive mainly include the following three aspects.

1) In steady state, it should keep the power device in ON/OFF state and prevent spurious change of the state caused by external or internal disturbance.
2) It should switch states between ON and OFF fast to reduce switching loss. Also, it should avoid dynamic hazards like crosstalk in gate-source and overvoltage in drain-source to maintain the reliability of the power device.
3) Especially for discrete devices, the gate drive should have compact structure and simple control method. It would be better to be embedded in an integrated circuit for small size, increased noise immunity, and lower cost.

Gate drive topologies can be primarily categorized into three groups: voltage source gate (VSG) drives, current source gate (CSG) drives, and resonant gate (RG) drives [8], [9]. The RG is able to reduce the gate drive loss [10]–[12]. However, the gate drive loss can be neglected compared to the switching loss of SiC MOSFETs especially in high power applications. Hence, the RG is not promising since it usually has a complicated structure.

VSG is the most widely used structure for MOSFETs because of its simple structure and low cost [13]–[17]. Fig. 1 depicts a typical VSG structure. A constant voltage V_{dr} is provided, and the half bridge controls the gate drive output.

Fig. 2 shows the typical turn-ON switching transient waveforms in a phase-leg, where the lower MOSFET is the active switch [7]. The transient includes four subintervals. From t_a to t_b, the period is called turn-ON delay subinterval. The pulsewidth modulation (PWM) turn-ON signal is given, and the lower MOSFET gate voltage rises to the threshold voltage V_{th}. Starting from t_b, the MOSFET is ON, and the drain current increases until it reaches

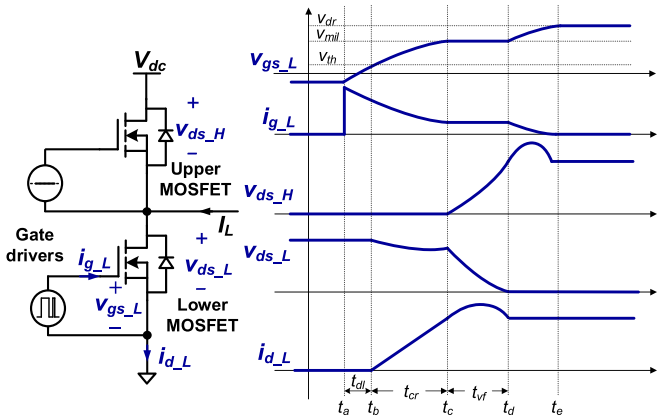

Fig. 2. Typical turn-ON transient waveform of a phase-leg with VSG [7].

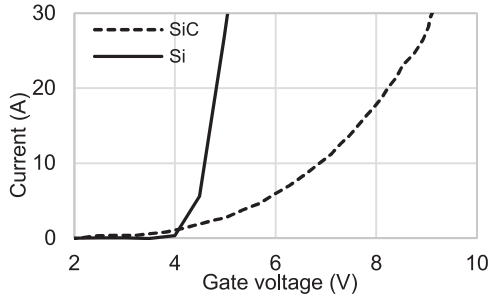

Fig. 3. Transfer characteristics of SiC MOSFET and Si CoolMOS [18].

the load current at t_c. With the constant gate drive output voltage of the VSG, the gate current decreases as the gate voltage rises from t_a to t_c. The drain-source voltage drops from t_c to t_d. In this period, the gate current is mainly used to discharge the device transfer capacitance, and the gate voltage is clamped at the Miller voltage V_{mil}. After t_d, the MOSFET is fully ON, and the gate voltage continues to rise to the gate drive output voltage V_{dr}.

The switching loss is mainly generated during the turn-ON time from t_b to t_d, where drain-source current and voltage have overlap. SiC MOSFETs have modest transconductance as shown in Fig. 3 compared with Si MOSFETs [18]. As a consequence, the gate current drop from t_b to t_d is higher, and both turn-ON time and switching loss increase. According to the test results in [7], the conventional VSG is not able to provide enough gate current to fully utilize the switching speed capability of SiC MOSFETs.

To increase the switching speed of power devices, CSGs have been developed to enhance the gate current during the switching transient [5], [19]–[26]. However, these CSGs cannot maintain constant current due to the large voltage drop across the high internal gate resistance of the SiC MOSFET. In [27], a CSG that can keep the gate current constant throughout the switching transient is proposed. Nevertheless, it requires accurate timing control to avoid overcharging the gate capacitance, which is not practical in real applications with load changing. Moreover, the required bidirectional switches as well as the inductor in the circuit make the gate drive complicated and difficult to be integrated. In general, CSG is not popular considering the compact, reliable and low cost requirements of the gate drives for SiC MOSFETs, especially for discrete devices.

Based on the analysis of the existing gate drive topologies, this article proposes a charge pump gate (CPG) drive circuit that can reduce the turn-ON switching loss of SiC MOSFETs. It has the advantage of simple structure, and no additional control is needed. Sufficient gate current can be provided throughout the turn-ON transient of the SiC MOSFET without introducing overcharging.

This article is organized as follows. Sections II and III give the derivation and operating principles of the proposed CPG topology. Section IV summarizes the benefits and challenges of the CPG. Section V provides the key parameter design. Section VI conducts the switching and gate drive loss calculation with the proposed CPG. Section VII demonstrates the experimental results. Finally, Section VIII concludes the article.

II. Derivation of Proposed CPG Topology

From Section I, the bottleneck of increasing the turn-ON switching speed of SiC MOSFETs is the limited gate current during the switching transient. To find a solution, the impact factors of gate current during the turn-ON transient with a typical VSG should be investigated.

From the start of turn-ON, the gate voltage first increases until the drain current reaches the peak value. During this period, the gate loop is an *RC* first order network, which consists of external gate resistance $R_{g(\text{ext})}$, internal gate resistance $R_{g(\text{int})}$, and gate capacitance C_{gs}. The gate current can be expressed as

$$i_g(t) = \frac{V_{dr}}{R_{g(\text{ext})} + R_{g(\text{int})}} \exp\left(-\frac{t}{\left(R_{g(\text{ext})} + R_{g(\text{int})}\right) C_{gs}}\right) \tag{1}$$

where V_{dr} is the gate drive supply voltage.

After the drain current approaches its peak, the drain-source voltage starts to drop. Gate current mainly discharges the transfer capacitance, and the gate voltage is clamped to the Miller voltage V_{mil}. In this period, the gate current can be regarded as constant

$$i_g(t) = \frac{V_{dr} - V_{\text{mil}}}{R_{g(\text{ext})} + R_{g(\text{int})}} = \frac{V_{dr} - V_{th} - \frac{I_L}{g_m}}{R_{g(\text{ext})} + R_{g(\text{int})}} \tag{2}$$

where V_{th} is the MOSFET gate threshold voltage, I_L is the load current, and g_m is the MOSFET transconductance.

Among the variables in (1) and (2), I_L is determined by the application, while $R_{g(\text{int})}$, C_{gs}, V_{th} and g_m are intrinsic characteristics of the SiC MOSFET. As a result, the only changeable parameters are gate drive supply voltage V_{dr} and the external gate resistance $R_{g(\text{ext})}$.

By applying higher gate drive supply voltage, gate current can be increased. However, the gate voltage rating of SiC MOSFETs is usually around 20 V, which does not leave much margin for increasing the voltage. On the other hand, reducing external gate resistance also introduces limited improvement because of the relatively large internal gate resistance of SiC MOSFETs, which is normally from 4 to 10 Ω [3]–[5]. As a result, it is difficult to increase the switching speed of SiC MOSFETs with conventional VSGs.

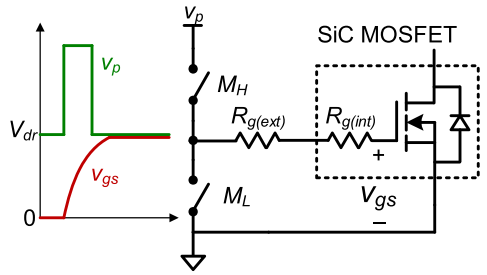

Fig. 4. Ideal supply voltage of gate drive.

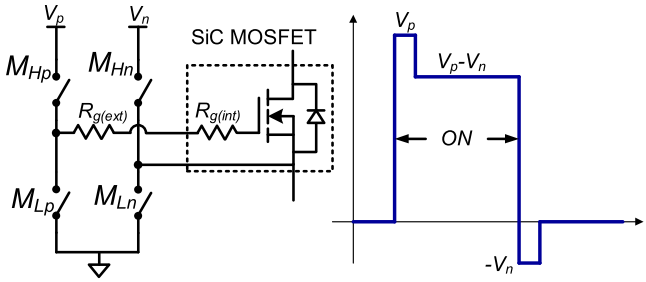

Fig. 5. Four-level gate drive circuit and operating waveform.

Considering the switching process, there are two main requirements for the gate drive. First, it should provide sufficient gate current during the switching transient to shrink the switching time. Second, the gate voltage should be kept under the rating of the MOSFET in both transient and steady state. As mentioned earlier, the gate drive supply voltage cannot be too high mainly due to the second requirement. However, as shown in Fig. 4, the dynamic supply voltage v_p can be higher than the gate voltage rating during the switching transient since it takes time for gate voltage v_{gs} to increase. As long as v_p drops back to the normal value V_{dr} (lower than the gate voltage rating) before v_{gs} approaches V_{dr}, there is no risk of overcharging the gate.

In [28]–[31], four-level gate drives (4LG) were adopted to achieve such function. A typical 4LG as well as its operating waveform are shown in Fig. 5. Two power supplies and two half-bridges provide four different gate drive voltages, namely V_p, $V_p - V_n$, 0 and $-V_n$. During the turn-ON switching transient, V_p is used to enhance the turn-ON speed. In steady state, the voltage drops to $(V_p - V_n)$.

However, such 4LG has two drawbacks. First, due to the limited negative gate voltage rating, V_n (e.g. 5 V) is usually much lower than V_p (e.g. 20 V). As a consequence, the voltage enhancement during the turn-ON transient is limited. To further increase the voltage, additional power supplies or transformers are required [31], which significantly increase the complexity and cost of the gate drive.

Second, the voltage shift from V_p to $(V_p - V_n)$ requires an accurate control signal to avoid gate overvoltage, which not only increases the complexity of the circuit, but also cannot adaptively fit for different load and bus voltage conditions, where the switching transient time changes. Therefore, the required gate drive should have the ability to automatically change the voltage level and guarantee that the gate voltage is always lower than the rating.

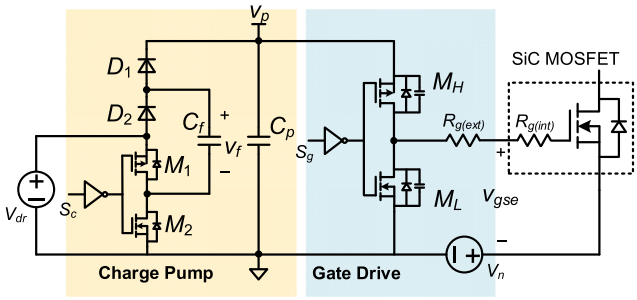

Fig. 6. Circuit of the proposed CPG.

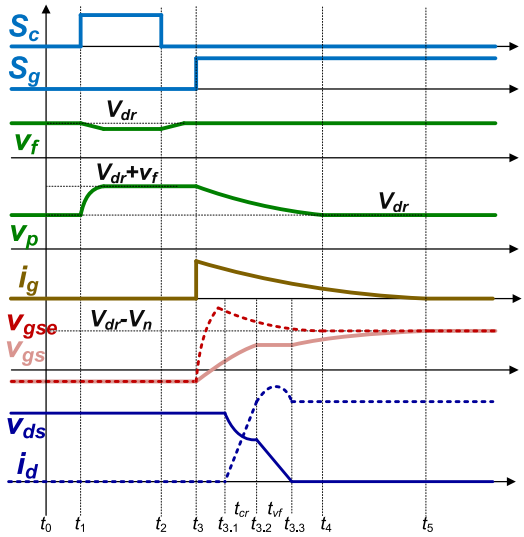

Fig. 7. Operation waveforms of the proposed CPG.

With the aforementioned idea and requirements, Fig. 6 shows the proposed CPG drive. It consists of two main parts: a charge pump circuit and a typical VSG drive. The charge pump utilizes the flying capacitor structure, which consists of a pair of MOSFETs M_1 and M_2, two diodes D_1 and D_2, and two capacitors C_f and C_p. C_f is the flying capacitor while C_p is the charge-storage capacitor. The VSG is a totem-pole bridge including two MOSFETs M_H and M_L. $R_{g(\text{ext})}$ is the external gate resistance, while $R_{g(\text{int})}$ is the internal gate resistance. v_p is the voltage across C_p, which is also the gate drive output voltage. The power supply V_{dr} is connected with M_1 and M_2. Another power supply V_n provides the required negative voltage across the gate-source during the OFF state.

III. Operating Principle of the Proposed CPG

During one typical turn-ON switching period, there are five modes, and the key waveforms are illustrated in Fig. 7, which includes the charge pump control signal S_c, gate drive output control signal S_g, the flying capacitor voltage v_f, the pump capacitor voltage v_p, the gate current i_g, the external and real gate-source voltage v_{gse} and v_{gs}. The equivalent circuit in each

subinterval is plotted in Fig. 8, and the operation during the turn-ON transient is briefly explained as follows.

1) Subinterval 1 (t_0-t_1): *OFF Steady State*. Before t_1, both S_c and S_g are in low level, and M_2 and M_L are in ON state. In this state, both v_f and v_p equal to V_{dr} and do not change if the forward voltage drop of D_1 and D_2 is neglected. The gate drive output is low to keep the SiC MOSFET in OFF state.
2) Subinterval 2 (t_1-t_2): *Voltage Pump State*. At t_1, S_c changes to high level, and M_1 is turned ON. As a result, D_1 conducts while D_2 is OFF. The flying capacitor C_f transfers energy to the charge-storage capacitor C_p. Assuming the energy transfer is lossless, the relationship between v_p and v_f at t_2 can be expressed as

$$\begin{cases} v_p\left(t_2\right) = v_f\left(t_2\right) + V_{dr} \\ C_f {v_f}^2\left(t_2\right) + C_p {v_p}^2\left(t_2\right) = \left(C_f + C_p\right) {V_{dr}}^2. \end{cases} \tag{3}$$

If the capacitance C_f is much higher than C_p, the voltage drop on v_f can be neglected, and $v_p(t_2)$ is pumped to $2V_{dr}$. Note that since the energy directly flows from one capacitor to the other, this time period can be very short. By the end of this subinterval, the required high supply voltage is established.

3) Subinterval 3 (t_2-t_3): *Standby State*. At t_2, S_c is pulled down to turn ON M_2 and turn OFF M_1. In such case, D_1 is off as v_p is higher than v_f. Because part of the energy on C_f is given to C_p, D_2 conducts and the power supply V_{dr} charges C_f. In this state, C_p is disconnected from C_f, and v_p remains constant at high voltage level. Note that this subinterval can also be very short as long as D_1 is OFF before the gate drive output signal S_g becomes high. The gate drive output is still low, and the SiC MOSFET is in OFF state.
4) Subinterval 4 (t_3-t_4): *Gate-charging State I*. At t_3, S_g turns to high, and the gate drive starts to provide current to charge the SiC MOSFET gate capacitance. Because v_p approximately equals to $2V_{dr}$ at the beginning of this state, the gate current can be enhanced compared with the conventional VSG. The gate voltage v_{gs} starts to increase from $-V_n$, and the SiC MOSFET is turned ON when the gate threshold voltage V_{th} is reached.

Since v_p is higher than V_{dr}, C_p is disconnected from C_f and V_{dr}, and there is no source to provide energy to charge C_p. Therefore, v_p keeps decreasing during the charging process, and gate voltage approaches to v_p in the end. By tuning the external gate resistance $R_{g(\mathrm{ext})}$, the decreasing rate of v_p can be regulated, which enables the change of switching speed like a typical VSG.

The key point of this CPG is that the capacitance C_p should be selected to guarantee that v_p can finally reach V_{dr}. If C_p is too large and has too much stored energy, the steady state v_p after the gate charging process can be higher than V_{dr}, which results in overcharging. The detailed analysis of C_p calculation is provided in Section V. It should be noted that the external gate-source voltage v_{gse} can be dynamically higher than $(V_{dr} - V_n)$ because of the internal gate resistance of the SiC MOSFETs. However, the

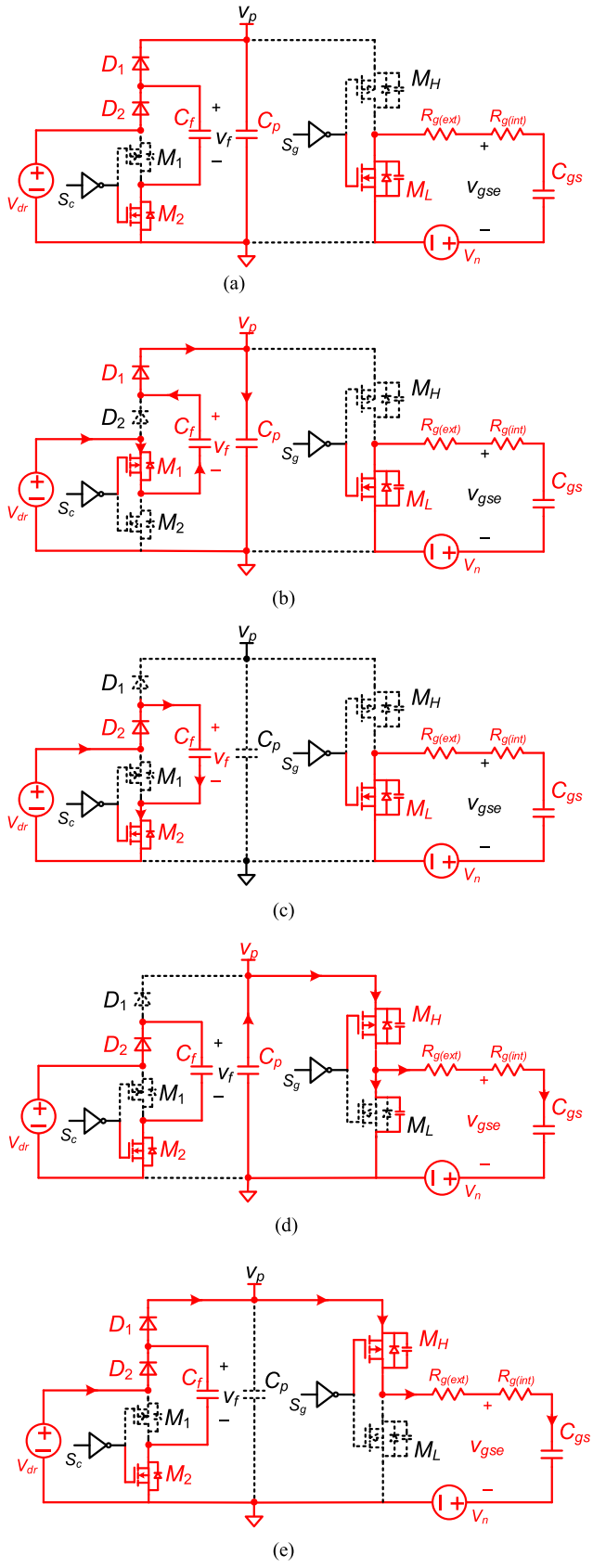

Fig. 8. Equivalent circuits in different subintervals of the proposed CPG. (a) Subinterval 1. (b) Subinterval 2. (c) Subinterval 3. (d) Subinterval 4. (e) Subinterval 5.

real gate-source voltage keeps increasing and does not exceed $(V_{dr} - V_n)$ as long as v_p can drop back to V_{dr}.

5) Subinterval 5 (t_4-t_5): *Gate-charging State II*. In subinterval 4, v_p continues to decrease until it reaches V_{dr} at t_4, while the gate voltage is still increasing. Then, D_1 naturally conducts to connect C_p with V_{dr}. Hence, V_{dr} directly provides energy to charge the gate, and the gate drive becomes a typical VSG throughout the rest of the MOSFET ON state.

The turn-OFF process of the proposed CPG is the same as a typical VSG since the turn-OFF loss is not as large as the turn-ON loss. However, the same circuit can also be adopted to reduce the turn-OFF loss.

IV. Benefits and Challenges of the Proposed CPG

The benefits are listed as follows.

1) The pumped gate drive output voltage enables higher gate current that charges the gate capacitance during the turn-ON switching transient compared with the conventional VSG. As a result, the turn-ON switching loss is reduced.
2) The pumped voltage naturally drops back to normal gate supply voltage without any additional control, which avoids overcharging and has a simple gate drive structure at the same time.
3) The proposed CPG is still a voltage source based gate drive, and the implementation is the same as a typical VSG for the end-user. The SiC MOSFET turn-ON switching speed can be easily tuned by changing the external gate resistance. Thus, it is convenient to replace the conventional VSG in power converters with the proposed CPG.
4) The energy transfer time is short between capacitors, resulting in a short charge pump time. Therefore, the time delay between PWM signal and device turn-ON is reduced.
5) No extra power supply is required compared with a conventional VSG, which keeps costs low.
6) No inductor is required, which makes the proposed CPG easy for integration.
7) The control signals of the transistors share the same ground, which avoids complex level shifters or floating drives.

The challenges are listed as follows.

1) The drop of the gate drive output voltage is determined by the charge-storage capacitor value C_p. Thus, C_p needs to be carefully selected considering the gate capacitance C_{gs}. If C_p is too large, the pumped voltage cannot decrease to the normal voltage V_{dr}, which can introduce overcharging. Otherwise, if C_p is too small, the pumped voltage reduces too quickly during the switching transient, which deteriorates the switching speed improvement.
2) The increased turn-ON speed results in higher *dv*/*dt*, leading to more significant influence from parasitics. For example, higher drain-source overvoltage and crosstalk phenomenon can occur on the synchronous device, and electromagnetic interference (EMI) can become worse. These side effects from increasing the switching speed should be taken into consideration when applying the proposed CPG.

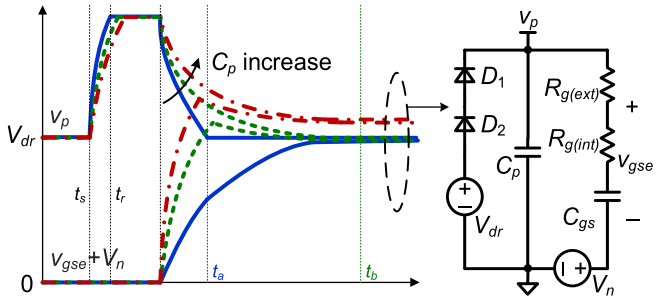

Fig. 9. Voltage waveforms during turn-ON transient and equivalent circuit with different C_p.

V. Parameter Design and Selection

A. Capacitance Design

As mentioned earlier, the key point in designing the proposed CPG is to select proper capacitance C_p. Fig. 9 shows the waveforms of the pumped voltage v_p and the external gate to ground voltage $(v_{\rm gse} + V_n)$ with different C_p. The equivalent circuit after the SiC MOSFET turns ON is also plotted. During the turn-ON transient, C_p transfers charge to C_{gs}. In the end, the voltage across the two capacitances is the same. The main difference is whether v_p can drop to V_{dr} to conduct D_1 and D_2, and it is determined by the relationship between C_p and C_{gs}.

If C_p is too small, as shown by the blue line in Fig. 9, there is not sufficient stored charge for C_{gs}. As a result, v_p decreases quickly and reaches V_{dr} even when $(v_{\rm gse} + V_n)$ is still low. Then the required charge is provided by V_{dr}, and the gate drive is the same as the conventional VSG. In this case, the switching speed improvement is limited.

On the other hand, oversized C_p can have severe consequences. As shown by the red line, v_p drops slowly as C_p has more stored charge. In the end, $(v_{\rm gse} + V_n)$ rises higher than V_{dr}, which results in overcharging and can cause reliability issues for the gate of the SiC MOSFET.

The ideal case is shown by the green line. v_p reduces to V_{dr} at the same time when $(v_{\rm gse} + V_n)$ reaches v_p. Under this circumstance, no overcharging occurs, and the switching speed improvement is maximized. The following calculation presents how to select such proper C_p.

Once M_H is turned ON, part of the charge stored in C_p is used to charge the output capacitance of M_L, which is represented as C_{OSSL}. Then the output of the gate drive becomes high level, and C_p provides charge to the gate capacitance C_{gs} to turn ON the SiC MOSFET. After the drain current of the SiC MOSFET rises to the load current, the gate current discharges the transfer capacitance C_{gd} of the SiC MOSFET and decreases the drain-source voltage. Therefore, if D_1 and D_2 do not conduct, and V_{dr} does not provide energy to C_p, the charge in C_p is transferred to the gate capacitance C_{gs}, the transfer capacitance C_{gd} of the SiC MOSFET, and the output capacitance C_{OSSL} of M_L

$$Q_p = Q_{gs} + Q_{gd} + Q_{OSSL} \tag{4}$$

where Q_p is the lost charge in C_p, Q_{gs} and Q_{gd} are the gate-to-source charge and gate-to-drain charge of the SiC

MOSFET, and Q_{OSSL} is the received charge of C_{OSSL} during the turn-ON transient.

When the gate voltage goes into steady state at t_b in Fig. 9, the relationship between v_p and the gate voltage is

$$v_p(t_b) = v_{gs}(t_b) + V_n = V_{dr}. \tag{5}$$

Therefore, the charge transfer during the turn-ON transient is derived as

$$\begin{cases} V_{p0} - \frac{Q_p}{C_p} = \frac{Q_{OSSL}}{C_{OSSL}} = V_n + \frac{Q_{gs}}{C_{gs}} = V_{dr} \\ \frac{Q_{gd}}{C_{gd\_Q}} = V_{dc} \end{cases} \tag{6}$$

where V_{p0} is the initial voltage of v_p, which is approximately $2V_{dr}$. V_{dc} is the dc-bus voltage, and C_{gd_Q} is the charge equivalent transfer capacitance of the SiC MOSFET at V_{dc}. Thus, the required C_p can be calculated as

$$C_p = \frac{C_{gs}(V_{dr} - V_n) + C_{gd\_Q}V_{dc} + C_{OSSL}V_{dr}}{V_{dr}}. \tag{7}$$

Note that this is the maximum C_p that can be used to avoid overcharging. To leave some margin, the selected C_p should be a little lower than the calculated value from (7).

The turn-ON delay caused by charging C_p should be taken into consideration. As shown in Fig. 9, the required time to charge C_p is from t_s to t_r. During this time interval, the gate signal S_g cannot be applied to turn ON the SiC MOSFET. The charging time is determined by C_p and the resistance of the printed circuit board (PCB) traces connecting C_p and C_f. Normally, the trace length can be easily controlled under 5 mm, while the width and thickness is higher than 10 mil and 0.5 oz/ft^2. So the resistance is calculated to be lower than 20 mΩ. From (7), C_p should be the same level as C_{gs} since C_{gd_Q} and C_{OSSL} are much lower than C_{gs}. For a typical SiC discrete MOSFET, C_{gs} is less than 10 nF. As a result, the delay time is less than 1 ns, which can be neglected as long as the SiC MOSFET operates at sub-MHz range.

In terms of C_f in Fig. 6, as mentioned in Section III, it should be much higher than C_p. In practice, choosing a C_f that is 50 times higher than C_p should be enough.

B. Signal Generation

The proposed CPG only needs two control signals, and they can be easily realized with one PWM input signal and some logic gates.

The realization of the logic signals to control the proposed CPG is shown in Fig. 10(a). The delay units can be simply implemented with *RC* filters with different values. Two logic integrated circuits are used to generate the required signals. Thus, the control signal generation is simple and the units can be easily integrated. The logic waveforms for the control signals are illustrated in Fig. 10(b).

VI. Loss Analysis

A. Switching Loss

The turn-ON switching loss is mainly generated by the overlap between drain current and drain-source voltage. It can be

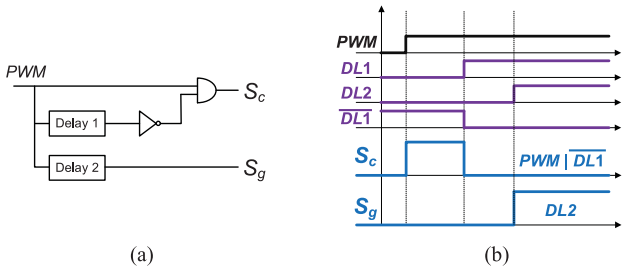

Fig. 10. Control logic realization for proposed CPG. (a) Circuit. (b) Waveforms.

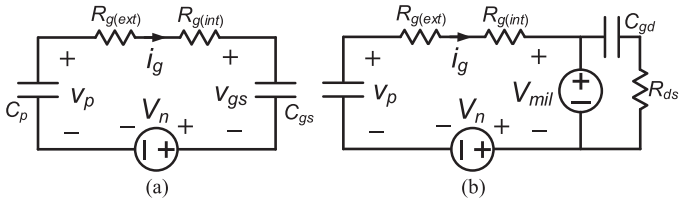

Fig. 11. Equivalent circuit of gate loop during turn-ON transient. (a) t_3 to $t_{3.2}$. (b) $t_{3.2}$ to $t_{3.3}$.

expressed as

$$E_{on} = \int_0^{t_{ov}} i_d v_{ds} dt \tag{8}$$

where t_{ov} is the overlap time between drain current and drain-source voltage. In Figs. 2 and 7, it equals to the sum of the current rise time t_{cr} and the voltage fall time t_{vf}. To simplify the analysis, the drain current and the drain-source voltage during the switching transient can be approximately regarded as linearly increasing or decreasing. Therefore, the switching loss can be indicated by comparing t_{cr} and t_{vf} with different gate drives.

The turn-ON transient starts at t_3 in Fig. 7. From t_3 to $t_{3.2}$, v_p decreases while v_{gs} increases, and the equivalent circuit is plotted in Fig. 11(a). The initial voltage of v_p and v_{gs} is $2V_{dr}$ and $-V_n$, respectively. The voltage relationship in the gate loop can be written as

$$2V_{dr} - \frac{1}{C_p}\int_0^t i_g(t)\,dt = R_g i_g(t) + \frac{1}{C_{gs}}\int_0^t i_g(t)\,dt \tag{9}$$

where R_g is the sum of $R_{g(ext)}$ and $R_{g(int)}$.

The gate current can be calculated as

$$i_g(t) = \frac{2V_{dr}}{R_g}\exp\left(-\frac{1}{R_g C_e}t\right) \tag{10}$$

where C_e is the equivalent capacitance in the gate loop

$$\frac{1}{C_e} = \frac{1}{C_p} + \frac{1}{C_{gs}} \tag{11}$$

where v_p and v_{gs} during the charging are

$$\begin{aligned} v_p(t) &= 2V_{dr} - \frac{1}{C_p}\int_0^t i_g(t)\,dt \\ &= 2V_{dr} - \frac{2V_{dr}C_e}{C_p}\left[1 - \exp\left(-\frac{1}{R_g C_e}t\right)\right] \end{aligned} \tag{12}$$

$$v_{gs}(t) = \frac{1}{C_{gs}}\int_0^t i_g(t)\,dt - V_n = \frac{2V_{dr}C_e}{C_{gs}}\left[1-\exp\left(-\frac{1}{R_gC_e}t\right)\right] - V_n. \quad (13)$$

The current rise time t_{cr} is from $t_{3.1}$ to $t_{3.2}$. At $t_{3.1}$, v_{gs} is equal to the threshold voltage V_{th}. At $t_{3.2}$, v_{gs} is equal to the Miller voltage V_{mil}. With (13), the time interval from $t_{3.1}$ to $t_{3.2}$ is calculated as

$$t_{cr(\text{CPG})} = t_{3.2} - t_{3.1} = R_gC_e\ln\left[\frac{2V_{dr}C_e - (V_{th}+V_n)C_{gs}}{2V_{dr}C_e - (V_{\text{mil}}+V_n)C_{gs}}\right] \quad (14)$$

where V_{mil} is related to the load current I_L and the transconductance of the SiC MOSFET g_m

$$V_{\text{mil}} = V_{th} + \frac{I_L}{g_m}. \quad (15)$$

Starting from $t_{3.2}$, the gate current discharges the transfer capacitance C_{gd}, and the gate voltage is clamped at V_{mil}. The equivalent circuit changes to Fig. 11(b). The voltage relationship is

$$v_p(t_{3.2}) - \frac{1}{C_p}\int_0^t i_g(t)\,dt = R_gi_g(t) + V_{\text{mil}} + V_n. \quad (16)$$

The initial voltage of v_p at $t_{3.2}$ can be calculated by (12)

$$v_p(t_{3.2}) = 2V_{dr} - \frac{(V_{\text{mil}}+V_n)C_{gs}}{C_p}. \quad (17)$$

The gate current is derived as

$$i_g(t) = \frac{V_0}{R_g}\exp\left(-\frac{1}{R_gC_p}t\right) \quad (18)$$

where $V_0 = v_p(t_{3.2}) - V_{\text{mil}} - V_n$.

The gate drive output voltage v_p is

$$v_p(t) = v_p(t_{3.2}) - \frac{1}{C_p}\int_0^t i_g(t)\,dt = v_p(t_{3.2})\exp\left(-\frac{1}{R_gC_p}t\right). \quad (19)$$

During the voltage fall time t_{vf} from $t_{3.2}$ to $t_{3.3}$, the voltage across the transfer capacitance decreases from V_{dc} to around zero. The process is expressed as

$$\frac{1}{C_{gd}}\int_0^{t_{vf}} i_g(t)\,dt = V_{dc}. \quad (20)$$

Substituting (18) into (20), the voltage fall time can be calculated

$$t_{vf(\text{CPG})} = R_gC_p\ln\left(\frac{V_0C_p}{V_0C_p - V_{dc}C_{gd}}\right). \quad (21)$$

In terms of the conventional VSG, the equivalent circuit can be obtained by replacing C_p in Fig. 11 with a constant voltage source V_{dr}. The calculation procedure of t_{cr} and t_{vf} is similar to that with the proposed CPG, and the calculation results are

$$t_{cr(\text{VSG})} = R_gC_{gs}\ln\left(\frac{V_{dr}-V_{th}-V_n}{V_{dr}-V_{\text{mil}}-V_n}\right) \quad (22)$$

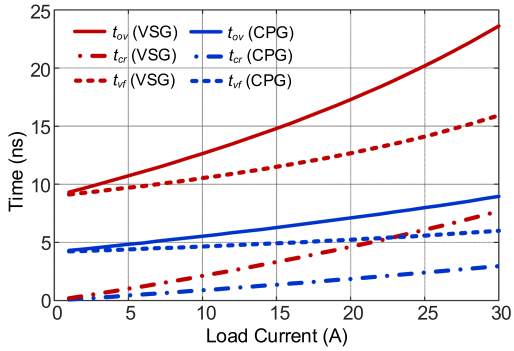

Fig. 12. Turn-ON switching time comparison between conventional VSG and the proposed CPG under different loads.

$$t_{vf(\text{VSG})} = R_gC_{gd}\frac{V_{dc}}{V_{dr}-V_{\text{mil}}-V_n}. \quad (23)$$

Based on (14) and (21)–(23), the turn-ON switching time is calculated for a 1.2 kV, 30 A SiC MOSFET [4] with zero external gate resistance, and the results at different load conditions are plotted in Fig. 12. Both the current rise time and voltage fall time achieve significant improvement especially at high load currents. Compared with the conventional VSG, the total turn-ON switching time is reduced by 60% at full load with the proposed CPG. Thus, lower turn-ON switching loss is achieved.

B. Gate Drive Loss

The gate drive loss of the proposed CPG is mainly generated in two intervals. First, energy is lost when C_p is pumped up by the flying capacitor C_f. Second, during the turn-ON transient, all the transferred energy from C_p to C_{gs}, C_{gd}, and C_{OSSL} is dissipated.

Assuming C_f is much larger than C_p, during the charge pump state from t_1 to t_2 in Fig. 7, v_p increases from V_{dr} to $2V_{dr}$. C_f can be regarded as a constant voltage source, and v_f does not change. According to the energy transfer theory, the amount of energy transferred to the capacitor equals to the amount of energy dissipated in the circuit. Thus, the energy loss from t_1 to t_2 is written as

$$E_{g1} = \frac{1}{2}C_p(2V_{dr})^2 - \frac{1}{2}C_pV_{dr}{}^2 = \frac{3}{2}C_pV_{dr}{}^2. \quad (24)$$

During the turn-ON transient, the initial and final voltage of v_p is $2V_{dr}$ and V_{dr}, respectively. Therefore, the energy loss E_{g2} from t_2 to t_5 is the same as E_{g1}. Neglecting the loss of other parts in the CPG, the total gate drive loss during one switching period is

$$E_{g(\text{CPG})} = E_{g1} + E_{g2} = 3C_pV_{dr}{}^2. \quad (25)$$

In terms of the conventional VSG, the gate drive loss is calculated by

$$E_{g(\text{VSG})} = V_{dr}Q_g \quad (26)$$

where Q_g is the total gate charge of the SiC MOSFET, which usually can be obtained from the device datasheet.

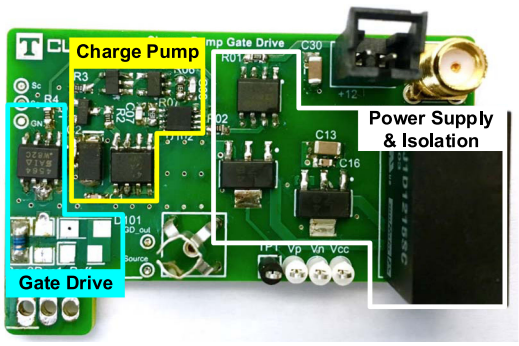

Fig. 13. Prototype of the proposed CPG.

TABLE I
COMPONENTS AND PARAMETERS OF CPG

M_1, M_2	SI4599 P and N channel MOSFETs, Vishay, 40 V, 5 A	M_H, M_L	SI4559 P and N channel MOSFETs, Vishay, 60 V, 4 A
D_1, D_2	SS24 Schottky diode, ONSemi, 40 V, 2 A	C_p	Calculated with (7)
		C_f	Around 50 × C_p

With the same SiC MOSFET used in Fig. 12, the gate drive loss of the proposed CPG is calculated to be 1.7 μJ, while that of the conventional VSG is 1.0 μJ. Therefore, the gate drive loss increases with the proposed CPG. However, the typical switching loss of the SiC MOSFET is much higher than 100 μJ. Thus, the increased gate drive loss can be neglected compared to the reduction of the turn-ON switching loss with the proposed CPG.

VII. Experimental Results and Discussion

A. Hardware Setup

The proposed CPG is developed, and the prototype is shown in Fig. 13. The CPG can change to a conventional VSG by disabling the signal S_c. Thus, comparison experiments can be conducted for both the proposed CPG and conventional VSG on the same gate drive board. The proposed CPG has more components and increased size. However, all the added components are discrete semiconductor devices with low power and voltage ratings, which are easy to be integrated. The components and parameters used for the gate drive are given in Table I. Double pulse test (DPT) is implemented to evaluate the performance of the SiC MOSFETs with the proposed CPG.

The architecture of a typical DPT is drawn in Fig. 14(a). Two pulses with different time intervals are provided to turn ON the device under test. Fig. 14(b) plots the ideal waveforms of a DPT. With the waveform data, the switching transient can be analyzed. In [32], a detailed design and implementation method of DPT for wide band-gap devices has been introduced and is followed in the test. Fig. 15 illustrates the testing platform of the DPT.

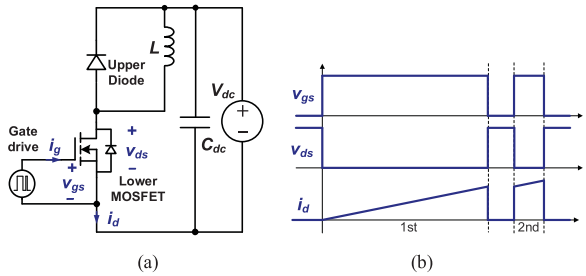

Fig. 14. Double pulse test. (a) Architecture. (b) Ideal waveforms.

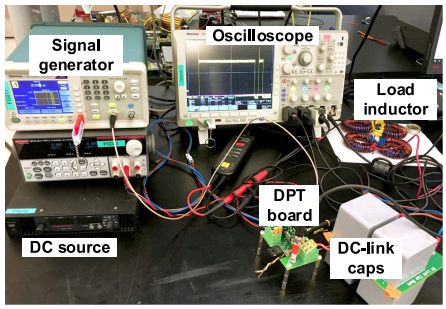

Fig. 15. Testing platform of DPT.

TABLE II
PARAMETERS OF TESTED SiC MOSFETs

	Device A	Device B
Part No.	C3M0075120K	SCT3030KL
Manufacturer	Wolfspeed	Rohm
Packaging	TO-247 4pin	TO-247 3pin
Voltage	1.2 kV	1.2 kV
Current	30 A	72 A
$R_{g(int)}$	10.5 Ω	5 Ω
C_{gs}	1.4 nF	2.2 nF
C_{gd_Q}	8.7 pF	98 pF
V_{dr}	19 V	18 V
V_n	4 V	0

To comprehensively investigate the performance of the proposed CPG, two SiC MOSFETs from different manufacturers are tested. The device parameters are given in Table II. To leave enough margin for the drain-source voltage and avoid the influence of crosstalk from the upper device, a 1.7 kV SiC Schottky diode (C3D25170H from Wolfspeed) is used as the upper device (synchronous switch).

B. Experimental Results

The basic charge pump function of the proposed CPG is evaluated first. Based on the calculation from (7), C_p should be 1.7 nF for the tested SiC MOSFET. Fig. 16 shows the tested pumped voltage and external gate voltage with different C_p values for device A, which has 1.4 nF gate capacitance. When

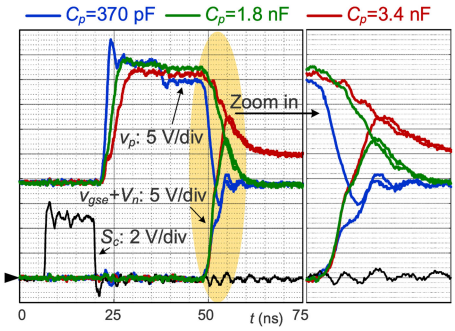

Fig. 16. Tested waveforms of pumped voltage and external gate voltage with different C_p.

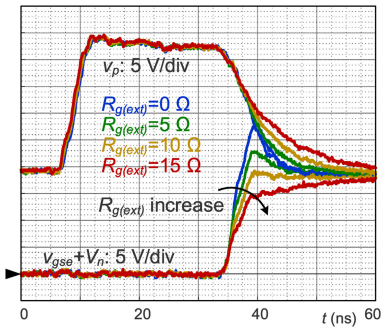

Fig. 17. Tested waveforms of pumped voltage and external gate voltage with different $R_{g(\mathrm{ext})}$.

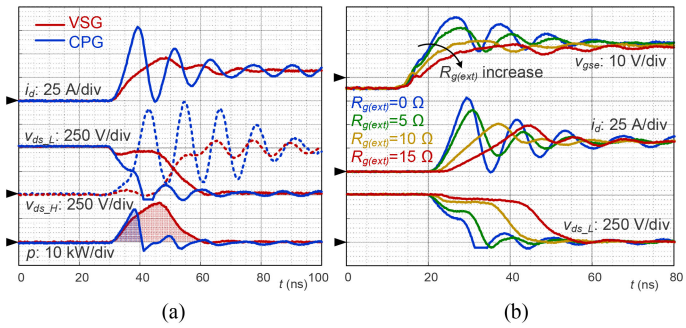

Fig. 18. Tested turn-ON transient waveforms for Device A at 500 V, 30 A. (a) Comparison between CPG and VSG with zero $R_{g(\mathrm{ext})}$. (b) CPG with different $R_{g(\mathrm{ext})}$.

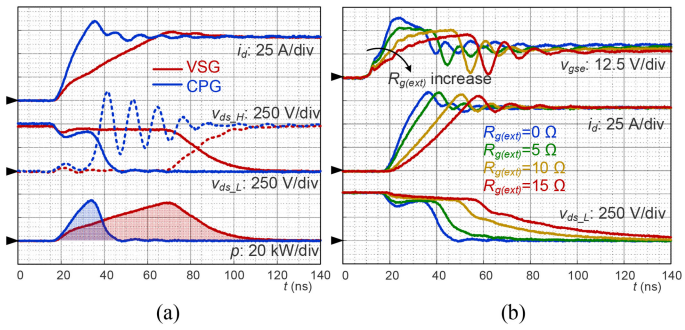

Fig. 19. Tested turn-ON transient waveforms for device B at 500 V, 65 A. (a) Comparison between CPG and VSG with zero $R_{g(\mathrm{ext})}$. (b) CPG with different $R_{g(\mathrm{ext})}$.

C_p is 370 pF, v_p decreases quickly while $(v_{\mathrm{gse}} + V_n)$ rises slowly, resulting in higher switching loss. When C_p is 3.4 nF, the final static gate-source voltage v_{gse} is 21 V, which exceeds the gate voltage rating of the tested SiC MOSFET (19 V). When C_p is 1.8 nF, however, the final static voltage is the same as the blue curve, which equals to V_{dr}, and the gate voltage rises much more rapidly than the blue curve. Note that $(v_{\mathrm{gse}} + V_n)$ can be higher than v_p because the SiC MOSFET has 10.5 Ω internal gate resistance, while the external gate resistance is zero. The capacitance value in this case is slightly higher than the calculation result (1.7 nF) from (7). It is mainly because the calculation neglects the energy loss during the charge transfer. Generally, the testing result can match well with the analysis in Fig. 9.

The switching speed of the SiC MOSFET can be tuned by changing the external gate resistance. Fig. 17 illustrates the tested pumped voltage and external gate voltage with different $R_{g(\mathrm{ext})}$ when C_p is 1.8 nF. The gate voltage rises slower with larger $R_{g(\mathrm{ext})}$. Therefore, the usage of the CPG is the same as a conventional VSG, and the switching speed can be easily regulated. Remarkably, the steady state v_p is independent of $R_{g(\mathrm{ext})}$, and it approaches to V_{dr}.

The tested turn-ON transient waveforms with the proposed CPG and the conventional VSG for Device A are plotted in Fig. 18(a). Both gate drives utilize zero external gate resistance. Clearly, both the current rise time and voltage fall time are greatly reduced, which indicates much faster switching speed with the proposed CPG. The shaded area of the instantaneous power suggests that the turn-ON switching loss is also significantly decreased. Fig. 18(b) demonstrates the transient waveforms of the proposed CPG with different external gate resistances. By increasing the resistance, the switching speed is slowed. Detailed data analysis will be presented in the following section.

Fig. 19(a) and (b) shows the tested waveforms for device B. Similar to the result for device A, the proposed CPG can achieve much higher switching speed.

C. Data Analysis

With the data of the DPT waveforms, the switching loss can be obtained with the integral of the product of the drain-source voltage and drain current during the switching transient. The comparison of the turn-ON time and loss for device A is given in Fig. 20(a) and (b). The proposed CPG with various $R_{g(\mathrm{ext})}$ and the conventional VSG with zero $R_{g(\mathrm{ext})}$ are illustrated. In addition, the result with the CSG drive in [27] is included since it is tested with the same SiC MOSFET and under the same operating conditions. From Fig. 20(a), with zero $R_{g(\mathrm{ext})}$, the proposed CPG can achieve 67.4% reduction in turn-ON switching time compared with VSG. Moreover, the turn-ON time of the CPG is even less than that of the CSG, where constant gate current is provided. As the external gate resistance increases, the switching time of the CPG increases. Nevertheless, until $R_{g(\mathrm{ext})}$ reaches 15 Ω, the turn-ON time of the CPG is lower than the VSG with zero $R_{g(\mathrm{ext})}$.

The turn-ON loss exhibits a similar trend. At full load and with zero $R_{g(\mathrm{ext})}$, the proposed CPG has 71.7% reduction in turn-ON

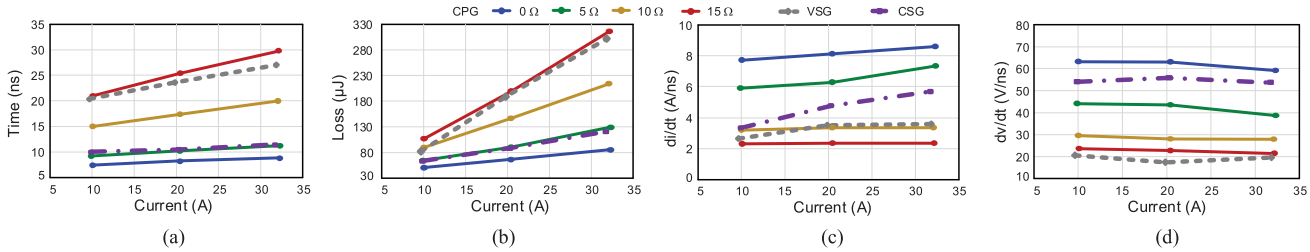

Fig. 20. Performance comparison of proposed CPG with different $R_{g(\mathrm{ext})}$, VSG and CSG for Device A. (a) Turn-ON time. (b) Turn-ON loss. (c) Average *di/dt*. (d) Average *dv/dt*.

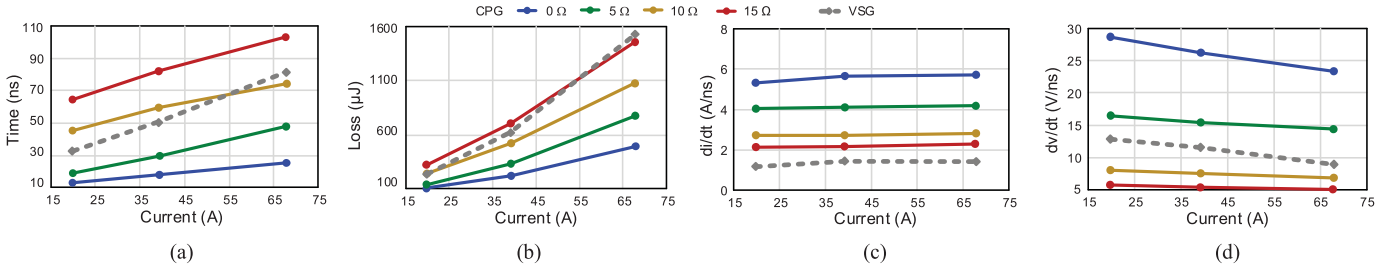

Fig. 21. Performance comparison of proposed CPG with different $R_{g(\mathrm{ext})}$ and VSG for Device B. (a) Turn-ON time. (b) Turn-ON loss. (c) Average *di/dt*. (d) Average *dv/dt*.

loss compared with the VSG, and 29.4% reduction compared with the CSG.

The average *di/dt* and *dv/dt* during the switching transient are plotted in Fig. 20(c) and (d). The *di/dt* with zero $R_{g(\mathrm{ext})}$ at full load condition is 2.4 times of the VSG, and the achieved maximum *di/dt* is 8.6 A/ns. The *dv/dt* is 3.0 times higher than the VSG with a maximum value of 63.2 V/ns.

Similarly, significant improvement is shown with device B, as illustrated in Fig. 21. The proposed CPG achieves 69.5% decrease of the turn-ON time and 67.9% decrease of the turn-ON loss at full load and with zero $R_{g(\mathrm{ext})}$. The corresponding *di/dt* and *dv/dt* is 4.0 and 2.6 times higher than the VSG, and the maximum value is 12.3 A/ns and 28.7 V/ns, respectively.

D. Challenges and Discussion

Despite the higher switching speed, there are also challenges when utilizing the proposed CPG. As can be observed from Figs. 18(a) and 19(a), the turn-ON drain-source voltage oscillation across the upper devices (synchronous switch) is significantly increased because of the high switching speed. The mechanism of the oscillation is shown in Fig. 22 [33]. After the load current commutates from the upper to the lower device, the drain-source voltage of the lower device decreases. The generated *dv/dt* results in a resonance between the output capacitance C_{OSSH} of the upper device and the stray inductance L_{ds}, causing oscillation and overvoltage. Higher switching speed of the lower device leads to higher *dv/dt*, contributing to more severe oscillation across the upper device.

The overvoltage with different gate resistances is shown in Fig. 23. With zero $R_{g(ext)}$, the overvoltage is 492 V with device A, and 384 V with device B. In hard switching applications, there is always tradeoff between higher switching speed and

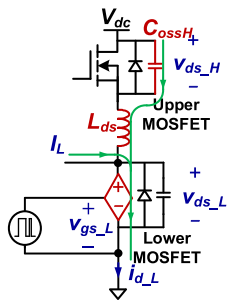

Fig. 22. Mechanism of overvoltage across upper device.

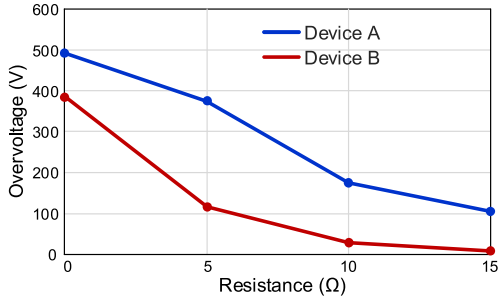

Fig. 23. Turn-ON drain-source overvoltage of synchronous switch with different $R_{g(\mathrm{ext})}$.

detrimental side effect resulting from parasitics. However, since the synchronous switch turns OFF with zero current, the voltage overshoot does not increase the overall switching loss.

Another issue caused by the higher switching speed and parasitics is the crosstalk in an FET-FET phase-leg architecture. To evaluate the crosstalk with the proposed CPG, the upper device is changed to a SiC MOSFET, which is the same as the

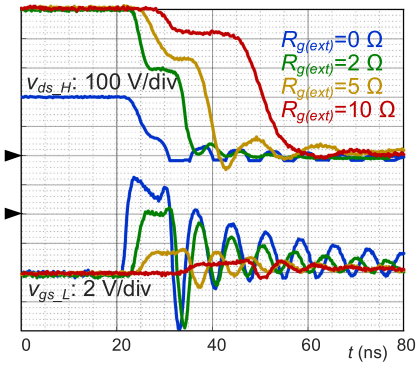

Fig. 24. Tested crosstalk waveform for device A with different $R_{g(\text{ext})}$.

lower device. The upper device operates as the active switch, and the gate voltage of the lower device is monitored. As shown in Fig. 24, with zero $R_{g(\text{ext})}$, the gate voltage of the lower device increases to 2 V during the turn-ON transient when dc voltage is 200 V, which has the potential to cause shoot-through. With higher $R_{g(\text{ext})}$, the gate voltage decreases and keeps under the threshold voltage. Thus, the proposed CPG can achieve higher switching speed without causing shoot-through in most cases.

In extreme cases that require ultra-fast switching speed such that zero $R_{g(\text{ext})}$ is required, anticrosstalk auxiliary circuits [28], [31], [34], [35] can be adopted to mitigate the issue. It is worth noting that the proposed CPG can also be implemented to dynamically decrease the gate voltage of the synchronous switch during the turn-ON transient, so that the device is more difficult to be falsely turned ON.

Generally, higher overvoltage and worse crosstalk is the intrinsic penalty of the switching speed increase. However, the value of the proposed CPG is not deteriorated by these side effects. From Figs. 20 and 21, even though the gate resistance of the proposed CPG increases to 10 Ω, the switching loss is still much lower than the conventional VSG. With such higher resistance, the overvoltage is within the acceptable range, and the crosstalk does not cause shoot-through according to Figs. 23 and 24.

In real applications, it is up to the designer to decide the proper switching speed to achieve good balance in different aspects of converter performance, which is the same way for a conventional VSG implementation. Thus, the proposed CPG provides the potential to further increase the switching speed and reduce the switching loss of the SiC MOSFET, which is difficult to achieve with the conventional VSGs.

VIII. Conclusion

The turn-ON switching speed of the SiC MOSFET is difficult to increase with conventional VSGs because of the large internal gate resistance and the limited gate voltage rating. This article proposes a CPG drive utilizing a charge transfer technique, which can dynamically increase the gate drive output voltage during the turn-ON switching transient to increase the switching speed. With the proper capacitance selection for the proposed CPG, the gate drive voltage can automatically drop back to the normal ON state value without additional control, which avoids the overcharging issue and yields a simple gate drive structure.

The function of the proposed CPG is verified with DPTs with different load and external gate resistances. Two SiC MOSFETs from different manufacturers are tested and compared to the results with the conventional VSG. Under full load condition, the turn-ON switching time of the CPG is decreased by 67.4% and 69.5% for the two MOSFETs, while the turn-ON switching loss achieves a reduction of 71.7% and 67.9%, respectively. The challenge of implementing the proposed CPG is the larger parasitic influence such as the overvoltage and crosstalk caused by the higher *di*/*dt* and *dv*/*dt* as a result of the increased switching speed. The end-user can tune the external gate resistance to adjust the switching speed, which is the same as a conventional VSG.

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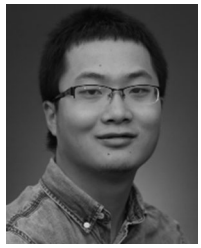
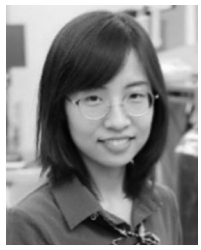


Handong Gui (Student Member, IEEE) received the B.S. and M.S. degrees from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2013 and 2016, respectively, and the Ph.D. degree from the University of Tennessee, Knoxville, TN, USA, in 2020, all in electrical engineering.

From October 2019 to March 2020, he was with the University of Cambridge, U.K., as a Visiting Scholar. He has authored or coauthored over 40 journal and conference papers and one book chapter. His research interests include wide band-gap devices and applications, multi-level converters, and electrified transportations.



Jingjing Sun (Student Member, IEEE) received the B.S. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2016, and the M.S. degree in 2018 from the University of Tennessee, Knoxville, USA, where she is currently working toward the Ph.D. degree in power electronics with CURENT.

Her research interests include applications of wide band-gap semiconductor devices, high-efficiency power supply design, and hardware-based emulation of data center power supply systems.

Leon M. Tolbert (Fellow, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Georgia Institute of Technology, Atlanta, Georgia, in 1989, 1991, and 1999, respectively.

From 1991 to 1999, he was with the Oak Ridge National Laboratory, Oak Ridge, TN, USA. He was an Assistant Professor with the Department of Electrical and Computer Engineering, The University of Tennessee, Knoxville, TN, USA, in 1999. He is currently the Min H. Kao Professor with the Min H. Kao Department of Electrical Engineering and Computer Science, The University of Tennessee. He is also a Founding Member of the NSF/DOE Engineering Research Center, Center for Ultra-Wide-Area Resilient Electric Energy Transmission Networks (CURENT), UTK. He is also an Adjunct Participant with the Power Electronics and Electric Machinery Research Center, Oak Ridge National Laboratory.

Dr. Tolbert is a Registered Professional Engineer with the state of Tennessee. He was the recipient of the 2001 IEEE Industry Applications Society Outstanding Young Member Award, and Six prize Paper Awards from the IEEE Industry Applications Society and IEEE Power Electronics Society. He was an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS, from 2007 to 2013. He was a Member-At-Large to the IEEE Power Electronics Society Advisory Committee from 2010 to 2012, Chair of the PELS Membership Committee from 2011 to 2012, and a member of the PELS Nominations Committee from 2012 to 2014. From 2014 to 2017, he was the Paper Review Chair for the Industry Power Converter Committee of the IEEE Industry Applications Society.