An Ultrahigh Step-Up Quadratic Boost Converter Based on Coupled-Inductor

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***Abstract*—In this article, an ultrahigh step-up quadratic boost converter based on coupled-inductor is proposed. The voltage gain of the proposed converter can be enhanced significantly by increasing the duty cycle due to the quadratic boost structure. A coupled-inductor integrated with a voltage doubler cell is applied to further improve conversion ratio and reduce voltage stresses. The leakage inductor current is utilized to achieve zero-current switching for output diode. Meanwhile, high efficiency is possible as the energy of the leakage inductor is recycled and transferred to the load. The operating principle and steady-state analysis are provided, and a 280-W prototype is designed to verify the validity of the proposed converter.**

***Index Terms*—Coupled-inductor, low voltage stress, quadratic boost, ultrahigh step-up.**

I. Introduction

As THE reserves of conventional fossil fuels can hardly satisfy the growing demand, the worldwide resource crisis becomes more and more serious [1]. In order to meet energy demand and curb environmental pollution, renewable energy generation systems, such as solar and fuel cell power, are becoming a focus of current research [2]. However, the terminal voltage of the renewable power generating unit is usually low and fluctuant. A high step-up dc–dc converter with a wide input voltage range is necessary to generate the required dc bus voltage for the grid connection [3]. In addition, a low input current ripple is also necessary, as it can increase the lifetime of renewable energy sources [22].

Theoretically, the conventional boost converter (CBC) has an infinite voltage gain by increasing the duty cycle of the main switch; therefore, it is an important candidate for step-up occasions. However, the voltage stress of the main switch equals the output voltage, which means a high voltage rating switch with an increased cost and large ON-resistance is required. In addition, when an extremely high duty cycle is applied, the efficiency and gain of CBC will decrease dramatically due to the equivalent series resistance (ESR) of the inductor and reverse recovery problem of output diode. Taking the abovementioned reasons into account, the application of CBC is limited to those not needing a high voltage conversion ratio [4].

To achieve a high voltage gain with proper duty cycle, many voltage lift techniques, including switch-capacitor (SC) and switch-inductor (SL) structures, have been investigated [5]–[13]. The SC-based converters (SCCs) are widely used because of their characteristics of reduced voltage stress and improved voltage gain [5]–[8]. However, these converters suffer large transient current, which will influence the service life of equipment [9]. A small resonant inductor can be inserted into SCC to suppress the current peak, and zero voltage switching of the main switch can be achieved by utilizing resonant current [10]. Nevertheless, when a higher voltage gain is required, the demand for SC cells is further increased, resulting in high cost and low power density. The SL-based converters (SLCs) are also valuable boost topologies, where inductors are charged in parallel and discharged in series to achieve high output voltage [11]–[13]. However, plenty of magnetic devices are needed in SLC.

The coupled-inductor (CL) technique is introduced as it allows employing turns ratio besides the duty cycle to improve the voltage gain. Thus, the duty cycle is varied in a suitable range and the power loss is reduced in CL-based converters (CLCs). In practice, the flyback converter is widely used due to its simple structure and modulation scheme [14]. However, it suffers from high voltage spike over the main switch. To suppress the voltage spike and recycle energy stored in leakage inductor, many clamping circuits are applied to CLCs [15], [16]. Furthermore, many voltage-lift circuits, which can clamp the voltage of switch with an improved voltage gain, are also carried out [17]–[20]. It is necessary to point out that the CLCs mentioned above rely on the turns ratio of CL heavily to achieve an ultrahigh voltage gain. A high turns ratio will deteriorate the performance of the system as it leads to large leakage inductance and high current ripple. In order to overcome this problem, a CL-based SCC with an ultrahigh gain is proposed in [20] and [21], but they still face high current ripple. The interleaved CLCs with winding-cross-coupling are well-known for its low input current ripple [22]. Nevertheless, the duty cycle of the main switches must be greater than 0.5, making the topologies unsuitable for the

Manuscript received November 21, 2019; revised February 12, 2020; accepted May 16, 2020. Date of publication May 19, 2020; date of current version July 31, 2020. This work was supported in part by the National Natural Science Foundation of China under Grants 61573155 and 51877085, in part by the Guangdong Natural Science Foundation under Grant 2018A030313066, in part by the Central University of SCUT under Grant 2018ZD50, and in part by the Guangdong Key Laboratory of Clean Energy Technology. Recommended for publication by Associate Editor O. Lucia. *(Corresponding author: Junfeng Liu)*.

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Digital Object Identifier 10.1109/TPEL.2020.2995911

occasions with high voltage fluctuation. To solve this problem, the integration of CL and the single-ended primary inductor converter (SEPIC) is proposed in [23]. However, the voltage gain is not high enough.

The cascaded boost is an interesting topology because of its quadratic voltage gain versus the duty cycle [24]. This topology consists of two boost stage; thus, the structure called the quadratic boost converter (QBC) is derived by integrating two switches into one to improve the power density [25]. Although the output voltage of QBC is significantly improved, the main switch will suffer from high voltage stress. In [26]–[28], the CL-based QBCs are researched. To be specific, the filter inductors of the second boost stage are replaced by CL, and the voltage multipliers are applied to the secondary winding of CL to further increase the voltage gain. As a result, a high voltage gain with reduced input current ripple is achieved.

In this article, a novel converter based on an improved QBC and CL is proposed. The voltage doubler cell is also employed to improve the gain characteristic. This topology can achieve an ultrahigh voltage conversion ratio, which is much higher than that in the other converters based on QBC. The main properties are summarized as follows.

1) The voltage conversion ratio is effectively enhanced by improving the input voltage of the second boost stage of the QBC.
2) The voltage stresses of main switches are reduced, which means low voltage rating switches with small ON-resistance can be used to reduce the conduction losses.
3) The energy stored in the leakage inductor is recycled, and then transferred to the load.

II. Description of the Proposed Converter

A. Circuit Topology

The proposed converter is the combination of an improved QBC and a voltage doubler through a CL. The structure of the proposed converter is shown in Fig. 1(a). It can be found that the first boost stage of improved QBC contains an inductor L_1, a switch S_1, two diodes (D_1 and D_2), and two capacitors (C_1 and C_2). The two capacitors are connected in series to charge the CL of the second boost stage. The equivalent circuit of the proposed converter with considering the magnetic inductor L_m and leakage inductor L_k of CL is given in Fig. 1(b). The primary and secondary sides of CL are named N_p and N_s, respectively. During the operation process, L_m is used as a filter inductor to adjust the output voltage of the second boost stage. N_s is imbedded into the voltage doubler cell, composed of two diodes (D_{o2} and D_{o3}) and two capacitors (C_{o2} and C_{o3}), to further increase the voltage gain and reduce the voltage stress. Meanwhile, the energy stored in L_k is absorbed by capacitor C_{o1} and then transferred to the load.

B. Operating Principles

The operating principles of the proposed converter are provided in this part. Before the analyses, some assumptions are considered as follows.

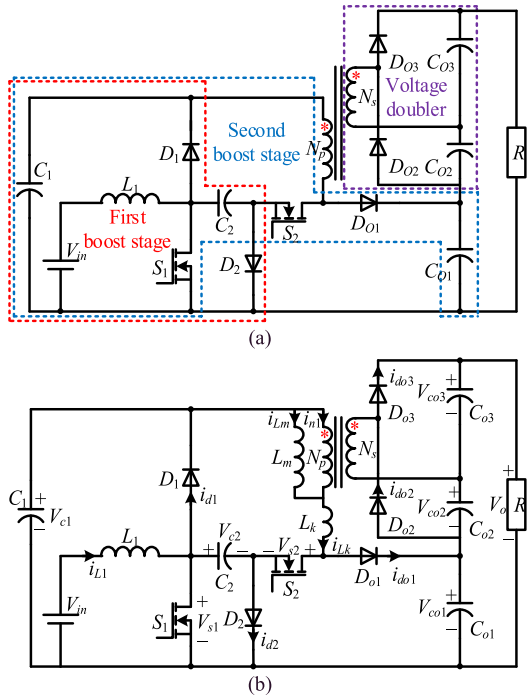

Fig. 1. Circuit of the proposed converter. (a) Schematic diagram. (b) Equivalent circuit.

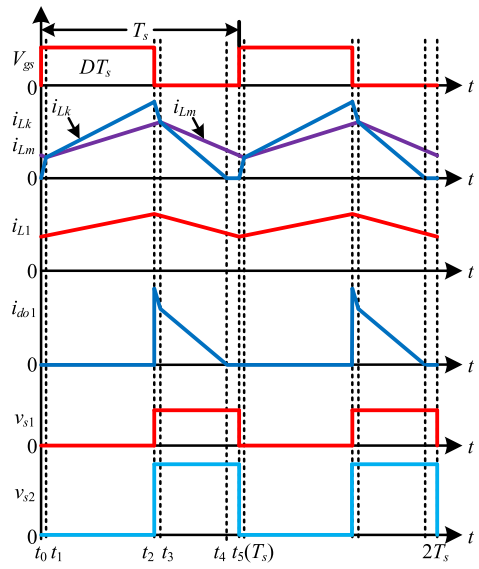

Fig. 2. Key waveforms of the proposed converter.

1) All components in the circuit are ideal devices, especially the parasitic capacitors of switches, and the forward voltage drops of diodes are ignored. Meanwhile, the equivalent resistances of inductors and capacitors are also not considered.
2) Capacitors and inductors are large enough; thus, voltage ripples of capacitors and current ripple of L_1 are ignored.
3) The turns ratio of CL is defined as n, which equals N_p/N_s.

The key waveforms of the proposed converter are given in Fig. 2. It can be found that the switches S_1 and S_2 share the

same driving signal, which means they will be turned ON or OFF simultaneously. There are five switching modes during one operating period, and they are defined as Mode I, II, III, IV, and V, respectively. In addition, the equivalent circuit of each mode is illustrated in Fig. 3. The steady-state analyses are provided in detail as follows.

Mode I [t_0–t_1]: As shown in Fig. 3(a), S_1 and S_2 are both turned ON at t_0. Diode D_{o2} is forward biased, while diodes D_1, D_2, D_{o1}, and D_{o3} are reverse biased. The voltage over L_m is clamped by C_{o2}, and the energy stored in L_m is transferred to C_{o2} through D_{o2} and N_p. Thus, i_{Lm} decreases linearly. Capacitors C_1 and C_2 are connected in series to release their energy to the primary side of CL; thus, the current i_{Lk} increases rapidly. In the first boost stage, inductor L_1 is charged by $V_{\rm in}$, and i_{L1} increases linearly.

Mode II [t_1–t_2]: As shown in Fig. 3(b), S_1 and S_2 keep conducting. Diode D_{o3} is forward biased, while diodes D_1, D_2, D_{o1}, and D_{o2} are reverse biased. The energy stored in C_1 and C_2 is transferred to C_{o3} through N_s and D_{o3}. Meanwhile, L_m and L_k are also charged by C_1 and C_2. Currents i_{Lm} and i_{Lk} increase linearly. In the first boost stage, L_1 is charged by $V_{\rm in}$, and i_{L1} increases linearly.

Mode III [t_2–t_3]: As shown in Fig. 3(c), switches S_1 and S_2 are turned OFF at t_2. Diodes D_1, D_2, D_{o1}, and D_{o3} are forward biased, while diode D_{o2} is reverse biased. The voltage across S_2 is clamped by C_{o1}. The voltage over L_m is clamped by C_{o3}, and they are charged by L_k. Thus, current i_{Lm} increases linearly, while i_{Lk} decreases rapidly. In the first boost stage, inductor L_1 releases its energy to C_1 and C_2, and i_{L1} starts to decreases linearly.

Mode IV [t_3–t_4]: As shown in Fig. 3(d), switches S_1 and S_2 are still OFF. Diodes D_1, D_2, D_{o1}, and D_{o2} are forward biased, while diode D_{o3} is reverse biased by C_{o3}. The energy stored in L_m is transferred to C_{o2} through N_s and D_{o2}. The energy stored in L_k is recycled by C_{o1}. Thus, currents i_{Lm} and L_k decrease linearly. In the first boost stage, inductor L_1 still releases its energy to C_1 and C_2. This mode will end at t_4 when i_{Lk} decreases to 0. As a result, D_{o1} is turned OFF with zero current switching (ZCS).

Mode V [t_4–t_5]: As shown in Fig. 3(e), switches S_1 and S_2 are still OFF. Diodes D_1, D_2, and D_{o2} are forward biased, while diodes D_{o1} and D_{o3} are reverse biased. The voltage over L_m is clamped by C_{o2} and the energy stored in L_m is transferred to C_{o2}. In the first boost stage, inductor L_1 still releases its energy to C_1 and C_2.

III. Analysis of the Proposed Converter

A. Analysis of the Voltage Gain

In the first boost stage, the voltages over capacitors C_1 and C_2 are V_{c1} and V_{c2}, respectively. By using the volt–second balance principle to L_1, V_{c1} and V_{c2} can be derived as

$$V_{c1} = \frac{V_{\rm in}}{1-D} \tag{1}$$

$$V_{c2} = \frac{V_{\rm in}}{1-D}. \tag{2}$$

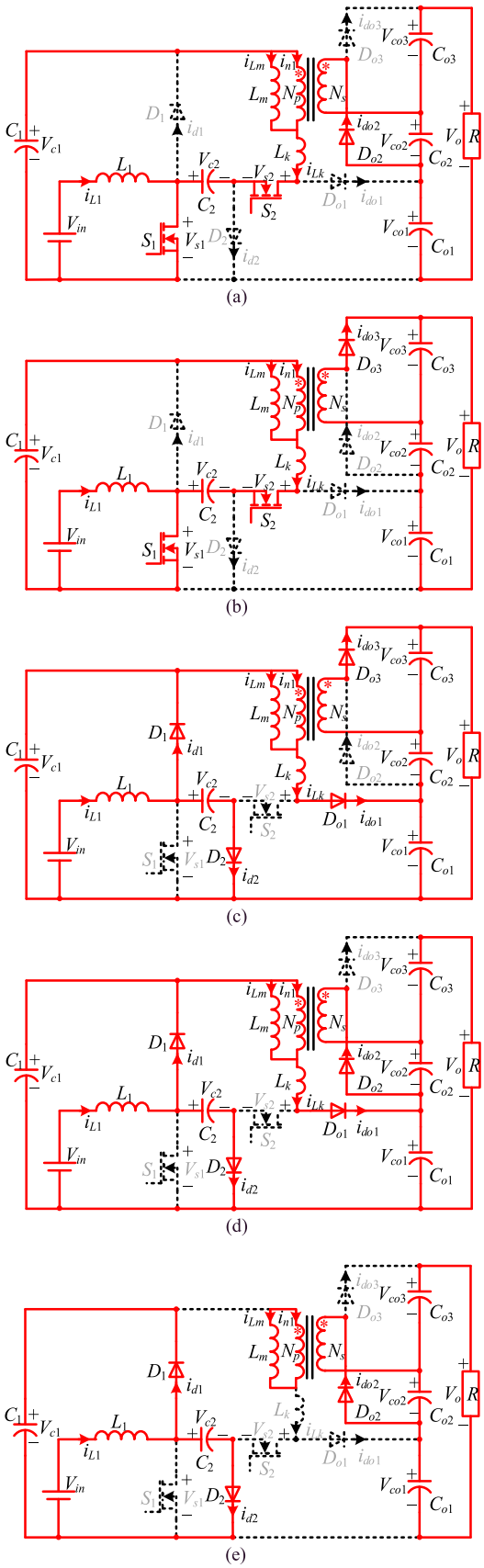

Fig. 3. Equivalent circuits of each switching state. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V.

In the second boost stage, the leakage inductor is much smaller than the magnetizing inductor. Thus, Modes I and III, caused by leakage inductor, are short. As a result, they can be ignored during the analysis.

As described in Mode II, diode D_{o3} is turned ON, and the current through D_{o3} can be described as

$$i_{do3} = \frac{i_{Lk} - i_{Lm}}{n} = \left(\frac{V_{Lk\_\mathrm{on}}}{nL_k} - \frac{V_{Lm\_\mathrm{on}}}{nL_m}\right) t (0 < t < DT_s) \tag{3}$$

where V_{Lk_on} and V_{Lm_on} are the voltages over leakage inductor and magnetic inductor, respectively, when switches are turned ON. D and T_s are the duty cycle and operating period of power switches.

In Mode IV, D_{o1} and D_{o2} are forward biased simultaneously, and the currents i_{do1} and i_{do2} are described as

$$i_{do1} = i_{Lm\_\max} - \frac{V_{Lm\_\mathrm{off}}}{L_m}(t - DT_s) \quad (DT_s < t < DT_s + D_aT_s) \tag{4}$$

$$i_{do2} = \frac{i_{Lm} - i_{Lk}}{n} = \left(\frac{V_{Lm\_\mathrm{off}}}{nL_m} - \frac{V_{Lk\_\mathrm{of}f}}{nL_k}\right)(t - DT_s) \quad (DT_s < t < DT_s + D_aT_s) \tag{5}$$

where V_{Lm_off} and V_{Lk_off} are the voltages over leakage inductor and magnetic inductor, respectively, when switches are turned OFF, D_a is the ratio between duration time of Mode IV and operation period. $i_{Lm\_\max}$ is the peak current through L_m.

In Mode V, D_{o1} is reverse biased, while D_{o2} is forward biased. The current through D_{o2} is expressed as

$$i_{do2} = \frac{i_{Lm\_\max} - V_{Lm\_\mathrm{off}}(t - DT_s)}{n} \quad (DT_s + D_aT_s < t < T_s). \tag{6}$$

As the average currents of capacitors are zero in the whole operation period, the average values of i_{do1}, i_{do2}, and i_{do3} are equal to the output current i_o. The following expressions can be derived:

$$\int_{DT_s}^{(D+D_a)T_s} i_{Lk}dt = i_o \tag{7}$$

$$\int_{0}^{DT_s} (i_{Lk} - i_{Lm})dt = ni_oT_s \tag{8}$$

$$\int_{DT_s}^{(D+D_a)T_s} (i_{Lm} - i_{Lk})dt + \int_{(D+D_a)T_s}^{T_s} i_{Lm}dt = ni_oT_s. \tag{9}$$

Substituting (3) into (8), the relationship between V_{Lm_on} and V_{Lk_on} can be further expressed as

$$\frac{V_{Lk\_\mathrm{on}}}{L_k} - \frac{V_{Lm\_\mathrm{on}}}{L_m} = \frac{2ni_o}{D^2T_s}. \tag{10}$$

In addition, when switches are turned ON, the input voltage of the second boost stage is shared by L_k and L_m. Thus, the following expression can be derived:

$$V_{Lk\_\mathrm{on}} + V_{Lm\_\mathrm{on}} = V_{\mathrm{in}} + V_{c1} + V_{c2} = 2V_{c2}. \tag{11}$$

Combining (10) and (11), V_{Lm_on} and V_{Lk_on} can be calculated as

$$V_{Lm\_\mathrm{on}} = \frac{2L_m}{L_m + L_k}\left(V_{c2} - \frac{L_k i_o}{D^2T_s}\right) \tag{12}$$

$$V_{Lk\_\mathrm{on}} = \frac{2L_k}{L_m + L_k}\left(V_{c2} + \frac{L_m i_o}{D^2T_s}\right). \tag{13}$$

Simultaneously, V_{Lm_off} can be calculated by applying the volt–second balance principle to L_m as

$$V_{Lm\_\mathrm{off}} = \frac{D}{1-D}V_{Lm\_\mathrm{on}}. \tag{14}$$

According to (4), (5), (8), and (9), $i_{Lm\_\max}$ and D_a can be derived as

$$i_{Lm\_\max} = \frac{T_s(1-D)^2V_{Lm\_\mathrm{off}} + 2i_o(n+1)L_m}{2(1-D)L_m} \tag{15}$$

$$D_a = \frac{4(1-D)i_oL_m}{T_s(1-D)^2V_{Lm\_\mathrm{off}} + 2i_o(n+1)L_m}. \tag{16}$$

By observing (16), D_a is always less than 1-D. L_k will decrease from $i_{Lm\_\max}$ to zero before switches are turned ON, which means the ZCS is always feasible for D_{o1} in the proposed converter. Meanwhile, V_{Lk_off} can be expressed as

$$V_{Lk\_\mathrm{off}} = \frac{\left[T_s(1-D)^2V_{Lm\_\mathrm{off}} + 2i_o(n+1)L_m\right]^2 L_k}{8(1-D)^2L_m^2i_oT_s}. \tag{17}$$

According to the current flow paths in Fig. 3, the voltages over C_{o1}, C_{o2}, and C_{o3} can be derived as

$$\begin{cases} V_{co1} = V_{\mathrm{in}} + V_{c1} + V_{Lm\_\mathrm{off}} + V_{Lk\_\mathrm{off}} \\ V_{co2} = nV_{Lm\_\mathrm{off}} \\ V_{co3} = nV_{Lm\_\mathrm{on}}. \end{cases} \tag{18}$$

Furthermore, C_{o1}, C_{o2}, and C_{o3} are always connected in series for supplying power to the load. Thus, the output voltage V_o can be calculated as

$$V_o = V_{co1} + V_{co2} + V_{co3}. \tag{19}$$

In the ideal case, the primary and secondary sides of CL are completely coupled, which means i_{Lk} is zero. Thus, the voltages over capacitors can be rewritten as follows:

$$\begin{cases} V_{co1} = \frac{1+D}{(1-D)^2}V_{\mathrm{in}} \\ V_{co2} = \frac{2nD}{(1-D)^2}V_{\mathrm{in}} \\ V_{co3} = \frac{2n}{1-D}V_{\mathrm{in}}. \end{cases} \tag{20}$$

The ideal voltage gain can be obtained as

$$M = \frac{V_o}{V_{\mathrm{in}}} = \frac{2n + 1 + D}{(1-D)^2}. \tag{21}$$

The curves of theoretical voltage gain versus duty cycle with considering the effects of L_k, L_m, and n are presented in Fig. 4. The voltage curves with different leakage inductance values are shown in Fig. 4(a), where the voltage gain decreases with the increase of leakage inductor. Especially the ideal voltage gain curve, corresponding with (21), can be obtained, when L_k

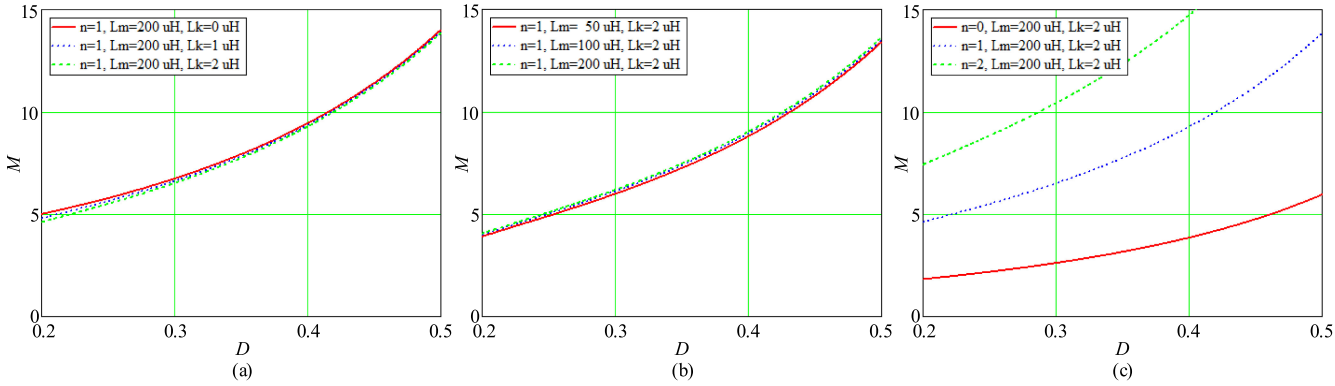

Fig. 4. Theoretical voltage gain versus duty cycle with considering the effects of different parameters. (a) Effect of leakage inductor on voltage gain. (b) Effect of the magnetic inductor on voltage gain. (c) Effect of turns ratio on voltage gain.

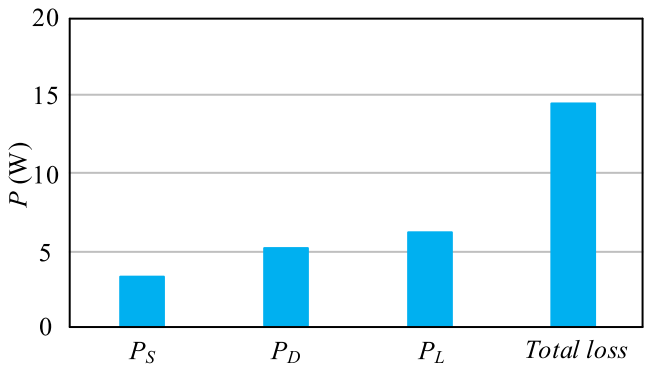

Fig. 5. Loss distribution of the proposed converter at 280 W.

TABLE I
NORMALIZED STRESSES OF THE PROPOSED ICL-QBC

Devices	Voltage stresses($/V_o$)	Current stresses($/i_o$)
S_1	(1-D)/(2n+1+D)	(n+nD+2D)/(1-D)^2
D_1	(1-D)/(2n+1+D)	(n+1)/(1-D)
D_2	(1-D)/(2n+1+D)	(n+D)/(1-D)
S_2	(1+D)/(2n+1+D)	(n+D)/(1-D)
D_{o1}	2/(2n+1+D)	1
D_{o2}	2n/(2n+1+D)	1
D_{o3}	2n/(2n+1+D)	1

equals 0. To explore the relationship between the voltage gain and L_m, the curves with different magnetic inductance values are provided in Fig. 4(b). It can be derived that the effect of leakage inductor on voltage gain is reduced as L_m increases. Moreover, Fig. 4(c) depicts three voltage gain curves versus the duty cycle under different turns ratio n. It intuitively indicates that the proposed converter is able to further improve the voltage gain by increasing the turns ratio of CL.

B. Analysis of Voltage and Current Stresses

In the first boost stage, as L_1 and V_{in} are connected in series, the average current i_{L1_ave} of L_1 can be calculated in the following equation by utilizing the conservation of energy principle:

$$i_{L1\_\text{ave}} = i_{\text{in\_ave}} = \frac{V_o}{V_{\text{in}}} = \frac{2n+1+D}{(1-D)^2} i_o. \tag{22}$$

Furthermore, the average current i_{Lm_ave} of L_m can be expressed as the following equation, since L_m operates as a filter inductor for the second boost circuit:

$$i_{Lm\_\text{ave}} = i_{Lm\_\max} - \frac{V_{Lm\_\text{off}}(1-D)T_s}{2} = \frac{n+1}{1-D} i_o. \tag{23}$$

By using the ampere–second principle to capacitors C_1 and C_2, the average currents through D_1 and D_2 satisfy the following relationship:

$$i_{D1\_\text{ave}} T_s = \int_0^{(D+D_a)T_s} i_{Lk} dt \tag{24}$$

$$i_{D2\_\text{ave}} T_s = \int_0^{DT_s} i_{Lk} dt. \tag{25}$$

From Fig. 3(b), it can be found that the average current i_{S2_ave} of S_2 equals to i_{D2_ave}, and the average current i_{S1_ave} of S_1 can be obtained as follows:

$$i_{S1\_\text{ave}} T_s = i_{L1\_\text{ave}} DT_s + \int_0^{DT_s} i_{Lk} dt. \tag{26}$$

Referring to the aforementioned description of the converter, the voltage stresses and current stresses of the semiconductors are summarized in Table I.

In Table I, it can be found that the high output voltage of the converter is divided into three parts and shared by output diodes. Meanwhile, the problem of high switch voltage stress in conventional QBC is also overcome. As a result, the voltage stresses of the proposed converter are reduced. Finally, the types of semiconductors can be chosen based on Table I in prototype design.

TABLE II
VALUES OF CAPACITORS AND INDUCTORS

Devices	Voltage/Current stresses	Minimum values
C_1	$V_{in}/(1\text{-}D)$	$(n+D)i_oT_s/DV_{in}x_{c1}\%$
C_2	$V_{in}/(1\text{-}D)$	$(n+D)i_oT_s/V_{in}x_{c2}\%$
C_{o1}	$(1+D)V_{in}/(1\text{-}D)^2$	$(1\text{-}D)^2(1\text{-}D_a)T_si_o/(1+D)V_{in}x_{co1}\%$
C_{o2}	$2nDV_{in}/(1\text{-}D)^2$	$(1\text{-}D)^2DT_si_o/2nDV_{in}x_{co2}\%$
C_{o3}	$2nV_{in}/(1\text{-}D)$	$(1\text{-}D)^2T_si_o/2nV_{in}x_{co3}\%$
L_1	$(2n+1+D)i_o/(1\text{-}D)^2$	$D(1\text{-}D)^2V_{in}T_si_o/(2n+1+D)\,x_{L1}\%$
L_m	$2nV_{in}i_o/(1\text{-}D)$	$V_{in}DT_si_o/(n+1)$

C. Selections of Inductors and Capacitors

According to the operating principles, the current ripple of L_1 can be calculated by the following equation:

$$\Delta i_{L1} = \frac{V_{\text{in}}DT_s}{L_1}. \tag{27}$$

Assuming the maximum current ripple rate of L_1 is $x_{L1}\%$, the following equation should be satisfied:

$$x_{L1}\% \geq \frac{\Delta i_{L1}}{i_{L1\_\text{ave}}}. \tag{28}$$

In the second boost stage, L_m needs to be operated with a continuous current. Based on (12) and (23), the critical condition for a continuous i_{Lm} can be described as

$$i_{Lm\_\text{ave}} \geq \frac{V_{Lm\_\text{on}}DT_s}{2L_m}. \tag{29}$$

As for the capacitor selection, the voltage ripple is an important reference. Assuming the maximum voltage ripple rate of the capacitor is $x_{ci}\%$, the capacitance can be expressed as

$$C_i \geq \frac{\int_0^{t_{ci}} i_{ci}dt}{V_{ci}x_{ci}\%} \tag{30}$$

where t_{ci} and i_{ci} are the charging current and charging time of the capacitor, respectively.

Based on the analysis mentioned above, the minimum values of capacitors and inductors are given in Table II. In addition, it is necessary to emphasize that a large magnetic inductor can alleviate the influence of the leakage inductor on voltage gain, which is testified in Fig. 4(b). However, the volume of the core is in proportion to the inductance. Thus, a tradeoff between volume and inductance should be considered in the CL designation.

D. Loss Analysis

The losses of the system can be divided into switch losses P_S, diode losses P_D, and inductor losses P_L. Furthermore, *Ps* contains switching loss P_{S_S} and conduction loss P_{S_C}. The switching loss is generated due to the turn-ON and turn-OFF delays of the switch, and it can be calculated by linearizing the voltage and current of the switch during the switching period as

$$P_{S\_S} = \frac{V_{ds}(I_{\text{on}}t_{\text{on}} + I_{\text{off}}t_{\text{off}})f_s}{6} \tag{31}$$

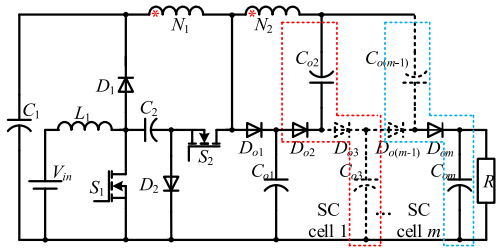

Fig. 6. Circuit of the improved structure.

where f_s is the operating frequency, t_{on} and t_{off} represent the turn-ON and turn-OFF delays, I_{on} and I_{off} are the turn-ON and turn-OFF currents, and V_{ds} is the voltage over switch. Assuming the ON-resistance and rms current of the switch are R_{on} and I_s, respectively, conduction loss of the switch can be calculated by

$$P_{S\_C} = I_s^2R_{\text{on}}. \tag{32}$$

The diode losses are caused by the threshold voltage V_d of the diode. When the average current of the diode is I_d, P_D can be described as

$$P_D = I_dV_d. \tag{33}$$

The inductor losses consist of core loss $P_{L\_C\text{ore}}$ and copper loss $P_{L\_C\text{opper}}$. The copper loss can be derived according to the following equation, where R_L and I_L are the ESR and rms current of the inductor, respectively:

$$P_{L\_\text{Copper}} = I_L^2R_L. \tag{34}$$

The core loss can be acquired as follow:

$$P_{L\_\text{Core}} = K_{Fe}f_s\left(\frac{\Delta B}{2}\right)^a V_e. \tag{35}$$

where K_{Fe} and α are determined by the core model and material. ΔB is related to the current ripple of the inductor. V_e is the volume of the core.

In order to observe the loss distribution of the system intuitively, the losses of each part are calculated by bringing in the related parameters into (31)–(35) at rating power, and then graphically represented in Fig. (5). It can be found that most power loss occurs in inductors. This situation is caused by the large ESRs of inductors. Meanwhile, the losses of switches are small as switches with low ON-resistances are employed.

E. Improved Structure Based on Switched-Capacitor

Actually, the voltage conversion ratio of the proposed converter has a positive correlation with the turns ratio n of CL, which means a large turns ratio is required for the ultrahigh voltage gain. However, it is impossible to get an extremely large turns ratio for the CL in practice, because the coupling coefficient of CL will deteriorate with the increasing of n. To overcome this issue, the improved structure based on SC is given in Fig. 6, where the number of SC cells is m. The ideal voltage gain of the

TABLE III
COMPARISONS OF THE PROPOSED CONVERTER AND OTHER HIGH STEP-UP TOPOLOGIES

Topologies	device Numbers			Voltage gain	Maximum voltage stress	Voltage stress of output	Voltage stress of	Current	Theoretical
	SD	*C*	*MC*	(*M*)	of switch($/V_{in}$)	diode($/V_{in}$)	output capacitor($/V_{in}$)	ripple	efficiency
Ref. [12]	9	1	4	$\frac{1+3D}{1-D}$	$\frac{M+1}{2}$	$M+1$	M	Large	95.36%
Ref. [20]	5	4	1	$\frac{2n+1-nD}{1-D}$	$\frac{M-n}{n+1}$	$M-n$	M	Large	91.07%
Ref. [25]	4	2	2	$\frac{1}{(1-D)^2}$	M	M	M	Small	94.17%
Ref. [28]	7	5	2	$\frac{n+nD+1}{(1-D)^2}$	$\frac{2M(2n+1)+n(W+n)}{2(2n+1)^2}$	$\frac{2Mn(2n+1)+n^2(W+n)}{2(2n+1)^2}$	M	Small	93.01%
Proposed	7	5	2	$\frac{2n+1+D}{(1-D)^2}$	$\frac{4M(n+1)-n(Q+1)}{4(n+1)^2}$	$\frac{4M(n+1)+Q+1}{4(n+1)^2}$	$\frac{4M(n+1)-n(Q+1)}{4(n+1)^2}$	Small	95.05%

$Q-\sqrt{8Mn+8M+1}$; $W-\sqrt{8Mn+4M+1}$; SD – Semiconductor device; C–Capacitor; MC – Magnetic core.

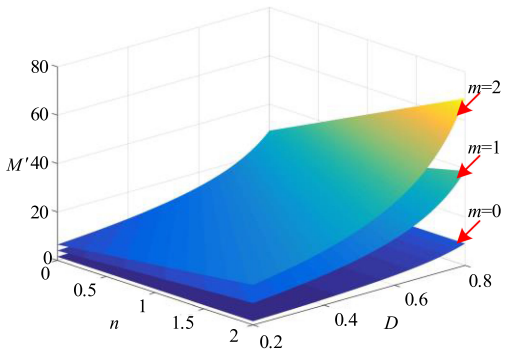

Fig. 7. Surfaces of voltage gain versus duty cycle and turns ratio with the different SC cells number of the improved structure.

structure can be derived as

$$M' = \frac{2m(n+1)+1+D}{(1-D)^2}. \tag{36}$$

According to (36), the surfaces depicted the voltage gain versus duty cycle and turns ratio with different *m* are presented in Fig. 7. It can be noted that the output voltage of the converter in Fig. 6 can be regulated by employing different SC cells, setting various turns ratio and changing the duty cycle of switches. As a consequence, the topology can achieve an ultrahigh voltage with a small turns ratio. It has broad application prospects in the future.

IV. COMPARISONS WITH EXISTING HIGH STEP-UP TOPOLOGIES

In this section, the proposed converter is compared with existing topologies in [12], [20], [25], and [28] that also provide high voltage gains. The voltage gains and the normalized equations described the voltage stresses, which are given in Table III. Furthermore, they are graphically represented in Fig. 8. The numbers of components applied in each compared circuit are also summarized. The input current ripple is considered, as a low current ripple can extend the service life of renewable energy sources [22].

For the fair of the comparison, the turns ratio *n* in Table III is defined as 2 uniformly. The voltage gains of these structures are compared in Fig. 8(a), which intuitively indicates that the proposed converter can achieve a higher voltage gain than the other four converters with the same duty cycle. Meanwhile, the voltage stresses of the output diode and capacitor of the proposed converter are lower than other converters with the same voltage gain, which are proved in Figs. 8(c) and (d). Also, the comparison of voltage stresses over switches is provided in Fig. 8(b). It can be observed that the switches in the proposed converter suffer from lower stresses than the converters in [12], [20], and [25]. Thus, a high voltage gain with reduced voltage stresses is achieved in the proposed converter.

When the device numbers are considered, the topologies in [20] and [25] have an advantage compared with the proposed converter, as listed in Table III. However, they are not suitable for the renewable energy generation systems, as the input current ripple is large in [20] and the voltage stresses are high in [25]. In addition, it is necessary to point that the proposed converter is obviously superior to the topology in [28] because of the higher voltage gain and lower voltage stresses with the same device number.

Finally, the theoretical efficiencies are compared under the same parameters. For the fair of the comparison, all converters are operated at 280 W with a voltage gain of 14. It can be found that the proposed converter owns the highest efficiency except for [12] in Table III. Although the efficiency in [12] is a little higher than the proposed converter, it suffers a lager input current ripple.

V. EXPERIMENTAL RESULTS

In order to verify the performance of the proposed converter, a 280-W prototype is built and tested in this section. The electrical

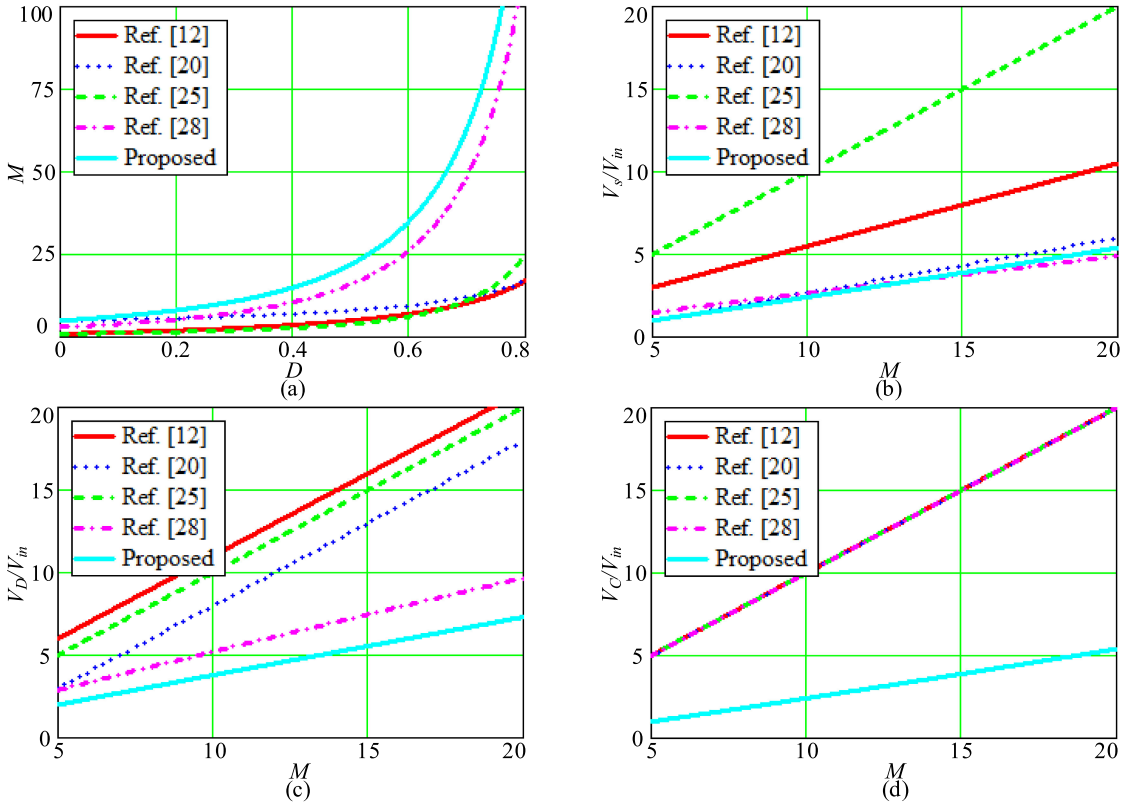

Fig. 8. Performance comparisons of the proposed converter and other high step-up topologies with $n = 2$. (a) Comparison of voltage gains. (b) Comparison of switch voltage stresses. (c) Comparison of diode voltage stresses. (d) Comparison of capacitor voltage stresses.

TABLE IV
PARAMETERS AND DEVICE TYPES OF THE PROTOTYPE

Device	Type	Parameter	Value
S_1	IRFP4110	L_{m1}, L_{m2}	100 μH
S_2	IRFP4668	L_k	1.5 μH
D_1, D_2	STF15100	C_1, C_2	220 μF
D_{o1}- D_{o3}	MBRF40250TG	C_{o1}-C_{o3}	20 μF

specifications are $V_{\text{in}} = 20$ V, $V_o = 280$ V, $D = 0.5$, and $f_s = 50$ kHz. The parameters and device types, listed in Table IV, are chosen based on Tables I and II. The experiment results are presented in Figs. 8–13.

Fig. 9 shows the experimental waveforms of driving signal V_{gs}, voltages V_{S1} over S_1 and V_{S2} over S_2. It can be found that the voltage stresses of S_1 and S_2 are 40 and 120 V, respectively. The switches voltage stresses are reduced effectively, and low power rating switches with small ON-resistance can be employed in the proposed converter.

Figs. 10 and 11 show the experimental waveforms of voltages V_{d1} over D_1, V_{d2} over D_2, V_{do2} over D_{o2}, and V_{do3} over D_{o3}. It can be found that both the voltage stresses of D_1 and D_2 are 40 V. Meanwhile, the voltage stresses of D_{o2} and D_{o3} are 160 V. The experimental results agree well with the theoretical analysis described in Table I.

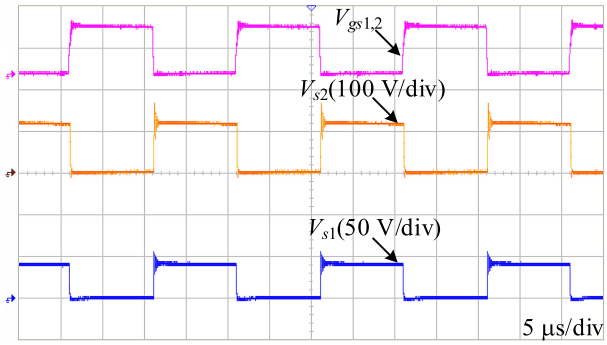

Fig. 9. Experiment waveforms of voltages over switches S_1 and S_2.

Fig. 12 shows the voltage V_{do1} over D_{o1} and the current i_{do1} flowing through D_{o1}. It can be found that the voltage stress of D_{o1} is 160 V, which is the same as V_{do2} and V_{do3}. Thus, the output voltage is shared by D_{o1}, D_{o2}, and D_{o3}. The diode voltage stresses are reduced effectively. i_{do1} will decrease to zero before switches are turned ON, which means ZCS turned-OFF for D_{o1} is achieved. Therefore, the reverse recovery problem of D_{o1} is avoided and the EMI performance of the topology can be improved [29].

Fig. 13 shows the current i_{L1} flowing through L_1 and the current i_{Lk} flowing through L_k. It can be found that the currents increase when switches are turned ON and decrease when

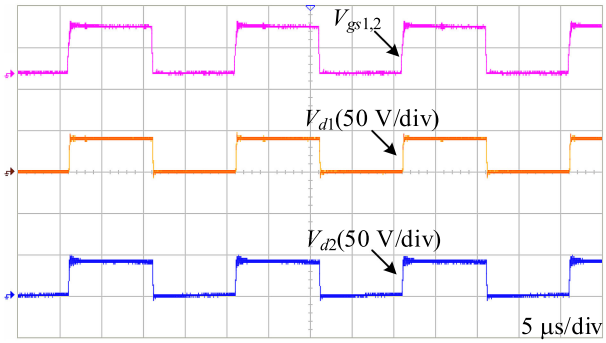

Fig. 10. Experiment waveforms of voltages over diodes D_1 and D_2.

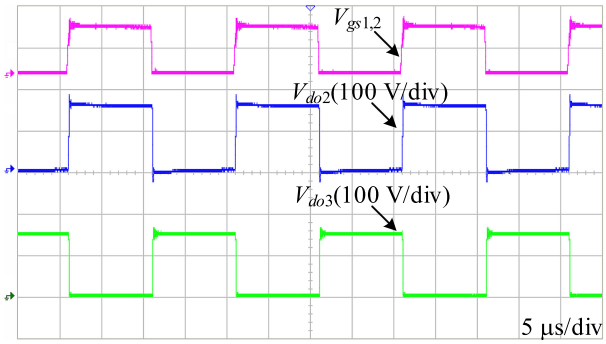

Fig. 11. Experiment waveforms of voltages over diodes D_{o2} and D_{o3}.

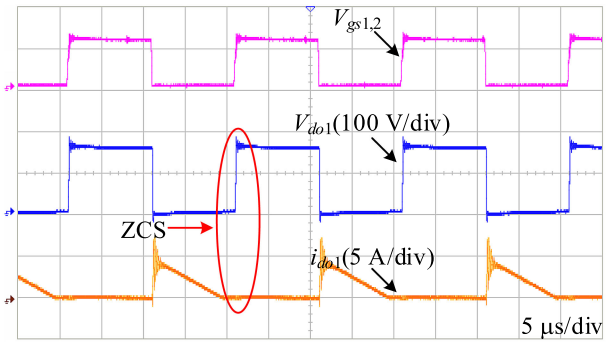

Fig. 12. Experiment waveforms of voltage over D_{o1} and the current flowing through D_{o1}.

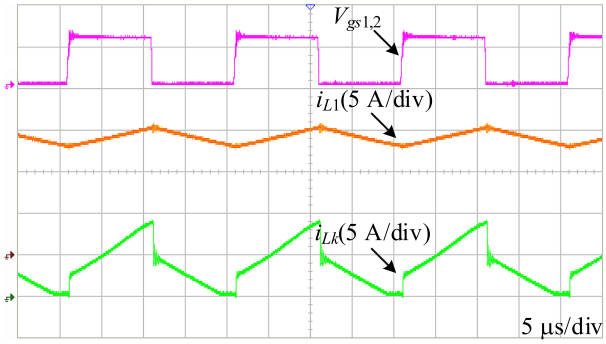

Fig. 13. Experiment waveforms of currents flowing through L_1 and L_k.

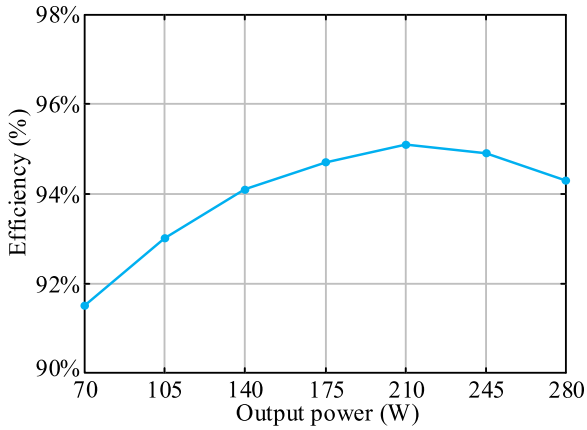

Fig. 14. Experimental efficiency versus output power.

switches are turned OFF. Current i_{L1} is continuous with a low current ripple. The experimental waveforms are consistent with the theoretical analysis shown in Fig. 2.

Fig. 14 shows the experimental efficiency over a wide range of output power. An efficiency of 94.3% is observed at the rating power of 280 W, which is less than the theoretical one in Table III. The difference is acceptable as the line resistance and contact impedance are ignored in the theoretical calculation. In addition, the peak efficiency is achieved at an output power of 210 W.

VI. Conclusion

An ultrahigh step-up converter is proposed in this article, which consists of an improved QBC and a voltage doubler. The two parts are integrated by a CL; thus, a high voltage gain with reduced voltage stresses is achieved. This converter can be applied to the renewable energy generation system due to high voltage gain, low current ripple, and wide input voltage range. The ZCS turn-OFF for the output diode of the QBC is achieved by using a leakage inductor. Meanwhile, the energy stored in the leakage inductor is recycled to the load, thus high efficiency. A 280-W prototype is built to verify the theoretical validity, and the efficiency of 94.3% is achieved at rating power.

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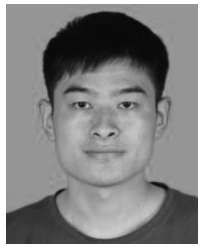

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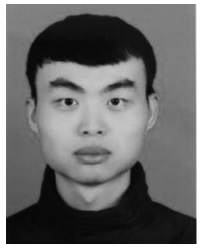

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