A Step-Up Nonisolated Modular Multilevel DC–DC Converter With Self-Voltage Balancing and Soft Switching

Changjiang Sun, *Member, IEEE*, Xin Zhang, *Senior Member, IEEE*, and Xu Cai

***Abstract*—Evolving from the popular modular multilevel ac–dc converter, the single-stage nonisolated modular multilevel dc–dc converter (MMDC) is advantageous for medium- and high-voltage applications. However, exploiting ac circulating power to balance the submodule energy, when utilized for high step ratio applications, existing MMDC topologies suffer from circulating current through the arms and large filter inductor at the low-voltage side. To overcome these issues, this article presents a new power transfer mechanism to balance the submodule energy automatically by reconstructing the half-bridge submodule into a quasi-resonant circuit. Based on this submodule structure, a new MMDC topology for step-up applications is proposed. Compared to the existing MMDCs, the proposed one offers the following advantages. First, the common-mode circulating current through the lower and upper arms is avoided. Second, the self-balancing of the capacitor voltages is guaranteed by the proposed modulation method to insert and bypass adjacent submodules in a complementary manner. Third, the soft-switching operation is achieved for the majority of the switches to alleviate switching losses. Fourth, the voltage stress across the input side inductor is limited to the submodule voltage, thereby reducing the size of the inductor. Simulation analysis and experimental results verify the performance of the proposed MMDC.**

***Index Terms*—Compensating power transfer, modular multilevel dc-dc converter (MMDC), self-voltage balancing, submodule topology.**

I. Introduction

HIGH-VOLTAGE direct current technology is a promising solution for delivering large-scale renewable energy with a long transmission distance because of the reduced power losses and low reactive power requirements [1], [2]. Extending the dc concept to renewable energy collection systems and constructing dc distribution grids can spare extra conversion stages, reduce costs, and improve control flexibility [3]–[5].

Analogous to transformers in the ac power system, high-power dc–dc converters are critical components in the dc grid to match different voltage levels and to interface with energy sources [6], [7]. The conventional low-voltage two-level dc–dc converter topologies, such as boost circuit, cannot be directly scaled up for the grid-scale applications because the series connection of semiconductor switches, such as IGBTs, may result in static and dynamic voltage sharing issues [8].

The emerging modular multilevel converter (MMC) is an attractive topology for medium- and high-voltage ac–dc conversion applications because of its modularity and high reliability [9]–[10]. Connecting ac terminals of two MMCs via a transformer to realize dc–ac–dc conversion, the authors in [11] and [12] have proposed the isolated modular multilevel dc–dc converter topology (IMMDC). Improved operating methods and high-efficiency control strategies of the IMMDC have been developed in [13]–[17]. Although the IMMDC reaps benefits from the MMC topology, two ac–dc conversion stages in the converter lead to high losses. Moreover, the cost and footprint of the coupled transformer rated for the full transmission power are considerable.

Directly reformed from the MMC phase leg, the single-stage nonisolated modular multilevel dc–dc converter (MMDC) proposed in [18] and [19] has the advantages of small volume and weight, low cost, and high efficiency. This kind of converter is a better choice when galvanic isolation is not a strict requirement and the compact design takes top priority. The promising application scenarios are interconnecting dc grid with different voltage levels and harvesting renewable energy sources, such as wind turbines and PV strings into the medium-voltage dc grid [20], [21].

The most critical issue of the MMDC is the energy balance of submodule capacitors because the upper and lower arms absorb different amounts of power from the dc sides. A compensating power transfer loop should be established between the arms to ensure the stability of the submodule voltages. Based on the orthogonality of power flow at different frequencies, the transfer of compensating power is realized via injecting common-mode ac current through the arms in [18] and [19]. By exploiting this mechanism to balance submodule energy, numerous variants

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of MMDC have been developed in the literature [22]–[24]. Although effective, this principle of power transfer suffers from drawbacks when the MMDC is utilized for high step-up ratio application scenarios [25]. First, the injected circulating current flows through the arms, resulting in high conduction and switching losses of the hard-switched devices. Second, large filter inductors are required to prevent the injected ac voltages and currents from propagating to the dc sides. Moreover, submodule voltage and arm current sampling circuits along with the voltage balancing algorithms complicate the control system.

A circulating current optimization strategy for MMDC has been presented in [26] by expending the amplitude of the injected ac voltage in the arms to the maximum extent. The stepped two-level operation method has been proposed in [27] and [28] to increase the voltage utilization ratio and further diminish the circulating current. However, this operation requires larger inductor filters at the low-voltage side to attenuate the ac component current. Instead of injecting harmonic current and voltages, in the resonant MMDC proposed in [29], compensating power transfer in the arms is achieved by rotational resonance between the submodule capacitors and the high-voltage side inductor. Inserting and bypassing the submodules in a rotational manner increases the equivalent switching frequency and realizes natural voltage balancing between the submodules. However, the common-mode resonant current exists in the arms, and a large filter capacitor is required at the high-voltage side to prevent the resonant current from propagating to the dc grid.

This article presents a new step-up MMDC topology with the self-voltage balancing capability for dc grid applications to connect wind turbines with the medium-voltage dc bus. Based on the power transfer mechanism introduced in [30], automatic submodule energy balancing of the MMDC is realized by reconstructing the half-bridge submodule (HBSM) into a quasi-resonant submodule (QRSM). In the QRSM, an *L-D* branch consisting of a diode in series with a small resonant inductor, which can be realized by the stray inductance, is added to link the positive poles of the adjacent submodule capacitors. The *L-D* branch provides the compensating power transfer loops between the submodules in the form of half-wave sinusoid current without reactive component, avoiding the common-mode ac current through the arms. The resonance operation facilitates zero-current-switching (ZCS), and zero-voltage-switching (ZVS) features for the majority of the switches, while the remaining switches only need to switch OFF the dc component current, leading to a significant reduction of switching losses. Distinct from the modulation schemes for MMC, this article presents a new modulation scheme for the proposed MMDC to insert and bypass every two adjacent submodules complementarily. Based on this modulation method, the compensating power is transferred through the arms automatically, and self-balancing of the submodule voltages is achieved. Since the amplitude of the square-wave voltage applied to the low-voltage side inductor is limited to the submodule voltage level, a smaller inductor is enough to suppress the current ripples at the input side when compared with conventional HBSM-based MMDC.

The remainder of this article is organized as follows. Derivation of the QRSM circuit and the proposed MMDC topology are presented in Section II. Based on the operating principles and modulation strategies illustrated in Section III, the design criteria of the new MMDC are explained in Section IV. Section V evaluates the performance of the proposed MMDC. The topology, operating principle, and control strategy of the proposed QRSM-based MMDC are verified by the simulation and experimental results in Sections VI and VII. Finally, Section VIII concludes this article.

II. Proposed QRSM-Based MMDC Topology

The conventional HBSM circuit is reconstructed into a QRSM circuit in this article. Fig. 1(a) depicts the derivation process of the QRSM topology. An *L-D* circuit consisting of a diode and a small resonant inductor $L_{\rm r}$, which can be realized by the stray inductance or an auxiliary air-core inductor if necessary, is added to link the positive poles of the adjacent capacitors. In the obtained QRSM SM_n as shown in Fig. 1(a), C_n, C_{n+1}, and L_r form a resonant loop when $\mathrm{T}_{1,n}$ and $\mathrm{D}_{3,n}$ are conducting. C_n releases charge to C_{n+1} via this loop, thereby enabling an upward power transfer. Since the common-mode alternating current through the lower and upper arms is absent in the proposed MMDC, bidirectional switches are not needed when the converter is utilized for the step-up applications. Therefore, some switching devices from the original HBSM can be omitted, resulting in the upper-arm and lower-arm QRSMs, as shown in Fig. 1(a).

Fig. 1(b) shows the topology of the proposed step-up MMDC with the QRSMs cascaded in a string to withstand the dc voltage. The string is composed of lower and upper arms, where different QRSM circuits are utilized in accordance with Fig. 1(a). A filtering inductor $L_{\rm f}$ is utilized at the low-voltage side to attenuate the current ripples. A small choke is necessary at the high-voltage side to accommodate the switching action and the voltage variation of the capacitors. Although a one-string architecture of MMDC is presented here, a multiphase topology can be easily formed by adding additional strings in parallel to increase the power capacity.

III. Operating Principle of Proposed MMDC

The proposed compensating power transfer mechanism along with the operating principles of QRSM-based MMDC is illustrated in this section. For simplification, the theoretical developments are based on the following assumptions.

1) The converter is lossless.
2) The QRSMs are identical.
3) The capacitor voltages are well balanced in steady-state.
4) The capacitor voltage ripples are negligible compared with the average capacitor voltage.

A. Mathematical Model and Modulation Strategy

According to the QRSM circuit shown in Fig. 1(a), the capacitor of SM_n is inserted when $\mathrm{T}_{2,n}$ or $\mathrm{D}_{2,n}$ conducts current and bypassed when $\mathrm{T}_{1,n}$ or $\mathrm{D}_{1,n}$ conducts current. The instantaneous voltage inserted in the lower and upper arms can be actively controlled by adjusting the number of inserted capacitors. Fig. 2

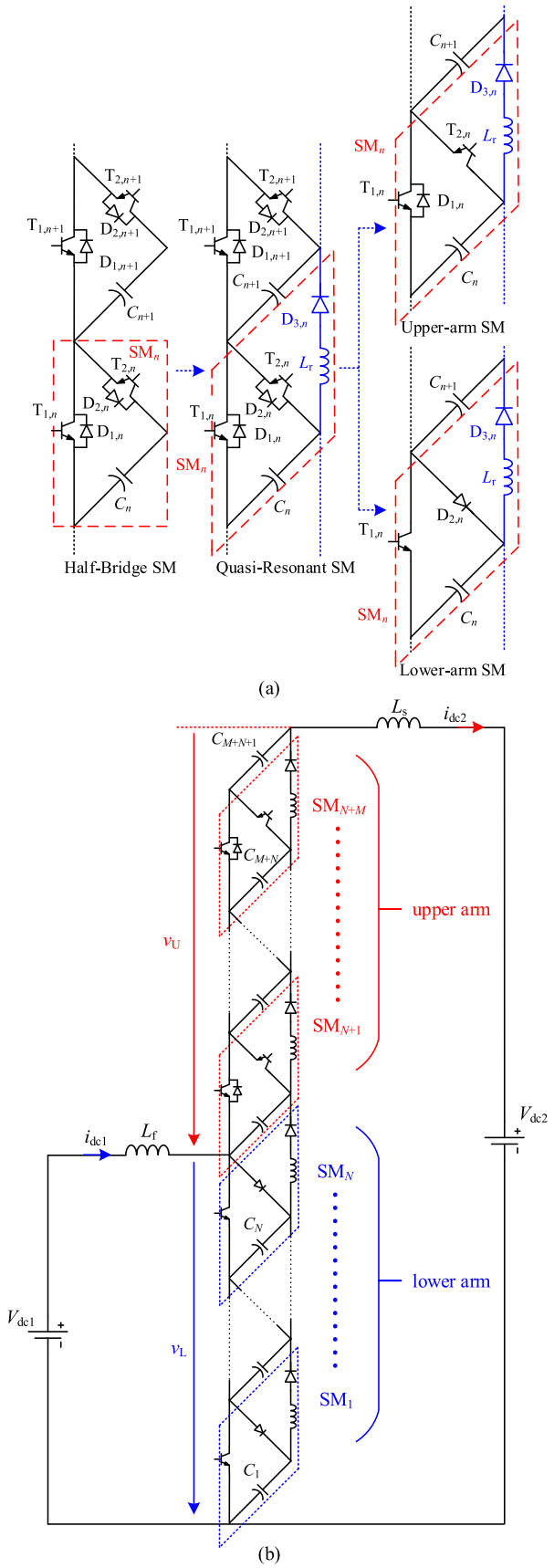

Fig. 1. Submodule derivation and topology of the proposed MMDC. (a) Derivation of the QRSM. (b) Schematic of the converter.

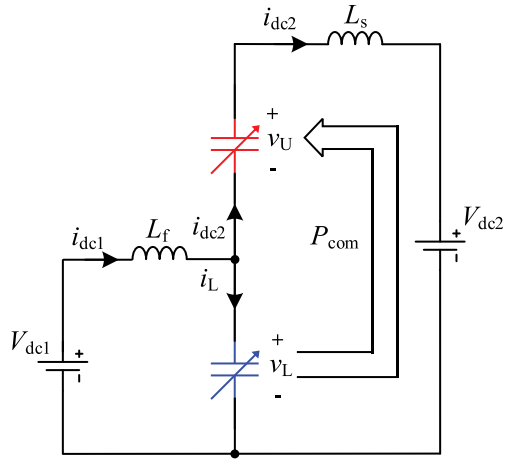

Fig. 2. Equivalent model of the proposed MMDC.

shows the equivalent model of MMDC, with the arms represented by two controllable voltage sources, namely v_{L} and v_{U}. According to Kirchhoff's voltage and current laws, we have

$$\begin{cases} V_{\mathrm{dc1}} = v_{\mathrm{L}} + \frac{L_{\mathrm{f}}\mathrm{d}i_{\mathrm{dc2}}}{\mathrm{d}t} \\ V_{\mathrm{dc2}} = v_{\mathrm{L}} + v_{\mathrm{U}} - \frac{L_{\mathrm{s}}\mathrm{d}i_{\mathrm{dc2}}}{\mathrm{d}t} \\ i_{\mathrm{dc1}} = i_{\mathrm{dc2}} + i_{L}. \end{cases} \tag{1}$$

Based on the volt-second balance principle of the inductor, the low-frequency equation of the converter can be derived as (2), in which V_{L}, V_{U}, I_{dc1}, I_{dc2}, and I_{L} represent the average values of v_{L}, v_{U}, i_{dc1}, i_{dc2}, and i_{L}, respectively

$$\begin{cases} V_{\mathrm{dc1}} = V_{\mathrm{L}} \\ V_{\mathrm{dc2}} = V_{\mathrm{L}} + V_{\mathrm{U}} \\ I_{\mathrm{dc1}} = I_{\mathrm{dc2}} + I_{L}. \end{cases} \tag{2}$$

When neglecting power losses in the converter, the input power is equal to the output power

$$P = V_{\mathrm{dc1}} I_{\mathrm{dc1}} = V_{\mathrm{dc2}} I_{\mathrm{dc2}}. \tag{3}$$

Substituting (2) into (3) leads to

$$V_{\mathrm{L}} I_{\mathrm{L}} = V_{\mathrm{U}} I_{\mathrm{dc2}}. \tag{4}$$

The left-hand side of (4) represents the absorbed dc power in the lower arm, and the right-hand side expresses the released power of the upper arm. Equation (4) reveals that an additional power transfer loop should be established between the arms to maintain the stability of the energy storage in the arms. For the step-up MMDC with power flowing from the low-voltage side to the high-voltage side, the amount of compensating power (i.e., P_{com}) that needs to be transferred from the lower arm to the upper arm can be calculated as (5), in which k is the conversion ratio (i.e., $k = V_{\mathrm{dc2}}/V_{\mathrm{dc1}}$)

$$P_{\mathrm{com}} = V_{\mathrm{U}} I_{\mathrm{dc2}} = \frac{(V_{\mathrm{dc2}} - V_{\mathrm{dc1}})\, P}{V_{\mathrm{dc2}}} = P(1 - 1/k). \tag{5}$$

In order to maintain the dc-side voltage, the conventional MMDCs are usually modulated in the inter-arm complementary

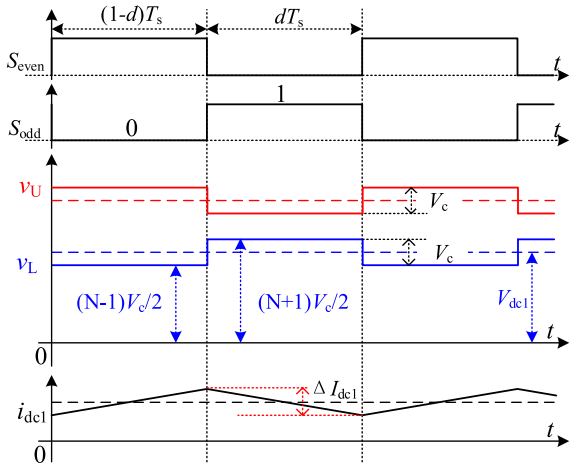

Fig. 3. Modulation signals and key waveforms of the proposed MMDC.

manner, i.e., a submodule in the lower arm is inserted (or bypassed) when a submodule in the upper arm is bypassed (or inserted). Unlike this, the proposed MMDC is modulated in an inter-submodule complementary manner, every two adjacent submodules are inserted alternately, i.e., the switching signals of the even-numbered QRSMs and odd-numbered QRSMs are complementary.

Fig. 3 shows the switching signals and key waveforms of the proposed MMDC. With 1 and 0 presenting insertion and bypass states, respectively, $S_{\rm even}$ and $S_{\rm odd}$ are the switching signals for the even-numbered QRSMs and odd-numbered QRSMs, respectively. $V_{\rm c}$ represents the average capacitor voltage. M and N are the numbers of submodules in the upper and lower arms. The inserted voltage in the lower arm (i.e., $v_{\rm L}$) switches between $(N\text{-}1)V_{\rm c}/2$ and $(N\text{+}1)V_{\rm c}/2$, and the inserted voltage in the upper arm (i.e., $v_{\rm U}$) switches between $(M\text{+}3)V_{\rm c}/2$ and $(M\text{+}1)V_{\rm c}/2$.

In Fig. 3, $v_{\rm L}$ and $v_{\rm U}$ are square-wave voltages with a dc bias, and their ac components are complementary. Given that the average voltage of $L_{\rm s}$ is zero, the high-side dc voltage can be obtained as

$$V_{\rm dc2} = v_{\rm L} + v_{\rm U} = \frac{(N+M+2)V_{\rm c}}{2}. \tag{6}$$

Equation (6) reveals that the total number of inserted submodules is well maintained, ensuring the stability of $V_{\rm dc2}$. Therefore, a relatively small high-voltage side inductor is sufficient to limit the current ripples caused by the switching actions and the voltage variation of the capacitors.

The low-side voltage $V_{\rm dc1}$ is equal to the average of $v_{\rm L}$ over one switching cycle. With d representing duty ratio of switching signals for the odd-numbered submodules we have

$$V_{\rm dc1} = V_{\rm L} = \frac{(N-1)V_{\rm c}}{2} + dV_{\rm c}. \tag{7}$$

According to (7), adjusting d can achieve the dynamic control of the low-side voltage or current. Besides, since the amplitude of the ac component in $v_{\rm L}$ is limited to submodule voltage $V_{\rm c}$, the input filter demand will be significantly reduced when compared with the conventional MMDC operation that generating large ac component in $v_{\rm L}$.

B. Power Transfer and Capacitor Voltage Balancing Process

The mathematical analysis of the MMDC indicates that an additional power transfer loop from bottom to the top of the submodule string should be established to maintain the voltage stability of the capacitors. QRSM topology, together with the proposed modulation strategy in this study, yields automatic power transfer between adjacent submodules and realizes the self-balancing of the capacitor voltages.

One important feature of the QRSM is that when a submodule is bypassed, its buffering capacitor will release charge to the upper-side capacitor through the *L-D* branch that links them. The key idea of the self-voltage balancing mechanism in this article is bypassing the odd-numbered and even-numbered submodules alternately to transfer the demanded compensating power from bottom to the top automatically. This section illustrates the power transfer process between the submodules and the self-balancing mechanism of the capacitor voltages by focusing on the typical submodule $\rm SM_{\it n}$ in the upper arm.

Fig. 4 shows the switching states of submodules $\rm SM_{\it n}$ and $\rm SM_{\it n-1}$, and Fig. 5 shows the corresponding switching signals and the voltage and current waveforms. To insert and bypass every two adjacent submodules in a complementary manner, switches $\rm T_{1,\it n-1}$, and $\rm T_{2,\it n}$ have the identical switching signals, and the switching signals of $\rm T_{1,\it n}$, and $\rm T_{2,\it n-1}$ are complementary to those of $\rm T_{2,\it n}$ and $\rm T_{1,\it n-1}$, respectively, when neglecting the deadtime interval. The operation states of $\rm SM_{\it n}$ and $\rm SM_{\it n-1}$ in one switching period are illustrated as follows.

1) State 1 [t_0, t_1], Fig. 4(a). With $\rm T_{2,\it n}$ turned ON and $\rm T_{2,\it n-1}$ turned OFF at t_0, the dc current $i_{\rm dc2}$ commutates from $\rm T_{2,\it n-1}$ to $\rm D_{1,\it n-1}$, resulting in the insertion of C_n and bypass of C_{n-1}. $\rm D_{3,\it n-1}$ is forward biased since the voltage of C_{n-1} $(v_{{\rm c},n-1})$ is larger than the voltage of C_n $(v_{{\rm c},n})$. Under this condition, C_{n-1}, C_n, and $L_{\rm r}$ form a resonant tank with the resonant current $i_{D3,n-1}$ gradually increasing from zero in a sinusoidal manner. Meanwhile, $v_{{\rm c},n-1}$ begins to decrease from its maximum value. Before $i_{D3,n-1}$ exceeds $i_{\rm dc2}$, $\rm D_{1,\it n-1}$ keeps conducting, and the voltage of $\rm T_{1,\it n-1}$ is clamped to zero. Therefore, zero-voltage turn-ON of $\rm T_{1,\it n-1}$ can be realized after a small deadtime delay.
2) State 2 [t_1, t_2], Fig. 4(b). $\rm T_{1,\it n-1}$ begins to conduct current with zero voltage when the resonant current $i_{D3,n-1}$ exceeds $i_{\rm dc2}$ at t_1. $i_{D3,n-1}$ keeps increasing and reaches the peak value when $v_{{\rm c},n}$ equals $v_{{\rm c},n-1}$. Thereafter, $v_{{\rm c},n-1} < v_{{\rm c},n}$ and $i_{D3,n-1}$ begins to decrease.
3) State 3 [t_2, t_3], Fig. 4(a). With the resonant current $i_{D3,n-1}$ decreasing below the dc current $i_{\rm dc2}$ at t_2, $\rm T_{1,\it n-1}$ is turned OFF naturally with zero current, and $\rm D_{1,\it n-1}$ begins to conduct current again. The conduction states of the switches return to that in Fig. 4 (a).
4) State 4 [t_3, t_4], Fig. 4(c). After C_{n-1}, C_n, and $L_{\rm r}$ resonate for half of the resonant cycle, the resonant current $i_{D3,n-1}$ falls back to zero, and $v_{\rm c}$ reaches the maximum value at t_3.

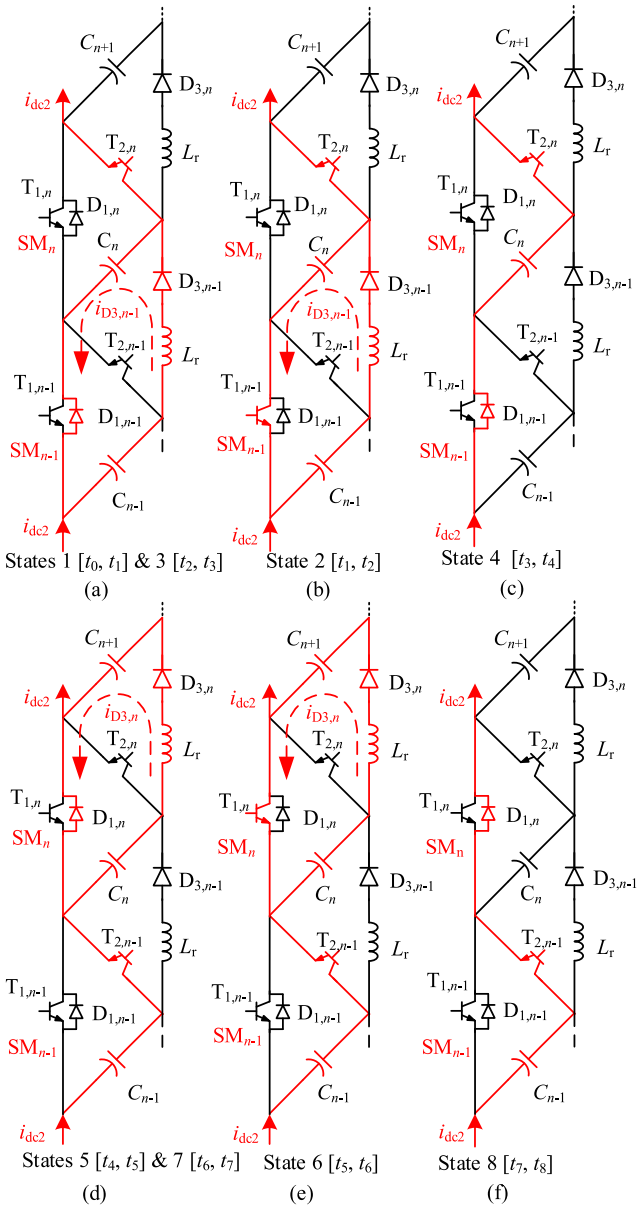

Fig. 4. Operation states of SM_n and SM_{n-1}. (a) States 1 and 3. (b) State 2. (c) State 4. (d) States 5 and 7. (e) State 6. (f) State 8.

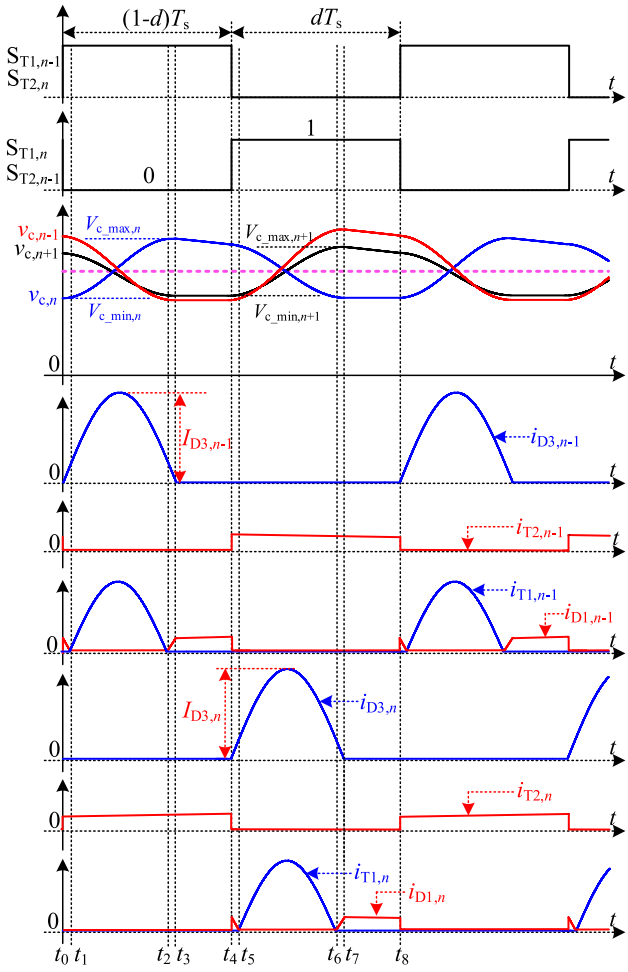

Fig. 5. Typical steady-state waveforms of SM_n and SM_{n-1}.

$D_{3,n-1}$ is reversely biased since $v_{c,n}$ is higher than $v_{c,n-1}$. Zero-current turn-OFF of $D_{3,n-1}$ is achieved during this process, avoiding the reverse-recovery losses.

5) States 5–8 [t_4, t_8], Fig. 4 (d)–(f). During the subsequent half of the switching cycle, C_n, C_{n+1}, and L_r form a resonant tank with $T_{2,n-1}$ turned ON and $T_{2,n}$ turned OFF at t_4. Similar to the charge transfer process from C_{n-1} to C_n during operation states 1–4, C_n releases charge to C_{n+1} during operation states 5–8. Similar to the soft-switching operation of $T_{1,n-1}$ and $D_{1,n-1}$, zero-voltage turn-ON and zero-current turn-OFF are realized for $T_{1,n}$, and zero-current turn-OFF is achieved for $D_{1,n}$.

By combining the previously presented eight operation states, the charging and discharging processes of capacitors in the typical QRSM are summarized as follows. When SM_n is inserted during the interval [t_0, t_3], its capacitor C_n absorbs charge from the lower-side submodule SM_{n-1} via the resonant tank composed of C_{n-1}, C_n, and L_r, meanwhile the dc current discharges it. During the interval [t_3, t_4], with the resonant current clamped at zero, the dc current discharges SM_n. When SM_n is bypassed during the interval [t_4, t_7], it releases charge to the upper submodule SM_{n+1} via the resonant tank composed of C_n, C_{n+1}, and L_r. During interval [t_7, t_8], with the resonant current staying at zero, the capacitor voltage of SM_n remains constant. The above processes realize the relay transmission of compensating power from the bottom to the top of the submodule string.

According to the conservation of charge, the total charge that SM_n absorbs from SM_{n-1} is equal to the total charge that released to SM_{n+1} plus the loss of charge caused by the dc current. The energy variation of the capacitor in SM_n in one switching cycle is zero, ensuring the natural stability of the submodule capacitor voltage. When focusing on the voltage ripples, the capacitor voltage of SM_n reaches its maximum value at t_3 (i.e., $V_{c,\max,n} = v_{c,n}(t_3)$), and reaches to the minimum value at t_0, t_7, and t_8 (i.e., $V_{c,\min,n} = v_{c,n}(t_7) = v_{c,n}(t_8) = v_{c,n}(t_0)$).

Extending the previously presented power transfer principle to an arbitrary QRSM, we can conclude that the submodule absorbs power from the lower-side submodule when it is inserted

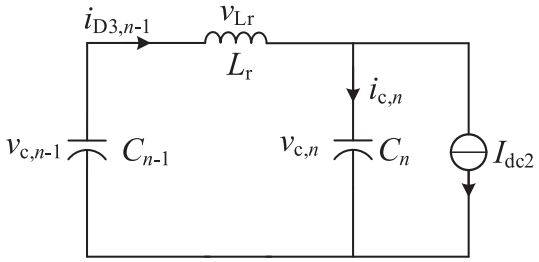

Fig. 6. Resonant circuit formed between SM_n and SM_{n-1}.

and releases power to the upper-side submodule when it is bypassed both via the resonant tank. Therefore, the compensating power can be transferred from bottom to top of the entire string by inserting and bypassing the even-numbered and odd-numbered submodules alternately. Charge transfer between the top submodule in the lower arm (i.e., SM_N in Fig. 1) and the bottom submodule in the upper arm (i.e., SM_{N+1} in Fig. 1) realizes power transfer between the arms. To maintain stable operation, P_{com}, which is calculated by (6) should be transferred from SM_N to SM_{N+1} via the resonant tank consisting of C_N, C_{N+1}, and L_r.

C. Analysis of Oscillation Amplitude and Capacitor Voltage Ripples

Resonance occurs during the charging and discharging process of each submodule capacitor to transfer the required compensating power from bottom to top of the string. The oscillation amplitudes of capacitor voltage and resonant current are related to the circuit parameters and transferred power of the converter.

For the typical adjacent submodules SM_n and SM_{n-1} in the upper arm, C_n, C_{n-1}, and L_r form a resonant tank during the interval [t_0, t_3] according to Figs. 4 and 5. By neglecting the resistive losses and ripples in the dc current through the arm, the equivalent model of the resonant circuit is derived as in Fig. 6 with I_{dc2} representing the average of i_{dc2}.

By taking the inductor and capacitor voltages as state variables, equations of the formed resonant circuit are expressed as in (8) with C representing the capacitance of the capacitors, in which $v_{c,n-1}(t_0)$ and $v_{c,n}(t_0)$ are the capacitor voltages at the initial time t_0

$$\begin{cases} v_{Lr} = L_r \frac{di_{D3,n-1}}{dt} \\ v_{c,n-1} = v_{c,n-1}(t_0) - \frac{1}{C}\int_{t_0}^{t} i_{D3,n-1} dt \\ v_{c,n} = v_{c,n}(t_0) + \frac{1}{C}\int_{t_0}^{t} (i_{D3,n-1} - I_{dc2}) dt. \end{cases} \tag{8}$$

According to the Kirchhoff's voltage law, the relationship between the voltages in Fig. 6 is

$$v_{c,n-1} = v_{Ls} + v_{c,n}. \tag{9}$$

By substituting (8) into (9), the resonant current in the *L-D* branch can be derived as in (10), where $\omega_r = \sqrt{2/L_r C}$, representing the resonant angular frequency

$$i_{D3,n-1} = \frac{I_{dc2}(1-\cos\omega_r(t-t_0))}{2} + \frac{[v_{c,n-1}(t_0) - v_{c,n}(t_0)]\sin\omega_r(t-t_0)}{\omega_r L_r}. \tag{10}$$

Given that the dc current I_{dc2} is far less than the oscillation amplitude, (10) can be simplified by neglecting the first item at the right-hand side. Therefore

$$i_{D3,n-1} \approx \frac{[v_{c,n-1}(t_0) - v_{c,n}(t_0)]\sin\omega_r(t-t_0)}{\omega_r L_r}. \tag{11}$$

By substituting (11) into (8), the capacitor voltages can be derived as

$$\begin{cases} v_{c,n-1} = v_{c,n-1}(t_0) - \frac{(v_{c,n-1}(t_0) - v_{c,n}(t_0))(1-\cos\omega_r(t-t_0))}{2} \\ v_{c,n} = v_{c,n}(t_0) + \frac{(v_{c,n-1}(t_0) - v_{c,n}(t_0))(1-\cos\omega_r(t-t_0))}{2}. \end{cases} \tag{12}$$

According to (12), after half of a resonant cycle, the capacitor voltages at time t_3 are calculated as in (13)

$$\begin{cases} v_{c,n-1}(t_3) = v_{c,n-1}(t_0) - [v_{c,n-1}(t_0) - v_{c,n}(t_0)] = v_{c,n}(t_0) \\ v_{c,n}(t_3) = v_{c,n}(t_0) + [v_{c,n-1}(t_0) - v_{c,n}(t_0)] = v_{c,n-1}(t_0). \end{cases} \tag{13}$$

Equation (13) reveals that capacitors C_n and C_{n-1} exchange their voltages during [t_0, t_3]. $v_{c,n}$ varies from its minimum value to the maximum value during this interval. Therefore, the peak-to-peak ripple of capacitor voltage $v_{c,n}$ can be derived as

$$\Delta V_n = v_{c,n-1}(t_0) - v_{c,n-1}(t_3) = v_{c,n}(t_3) - v_{c,n}(t_0). \tag{14}$$

During interval [t_4, t_7], SM_n releases charge to SM_{n+1}, and a resonant circuit similar to that shown in Fig. 6 is formed between them. By referring to the derivation process of (13) and (14), the peak-to-peak ripple of capacitor voltage $v_{c,n+1}$ in SM_{n+1} is derived as

$$\Delta V_{n+1} = v_{c,n+1}(t_7) - v_{c,n+1}(t_4) = v_{c,n}(t_4) - v_{c,n}(t_7). \tag{15}$$

Since the dc current i_{dc2} discharges C_n during interval [t_3, t_4], $v_{c,n}(t_4)$ is less than $v_{c,n}(t_3)$. Meanwhile, $v_{c,n}(t_7)$ is equal to $v_{c,n}(t_0)$ according charge conservation. Therefore, comparing (14) and (15), one has

$$\Delta V_{n+1} < \Delta V_n. \tag{16}$$

The capacitor voltage ripple of the upper submodule SM_{n+1} is smaller than that of SM_n. Equation (16) reveals that the capacitor voltage ripples decrease gradually from bottom to top of the upper arm, and the capacitor voltage ripple of the bottom submodule is the largest in the upper arm.

The capacitor voltage ripples in the lower arm can be calculated in the same way by analyzing the resonant circuits formed between every two submodules. By referring to the derivation of (16), we have $\Delta V_{n+1} > \Delta V_n$ for the lower arm where the dc current charges the inserted submodules constantly. This finding indicates that capacitor voltage ripples decrease gradually from top to bottom of the lower arm, i.e., the capacitor voltage ripple of the top submodule is the largest in the lower arm. Therefore, the capacitor voltage ripples in the proposed MMDC decreases gradually from the midpoint to the top and bottom of the submodule string, and the natural stability of the capacitor voltages is achieved without additional control.

IV. Design of Proposed MMDC

A. Submodule Capacitor Design

As shown in Fig. 5, the capacitor voltage ripples exhibit trapezoid-like shapes, and the intermediate values of the capacitor voltages approximate the average voltage, namely $V_{\rm c}$. Therefore, the maximum and minimum capacitor voltages of SM_n can be derived as

$$V_{\rm c\_max,}n = V_{\rm c} - \frac{\Delta V_n}{2},\ \text{and}\ V_{\rm c\_min,}n = V_{\rm c} - \frac{\Delta V_n}{2}. \quad (17)$$

Then the maximum energy fluctuation of SM_n which occurs during the interval $[t_0, t_3]$ can be expressed as

$$\Delta E_n = \frac{C}{2}\left(V_{\rm c} + \frac{\Delta V_n}{2}\right)^2 - \frac{C}{2}\left(V_{\rm c} - \frac{\Delta V_n}{2}\right)^2 = C\Delta V_n V_{\rm c}. \quad (18)$$

$\Delta E_{\rm n}$ also represents the amount of energy SM_n absorbs from the subjacent submodule SM_{n-1} when neglecting the discharging effect of the dc current during the interval $[t_0, t_3]$. According to the power transfer demand between the arms of the MMDC, the bottom submodule in the upper arm needs to absorb the compensating power of $P_{\rm com}$ from the lower arm. It exhibits the maximum energy fluctuation and voltage ripple. By combining (5) and (18), we have

$$P(1-1/k) = f_{\rm s}\Delta E_{\max} = f_{\rm s}C\Delta V_{\max}V_{\rm c}. \quad (19)$$

With $\varepsilon_{\rm v}$ representing the voltage fluctuation coefficient, the capacitance requirement for the QRSMs can be calculated as

$$C \geq \frac{P(1-1/k)}{\varepsilon_{\rm v} f_{\rm s} V_{\rm c}^2}. \quad (20)$$

B. Resonant Inductor (L_r) Design

The function of $L_{\rm r}$ is to limit the oscillation amplitude of the resonant current. According to (11), the linking inductor between the bottom capacitor in the upper arm and the top capacitor in the lower arm has the largest resonant current. The oscillation amplitude is

$$I_{\rm D3,max} \approx \frac{\Delta V_{\max}}{\omega_{\rm r} L_{\rm r}}. \quad (21)$$

By substituting $\Delta V_{\max} = \varepsilon_{\rm v} V_{\rm c}$ and $\omega_{\rm r} = \sqrt{2/L_{\rm r}C}$ into (21), and combining with (19), one has

$$L_{\rm r} \approx \frac{\varepsilon_{\rm v} P(1-1/k)}{2 f_{\rm s} I_{\rm D3,max}^2} \quad (22)$$

in which $I_{\rm D3,max}$ reflects current stress of the switch devices.

C. Input Filter (L_f) Design

According to the proposed modulation scheme to switch the adjacent submodules in a complementary manner, ripples of the input current shown in Fig. 3 can be expressed as

$$\Delta I_{\rm dc1} = \varepsilon_i I_{\rm dc1} = \left(\frac{(N+1)V_{\rm c}}{2} - V_{\rm dc1}\right)\frac{DT_{\rm s}}{L_{\rm f}} \quad (23)$$

where $\varepsilon_{\rm i}$ is the current ripple ratio, $I_{\rm dc1}$ is the rated input current, and D is the steady-state operating point of d. The $L_{\rm f}$ requirement can be solved by substituting (7) into (23)

$$L_{\rm f} \geq \frac{D(1-D)V_{\rm c}}{\varepsilon_i f_{\rm s} I_{\rm dc1}}. \quad (24)$$

D. Output Choke (L_s) Design

Given that capacitors with fluctuating voltages are switched in and out of the power circuit alternately, the variation of capacitor voltages, as well as the switching process, inevitably introduces voltage ripples at the output stage. The function of the output choke $L_{\rm s}$ is to eliminate the current ripples caused by the capacitor voltage fluctuation and switching actions.

Every two adjacent submodules are switched in and out in a complementary manner. If the even-numbered and odd-numbered submodules are at their maximum and minimum capacitor voltages, respectively, then the switching process to bypass the even-numbered submodules and insert the odd-numbered submodules causes the largest output voltage change. For simplification, the introduced output voltage ripple is regarded as a square wave, and the maximum capacitor voltage ripple $\Delta V_{\max}$ is utilized to represent the average ripple of submodules in the entire string. According to Fig. 3, the number of submodules inserted into the string is $(2+M+N)/2$ at any time. The amplitude of the square-wave voltage ripple at the output stage can then be calculated as $(2+M+N)\Delta V_{\max}/2$. By referring to the derivation process of (23), the output current ripple caused by the fluctuation of capacitor voltages can be estimated as in (25) with D and $I_{\rm dc2}$ representing the steady-state value of d and $i_{\rm dc2}$, respectively

$$\Delta I_{\rm dc2} = \varepsilon_i I_{\rm dc2} = \frac{\Delta V_{\max}(2+M+N)D(1-D)}{2 f_{\rm s} L_{\rm s}}. \quad (25)$$

Therefore, the inductance requirement of $L_{\rm s}$ can be calculated as

$$L_{\rm s} \geq \frac{\varepsilon_v V_{\rm c}(2+M+N)D(1-D)}{2\varepsilon_i f_{\rm s} I_{\rm dc2}}. \quad (26)$$

E. Selection of Duty Ratio and Switching Frequency (f_s)

Equations (20), (22), (24), and (26) indicate that increasing the switching frequency $f_{\rm s}$ can reduce the size and volume of passive components. However, the switching frequency $f_{\rm s}$ is also restricted by the resonant frequency of the QRSMs to ensure normal operation. By referring to Fig. 5, both the widths of intervals $[t_3,\ t_4]$ and $[t_4,\ t_8]$ should be no less than half of the resonant cycle to make sure that the resonant currents return to zero during every half switching cycle. Therefore, the frequency $f_{\rm s}$ should satisfy the constraint described in (27) with D representing the duty ratio (i.e., d) at the designed operating point in steady state and $f_{\rm r}$ representing the resonant frequency determined by the previously designed C and $L_{\rm r}$

$$\begin{cases} f_{\rm s} \leq 2Df_{\rm r} & \text{for } D \leq \frac{1}{2} \\ f_{\rm s} \leq 2\,(1-D)\,f_{\rm r} & \text{for } D \geq \frac{1}{2} \end{cases}. \quad (27)$$

Equation (27) reveals that $f_{\rm s}$ achieves the maximum value (i.e., $f_{\rm r}$) when D is designed as 0.5. A larger $f_{\rm s}$ will be allowed if D is designed closer to 0.5. Therefore, in practical applications,

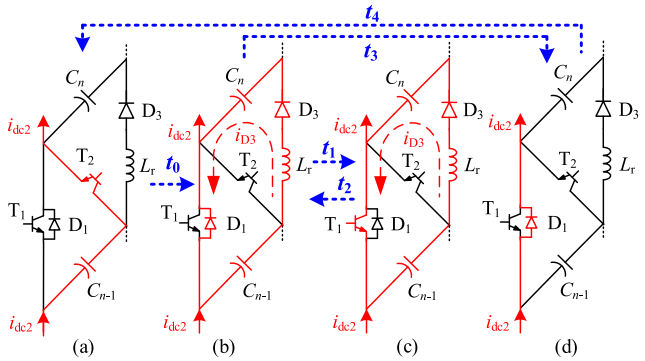

Fig. 7. Switching states of the typical submodule in the upper arm. (a) Before t_0. (b) During intervals $[t_0, t_1]$ and $[t_2, t_3]$. (c) During intervals $[t_1, t_2]$. (d) During intervals $[t_3, t_4]$.

D is suggested to be designed as 0.5. Meanwhile, f_s should be designed slightly lower than f_r to provide a sufficient dynamic variation range for the duty ratio.

F. Selection of the Number of Submodules (M and N)

By solving V_c in (19) and substituting the results into (21), the amplitude of the resonant current can be obtained as

$$I_{D3,max} \approx \frac{P(1-1/k)}{f_s C \Delta\omega_r L_r V_c}. \tag{28}$$

The resonant amplitude $I_{D3,max}$ in (28) is inversely proportional to the average submodule voltage V_c. Therefore, V_c should be designed as larger as possible to limit $I_{D3,max}$, thus achieving lower current stress and lower condition losses of the high power switches.

By substituting the designed value of D discussed in the previous subsection (i.e., $D = 0.5$) into (7), V_c can be calculated as

$$V_c = \frac{2V_{dc1}}{N}. \tag{29}$$

Based on (29), design a small N will result in a large V_c and help to reduce the resonant current amplitude. Ideally, selecting N as one achieves the optimal design. In practice, the design constraint upon N is the voltage level of the semiconductor devices, i.e., N should be selected based on (29) to limit V_c at an acceptable level for the power switches. After N is selected, M can be obtained via (6) with a given output voltage V_{dc2}.

V. Performance Analysis and Comparison

A. Soft-Switching Property

From the inter-submodule power transfer process described in Section III, switching states of a typical submodule SM_{n-1} in the upper arm can be summarized as shown in Fig. 7. The submodule stays inserted with the dc current flowing through T_2 [see Fig. 7(a)]. Turning OFF T_2 to bypass C_{n-1} at t_0 results in i_{dc2} commutating to D_1 [see Fig. 7(b)]. T_2 is gated OFF with a low current during this process since the amplitude of the dc current is relatively small. The resonant current i_{D3} begins to increase at t_0 and equals i_{dc2} at t_1. Turning ON T_1 during the interval $[t_0, t_1]$ can achieve the zero-voltage switching with its antiparallel diode conducting current. When i_{D3} exceeds i_{dc2}, T_1 starts to conduct current [see Fig. 7(c)]. The resonant current starts to decrease after reaching the peak value, resulting in the falling of current in T_1. When i_{D3} falls back equal to i_{dc2} at t_2, T_1 is naturally turned OFF with zero current, and the switching state returns to Fig. 7(b). When i_{D3} falls back to zero, D_3 is naturally turned OFF with zero current, preventing the reverse recovery problems [see Fig. 7(d)]. Turning ON T_2 will insert C_{n-1}, indicating the start of the subsequent switching period.

The above analysis shows that soft-switching operation is achieved for the majority of the switches in the upper-arm submodules, while the other switches are switched at low current. Zero-voltage and ZCS are achieved on T_1, ZCS is achieved on D_3, and low-current switching is achieved for D_1 and T_2. Analyzing the switching process in the lower-arm submodules in the same manner, we can find that D_3 is switched at zero current while T_1 and D_2 are switched at low current.

TABLE I
Comparison Results Between Proposed and Existing MMDCs

Items	MMDC in [27][28]	MMDC in [29]	Proposed MMDC
Output current i_{dc2}	AC	AC	DC
With circulating current or Not	YES	YES	NO
Total number of SMs	$2V_{dc2}/V_c$	V_{dc2}/V_c+1	$2V_{dc2}/V_c$-2
With soft-switching or Not	NO	Partly	YES
Switching losses	Large	Large	Small
Demand for voltage balancing control	Essential	Essential in Practice	Not Necessary

B. Performance Comparison

The performance of the proposed converter is compared with the conventional HBSM-based MMDC topology that operated under the stepped two-level method [27], [28] and the resonant MMDC presented in [29]. The comparison results are provided as in Table I. The main distinction among the three MMDC topologies is how the compensating power is transferred between the lower and upper arms. This affects the current waveforms, submodule structure, filter size, and current stress and losses of the semiconductor switches.

In the conventional HBSM-based MMDC, the power balance is realized by injecting ac voltages and common-mode harmonic current in the arms. The amplitude of injected circulating current should exceed that of dc current in the arms to ensure the conservation of the capacitor charge. Under this condition, the output current i_{dc2} is alternating current. Also, two-quadrant HBSMs with two IGBTs and two diodes should be used to provide loops for the reversed currents even when the converter is utilized for unidirectional applications.

The common-mode current flowing the arms increases the current stress and introduces significant switching losses in the

HBSM-based MMDC since the switches are turned ON and OFF with large currents. The stepped two-level operation presented in [27] and [28] can effectively reduce the circulating current by generating quasi-square wave voltages in the arms and increase the dc-voltage utilization ratio to the maximum extent. However, this scheme needs a large number of submodules in the arms. The total number of submodules utilized in the one-string MMDC is $2V_{\rm dc2}/V_{\rm c,}$ with the lower and upper arms are designed to handle the high-side voltage $V_{\rm dc2}$ alternately. Also, a large-side filter inductor is needed because a square-wave voltage with the amplitude of $V_{\rm dc2}$ is generated across the lower arm. Referring to the derivation process of (24). The required input filter inductance can be calculated as

$$L_{\rm f} \geq \frac{D(1-D)V_{\rm dc2}}{\varepsilon_i f_{\rm s} I_{\rm dc1}} = \frac{D(1-D)KV_{\rm c}}{\varepsilon_i f_{\rm s} I_{\rm dc1}} \tag{30}$$

in which K represents the number of submodules in one arm.

By comparing (30) with (24), it can be found that the requirement of input filter inductance in the proposed MMDC is $1/K$ of that in the MMDC in [28].

In the resonant MMDC presented in [29], the compensating power is transferred via the rotational resonance between the submodule capacitors and the high-voltage side inductor. Inserting and bypassing the submodules in a rotational manner decreases the actual switching frequency. However, the introduced resonant current is considerable large and flows through all the submodules and the output dc side, introducing large condition losses and large current ripple at the output side. The zero-voltage switching operation of IGBTs in the upper arm of the resonant MMDC is realized with the help of resonance; however, the clamped IGBTs in the lower arm need to switch OFF the resonant current, which is considerably large. By employing the rotational modulation manner, the number of submodules the resonant MMDC can be minimized as $(V_{\rm dc2}/V_{\rm c}+1)$ with different numbers of submodules installed at the lower and upper arms.

Similar to the proposed QRSM-based MMDC, the filter requirement at the input side of the resonant MMDC can be calculated as in (24), with the amplitude of the generated square-wave voltage reduced to the submodule level under the rotational modulation mode.

In the proposed QRSM-based MMDC, the compensating power is transferred via resistance between the adjacent submodules. By utilizing half-wave resonant current to transfer the compensating power, the alternating current through the arms and the dc side is avoided. Also, a certain number of switches from the original HBSMs can be omitted because the reverse current no longer exists when the converter is utilized for step-up applications. Soft-switching operations are realized for the majority of IGBTs and diodes, with the remaining switches gated OFF at low current. By alternately inserting and bypassing the adjacent submodules, the input-side filter size is significantly reduced, as shown in (24). According to (6), the total number of submodules required in the proposed converter is $(2V_{\rm dc2}/V_{\rm c}$-2).

It should be emphasized that the capacitor voltages are automatically balanced in the proposed MMDC with power balancing loop established among the adjacent submodules, the complex capacitor voltage sampling, and closed-loop balancing control are avoided. Under ideal conductions, the submodule voltages in the resonant MMDC can realize natural balance; however, without any power-sharing loop, the capacitor voltages may deviate due to the unbalanced losses of capacitors and switches. Therefore, voltage balancing control is still required in practice.

Based on the previously presented analysis, the comparison results are listed in Table I.

VI. Simulation Study

According to the modulation scheme illustrated in Section II, the control variable of the QRSM-based MMDC is the inserting duty ratio of odd-numbered submodules. Like the Boost converter, when the converter is utilized to connect two voltage sources, the input current can be controlled by adjusting d to track the reference signal via a PI controller.

In this article, the conventional HBSM-based, the QRSM-based, and the resonant MMDCs have been designed for a practical MVDC application to connect the rectified wind power with the collection dc bus. Simulation studies of these converters have been conducted in PLECS to verify the proposed topology and operating principles and conduct performance comparison. In the simulation models, to emulate the practical medium-voltage wind energy collection application, the input and output voltage of the MMDC are 1 and 6 kV, respectively. The rated power is 200 kW. ABB Hi-Pak IGBT devices of type 5SNA 2000K450300 are utilized as the main switches. The MMDCs is controlled to maintain the input current with dc sources connected at its input and output sides, respectively. In the study case of the proposed MMDC, there are 1 and 3 submodules in the lower and upper arms, respectively. Detailed parameters of the simulation model at the switching frequency of 1 kHz are listed in Table II in the Appendix section.

A. Steady-State Analysis

Fig. 8 depicts the steady-state simulation waveforms of the proposed MMDC when the transmission power is 200 kW at the switching frequency of 1 kHz. In Fig. 8(a), $S_{T2,3}$ represents the switching signal of the switch $T_{2,3}$ in the typical submodule SM_3, which is complementary to that of $T_{1,3}$. $i_{D3,2}$ and $i_{D3,3}$ represent the resonant currents in SM_2 and SM_3, respectively. $i_{T2,3}$, $i_{D1,3}$, $i_{T1,3}$, and $v_{T1,3}$ are the current and voltage waveforms of the corresponding switches denoted by the subscripts. In Fig. 8(b), v_{c1}–v_{c5} represent the submodule capacitor voltages. In Fig. 8(c), $i_{\rm dc1}$ and $i_{\rm dc2}$ are the input and output currents, respectively. $v_{\rm L}$ and $v_{\rm U}$ represent the generated voltages in the lower and upper arms, respectively.

In Fig. 8(a), SM_3 absorbs power from SM_2 when the resonant current $i_{D3,2}$ is not zero. SM_3 releases power to SM_4 when $i_{D3,3}$ is not zero. The variation process of the capacitor voltages reflects how power transfers among the submodules, verifying the proposed operating principles. Low-current switching is achieved for $T_{2,3}$ with only the dc component current flowing through it. When $T_{2,3}$ is switched OFF, the current commutates to $D_{1,3}$, clamping the voltage of $T_{1,3}$ to zero, creating the zero-voltage turn-ON condition for $T_{1,3}$. When $i_{D3,2}$ exceeds the dc current, $T_{1,3}$ begins to conduct current. Zero-current turn-OFFs of $T_{1,3}$ and $D_{3,3}$ are naturally achieved when the

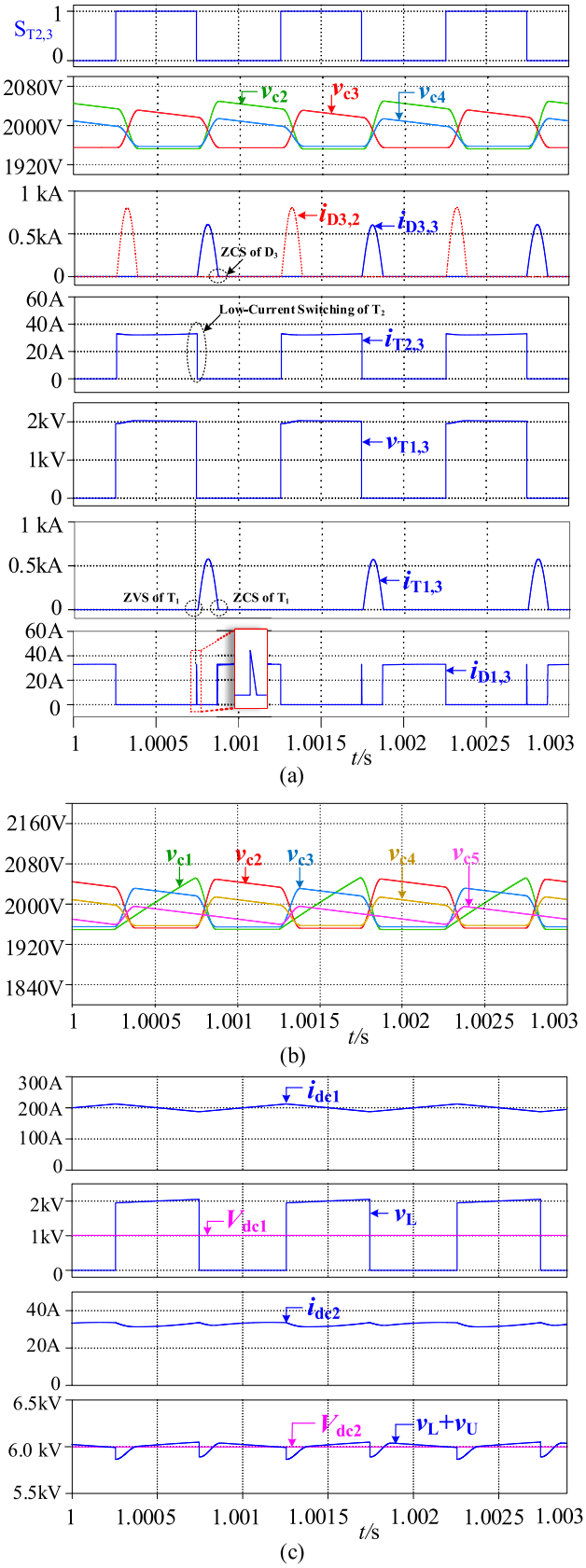

Fig. 8. Simulation waveforms of the proposed MMDC in steady-state. (a) Voltage and current waveforms in SM_2 and SM_3. (b) Capacitor voltage waveforms. (c) Voltage and current waveforms at the dc stage.

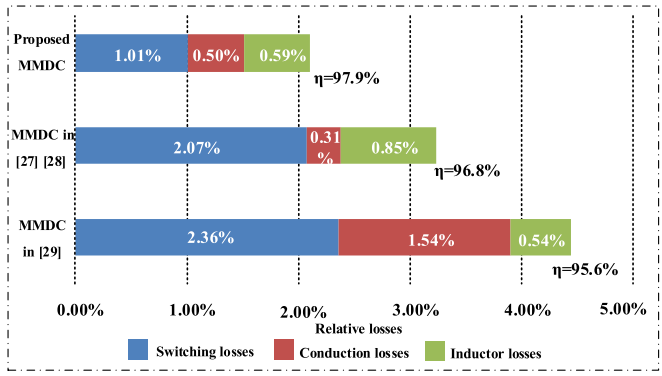

Fig. 9. Efficiency comparison between the proposed converter and existing MMDC topologies when $f_s = 1$ kHz.

resonant current returns to dc current level and zero, respectively. These simulation results are consistent with the analysis results in Section II.

As can be observed from Fig. 8(b), the submodule capacitor voltages are automatically balanced. The amplitude of voltage ripples decreases gradually from the bottom submodule to the top submodule of the upper arm, verifying the theoretical analysis results. Fig. 8(c) shows that the generated voltage at the output stage (i.e., v_L+v_U) is stable with acceptable ripples caused by the fluctuation of capacitor voltages when the proposed modulation method is utilized. A small choke at the output stage is sufficient to eliminate the dc current ripples. Moreover, the amplitude of the square-wave lower arm voltage v_L is limited to the submodule voltage level, indicating a significant reduction of the input filter inductance.

B. *Efficiency Comparison*

To verify the superiority of the soft-switching operation, based on power loss breakdown analysis, the conversion efficiency of the proposed converter is compared with the HBSM-based MMDC operated under the stepped two-level modulation scheme [27], [28] and the resonant MMDC presented in [29]. When MMDC is utilized for medium- and high-voltage applications, the power losses are dominated by the conduction and switching losses of semiconductor devices and the resistive losses of the inductor [29]. Therefore, the conversion efficiency is estimated based on the analysis of the above three items.

Semiconductor losses, including conduction and switching losses of the converters, are obtained by thermal simulation in PLECS utilizing the power-loss model of ABB Hi-Pak IGBT most 5SNA 2000K450300 provided by the manufacturer [31]. In the simulation study, the MMDCs are designed at the same voltage and power levels ($V_{dc1} = 1$ kV, $V_{dc2} = 6$ kV, $P = 200$ kW) and identical semiconductor devices are utilized. Power losses of each inductor are estimated by $P_{L,loss} = I^2_L R_L$ with I_L and R_L presenting the RMS current and equivalent resistor.

Figs. 9 and 10 compare the loss breakdown and efficiency of different MMDCs at the switching frequency of 1 and 2 kHz, respectively. As can be observed from the figures, the power loss is dominated by the switching losses. The resonant MMDC has the highest switching and conduction losses

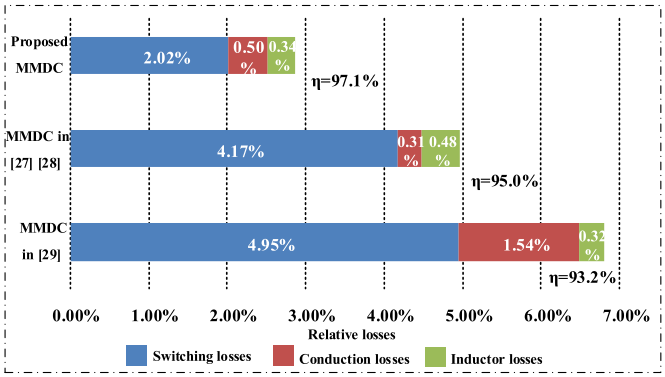

Fig. 10. Efficiency comparison between the proposed converter and existing MMDC topologies when $f_s = 2$ kHz.

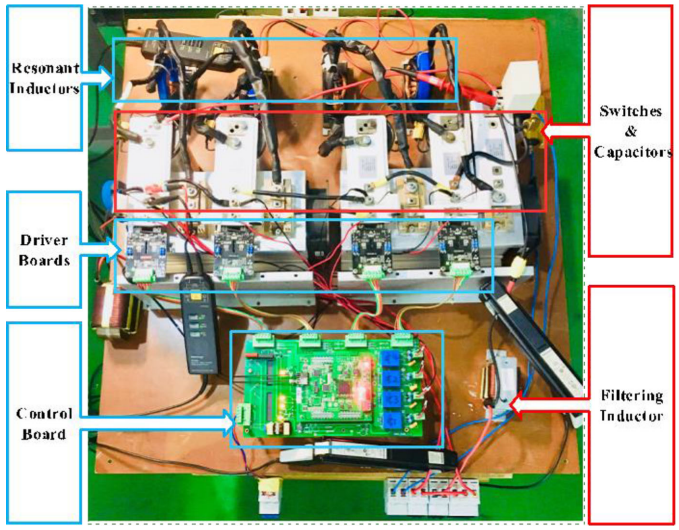

Fig. 11. Photograph of the QRSM-based MMDC prototype.

because the resonant current flows through the arms and the most lower-arm switches are turned OFF with high currents. The HBSM-based MMDC has the lowest conduction losses because the stepped two-level modulation scheme is utilized to reduce the common-mode current in the arms. Conduction losses of the QRSM-based MMDC are slightly higher than that of the HBSM-based MMDC due to the existence of resonant current and the adding of the *L-D* branch. However, the switching losses in the QRSM-based MMDC is significantly lower than that in the conventional HBSM-based MMDC because of soft-switching operations. Switching losses of hard-switched MMDC topology increases significantly when switching frequency increases. This problem is alleviated in the proposed soft-switching topology, indicating that higher switching frequency can be adopted to reduce the passive component size.

VII. Experimental Results

A scaled-down prototype of the QRSM-based MMDC rated at 1 kW has been constructed and tested. The input and output voltages are 50 and 300 V, respectively. The prototype converter includes four QRSMs in the submodule string, with one submodule in the lower arm and three submodules in the upper arm. The average capacitor voltage is 100 V. The switching frequency is 2 kHz. A photograph of the converter prototype is shown in Fig. 11. The main parameters of the prototype are listed in Table II in the Appendix section. In the experiment, a dc power supply and an inverter both controlled to maintain their dc voltages are utilized to provide and absorb the transferred power, respectively. The MMDC is controlled to maintain the input current via a PI controller.

A. Steady-State Results

With the transferred power maintained as 1 kW via controlling the input current, Fig. 12(a), (b), (c), and (d) show the measured capacitor voltages, resonant currents, the voltage and current waveforms at the dc stage, and waveforms of switches in the typical submodule of the upper arm (i.e., SM_3), respectively.

In Fig. 12(a), the capacitor voltages are self-balanced without any control. Moreover, in the upper arm, the amplitudes of voltage ripples decrease gradually from the bottom to the top submodule, and the bottom submodule presents the largest voltage ripples. This finding is consistent with the theoretical analysis and simulation results. Fig. 12(c) shows that, when the proposed modulation method is utilized, the generated voltage across the whole submodule string (i.e., v_L+v_U) is stable with acceptable ripples and small voltage sparks caused by switching actions. Moreover, the amplitude of square-wave lower-arm voltage v_L is limited to the submodule voltage level to reduce the size of the input filter inductance. Fig. 12(d) shows that soft switching is achieved for the majority of switches. T_1 is turned on after its voltage decreases to zero with D_1 conducting current. T_1 and D_3 are naturally turned OFF with their currents return to zero. These experimental results are in agreement with the theoretical analysis and the simulation results.

B. Dynamic Performance

Fig. 13 shows the dynamic responses of the capacitor voltages when the transferred power is stepped up from 500 W to 1 kW by adjusting the referenced input current command from 10 to 20 A, including the waveforms of input and output currents and two typical submodule voltages. As can be observed from the figure, the input current is well controlled to track the reference signal in less than 20 ms. Besides, the capacitor voltages are well balanced without divergence regardless of power variation, verifying the robust self-voltage balancing capability of the proposed MMDC.

C. Efficiency Analysis

Comparison of measured power at the input and output sides of the scaled-down prototype shows 91.3% efficiency when the transmission of power is 1 kW. After reconstructing the prototype into a conventional HBSM-based stepped two-level MMDC and operating the converter under the same condition, the measured efficiency is 90.9%.

The conversion efficiency is relatively low because conventional high-voltage IGBT modules are utilized in the prototype. The on-state voltage of the switches cannot be neglected when compared with the dc voltage, resulting in relatively high

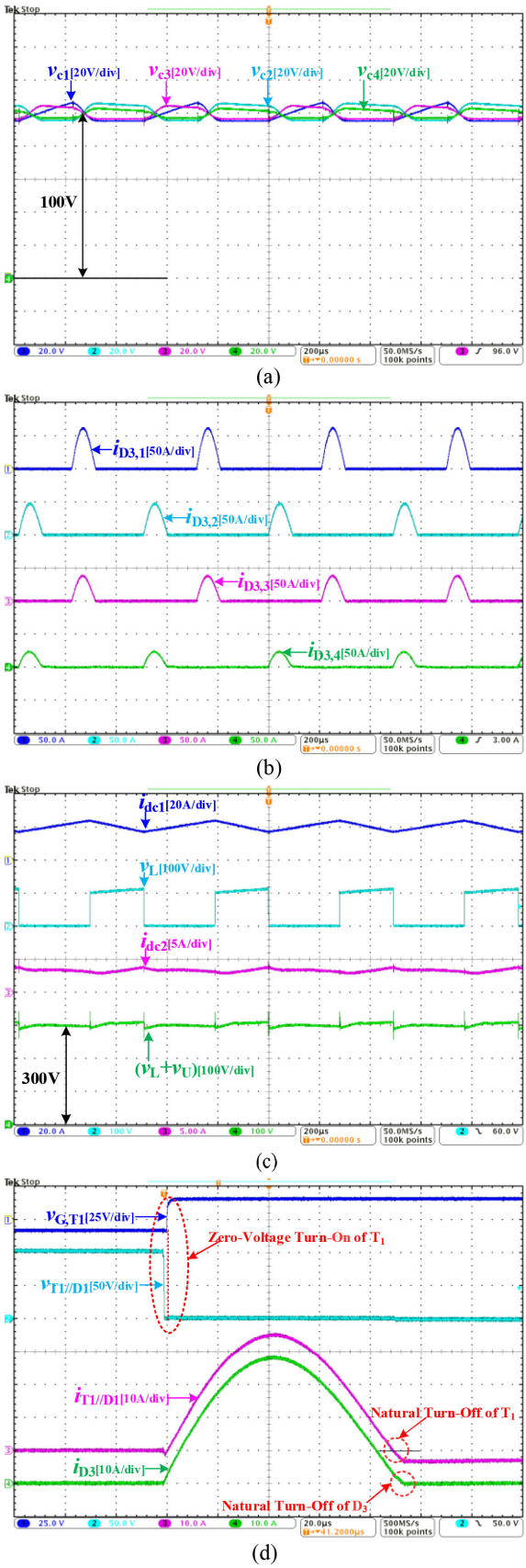

Fig. 12. Measured waveforms of the proposed MMDC. (a) Capacitor voltages. (b) Resonant currents. (c) Voltage and current waveforms at the dc stage. (d) Voltage and current of switches in the typical submodule (i.e., SM_3).

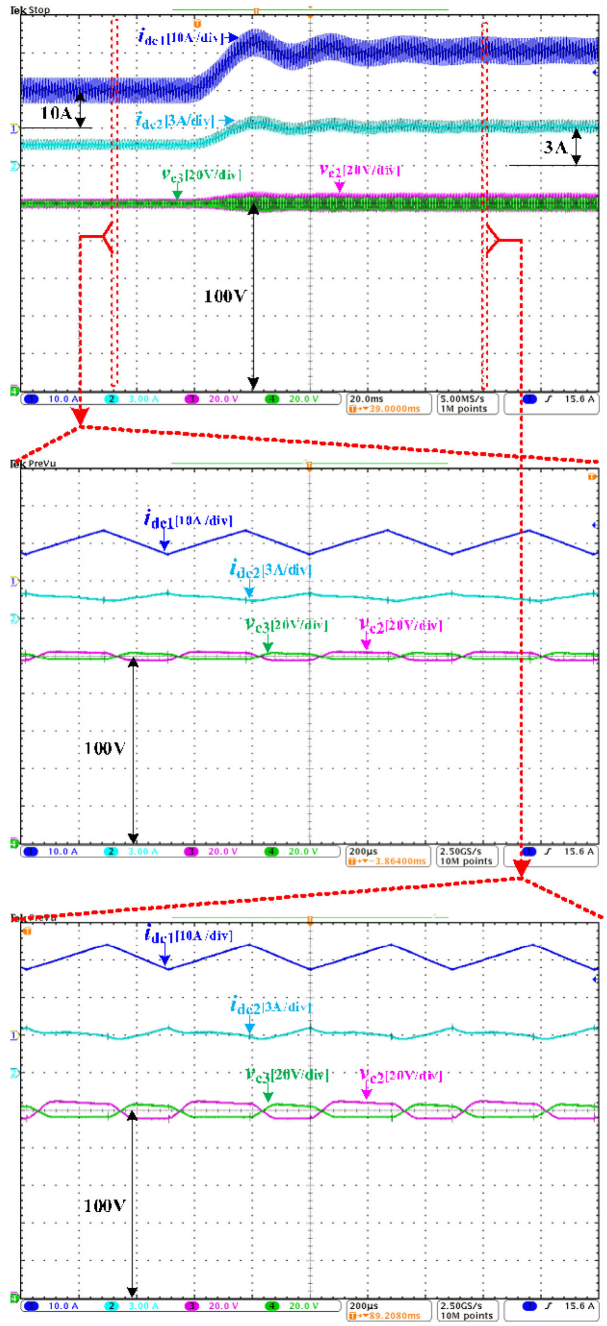

Fig. 13. Measured waveforms of MMDC when the input current steps up from 10 to 20 A.

condition losses. Employing a large number of switches in the scaled-down prototype aggravate this issue. Increasing the voltage and power levels to the practical MVDC applications as that studied in the simulation, the conversion efficiency will be relatively high because the on-state voltage of the IGBT devices is insignificant against the dc voltage, reducing the percentage contribution in conduction losses.

The above analysis shows that the conduction losses take a larger proportion in the scaled-down prototype than that in the simulation study. This explains why significant efficiency improvement is not found in the QRSM-based

MMDC prototype. Although it cannot fully reflect the efficiency property, the scaled-down prototype is a sufficient proof-of-concept of the proposed topology and control.

VIII. Conclusion

A novel MMDC for step-up applications, along with its modulation strategies, is presented in this article. By employing resonant currents to transfer compensating power between the adjacent submodules, the common-mode circulating current existing in conventional MMDCs flows through the arms and the output side is avoided. Also, soft switching is realized for the majority of switches with the remaining switches turned ON and OFF with only the dc component. Self-balancing of the capacitor voltages is achieved. Comparing with other MMDC topologies, the proposed one reduces the switching losses effectively, resulting in higher conversion efficiency.

Appendix

See Table II.

TABLE II
Parameters of Proposed MMDC in Simulation and Experiment

Parameters	Values in simulation	Values in experiment
Input voltage, V_{dc1}	1 kV	50 V
Output voltage, V_{dc2}	6 kV	300 V
Rated power, P	200 kW	1 kW
Submodule capacitor, C	800 uF	330 uF
Resonant inductor, L_r	5 uH	5 uH
Number of submodules in the upper arm, M	3	3
Number of submodules in the lower arm, N	1	1
Input filter inductor, L_f	10 mH	2 mH
Output choke, L_s	5 mH	1 mH

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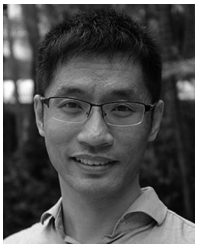

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