Letters

A Quasi-Three-Level PWM Scheme to Combat Motor Overvoltage in SiC-Based Single-Phase Drives

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***Abstract*—The emergence of fast switching wide-bandgap (WBG) power devices offers clear potential to implement higher power density and more efficient motor drives. However, the high voltage slew rate (dv/dt) of switching transients brought significant challenges that can hamper the wide adoption of WBG devices in motor drive applications. Specifically, the aggravated motor overvoltage oscillation, due to reflected voltage phenomenon under high dv/dt, is one of the most considerable challenges that degrade the motor lifetime. With filter networks acting as the mainstream mitigation method, the advantages of WBG-based motor drives are compromised due to additional size and power loss of the filters. This letter proposes a novel quasi-three-level pulsewidth modulation scheme as a software solution to eliminate motor overvoltage oscillations in cable-fed drives. The proposed scheme adopts a brief zero-voltage state, with a predetermined time, in the midway of each pole-to-pole voltage transition. This allows the voltage reflections along the cable to significantly discontinue after two propagation cycles, securing the motor operation at prescribed voltage levels. The proposed scheme is applicable to two-level voltage-source inverters (VSIs). In this letter, the scheme is presented on a single-phase two-level VSI motor drive, supported with theoretical and experimental proof of concept.**

***Index Terms*—High dv/dt, inverter-fed motor drives, motor overvoltage, reflected voltage phenomenon, silicon carbide (SiC), wide-bandgap (WBG) devices.**

I. Introduction

MOTOR drive systems are gaining improved performance with the adoption of wide-bandgap (WBG) power devices, such as those based on the silicon-carbide (SiC) material, due to their fast switching speed and elevated temperature capabilities [1]. This allows the motor drives to operate at higher switching frequencies with low switching loss and reduced cooling requirements, leading to higher efficiency and more compact system than a silicon-based counterpart [2]. However, the shorter rise/fall times associated with the fast switching speed result in a high voltage slew rate (dv/dt), which degrades the motor insulation and bearing while raises electromagnetic interference (EMI) problems [3].

Drive systems utilized in high ambient temperature and submersible applications obligate the machine and drive to be placed at separate locations where power cables are used for interconnection. Pulsewidth modulation (PWM) pulses traveling across power cables have similar behavior to traveling waves on transmission lines. The impedance mismatch between the cable and the motor results in successive voltage reflection, causing voltage oscillations at the motor terminals. With shorter rise/fall times, the reflected voltage phenomenon is more pronounced in SiC-based drives than traditional silicon-based counterparts, where the motor voltage can be doubled with shorter cable lengths, e.g., within several meters [4]. The reflected voltage oscillations stand behind the premature failure of the winding insulation of inverter-fed random-wound motors due to an accelerated aging of the insulation between the winding turns. The high values of motor turn-to-turn voltage due to reflected voltage oscillations can incept partial discharges that progressively yield to the degradation of polyamide-imide and polyester coating of motor coils [5].

The mainstream mitigation approach for reflected voltage phenomenon is employing passive filters either at the motor terminals as a matching impedance between the cable and the motor or at the inverter cabinet to flatten the high dv/dt of PWM pulses [6], [7]. Despite their effectiveness, the passive filters increase the drive system cost and size while induce additional power loss, countering the advantages of SiC devices.

This letter proposes a novel PWM scheme that eliminates motor overvoltage oscillations in SiC-based drives without sacrificing the beneficial attributes of SiC devices. The scheme implementation varies according to adopted power converter topologies, where for simple demonstration, this letter applies the proposed scheme to single-phase voltage-source inverters (VSIs) for low-power single-phase random-wound motors that are widely used for diverse applications in many industries. The generalization of the proposed scheme to high-power three-phase motor drives will be addressed in future publications. The proposed modulation scheme is developed based on bipolar

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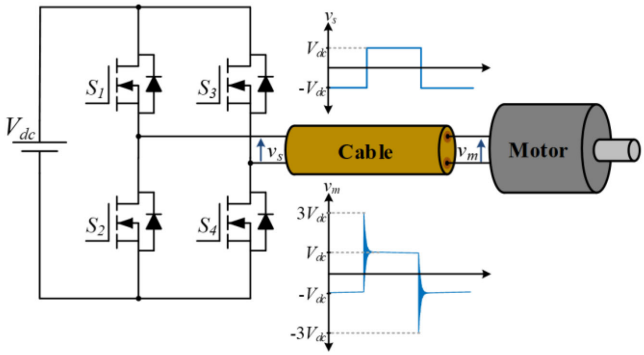

Fig. 1. Single-phase VSI feeding a single-phase ac motor through a power cable with the critical length.

sinusoidal PWM (SPWM). Therefore, the following section first investigates the voltage reflection mechanism in single-phase motor drives under the bipolar SPWM.

II. Voltage Reflection in Cable-Fed Motor Drives

VSIs are widely adopted to control electric machines in a wide-speed range, where the PWM technique is often utilized to generate the driving signals of the employed switching devices. It is well understood in the prior art that the motor voltage can reach up to twice the inverter voltage depending on the length of connection cables and the rise/fall time of the generated PWM voltage pulses [8]. This is demonstrated in Fig. 1, where a single-phase VSI supplies a motor through a power cable with the critical length, which causes full voltage reflection. With the bipolar SPWM, the switching devices S_1 and S_4 are simultaneously triggered complementary to S_2 and S_3. Thus, the output voltage at the inverter terminals v_s has bipolar voltage pulses with $2V_{\rm dc}$ peak-to-peak magnitude, where $V_{\rm dc}$ is the inverter dc-link voltage. The voltage at the motor terminals v_m is shown to have significant voltage oscillations at the rising and falling edges, where the inverter voltage experiences successive voltage reflections across the cable. This results in the motor voltage oscillating between $-V_{\rm dc}$ and $3V_{\rm dc}$, at the rising transition, in a damped manner before it settles at $V_{\rm dc}$. The peak-to-peak voltage magnitude at the motor terminals is $4V_{\rm dc}$, where the voltage has been doubled compared with the inverter peak-to-peak voltage, i.e., $2V_{\rm dc}$.

The full voltage reflection phenomenon for a bipolar voltage pulse is further illustrated using the bounce diagram shown in Fig. 2. The reflection coefficients at the inverter side Γ_s and at the motor side Γ_m are defined as follows [6]:

$$\Gamma_s = \frac{Z_s - Z_c}{Z_s + Z_c} \tag{1}$$

$$\Gamma_m = \frac{Z_m - Z_c}{Z_m + Z_c} \tag{2}$$

where Z_s, Z_c, and Z_m are the surge impedance of the inverter, cable, and motor, respectively. With L_c and C_c as the per-unit length cable inductance and capacitance, respectively, Z_c is

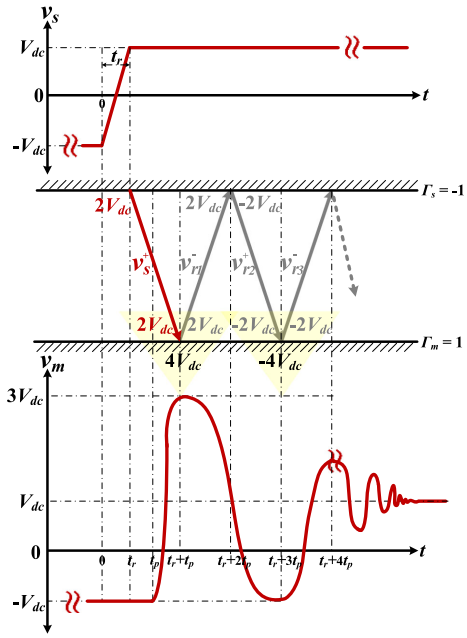

Fig. 2. Bounce diagram for full voltage reflection of a bipolar voltage pulse.

calculated as follows [6]:

$$Z_c = \sqrt{\frac{L_c}{C_c}}. \tag{3}$$

Typically, $Z_s \approx 0$ for a VSI resulting in $\Gamma_s = -1$, where the peak reflected voltage is primarily determined by Γ_m, as follows [6]:

$$V_m = (1 + \Gamma_m)\ V_s. \tag{4}$$

Since the motor surge impedance is always several times higher than that of the cable, the motor appears as an open circuit to the voltage surge traveling across the cable. That is, Γ_m is reasonably approximated to unity.

Referring to Fig. 2, at $t = 0$, the inverter voltage v_s ramps from $-V_{\rm dc}$ to $V_{\rm dc}$ within a rise time t_r. The $2V_{\rm dc}$ voltage surge travels through the cable within a propagation time t_p, where t_p is assumed to be much longer than t_r. The propagation time is calculated as a function of the cable length l_c and per-unit inductance and capacitance as follows [6]:

$$t_p = l_c\sqrt{L_c C_c}. \tag{5}$$

Due to the impedance mismatch between the motor and the cable, the $2V_{\rm dc}$ voltage surge (v_s^+) experiences wave reflection with a positive unity coefficient at the motor side, where the resultant voltage change is $4V_{\rm dc}$. Thus, the motor voltage v_m increases from $-V_{\rm dc}$ at $t = t_p$ to $3V_{\rm dc}$ at $t = t_r + t_p$. The $2V_{\rm dc}$ reflected voltage (v_{r1}^-) arrives the inverter side at $t = t_r + 2t_p$ and experiences a second forward reflection with a negative unity coefficient. This reflection does not affect the inverter voltage waveform since the inverter clamps the voltage to $V_{\rm dc}$. At $t = t_r + 3t_p$, the second reflected voltage (v_{r2}^+) arrives the motor side and experiences a third backward reflection (v_{r3}^-)

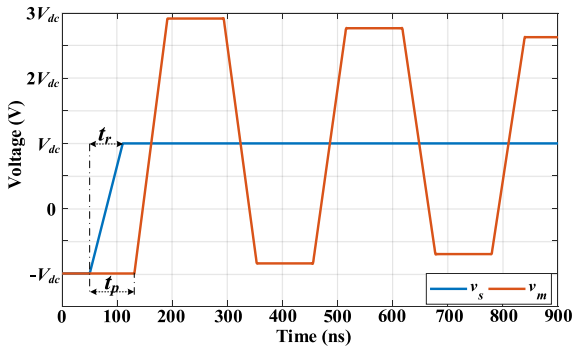

Fig. 3. Idealized inverter and motor voltage waveforms under full voltage reflection using a bipolar voltage pulse ($l_c = 15$ m, $t_p = 81$ ns, and $t_r = 60$ ns).

with positive unity coefficient resulting in a voltage change at the motor side equal to $-4V_{\rm dc}$, dropping the motor voltage to $-V_{\rm dc}$. The voltage reflection at both inverter and motor sides continues, however, with damped oscillations before the motor voltage settles at $V_{\rm dc}$. A MATLAB-based mathematical model for wave propagation through transmission lines is used to verify the theoretical analysis, as introduced in [9], simulating the full voltage reflection of a bipolar voltage pulse where the idealized inverter and motor voltages are shown in Fig. 3.

III. Proposed Quasi-Three-Level (Q3L) PWM Scheme to Combat Motor Overvoltage

The proposed PWM scheme is applicable to two-level VSIs, where it generally implies splitting the rising and falling transitions of each PWM voltage pulse into two equal-voltage steps separated by a brief intermediate voltage level. The time spent at the intermediate level is denoted as the dwell time t_d, which is precisely selected relative to t_r and t_p to turn OFF the voltage reflections across the cable, as later detailed. Since the resultant waveform has three voltage levels, it is denoted, hereafter, as a quasi-three-level waveform.

A. Q3L Waveform Generation

In single-phase VSIs, the Q3L waveform can be obtained by employing the bipolar SPWM technique. Unlike the unipolar SPWM where an intermediate voltage level requires access to half the dc-link voltage, the bipolar SPWM seamlessly realizes the intermediate voltage level by allowing the inverter to generate zero voltage for a time interval t_d in the midway of each pole-to-pole voltage transition. It should be noted that if the unipolar SPWM is directly used, i.e., without inserting additional intermediate voltage level, overvoltage oscillations are also expected at the motor side, however, limited to $2V_{\rm dc}$ compared with $3V_{\rm dc}$ as the case in the bipolar SPWM.

Referring to Fig. 1, the zero-voltage state can be realized by inserting a time shift t_d severally between the driving signals of the switching devices S_1 and S_4 and the switching devices S_2 and S_3. Driving signals generation for the four switching devices under Q3L PWM scheme is illustrated in Fig. 4, where a sinusoidal reference signal is compared with two triangular carrier

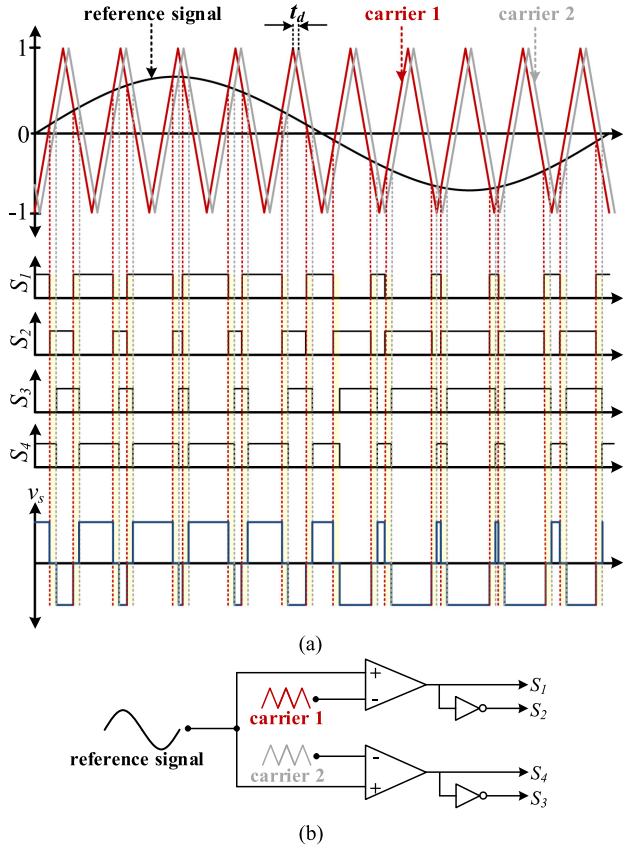

Fig. 4. Q3L waveform generation in a single-phase VSI. (a) Sketch of modulation scheme. (b) Scheme block diagram.

signals that have the same frequency but are chronologically shifted by t_d.

B. Dwell Time Setting of the Q3L Waveform

Fig. 5 elucidates the behavior of a Q3L waveform traveling through a power cable by showing the voltage reflection bounce diagram. At $t = 0$, the inverter voltage ramps from $-V_{\rm dc}$ to 0 within a rise time t_r. This voltage surge travels through the cable as the first incident wave to the motor side. At $t = t_r + t_p$, the first incident wave (v_{s1}^{+}) arrives the motor side and experiences a full reflection. That is, a reflected wave (v_{r1}^{-}) with $V_{\rm dc}$ propagates back from the motor side to the inverter side, where the resultant voltage change at the motor terminals is $2V_{\rm dc}$ (double the incident voltage value). Thus, at $t = t_r + t_p$, the motor voltage is $V_{\rm dc}$.

While v_{r1}^{-} is traveling from the motor side to the inverter side, the inverter voltage is settled at 0 V for a dwell time t_d. When v_{r1}^{-} arrives the inverter side, it immediately experiences another forward reflection with a negative unity coefficient. That is, at $t = t_r + 2t_p$, a second reflected wave (v_{r2}^{+}) with $-V_{\rm dc}$ is ready to propagate from the inverter side to the motor side. The conceptual idea of the proposed scheme is to set the dwell time of the Q3L waveform scheduling its second voltage step to propagate synchronously with the second reflected wave at the inverter side. This results in v_{r2}^{+} with $-V_{\rm dc}$ be countered by the second incident voltage step (v_{s2}^{+}) with $V_{\rm dc}$, as shown in Fig. 5.

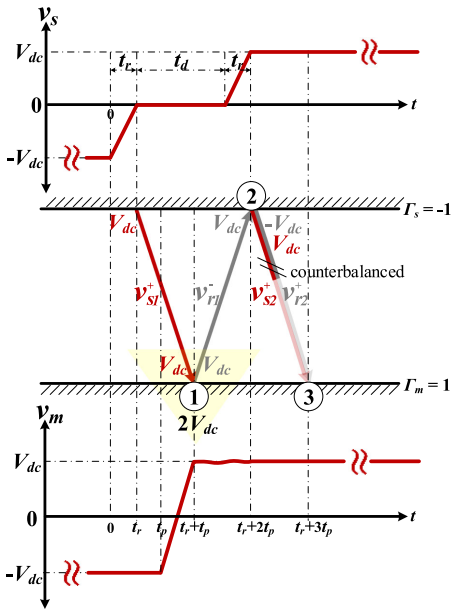

Fig. 5. Bounce diagram for the proposed Q3L waveform propagation.

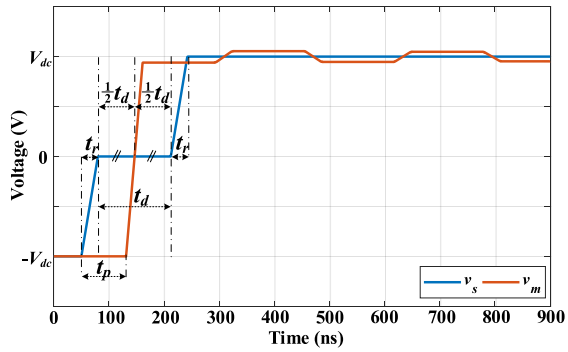

Fig. 6. Idealized inverter and motor voltage waveforms under proposed Q3L modulation scheme ($l_c = 15$ m, $t_p = 81$ ns, $t_r = 30$ ns, and $t_d = 132$ ns).

Accordingly, the voltage reflection through the cable is ideally discontinued after two propagation cycles, while the voltage at the motor side is maintained constant at $V_{\rm dc}$. Referring to Fig. 5, this is achieved when $t_r + 2t_p = 2t_r + t_d$. Therefore, the desired dwell time of the Q3L waveform during its rising edge is

$$t_{d_r} = 2t_p - t_r. \tag{6}$$

Likewise, the dwell time can be selected to eliminate the voltage reflections at the Q3L falling edge, as a function of the pulse fall time t_f as follows:

$$t_{d_f} = 2t_p - t_f \tag{7}$$

where the subscripts "r" and "f" denote the rising and falling transitions of the Q3L waveform, respectively.

Fig. 6 shows the idealized inverter and motor voltages under Q3L modulation with an optimum dwell time setting, using the mathematical wave propagation model of [9]. It is worth mentioning that although the inverter voltage is reshaped to a Q3L waveform with the deliberately inserted zero-voltage state, the motor voltage has a two-level waveform where the brief zero-voltage state is compensated by the wave propagation time. Also, it can be noticed that when the dwell time is optimized, i.e., $t_d = 2t_p - t_r$, the motor voltage crosses the inverter zero-voltage level at the dwell time midway, i.e., $v_m = v_s = 0$.

TABLE I
CABLE PARAMETERS FOR DWELL TIME ASSESSMENT

Cable gauge (AWG)	L_c (μH)	C_c (pF)	t_p (ns) per unit length
10	0.28	125.4	5.93
12	0.26	104.7	5.22
14	0.29	93.9	5.22

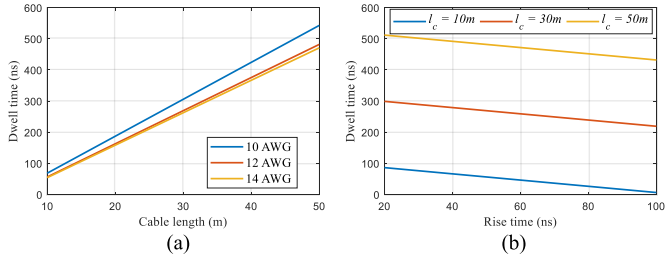

Fig. 7. Dwell time variation with (a) cable length ($t_r = 50$ ns) and (b) rise time (12 AWG cable).

C. Dwell Time Variation

Based on (6) and (7), the dwell time depends on the wave propagation time and the rise/fall time of the switching transition. Since the cable length determines the wave propagation time, as shown in (5), the dwell time is directly proportional to the cable length. Using the cable parameters listed in Table I, the variation of the dwell time is depicted with cable length, for different wire sizes, as shown in Fig. 7(a) at a constant rise time of the switching transition. Also, Fig. 7(b) shows the dwell time variation with the switching rise time for different cable lengths at the same wire size, where the dwell time decreases as the rise time increases.

It is worth mentioning that the dwell time setting is not affected by the inserted dead time between the same-leg switching devices. Also, with the cable lengths of motor drive systems usually less than 100 m, the required dwell time is limited to hundreds of nanoseconds, where in this range the dwell time has a negligible effect on the harmonic contents of the Q3L waveform and the dc-link voltage utilization. Thus, the Q3L modulation inherits the same harmonic profile of the bipolar SPWM, however, with reduced EMI performance since the Q3L waveform traverses in three levels (similar to unipolar SPWM) rather than two levels as in the bipolar SPWM.

D. Effect of Nonunity Reflection Coefficients

Elimination of further voltage reflections after two propagation cycles is significantly guaranteed even if the magnitude of Γ_m and Γ_s is less than unity. This can be elucidated by deriving the generalized form for the peak reflected voltage at the motor side with variable Γ_m and Γ_s. Referring to Fig. 5, the incident and reflected voltages at the time instants 1, 2, and 3 are listed in Table II. The peak reflected voltage at the motor side after

TABLE II
INCIDENT AND REFLECTED VOLTAGES WITHIN THREE PROPAGATION CYCLES

	Inbound voltage	Outbound voltage	Voltage change
①	V_{dc}	$\Gamma_m V_{dc}$	$V_{dc}(1+\Gamma_m)$
②	$\Gamma_m V_{dc}$	$V_{dc}(1+\Gamma_m\Gamma_s)$	$V_{dc}(1+\Gamma_m+\Gamma_m\Gamma_s)$
③	$V_{dc}(1+\Gamma_m\Gamma_s)$	$\Gamma_m V_{dc}(1+\Gamma_m\Gamma_s)$	$V_{dc}(1+\Gamma_m\Gamma_s)(1+\Gamma_m)$

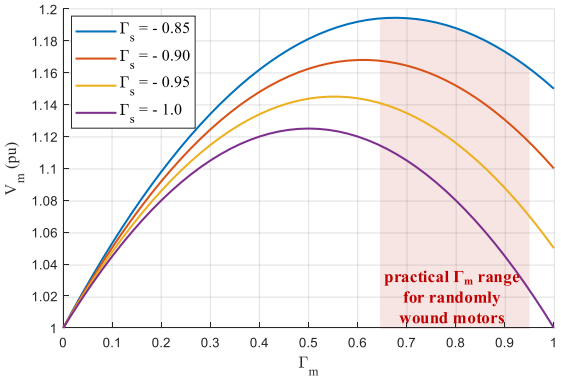

Fig. 8. Variation of the motor peak voltage with reflection coefficients using the proposed Q3L approach.

three propagation cycles, i.e., the sum of the voltage change at time instants 1 and 3, is given as $V_{\rm dc}(1+\Gamma_m)(2+\Gamma_m\Gamma_s)$. With $2V_{\rm dc}$ as the peak-to-peak magnitude of inverter voltage, the motor peak voltage V_m is calculated in per unit (p.u.) value as follows:

$$V_m = \frac{V_{\rm dc}\,(1+\Gamma_m)\,(2+\Gamma_m\Gamma_s)}{2V_{\rm dc}} = \frac{1}{2}\,(1+\Gamma_m)\,(2+\Gamma_m\Gamma_s)\,. \tag{8}$$

Based on (8), Fig. 8 shows the variation of the motor peak voltage with different Γ_m and Γ_s values when the proposed Q3L approach is applied. Typical Z_m and Z_c for random-wound motor drives (up to 500 hp) result in Γ_m ranges between 0.65 and 0.95 [10], where in this range, the motor overvoltage decreases as Γ_m increases. Since the VSI's dc-link capacitor behaves as a short circuit to the fast-rising pulse, practical Γ_s values are very close to -1. Thus, in Fig. 8, Γ_s ranges between -0.85 and -1, where it can be shown that the motor overvoltage is less than 20%.

IV. DWELL TIME ADAPTATION ALGORITHM

According to (6) and (7), the dwell time is determined based on the wave propagation time and the rise/fall time of the switching transition. In many practical cases, it is difficult to obtain an accurate value of the wave propagation time where the cable operating temperature may affect its insulation permittivity and, thus, change its electrical characteristics. Also, the rise/fall time of the switching transitions varies with the load current alternation and SiC MOSFET's parasitic capacitance. Since t_p and t_r are in the nanosecond range, a small deviation in these two parameters with operating conditions results in an inaccurate dwell time setting that negatively impacts the effectiveness of the proposed Q3L approach.

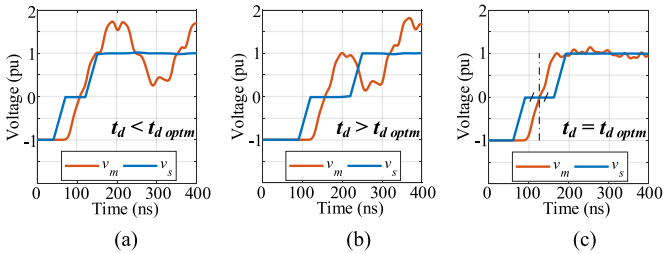

Fig. 9. Inverter and motor voltages under Q3L modulation at different dwell time settings. (a) t_d= 50 ns. (b) t_d= 100 ns. (c) t_d= 72 ns (l_c = 10 m, t_p = 51 ns, and t_r = 30 ns).

To precisely set the dwell time to its optimum value ($t_{d\ \rm optm}$) that significantly counterbalances the voltage reflections, a potential dwell time adaptation algorithm is proposed. The algorithm necessitates the motor voltage to be measured using a wideband (high bandwidth) voltage transducer to detect the time instant at which the motor voltage crosses the intermediate voltage level of the Q3L waveform, i.e., the zero-voltage level. Referring to Fig. 6, the optimum setting of the Q3L waveform implies the motor voltage crosses the zero-voltage level at the dwell time midway. This is further illustrated in Fig. 9, where a MATLAB simulation shows the inverter and motor voltages under Q3L modulation at different dwell time settings. In Fig. 9(a), the dwell time is set lower than the optimum value, where the motor voltage crosses the zero-voltage level after the dwell time midway. Fig. 9(b) shows the case when the dwell time is set larger than the optimum value, where the motor voltage crosses the zero-voltage level earlier than the dwell time midway. Common to Fig. 9(a) and (b), the motor overvoltage oscillations are partially mitigated, where the motor peak voltage is 1.72 p.u. and 1.82 p.u, respectively. Setting the dwell time to its optimum value results in significant overvoltage mitigation, as shown in Fig. 9(c), where the motor voltage crosses the zero-voltage level at the dwell time midway.

The proposed algorithm follows the Q3L waveform generation sequence presented in Fig. 4, however, updates the dwell time value for each switching transition. Thus, the algorithm detects the compare match between the reference signal and the carrier 1 and, accordingly, decides whether the switch S_1 is active high or low. At the compare match event, the algorithm starts to count the elapsed time until $v_m = 0$, where the counted time represents half the optimum dwell time value. Then, the algorithm updates the time shift between the two adopted carrier signals with the calculated dwell time as twice as the counted value, as shown in the flowchart of Fig. 10. The state of the switch S_4 is determined by comparing the reference signal with carrier 2, terminating the zero-voltage level of the Q3L waveform. Finally, the counter value is reset to zero and the algorithm is repeated for a new switching transition. In this way, the dwell time is adaptively optimized independent of t_p and t_r.

V. EXPERIMENTAL VERIFICATION

To verify the proposed approach, a single-phase VSI is used to supply a 3-hp 230-V induction motor at 50 Hz through

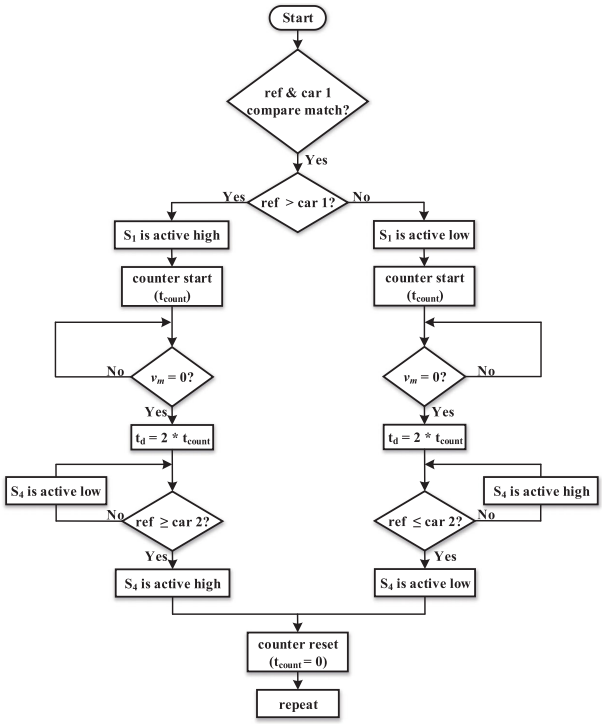

Fig. 10. Flowchart for the Q3L dwell time adaptation algorithm.

5.5-m-long 12 AWG polyvinyl chloride cable. The inverter is realized using the C2M0040120D SiC power MOSFETS, switched at 40 kHz, and supplied from 300 V dc link. The inverter board is carefully designed to minimize the power loop inductance in order to reduce the voltage ringing associated with each switching transition. The cable parameters are measured using an impedance analyzer, resulting in $L_c = 0.97\ \mu$H and $C_c = 45$ pF. Based on (5), the wave propagation time is calculated as $t_p = 36.3$ ns. The calculated propagation time is then confirmed using a high-speed digital oscilloscope as the interval between the time instants when the inverter and motor voltages start to ramp, where the propagation time is digitally measured as 36.5 ns (very close to the theoretically calculated value). The inverter is first modulated using the bipolar SPWM technique to practically assess the motor overvoltage due to full-wave reflection. Then, the proposed Q3L PWM scheme is adopted, where the dwell time is adjusted based on the adaptation algorithm illustrated in Fig. 10. The experimental results are presented in Figs. 11–13, where high-bandwidth (25 MHz) differential voltage probes are used in the measurements.

Fig. 11 shows the voltage doubling effect due to the reflected wave phenomenon when the VSI generates two-level voltage pulses being modulated with the traditional bipolar SPWM technique. While the inverter voltage traverses within ± 300 V, the motor voltage oscillates within ± 900 V envelopes in a damped manner. An enlarged view for one switching cycle of motor overvoltage oscillations is presented in Fig. 12(a) showing the motor voltage is 2 p.u. during both rising and falling voltage transitions. Further extended views showing how the motor

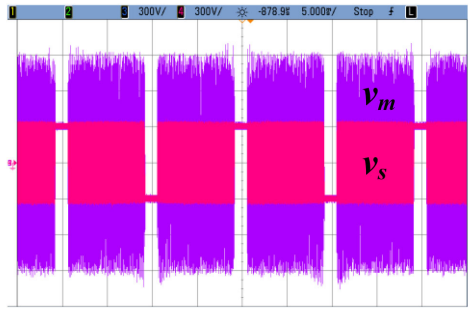

Fig. 11. Voltage doubling effect in the VSI-fed motor drive with the bipolar SPWM.

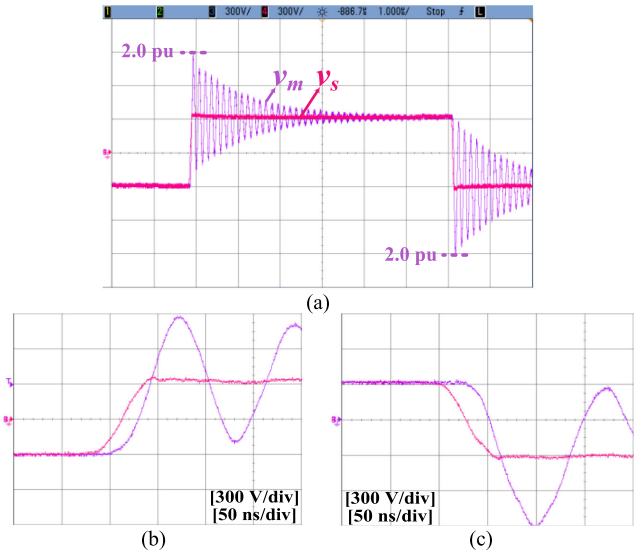

Fig. 12. Inverter and motor voltages under the bipolar SPWM technique. (a) One switching cycle view. (b) Extended view at rising transition. (c) Extended view at falling transition.

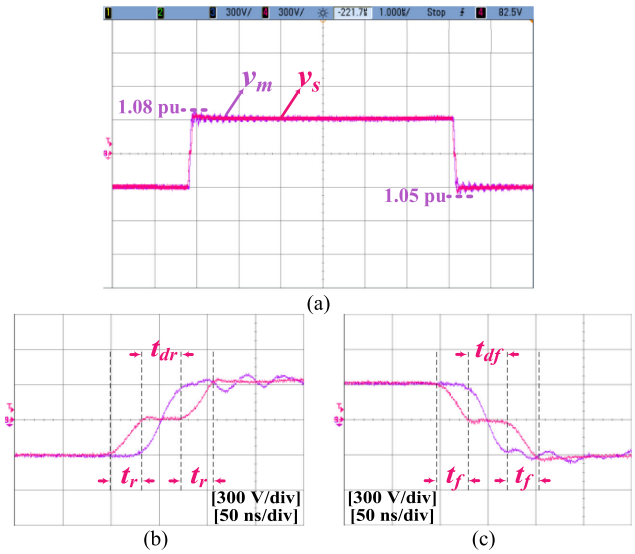

Fig. 13. Inverter and motor voltages under the proposed Q3L approach. (a) One switching cycle view. (b) Extended view at rising transition. (c) Extended view at falling transition.

voltage retardedly propagates after the inverter voltage during the rising and falling transitions are given in Fig. 12(b) and (c), respectively.

With the adoption of the proposed Q3L approach, Fig. 13(a) shows one switching cycle of the inverter and motor voltages, where the adaptively commanded dwell time significantly turns OFF the voltage reflections through the cable. As a result, the motor voltage settles around its nominal value with 8% and 5% brief overvoltage oscillations at the rising and falling transitions, respectively. This is further highlighted in Fig. 13(b) and (c) showing the motor voltage propagation in response to the Q3L inverter voltage during the rising and falling transitions, respectively. The switching times at the rising and falling transitions are digitally measured with the utilized high-frequency oscilloscope as $t_r = t_f = 33$ ns, while the corresponding dwell time is digitally measured as $t_d = 40$ ns. The commanded dwell time allows the motor voltage to traverse between the pole voltages in a two-level manner while crossing the zero-voltage level at the dwell time midway, as analyzed in Fig. 6. Comparing Fig. 13 with Fig. 12 marks higher than 90% reduction in motor overvoltage, verifying the capacity of proposed approach to significantly combat motor overvoltage transients due to reflected voltage phenomenon.

VI. Conclusion and Outlook

This letter establishes a novel concept in the SiC inverter modulation to eliminate motor overvoltage in SiC-based motor drives with power cables between the motor and the inverter. The concept generally implies reshaping the inverter two-level waveform into the Q3L waveform by temporarily incorporating an intermediate voltage level for a brief dwell time, which is precisely selected relative to the switching rise/fall time and the wave propagation time. This significantly turns OFF the voltage reflections across the cable after two propagation cycles, where the second incident voltage step counters the reflection of the first incident voltage step. Accordingly, the motor voltage is maintained around the nominal voltage level with slight overvoltage oscillations. To eliminate inaccurate setting of the dwell time due to variation of the rise/fall switching time and wave propagation time with operating conditions, a dwell time adaptation algorithm is used to ensure its optimum setting.

In this letter, the proposed Q3L approach has been analyzed and applied to a single-phase VSI-fed motor drive with the experimental proof of concept. However, the approach has the potential to be applied to a class of VSI topologies. Future research will be directed to applying the approach to three-phase VSI-fed motor drives, while providing generic system design guidelines.

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