A QR-ZCS Boost Converter With Tapped Inductor and Active Edge-Resonant Cell

M. Harasimczuk

***Abstract*—Boost dc/dc converters are widely used in renewable energy systems. With growing demand for high efficiency and high voltage gain, many new topologies have been published. This article proposes a novel zero current switching (ZCS) boost converter with a tapped inductor and active edge-resonant cell (AERC). To achieve high voltage gain, the tapped inductor was implemented in the structure of the converter, and by employing an AERC, ZCS of transistors was attained. Subsequently, by employing a resonant operation current, overshoots by leakage inductance were eliminated. This article presents an analysis, mathematical derivations, and laboratory test results. Finally, a 30–50 V input, 380 V output, and 750 W output power laboratory model operating with 45–100 kHz switching frequency was built and tested. The maximum reported efficiency was 96.6%. Soft switching of semiconductors was achieved in the whole output power range.**

***Index Terms*—Boost converters, dc–dc power converters, high voltage gain, resonant converters, zero current switching.**

I. Introduction

HIGH step-up dc/dc converters are required in many energy processing systems. For example, in European systems, the low-output voltage of single or parallel-connected photovoltaic panels need to be stepped up to 380 Vdc to ensure grid-inverter operation [1]. In a vehicle's high intensity discharge (HID) lamps, the low voltage, 9–16 V, of an acid battery must be stepped up to 80–100 V [2]. Another example is an uninterruptible power system, where the low voltage of the battery should be converted to 380 Vdc. In a conventional boost converter, it is not possible to obtain high voltage gain, high efficiency and high output power at the same time, for several reasons. First, in a conventional boost converter, obtaining a high voltage gain requires an extremely high duty cycle. This increases current ripple and conduction losses. Second, switch voltage stress is almost equal to output voltage. This forces the use of a transistor with higher voltage rating and higher $R_{ds(\mathrm{on})}$. Third, in a conventional boost converter, we also observe a significant reverse recovery current in the output diode, which increases switching losses.

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The author is with the Faculty of Electrical Engineering, Bialystok University of Technology 15-351, Białystok, Poland (e-mail: m.harasimczuk@pb.edu.pl).

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There are many methods to achieve high voltage gain [3], [4]. It may be obtained using a tapped inductor [1], [5]. Converters with a tapped inductor and high voltage gain are presented in [6]. In these circuits the reverse recovery problem was reduced due to leakage inductance, which limits d*i*/d*t* in the output diode. However, the leakage inductance of the coupled inductor causes voltage overshoots across the switches during turn-OFF; in these topologies a snubber circuit is required to reduce the semiconductor voltage ratings.

Many voltage clamp methods for reducing the voltage stress on the transistor and recovering the leakage energy are described in [7]. In [8]–[10] a nonisolated converter with a coupled inductor, an active switch and a passive clamp circuit is presented. The transistor operated with pulsewidth modulation (PWM) and its voltage rating was reduced. This enabled use of a transistor that lowered $R_{ds(on)}$ to minimize conduction losses. Passive clamp circuits recycle leakage energy and help reduce the transistor's turn-OFF voltage stress. The voltage gain can be further increased by additional winding [11] and/or switched capacitors [12]–[14]. Therefore, the clamp circuit in these converters requires additional diodes and capacitors. Converters with an active clamp circuit recover the leakage energy and limit semiconductors' voltage stress [15]–[17]. This circuit usually requires an additional transistor and a capacitor. In active clamp converters the ZVS technique may be used. This requires large leakage inductance or an external inductor. It leads to a loss of effective duty cycle; a coupled inductor with a higher turns ratio is required to compensate for duty loss.

High voltage gain can also be obtained in quadratic converters [18], [19]. These circuits utilize additional diodes, capacitors, and an inductor. Unfortunately, this solution suffers from high voltage stress on the switches, which has negative effects on the efficiency of the converter.

High voltage gain can be achieved using a multiphase interleaving technique [20]–[22]. This provides low current ripple and high-power density. Moreover, in interleaved converters the reverse recovery current of output diodes is reduced. A voltage lift technique [23]–[25] also ensures high voltage gain; unfortunately, its implementation requires additional capacitors and switches.

In [26]–[28], resonant converters with series capacitors are presented. In these circuits the reverse recovery current of the output diodes was reduced to zero. The resonant converters described in [26] and [28] operated in CRM, and this enables ZVS of the transistors. However, conduction losses in CRM are high, which limits the maximum output power. In [29], a

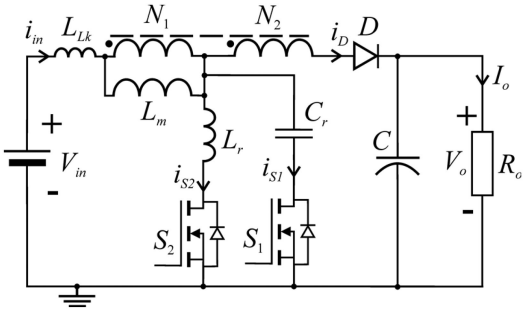

Fig. 1. Proposed converter.

quasi-resonant converter with a tapped inductor was presented. In this solution, ZVS of the transistor was obtained. However, in this circuit maximum voltage on transistor is high and depends on the output resistance. This restrict maximum output power.

Another method to achieve soft switching is a zero voltage/current transition (ZVT, ZCT) [30]–[32]. In this method, switches are subject to soft switching with low additional conduction losses. However, the transition circuit is complex and needs additional switches. Soft switching may be achieved using an AERC [33]–[35]. In an AERC, a resonant tank is used with an additional switch connected in series with the resonant capacitor, enabling a reduction of conduction losses. However, the voltage gain in these converters is low.

This article proposes a novel ZCS converter with an AERC and tapped inductor. Fig. 1 shows a schematic diagram of the proposed converter. The circuit has a simple structure consisting of two transistors turned ON at zero current and turned OFF at zero current and zero voltage. Soft switching of the transistors is possible using the resonant tank. Utilizing the tapped inductor ensures high voltage gain. In the proposed converter, transistor voltage spikes caused by current changes in the leakage inductance are reduced. The voltage gain in the converter depends on the duty ratio of transistor S_2. Turning ON switch S_1 reduces the current of switch S_2 and enables it to be turned OFF at zero current.

II. Electrical Scheme and Principle of Operation

The following assumptions were made in order to simplify the circuit analysis of the proposed converter.

1) Magnetic components are ideal with the exception of the leakage inductance of the tapped inductor.
2) The current in the magnetizing inductance L_m during one switching period is constant.
3) The voltage drop on forward biased diode *D* and resistance $R_{ds(\mathrm{on})}$ of the transistors are neglected; parasitic parameters of all elements are omitted.
4) The voltage of capacitor *C* during one switching period is constant.

Mode 1. [$t_1 - t_2$, Fig. 3*a*]: Before period $t_1 - t_2$, switch S_1 is turned ON and switch S_2 is turned OFF. Diode *D* is reverse biased. The output capacitor *C* supplies energy to the output resistance R_o. Mode 1 begins when diode *D* is turned ON. In this interval capacitor C_r resonates with leakage inductance L_{Lk}; it ends at ¾ of the resonant period when the capacitor current i_{S1} is equal to 0. The principal equations describing voltages and currents in this mode may be written as follows:

$$v_{Cr}(t-t_1) = \frac{V_o + nV_{\mathrm{in}}}{n+1} + Z_1 I_{in}\sin(\omega_1(t-t_1)) \quad (1)$$

$$v_{Cr}(t_2) = \frac{V_o + nV_{in}}{n+1} - Z_1 I_{in} \quad (2)$$

$$i_{in}(t-t_1) = I_{in}\frac{n\cos(\omega_1(t-t_1))+1}{n+1} \quad (3)$$

$$i_D(t-t_1) = I_{in}\frac{1-\cos(\omega_1(t-t_1))}{n+1} \quad (4)$$

$$t_2 - t_1 = 3\pi/2\omega_1 \quad (5)$$

where I_{in} is input current in interval $(t_4$–$t_8)$, $\omega_1 = (n+1)/(n(L_{Lk}C_r)^{1/2})$, $Z_1 = (n/(n+1))\cdot(L_{Lk}/C_r)^{1/2}$, and *n* is the turns ratio of the tapped inductor.

Mode 2. [$t_2 - t_3$, Fig. 3*b*]: At t_2 switch S_1 is turned OFF at zero current and zero voltage. In this mode, the current flows from source V_{in}, through the tapped inductor and forward biased diode *D* to resistor R_o and capacitor *C*. Thus, the energy from source V_{in} and the energy accumulated in the tapped inductor are transferred to the load. The interval t_2–t_3 can be given as follows:

$$t_3 - t_2 = t_{S2(\mathrm{off})} - (t_2 - t_1) - (t_8 - t_7) \quad (6)$$

where $t_{S2(\mathrm{off})}$ is the turn-OFF time of switch S_2.

In this mode, the input current i_{in} and diode *D* current i_D are equal and are given by

$$i_{in}(t-t_2) = i_D(t-t_2) = I_{in}/(n+1). \quad (7)$$

Mode 3. [$t_3 - t_4$, Fig. 3*c*]: To simplify the equation, leakage inductance L_{Lk} during this mode can be omitted. At t_3 switch S_2 is turned ON at zero current. During this mode the input current $i_{\mathrm{in}}(t_1)$ and resonant inductor current i_{S2} increase linearly, the diode current i_D decreases to zero. At t_4 diode *D* is turned OFF at zero current; the slope of current i_D is limited by the resonant inductance L_r. The interval t_3–t_4 is given by

$$t_4 - t_3 = \frac{I_{in}L_r}{v_{Cr}(t_3)}. \quad (8)$$

Mode 4. [$t_4 - t_5$, Fig. 3*d*]: In this mode, capacitor C_r and inductor L_r resonate for a half of the period, switch S_1 is turned-ON. Diode *D* is reverse biased. The energy from the output capacitor is transferred to the load.

Switch S_2 stays ON; the energy from the source is accumulated in the tapped inductor. The input current is equal to I_{in}. The interval t_4–t_5 is given by

$$t_5 - t_4 = \pi/\omega_2 \quad (9)$$

where $\omega_2 = 1/(L_rC_r)^{1/2}$.

During this mode, the voltage on capacitor C_r inverts its sign and can be given as

$$v_{Cr}(t_5) = \frac{-V_o - nV_{\mathrm{in}}}{n+1} + Z_1 I_{\mathrm{in}}. \quad (10)$$

Mode 5. [t_5–t_6, Fig. 3*e*]: This mode begins when the current in switch S_1 is equal to zero. During this interval, switch S_2 stays ON; energy from the source V_{in} is accumulated in the tapped

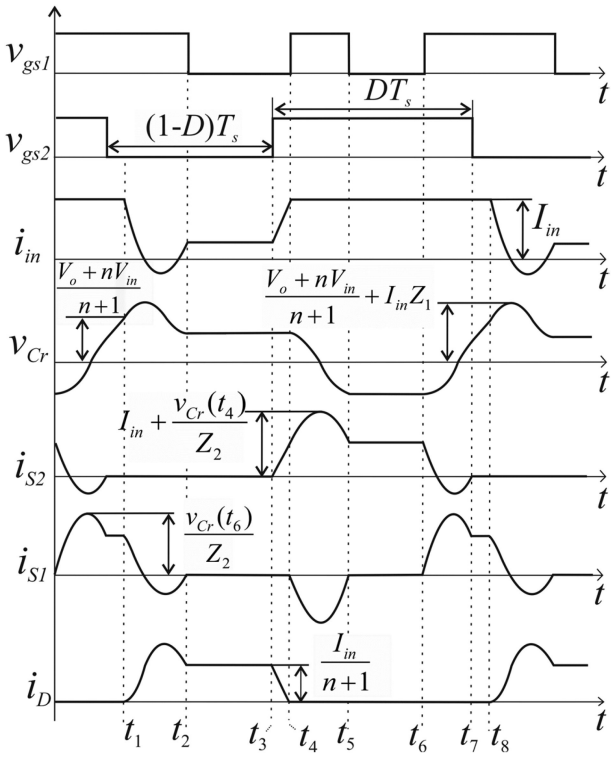

Fig. 2. Key waveforms of the proposed converter.

inductor. Energy from output capacitor C is transferred to the load. The interval t_5–t_6 can be described by

$$t_6 - t_5 = t_{S2(on)} - (t_5 - t_3) - (t_7 - t_6) \tag{11}$$

where $t_{S2(\mathrm{on})}$ is the turn-ON time of switch S_2.

Mode 6. [$t_6 - t_7$, Fig. 3*f*]: At t_6 switch S_1 is turned ON at zero current. Capacitor C_r is charged and resonates with inductor L_r. The current in switch S_2 decreases. Mode 6 ends when (t–t_6) $\geq$ T_r/4 and the current in transistor S_2 is equal to zero. At time t_7 switch S_2 turns OFF at zero voltage and zero current. The current in inductor L_r and switch S_2 is given by

$$i_{Lr}(t - t_6) = I_{in} + \frac{v_{Cr}(t_6)}{Z_2}\sin(\omega_2(t - t_6)) \tag{12}$$

where $Z_2 = (L_r/C_r)^{1/2}$.

Considering formula (12) and the waveforms in Fig. 2, the interval can be expressed as

$$t_7 - t_6 = \left(\pi + \arcsin\left(I_{in}\frac{Z_2}{v_{Cr}(t_6)}\right)\right)\frac{1}{\omega_2} \tag{13}$$

$$v_{Cr}(t_7) = v_{Cr}(t_6)\cos(\omega_2(t_7 - t_6)). \tag{14}$$

Achieving turn-OFF of S_2 at ZVZC requires a larger resonant current to flow through inductor L_r and capacitor C_r than the current I_{in}. For this purpose, the following inequality must be satisfied:

$$I_{in} \leq \frac{Z_1}{Z_2}\left(\frac{V_o + nV_{in}}{Z_1(n+1)} - I_{in}\right). \tag{15}$$

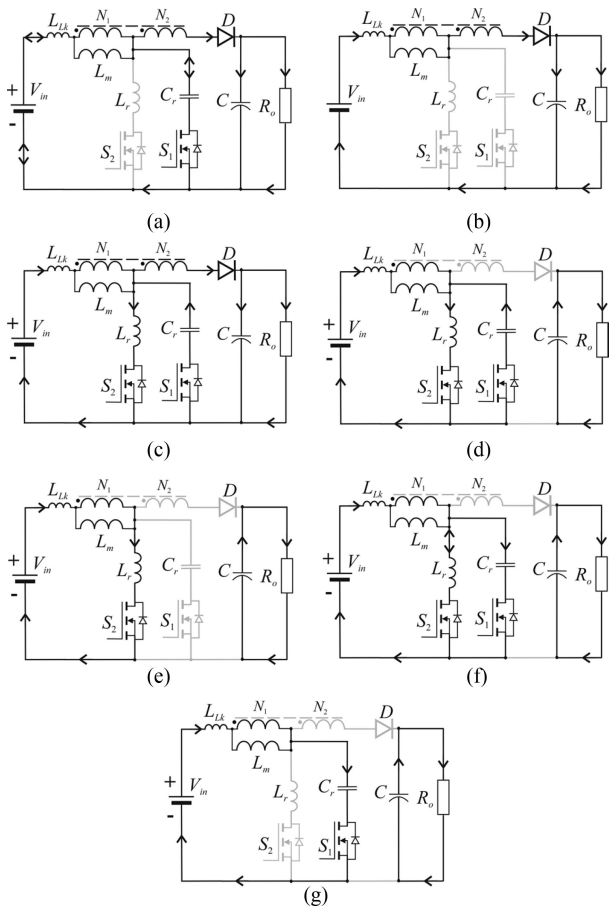

Fig. 3. Operation modes of the proposed converter.

Mode 7. [$t_7 - t_8$, Fig. 3*g*]: In this mode, capacitor C_r is charged with a constant current to a voltage level at which the diode is forward biased. This interval can be given as

$$t_8 - t_7 = \frac{v_{Cr}(t_1) - v_{Cr}(t_7)}{I_{in}}C_r. \tag{16}$$

III. Voltage Gain

Considering the shape of the waveforms given in Fig. 2 and using formulae (1)–(20), the average input current $I_{in(\mathrm{av})}$ and output current I_o can be obtained by (17), (18). The voltage gain of the converter can be determined by comparing its output and input power in accordance with the following:

$$I_{in(\mathrm{av})} \approx I_{in}\frac{nD+1}{n+1} \tag{17}$$

$$I_o \approx I_{in}\frac{1-D}{n+1} \tag{18}$$

$$V_{in}I_{in(\mathrm{av})} = V_oI_o \Rightarrow G_V \approx \frac{nD+1}{1-D} \tag{19}$$

where $D = t_{S2(on)}/T_S$, and T_S is the switching period.

Control characteristics for different turns ratios of the tapped inductor are presented in Fig. 4.

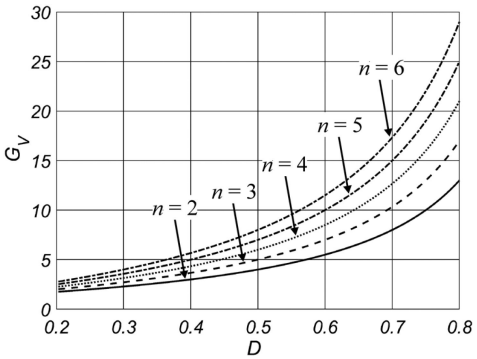

Fig. 4. Voltage gain of the converter.

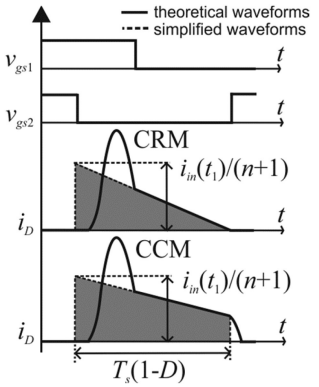

Fig. 5. Theoretical and simplified waveforms of output diode *D* in CRM and CCM.

IV. Critical and Continuous Conduction Mode

The analysis of the converter in (1)–(16) assumed constant currents in the magnetizing inductance. In a real circuit these currents are variable. Although their ripples have only a small effect on the voltage gain formula (19), they have an impact on the ZVZC turn-OFF of switch S_2. The obtaining of soft switching depends on the conduction mode.

A. Critical Conduction Mode

Critical conduction mode (CRM) requires transistor switching at a fixed frequency. That frequency can be calculated by determining the turn-OFF time of switch S_2 needed for the inductor current to decrease to zero. In this case, the resonance between leakage inductance L_{Lk} and capacitor C_r during mode 1 can be omitted. The resulting waveforms are shown in Fig. 5. The maximum diode current i_D in CRM is given by

$$i_{D(CRM)}(t_1) = \frac{i_{in(CRM)}(t_1)}{n+1} = \frac{(V_o - V_{in})(1-D)T_S}{2L_m(n+1)^2} \tag{20}$$

where $L_m(n+1)^2$ is the equivalent inductance of the series connected windings of the tapped inductor.

Considering the formulas (18), (20), and $I_o = V_o/R_o$, the frequency in CRM is given by

$$f_{s(CRM)} = \frac{R_o(G_V - 1)}{2L_m G_V (G_V + n)^2}. \tag{21}$$

In CRM, the inequality in (15) must be changed to ensure ZVZCS of switch S_2. For $f_r >> f_s$ it can be assumed that $i_{in}(t_6) = i_{in}(t_7) = i_{in}(t_1)$. In this case, to achieve ZVZCS of switch S_2 in CRM, the current $i_{in}(t_1)$ should be multiplied by 2. The two inequalities given below should be satisfied

$$2i_{in(CRM)}(t_1) = \frac{V_o + nV_{in}}{(n+1)Z_2} - \frac{2i_{in(CRM)}(t_1)Z_1}{Z_2} \tag{22}$$

$$Z_2 \le \frac{R_o}{2G_V(n+1)} - Z_1. \tag{23}$$

B. Continuous Conduction Mode

In continuous conduction mode (CCM), the switching frequency f_s is higher than the frequency in CRM (21).To calculate the current i_D in CCM, the resonance between C_r and L_{Lk} can be omitted. Both simplified and theoretical waveforms are presented in Fig. 5. The maximum current of diode *D* in CCM is given by

$$i_{D(CCM)}(t_1) = \frac{i_{in(CCM)}(t_1)}{n+1} = \frac{I_o}{1-D} + \frac{(V_o - V_{in})(1-D)T_S}{2L_m(n+1)^2}. \tag{24}$$

To ensure ZVZCS of switch S_2, inequality (15) must be satisfied. For $f_r >> f_s$, $i_{in}(t_6) = i_{in}(t_7) = i_{in}(t_1)$ can be assumed. In this case, using (24), the switching frequency f_s is given by

$$f_{s(CCM)} \ge \frac{R_o(G_V - 1)((n+1)(Z_1 + Z_2))}{2L_m G_V (G_V + n)^2 (R_o/G_V - (n+1)(Z_1 + Z_2))}. \tag{25}$$

V. Voltage and Currentstress of Power Devices

For the proposed converter, the maximum voltage v_{ds} on transistor S_1 occurs in mode 2 or 5. In mode 2, the voltage on the switch can be calculated as follows:

$$V_{ds1(\max)}(t - t_2) = Z_1 i_{in(\mathrm{CCM})}(t_1). \tag{26}$$

In mode 5 the maximum voltage on switch S_2 and capacitor C_r is given by

$$V_{ds1(\max)}(t - t_5) = (V_o + nV_{in})/(n+1) - Z_1 i_{in(CCM)}(t_1) \tag{27}$$

$$i_{in(CCM)}(t_1) = I_o \left(n + G_V + \frac{R_o(G_V - 1)}{2L_m f_s G_V (n + G_V)} \right). \tag{28}$$

The maximum voltage on switch S_2 occurs in mode 5 and is equal to the maximum voltage on capacitor C_r. The voltage is given by

$$V_{ds2(\max)} = (V_o + nV_{in})/(n+1) + Z_1 i_{in(CCM)}(t_1). \tag{29}$$

The maximum voltage on diode *D* occurs in mode 5 and is given by

$$V_{D(\max)}(t - t_5) = V_o + n(V_{in} + i_{in(CCM)}(t_1)Z_1). \tag{30}$$

To calculate the conduction losses in the converter's components, a minimum switching frequency was assumed (25), in addition to $i_{in}(t_6) = i_{in}(t_7) = i_{in}(t_1) = v_{Cr}(t_6) / Z_2$ and $i_{in}(t_3) = i_{in}(t_4) = i_{in}(t_5)$ Equations (31)–(35) are shown at the bottom of this page, where $L_{Lk} = 640$ nH, $D = 0.6$, $n = 4$.

To simplified rms current descriptions was defined parameter A (36). The values of rms currents in the power components are given by (31)–(34)

$$A = \frac{(Z_1 + Z_2)(G_V - 1)(n+1)}{L_m f_s (n + G_V)^2}. \tag{36}$$

The average current in diode D is equal to the output current I_o.

VI. Control Strategy

On the basis on key waveforms (see Fig. 2) and formulas (31)–(34) to obtain the possibly the highest efficiency, switch S_2 should be switching as low as possible frequency to maintain low proportion f_s/f_{r1} and f_s/f_{r2}. On the other hand, to achieve soft switching in CMM inequality (25) must be satisfied. Therefore, transistor S2 should be switching as the lowest frequency given by inequality (25). Fig. 6 shows relations between minimum output resistance and switching frequency. Characteristics were calculated for $L\mathrm{m} = 16$ uH, $N = 4$, $L_\mathrm{r} = 900$ nH, $C_\mathrm{r} = 240$ nF, and $L_\mathrm{Lk} = 630$ nH. According to example characteristics, increasing frequency above 100 kHz have small affect for minimum output resistance.

Switch S_1 is turned ON at the time t_6 to decrease switch S_2 current i_{Lr}, which enables it turning off at zero current. Switch S_1 should be turned off at the time t_2. Turn-ON time of switch S_1 is given by

$$t_{S1(on)} = (t_2 - t_1) + (t_8 - t_6). \tag{37}$$

Furthermore, switch S_1 could by also turn-ON in the interval t_4–t_5, this eliminate conduction of body diode and reduce conduction losses.

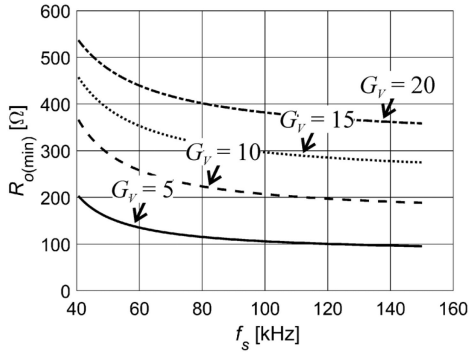

Fig. 6. Switching frequency variations of the proposed converter.

VII. Simulation Tests

Simulation tests were carried out to confirm the validity of the mathematical analysis of the converter and determine the parameters. During the simulation, zero voltage drops on semiconductor devices were neglected. Parasitic parameters of the converter, except for the leakage inductance, were omitted. Switching periods of semiconductor power components were considered negligible. The following parameters of the converter were assumed for the simulation: input voltage $V_{in} = 40$ V, output voltage $V_o = 380$ V, maximum switching frequency $f_s = 50$ kHz, resonant frequency $f_{r1} = 330$ kHz, efficiency $\eta = 1$, and output resistance $R_o = 110\ \Omega$.

The design of the simulation model requires the correct selection of its components, as described in the following.

1) Tapped inductor: the turns ratio of the tapped inductor should ensure the required voltage gain in a reasonable range of the duty cycle (the maximum duty cycle was $D \approx 0.6$). According to (19), the turns ratio n of the tapped inductor is equal to 4. Another important value of the tapped inductor is inductance; its current ripple has an influence on the turn-OFF of switch S_2 at ZVZC. Moreover, the greater the inductance

$$I_{S1(rms)} = \frac{I_o R_o (n + G_V)}{G_V (n+1)(Z_1 + Z_2)} \sqrt{\frac{Z_1 + Z_2}{2\pi Z_1} \frac{f_s}{f_{r2}} + \frac{1}{8}\left(3\frac{f_s}{f_{r1}} + 7\frac{f_s}{f_{r2}}\right)} \tag{31}$$

$$I_{S2(rms)} = \frac{I_o R_o (n + G_V)}{G_V (n+1)(Z_1 + Z_2)} \sqrt{\frac{f_s}{f_{r2}}\left(\frac{3}{8} - \frac{(1-A)^3 + 6A - 3}{3\pi}\right) + \frac{G_V - 1}{n + G_V}\left(\frac{A^2}{3} - A + 1\right)} \tag{32}$$

$$I_{in(rms)} = \frac{I_o R_o (n + G_V)}{G_V (Z_1 + Z_2)(n+1)^2} \times \sqrt{\frac{f_s}{f_{r1}}\left(\frac{3n^2}{8} + \frac{3}{4} - \frac{n}{\pi}\right) + \left(\frac{A^2}{3} - A + 1\right)\left(n(n+2)\left(\frac{1}{2\pi}\left(\frac{f_s}{f_{r1}} + \frac{f_s}{f_{r2}}\right) + \frac{G_V - 1}{n + G_V}\right) - \frac{3}{4}\frac{f_s}{f_{r1}} + 1\right)} \tag{33}$$

$$I_{D(rms)} = \frac{I_o R_o (n + G_V)}{G_V (Z_1 + Z_2)(n+1)^2} \sqrt{\frac{f_s}{f_{r1}}\left(\frac{9}{8} - \frac{1}{\pi}\right) + \left(\frac{A^2}{3} - A + 1\right)\left(\frac{n+1}{n + G_V} - \frac{1}{2\pi}\left(\frac{f_s}{f_{r1}} + \frac{f_s}{f_{r2}}\right) - \frac{3}{4}\frac{f_s}{f_{r1}}\right)} \tag{34}$$

$$L_r = \left[\frac{1}{2(n+1)}\left(\sqrt{\frac{4L_m f_s R_o (n+1)(G_V + n)^2}{\pi f_{r1}(R_o(G_V - 1) + 2L_m f_s G_V (G_V + n)^2)} + n^2 L_{Lk}} - n\sqrt{L_{Lk}}\right)\right]^2 \approx 420\ n\mathrm{H} \tag{35}$$

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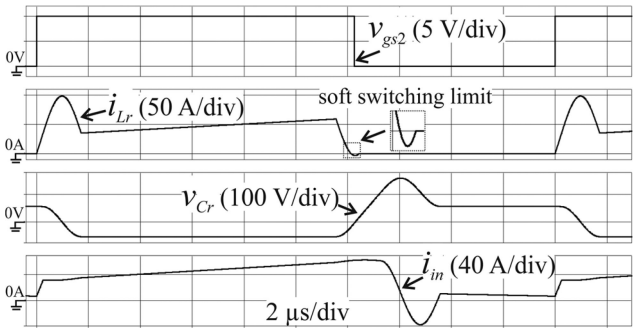

Fig. 7. Simulation waveforms.

of the tapped inductor, the greater the leakage inductance L_{Lk}. Consequently, it is more difficult to obtain turn-OFF of transistor S_2 at zero current (15). Using the simplified current waveform in Fig. 5, and assuming that the minimum current ripple Δi_{Lm} is 50% in the magnetizing inductance at maximum output power, the inductance L_m can be calculated as follows:

$$\Delta i_{in} = \frac{(V_o - V_{in})(1-D)T_S}{L_m(n+1)i_{in(CCM)}(t_1)} = 0.5 \tag{38}$$

$$L_m = \frac{R_o(2-\Delta i_{Lm})(G_V-1)}{G_V(G_V+n)^2 f_s} \approx 16\mu\text{H}. \tag{39}$$

2) Resonant components L_r and C_r: two constraints determine the resonant components—the resonant frequency and resonant impedance, appropriate to ensure turn-OFF of switch S_2 at ZVZC. In CCM the values of resonant components C_r, L_r can be obtained by transforming inequality (25). Resonant inductance L_r and resonant capacitance C_r are given by (35) and (40). Fig. 7 shows the waveforms of selected converter voltages and currents obtained as a result of simulation tests carried out in PSpice for the maximum output power.

$$C_r = \frac{1}{4\pi^2 f_{r1}^2 L_r} \approx 580 \text{ nF} \tag{40}$$

where $f_r = 1/(2\pi(L_rC_r)^{1/2}) = 330$ kHz.

According to the assumptions and inequalities (20) and (25), at the maximum output power during turn-OFF of switch S_2, the sum of the input current i_{in} and the current generated by the resonance of capacitor C_r and inductor L_r is close to zero and is equal to the current of switch S_2. This means that at this value of frequency and voltage gain the converter operates with the highest possible output power at which transistor S_2 remains softly switched OFF.

VIII. Experimental Tests

Experimental tests of the converter were carried out. The converter's resonant components and the magnetizing inductance of the tapped inductor were selected in accordance with (35), (38)–(40) for $\Delta i_{in} = 0.5$, $N = 4.5$, $G_V = 7.6$, $f_{r1} = 340$ kHz, $f_s = 100$ kHz, $P_{out} = 750$ W, and measured leakage inductance $L_{Lk} = 630$ nH. Table I gives the values of the converter's components and parameters. During testing, the transistors were switched by a Cyclon II FPGA module in an open-loop system. The laboratory model of the proposed converter is shown in

TABLE I
List of Power Components and Parameters of the Laboratory Model of the Converter

Parameter	Value/part number
input voltage V_{in}	(30–50) V
output voltage V_o	380 V
switching frequency f_s	(45–100) kHz
resonant frequency f_r	340 kHz
magnetizing inductance L_m	16.8 µH
turns ratio n ($N_2 : N_1$)	63:14
leakage inductance L_{Lk}	630nH
resonant capacitor C_r	240 nF (ceramic COG)
resonant inductor L_r	900nH
output capacitor C	2.2 µF
diode D	C4D05120A (V_{RRM} = 1.2 kV)
transistor S_1	IRFP4468 (V_{DSS} = 100 V)
transistor S_2	IRFP4668 (V_{DSS} = 200 V)

Fig. 9. Arnold Magnetic core was used to build tapped (MS-250026) and resonant (MS-150026) inductors. Table II gives the values of power dissipation, voltage and current ratings of the converter's components. Power losses in the cores were estimated using Oliver's equation (41). To reduce voltage spikes after turn-OFF transistors, parallel with each transistor were added RC snubber circuits ($R = 22\ \Omega$, $C = 1$ nF), power losses in snubbers were estimated by (42), (43)

$$P_{\text{CORE}} = V_e \times \left(\frac{f_s}{a/\Delta B^3 + b/\Delta B^{2.3} + c/\Delta B^{1.65}} + d{f_s}^2 \Delta B^2 \right) \tag{41}$$

$$P_{\text{SNUB1}} = f_s C_{\text{SNUB1}} (V_{ds1(\max)}(t-t_2)^2 + V_{ds1(\max)}(t-t_5)^2) \tag{42}$$

$$P_{\text{SNUB2}} = f_s C_{\text{SNUB2}} {V_{ds2(\max)}}^2 \tag{43}$$

where P_{CORE} depicts the power losses in core by hysteresis and eddy-current in mW, V_e—-effective core volume in cm^3, f is the frequency in Hz, $a = 10^6$, $b \approx 5{\cdot}10^8$, $c \approx 4{\cdot}10^6$, $d \approx 2.9{\cdot}10^{-14}$ denote the material parameters (the cores of resonant and tapped inductors are made with the same material), ΔB is the ac flux density in 100 μT, P_{SNUB1} and P_{SNUB2} are the estimated power losses in RC snubbers, and C_{SNUB1} and C_{SNUB2} are the snubbers, capacitance.

Conduction losses in the converter's semiconductors, the resonant components and the windings of the inductors can be calculated by following equations:

$$P_{S1} = {I_{S1(rms)}}^2 R_{ds1(on)} \tag{44}$$

$$P_{S2} = {I_{S2(rms)}}^2 R_{ds2(on)} \tag{45}$$

$$P_D = I_o V_{TO} + {I_{D(rms)}}^2 R_D \tag{46}$$

$$P_{\text{WIRE}(T)} = {I_{in(rms)}}^2 R_{PW} + {I_{D(rms)}}^2 R_{SW} \tag{47}$$

$$P_{\text{WIRE}(R)} = {I_{S2(rms)}}^2 R_{Lr} \tag{48}$$

$$P_{\text{CAP}} = {I_{S1(rms)}}^2 \frac{D.F.}{2\pi f_{r1} C_r} \tag{49}$$

TABLE II
VOLTAGE RATINGS AND MAXIMUM POWER DISSIPATIONS IN CONVERTER COMPONENTS

Parameter	Switch S_1	Switch S_2	Diode D	Tapped inductor	Resonant inductor L_r	Resonant capacitor C_r	RC snubbers
Voltage rating	$V_{ds1(\max)}$ = 68 V	$V_{ds2(\max)}$ = 152 V	$V_{D(\max)}$ = 978 V	-	-	$V_{Cr(\max)}$ = 152 V	-
Rms current	$I_{S1(\mathrm{rms})}$ = 21.7 A	$I_{S2(\mathrm{rms})}$ = 22.3 A	$I_{D(\mathrm{rms})}$ = 4 A	$I_{\mathrm{in(rms)}}$ = 22 A $I_{D(\mathrm{rms})}$ = 4 A	$I_{Lr(\mathrm{rms})}$ = 22.3 A	$I_{Cr(\mathrm{rms})}$ = 21.7 A	-
Average current	-	-	I_o = 2 A	-	-	-	-
Forward voltage	-	-	V_{TO} = 0.92 V*	-	-	-	-
Resistance	$R_{ds1(\mathrm{on})}$ = 2 mΩ	$R_{ds2(\mathrm{on})}$ = 8 mΩ	R_D = 101 mΩ*	R_{PW} = 6 mΩ R_{SW} = 75 mΩ	R_{Lr} = 1 mΩ	ESR= 0.4 mΩ	-
AC flux density ΔB	-	-	-	$\Delta B_{(T)}$ = 260 mT	$\Delta B_{(R)}$ = 510 mT	-	-
Conduction losses	P_{S1} = 0.9 W	P_{S2} = 4 W	P_D = 3.5 W	$P_{WIRE(T)}$ = 4.1 W	$P_{WIRE(R)}$ = 0.5 W	P_{Cr} = 0.2 W	P_{SNUB} = 2.9 W
Core losses	-	-	-	$P_{CORE(T)}$ = 4.2 W	$P_{CORE(R)}$ = 3.2 W	-	-

* calculated for 25 °C; total losses = 23.5 W.

where P_{S1} and P_{S2} are conduction losses in switches S_1 and S_2, $R_{ds1(\mathrm{on})}$ and $R_{ds2(\mathrm{on})}$ are switches S_1 and S_2 drain-source ON resistance, P_{D} is conduction losses in diode D, V_{TO} is the threshold voltage of diode D, R_D is the series resistance of diode D, $P_{\mathrm{WIRE}(T)}$ and $P_{\mathrm{WIRE}(R)}$ are conduction losses in windings of the tapped and resonant inductors, respectively, R_{PW} is the primary windings resistance, R_{SW} is the secondary windings resistance, R_{Lr} is resonant inductor resistance, P_{CAP} is conduction losses in resonant capacitor estimated for resonant frequency, $D.F.$ is the dissipation factor ($D.F. = 0.2\%$ for ceramic COG capacitors).

Table II gives maximum voltage ratings, currents and conduction losses calculated for the components of built laboratory model.

Values were obtained according with (26)–(49) at the maximum output power of the converter ($f_{\mathrm{s}} = 100$ kHz, $G_V = 7.6$, $R_o = 192\,\Omega$, $V_o = 380$ V). The highest power losses were calculated for the tapped inductor ($P_{\mathrm{WIRE}(T)} + P_{\mathrm{CORE}>(T)} = 8.3$ W). In switch S_2, the calculated power losses $P_{S2} = 4$ W were higher than in switch S_1; this is due to the higher $R_{ds(\mathrm{on})}$ resistance in switch S_2 than in switch S_1. Fig. 8 shows experimental waveforms of the proposed converter for three tested input voltages $V_{in} = 30$, 40, and 50 V, and three output powers $P_{out} = 150$, 380, and 750 W, waveforms were measured by digital oscilloscope Tektronix DPO5034. The experimental waveforms are convergent with the theoretical waveforms shown in Fig. 2. Drain-source voltages on transistors are shown in Fig. 8(a)–(f), voltages on output diode are shown in Fig. 8g-i. The voltage spikes across switches are caused by leakage inductance and parasitic capacitances of all switches, spikes across transistors were significantly suppressed by RC snubbers. The soft switching of the transistors is shown in Fig. 8(m)–(q). Turn-ON of switches S_1 and S_2 were achieved at zero current (see Fig. 8 (m), (o), (p)), and turn-OFF at zero current and zero voltage (see Fig. 8 n, o, q). To ensure ZVZC turn-OFF, the transistors must be turned OFF when their current starts to flow in the opposite direction. In the case when the switches are turned OFF, the current starts to flow through their forward biased body diodes. Fig. 10 shows comparison between efficiency obtained by the laboratory model and efficiency obtained by using (31)–(49) in accordance with the following:

$$P_{\mathrm{loss}} = P_{S1} + P_{S2} + P_D + P_{WIRE(T)} + P_{CORE(T)} + P_{\mathrm{WIRE}</\mathrm{rm}>(\mathrm{R})} + P_{CORE(R)} + P_{Cr} + P_{SNUB} \quad (50)$$

$$\eta = \frac{P_{\mathrm{out}} \cdot 100\%}{P_{\mathrm{out}} + P_{\mathrm{loss}}}. \quad (51)$$

Efficiency were measured by power analyser HIOKI 3390. There is slight difference between measured and theoretical efficiency. According to inequality (25) and Fig. 6, the maximum voltage gain G_V that can be obtained is limited by load resistance. Fig. 11 shows switching frequency comparison between frequency measured in CCM mode and theoretical. Theoretical frequency was calculated accordance with (25) and with divided voltage gain GV by assumed efficiency $\eta = 95\%$.

For $V_{in} = 30$ V and 12.7 voltage gain, the maximum output power was 500 W, for $V_{in} = 40$ V and $G_V = 9.5$ the maximum output power was 620 W, for $V_{in} = 50$ V and $G_V = 7.6$ the maximum output power was 750 W. The maximum measured efficiency 96.6% was obtained at 7.6 voltage gain and 620 W output power.

IX. PERFORMANCE COMPARISON

Table III shows a comparison of performance parameters between the proposed converter and other converters described in the literature. Fig. 12 shows comparison of voltage gain between proposed converter and other converters with resonant cell. The proposed converter uses a soft switching technique as in the basic ZCS-PWM boost converter [35] and a tapped inductor to increase voltage gain and reduce transistor voltage ratings. A tapped inductor and resonant cell are also used in [29]. However, in this converter voltage gain substantially depends on output resistance R_o and resonance impedance Z. Otherwise, in proposed converter voltage gain is much higher. Fig. 13 shows comparison of main transistor voltage stress between proposed converter and other converters with resonant cell. Voltage stress on main transistor of proposed converter were calculated for $L_m = 16\ \mu$H, $L_{Lk} = 630$ nH, $f_{\mathrm{s}} = 100$ kHz, $C_{\mathrm{r}} = 240$ nF, and $R_{\mathrm{o}} = 235\ \Omega$. In [35], maximum voltage on main transistor is similar to output voltage. In [29], due to resonance, maximum voltage on transistor depends on R_{o}/Z and for high output power could be higher than output voltage. In the proposed converter, maximum voltage on main switch is low despite the utilized soft switching technique.

It is found that only the proposed converter uses a coupled inductor and soft switching of transistors without loss of effective duty cycle as in an active clamp converter [16], [17] or

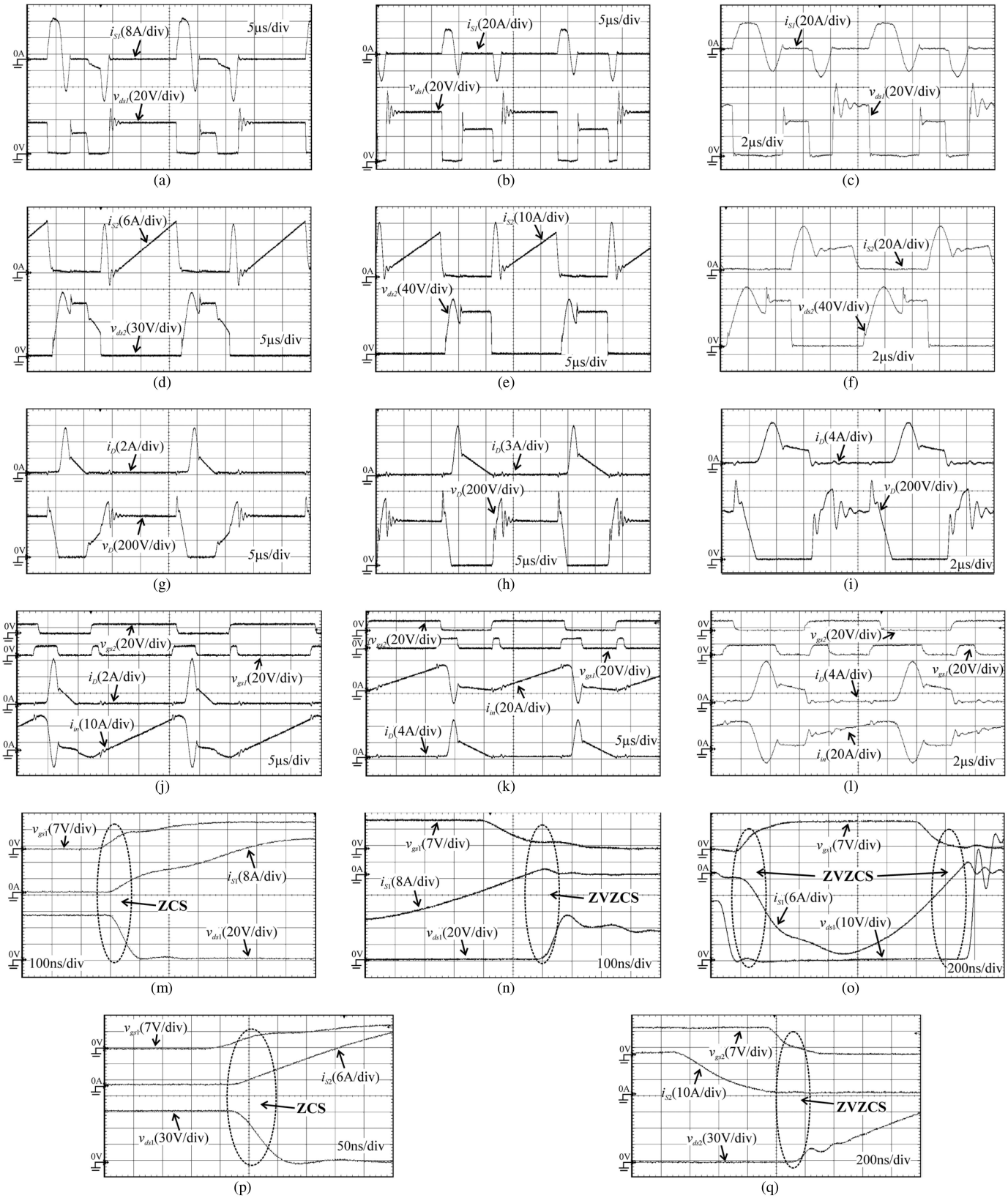

Fig. 8. Experimental results: v_{gs1} is the gate-source voltage on switch S_1, v_{gs2} is the gate-source voltage on switch S_2, v_{ds1} is the drain-source voltage on switch S_1, v_{ds2} is the drain-source voltage on switch S_2, v_d is the voltage on output diode D, i_{in} is the input current, i_{S1} is the current in switch S_1, i_{S2} is the current in switch S_2, i_D is the current in output diode D. (a), (d), (g), (j) are the waveforms at $P_{out} = 150$ W and $V_{\rm in} = 30$ V. (b), (e), (h), (k) are the waveforms at $P_{out} = 380$ W and $V_{in} = 40$ V. (c), (f), (i), (l) are the waveforms at $P_{out} = 750$ W and $V_{in} = 50$ V. (m) turn-ON of switch S_1 at time t_6. (n) turn-OFF of switch S_1 at time t_2. (o) turn-ON and turn-OFF switch S_1 at times t_4 and t_5. (p) turn-ON of switch S_2. (q) turn-OFF of switch S_2.

TABLE III
PERFORMANCE COMPARISON

Converter	Basic boost converter	Converter in [10]	Converter in [14]	Converter in [16]	Converter in [28]	Converter in [29]	Converter in [35]	Proposed converter	Optional converter
Active switches	1	1	1	2	2	1	2	2	2
Diodes	1	2	3	1	2	1	1	1	2
Voltage gain	$\frac{1}{1-D}$	$\frac{nD+1}{1-D}$	$\frac{n+2}{1-D}$	$>>\frac{nD+1}{1-D}$	$\frac{n+2}{1-D}$	$f\left(\frac{Q,n,}{f_s/f_r}\right)$	$\frac{1}{1-D}$	$\frac{nD+1}{1-D}$	$\frac{n+1}{1-D}$
Voltage stress of main active switch	V_{out}	$\frac{V_{out}}{nD}$	$\frac{V_{out}}{n+2}$	$\frac{V_{out}}{nD+1}$	$\frac{V_{out}}{n+2}$	$f\left(\frac{Q,n,}{f_s/f_r}\right)$	V_{out}	$\frac{V_{out}}{nD+1}+Z_1I_{in}$	$\frac{V_{out}}{n+1}+Z_1I_{in}$
Voltage stress of output diode	V_{out}	$\frac{nV_{out}}{nD+1}$	V_{out}	$V_{out}+nV_{in}$	$\frac{V_{out}(n+1)}{n+2}$	$f\left(\frac{Q,n,}{f_s/f_r}\right)$	$2V_{out}$	$V_{out}+nV_{in}$ $+(n+1)Z_1I_{in}$	$V_{out}+Z_1I_{in}$
Reverse recovery problem	serious	medium	medium	small	small	small	medium	small	small
Conduction losses	large	medium	small	medium	small	large	large	medium	small
Boost technique	SI*	CI**	CI with SC***	CI	CI with SC	CI	SI	CI	CI with SC
Turn-on condition of main active switch	hard	ZCS	ZCS	ZVS	ZVS	ZVS	ZCS	ZCS	ZCS
Turn-off condition of main active switch	hard	hard	hard	ZVS	hard	ZVS	ZVZCS	ZVZCS	ZVZCS

*SI- single inductor, **CI – coupled inductor, ***SC – switched capacitor.

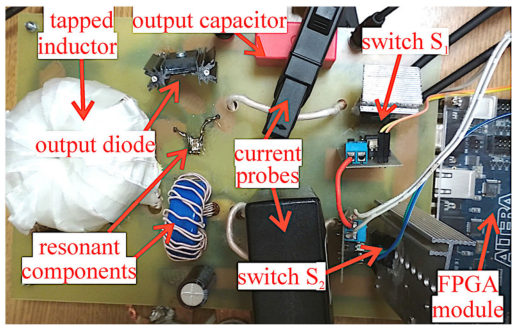

Fig. 9. Laboratory model of proposed converter.

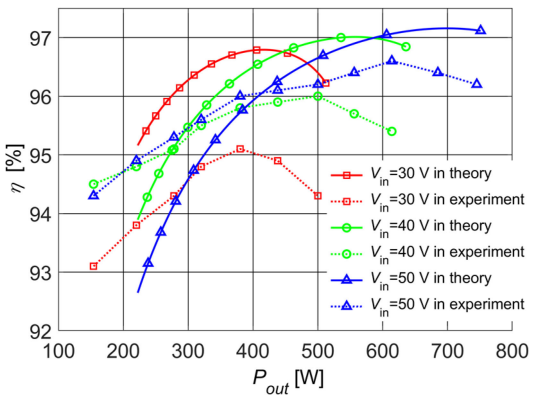

Fig. 10. Conversion efficiency for $V_o = 380$ V.

quasi-resonant ZVS boost converter with tapped inductor [29]. An AERC may be used in a converter with coupled inductor and switched capacitor (see Fig. 14). This improves voltage gain and reduces the voltage ratings of all switches.

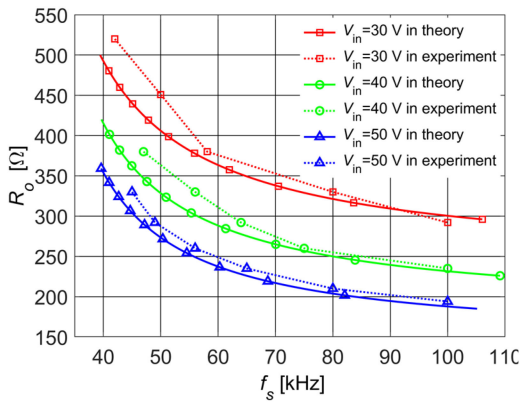

Fig. 11. Switching frequency comparison of experiment with theory.

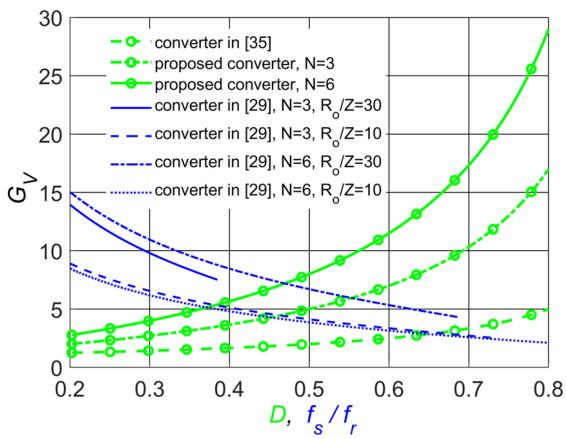

Fig. 12. Voltage gain comparison of the proposed converter with [29] and [35].

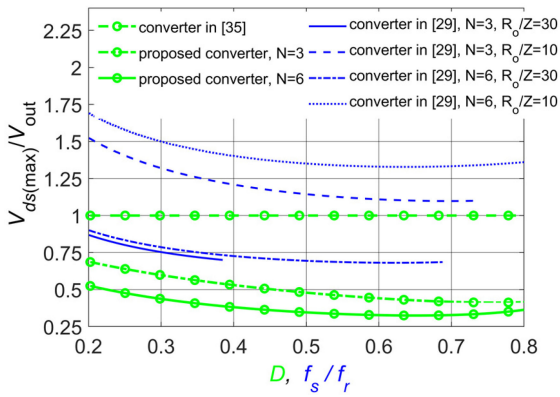

Fig. 13. Main transistor voltage stress comparison of the proposed converter with [29] and [35].

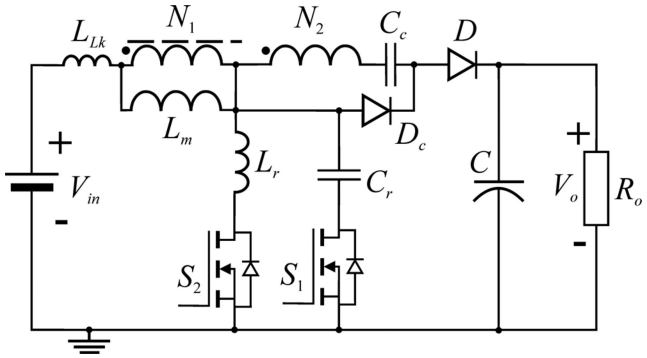

Fig. 14. Optional converter.

X. Conclusion

This article presents a ZCS boost converter with tapped inductor and active edge-resonant cell for low-voltage, high-current applications. By using resonant circuit, the transistors are turning ON at zero current and turning OFF at zero current and zero voltage. With this topology, the voltage overshoot problem related to the negative effect of leakage inductance was eliminated. Owing to a simple structure using a tapped inductor, it was possible to use switches with a lower voltage rating and low $R_{ds(\mathrm{on})}$. As a result, conduction losses decreased. Two modes of operation were examined: CRM and CCM. An optimal selection of the resonant tank components made it possible to achieve soft switching over the entire output power range and to minimize resonance losses. A laboratory model of the converter, with a rated power of 750 W, was built and tested. High efficiency and high voltage gain were achieved. The maximum measured efficiency was 96.6% and the maximum voltage gain was over 12.

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Michał Harasimczuk was born in Białystok, Poland. He received the M.Sc. and Ph.D. degrees in electrical engineering from the Bialystok University of Technology, Bialystok, Poland, in 2013 and 2019, respectively.

He is currently with the Faculty of Electrical Engineering, Bialystok University of Technology. His research interests include the power electronics, soft-switching power converters, and photovoltaic systems.