AC–AC Hybrid Boost Switched-Capacitor Converter

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***Abstract*—In this article, a hybrid boost switched-capacitor converter operating as an ac–ac solid-state autotransformer is presented. The topology integrates a basic inductive switching cell and a switched-capacitor ladder cell, performing a direct energy conversion with a high-gain output voltage. The theoretical analysis presents the main operational characteristics of the hybrid converter, including the voltage stresses across the devices, the equivalent average electric circuit model, and the calculation of current stresses considering the partial charging of the capacitors. A design methodology is described, focusing on the modulation technique and criteria for determining capacitors, semiconductor devices, inductor, and switching frequency. Validation was carried out based on simulation and experimental results obtained with a single-phase prototype with 55/220-V voltage conversion and 1-kVA rated power at 60 Hz. Additional tests verified the operation at different grid frequencies, loads (inductive and nonlinear), and with 14 different input–output connections.**

***Index Terms*—AC–AC hybrid boost converter, single-phase solid-state autotransformer, switched capacitor.**

I. Introduction

AUTOTRANSFORMERS have been applied for decades in residential and industrial systems as devices that adjust the voltage levels between the electric grid and equipment, when isolation is not required. These devices are usually bulky and are not able to supply all loads maintaining the energy quality. To address these issues, conventional autotransformers have been replaced by power converters, which are able to regulate output voltage/current, correct the power factor, and reduce harmonics effects.

The first ac–ac converters developed employed TRIACs, silicon controlled rectifiers, or thyristors, regulated the voltage and/or frequency, and operated with low switching frequency. Although these converters are applied in the industry, they present some limitations, which are as follows: voltage gain lower than unity, high input current total harmonic distortion, and output frequency lower than the input frequency [1].

Pulsewidth modulated ac–ac converters can overcome some of the aforementioned disadvantages. They switch at higher frequencies and are classified into two main categories [2]. The indirect converters perform an ac–dc–ac conversion and decouple the input and output voltage/current dynamics, being able to change both voltage/current levels and frequencies. However, two converters are needed, and the maintenance of a dc link requires either an energy storage element or a complex modulation technique and higher switch count. Direct ac–ac converters do not present a dc link and are usually smaller and lighter than the indirect converters. An example is the conventional matrix converter, which can vary the output frequency and voltage, at the cost of complex modulation and higher switch count [3]. Another category of direct converters is derived from the basic dc–dc topologies, such as buck and boost, and can be employed by modifying the switching realization [4], [5]. Their output and input frequencies are equal, and the peak/effective output voltage values can be controlled. These topologies usually require four-quadrant switches, which need special modulation to avoid commutation problems.

Switched-capacitor converters (SCCs) are well known in the field of low-voltage electronics, given their simplicity and high conversion rate [6]. Recently, these converters have been operated at higher voltage and power levels as alternatives for the ac–ac fixed frequency direct conversion. In general, they are almost absent of magnetic elements, provide high voltage gain, and equalize voltages across capacitors and switches. In contrast, pure SCCs usually operate in open loop, because the output voltage control is hard to achieve. The first topologies proposed were voltage doublers, and they were presented with [7] and without [8] differential connections. This concept was tested as a split-phase autotransformer [9], as part of an inverter [10] and further developed for more switched-capacitor cells [11], increasing the voltage conversion ratio. Other topologies are aimed at improving the efficiency for higher voltage gains [12]–[14]. Pure ac–ac SCCs have also been developed for three-phase systems [15], [16], presenting simplicity and good performance.

In order to achieve a controllable output voltage, hybrid converters have been presented [17], aggregating the characteristics of high voltage gain and sharing the voltage stresses of switched-capacitor cells in conventional topologies, such as boost and buck converters. As opposed to pure SCCs, hybrid converters can be controlled via duty cycle variations because of the presence of an inductive element. Some cells also operate as resonant converters [18], [19], and these have smaller inductances and operate with zero-current switching.

The hybrid boost switched-capacitor converter (HBSCC) has been employed in dc–dc [20], ac–dc [21], and dc–ac [22] systems. However, its use in ac–ac conversion has not previously been proposed, and there are some interesting challenges in this

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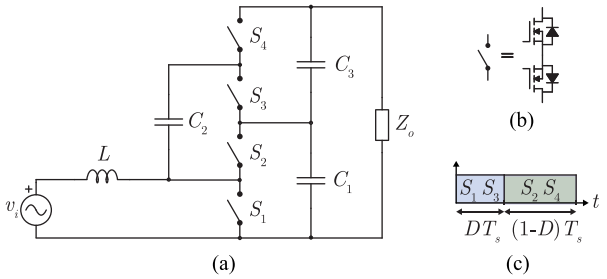

Fig. 1. Schematics showing (a) the proposed ac–ac HBSCC, (b) switch realization, and (c) modulation signals.

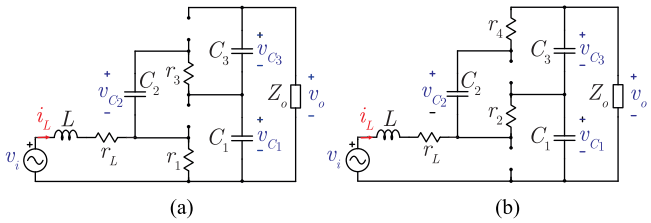

Fig. 2. Operating stages during a switching period. (a) First stage ($0 < t < DT_s$). (b) Second stage ($DT_s < t < T_s$).

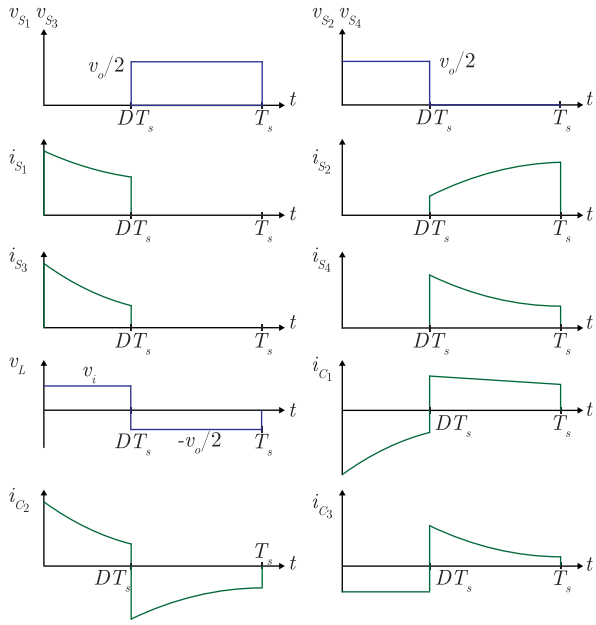

Fig. 3. Theoretical waveforms during a switching period for $v_o > 0$.

case that will be addressed herein. The topology provides a high voltage gain, and the output voltage follows the shape of the input voltage, maintaining the mains frequency.

The rest of this article is organized as follows. In Section II, the steady state is analyzed. Section III shows a design example, and Section IV presents the experimental results. In Section V, new derived topologies are presented. Finally, Section VI concludes this article.

II. Proposed Topology

The proposed topology is presented in Fig. 1(a). It combines a boost converter with a switched-capacitor cell. The structure is composed of an input inductor L, a switched-capacitor C_2, two output capacitors C_1 and C_3, and four switches S_1–S_4. As the converter operates with alternating voltages and currents, the switches must operate in all four quadrants. One possible switching realization is shown in Fig. 1(b), in which two MOSFETs are connected in an antiseries configuration.

The analysis of the operating stages during a switching period considers that the switching frequency f_s is much higher than the mains frequency f_g. In addition, an instant at which the input current and the output voltage are positive is considered. Following the command signals shown in Fig. 1(c), the converter presented in Fig. 1(a) operates in two topological stages (see Fig. 2), as described in the following.

1) *First operating stage ($0 < t < DT_s$) [see Fig. 2(a)]:* Switches S_1 and S_3 are turned ON, while S_2 and S_4 are turned OFF. The input inductor L stores energy and its current increases. Energy from capacitor C_1 is transferred to capacitor C_2, while capacitors C_3 and C_1 supply energy to the load Z_o.
2) *Second operating stage ($DT_s < t < T_s$) [see Fig. 2(b)]:* Switches S_2 and S_4 are turned ON, while S_1 and S_3 are turned OFF. The energy stored in inductor L is transferred to capacitor C_1. Capacitor C_3 is charged from C_2.

Theoretical waveforms during a switching period with a positive output voltage are shown in Fig. 3. It should be noted that the maximum blocking voltage of each switch is equal to half of the peak output voltage. Moreover, the current waveforms present exponential characteristics, as a result of the switched-capacitor ladder cell.

Waveforms in a grid period for a unity power factor load are shown in Fig. 4. It should be noted that the input current leads the input voltage, because of the reactive power related to the capacitors. Moreover, the input current does not present discontinuities; therefore, an input filter may not be necessary.

A. Modulation Technique

Direct ac–ac converters usually suffer from commutation problems, because there is no available path for the input current during the dead time, leading to overvoltage across the semiconductors. The proposed converter can be modulated by allowing one MOSFET of each switch to be turned ON during an output voltage half-cycle [23], in which it operates as a synchronous dc–dc topology. An equivalent circuit considering the inductor and capacitors as current and voltage sources, respectively, is shown in Fig. 5(a). The modulation technique employed, shown in Fig 5(b), is dependent on the measurement of the output voltage, which is already performed for the voltage regulation and thus requires no additional hardware cost. It generates the signal commands shown in Fig. 5(c), which leads to the drain–source voltages [see Fig. 5(d)].

The current path is shown in Fig. 6 for positive inductor current and capacitor voltages. The output voltage is applied either across the MOSFETs S_{2b} and S_{4b} or S_{1b} and S_{3b}.

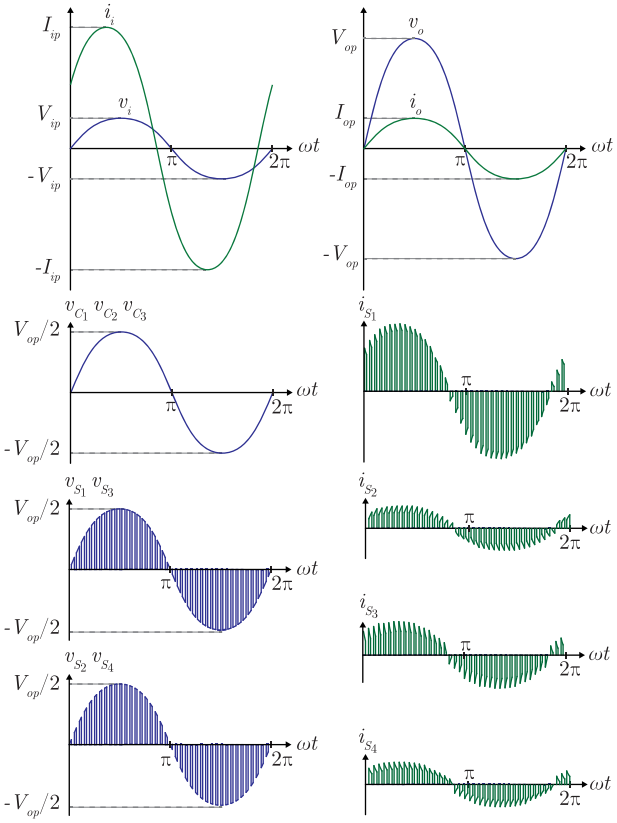

Fig. 4. Theoretical waveforms during a grid period for a resistive load.

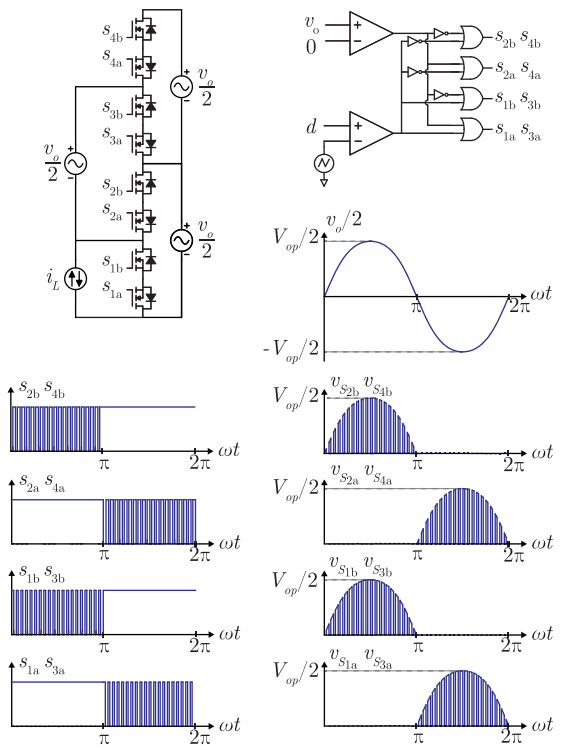

Fig. 5. Schematics showing (a) equivalent circuit considering inductor and capacitors as current and voltage sources, respectively, (b) modulation technique, (c) drive signals, and (d) capacitor and drain–source switch voltages.

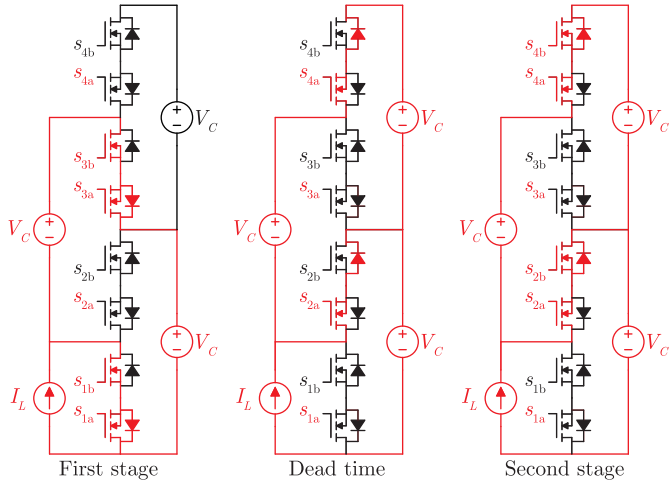

Fig. 6. Current path during each operating stage.

B. Ideal Analysis

The converter is analyzed based on Fig. 2, in which all of the conducting resistances are neglected. For the first operating stage [see Fig. 2(a)], the equations are

$$\begin{aligned} v_L &= v_i \\ v_{C_1} &= v_{C_2} \\ i_{C_1} + i_{C_2} &= -i_o \\ i_{C_3} &= -i_o \end{aligned} \tag{1}$$

and for the second operating stage [see Fig. 2(b)], we have

$$\begin{aligned} v_L &= v_i - v_{C_1} \\ v_{C_3} &= v_{C_2} \\ i_{C_1} &= i_L - i_o \\ i_{C_2} + i_{C_3} &= -i_o. \end{aligned} \tag{2}$$

If the capacitances are large enough, the voltages across the capacitors can be considered as constants during an operating stage. Thus, from (1) and (2), it is concluded that the averaged voltage values across the capacitors C_1, C_2, and C_3 are equal, i.e.,

$$\langle v_{C_1} \rangle = \langle v_{C_2} \rangle = \langle v_{C_3} \rangle = \frac{\langle v_o \rangle}{2}. \tag{3}$$

Considering that the first operating stage occurs during DT_s and the second stage during $(1-D)T_s$, the average voltage across the inductor L is given by

$$\langle v_L \rangle = \left\langle L \frac{di_L}{dt} \right\rangle = \langle v_i \rangle - (1-D)\frac{\langle v_o \rangle}{2}. \tag{4}$$

As the variables are ac, they are considered as phasors [24]. Because of the grid frequency voltage drop, the average value of the inductor voltage is not null during a switching period (only during a grid period) and is given by

$$\langle v_L \rangle = \left\langle L \frac{di_L}{dt} \right\rangle = L \frac{d}{dt} \langle i_L \rangle + j\omega L \langle i_L \rangle. \tag{5}$$

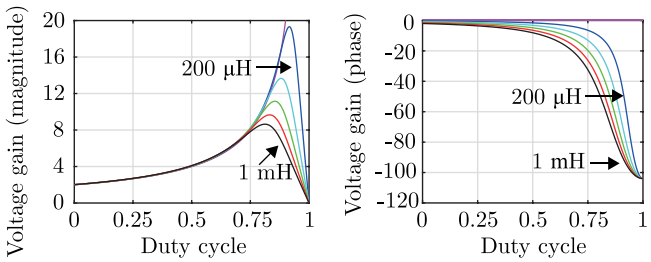

Fig. 7. Magnitude and phase of voltage gain for different duty cycles and input inductances.

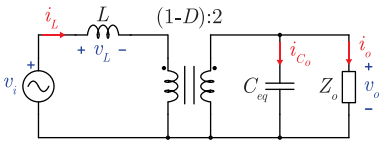

Fig. 8. Averaged equivalent electric circuit.

Substituting (5) into (4) and considering that the derivative of the average value of the inductor current is equal to zero, the output voltage in sinusoidal steady state is obtained as

$$\langle v_o \rangle = \frac{2}{1-D}\left(\langle v_i \rangle - j\omega L \langle i_L \rangle\right). \tag{6}$$

Capacitor equations are analyzed similarly to the inductor equations, leading to the input current

$$\langle i_L \rangle = \frac{2}{1-D}\langle i_o \rangle + j\frac{\omega(C_1+C_2+C_3)}{2(1-D)}\langle v_o \rangle. \tag{7}$$

Applying (7) in (6), the output voltage gain is obtained in terms of input voltage and output current as

$$\langle v_o \rangle = \frac{1}{1-\dfrac{\omega^2 L(C_1+C_2+C_3)}{(1-D)^2}}\left(\frac{2\langle v_i \rangle}{1-D} - \frac{4j\omega L\langle i_o \rangle}{(1-D)^2}\right). \tag{8}$$

If the load is an impedance $Z_o = R_o + jX_o$, i_o is substituted by v_o/Z_o and the voltage gain is given by

$$\frac{v_o}{v_i} = \frac{\frac{2}{1-D}}{1-\frac{\omega^2 L(C_1+C_2+C_3)}{(1-D)^2} + \frac{4\omega L X_o}{(1-D)^2|Z_o|^2} + j\frac{4\omega L R_o}{(1-D)^2|Z_o|^2}}. \tag{9}$$

Left and right subfigures of Fig. 7 show the magnitude and phase of the voltage gain, respectively, as a function of the duty cycle for different values of input inductance $L = 200, 400, 600, 800,$ and 1000 μH ($C_1, C_2, C_3 = 20$ μF, $Z_o = 80$ Ω, and $f_g = 60$ Hz). It can be observed that the voltage gain is similar to the double of a boost converter and is influenced by the input inductance only for duty cycle values above 0.75.

Equations (6) and (7) are used to generate an equivalent low-frequency model, as shown in Fig. 8 (herein, low frequency means grid frequency). The capacitance C_{eq} is given by $(C_1 + C_2 + C_3)/4$.

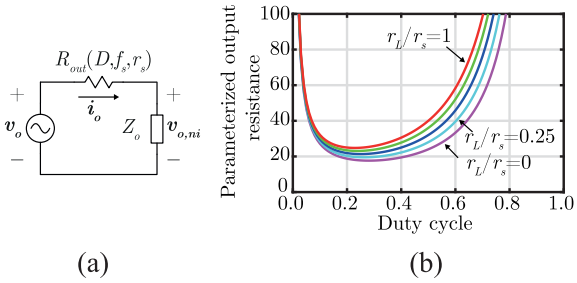

Fig. 9. Schematics showing (a) equivalent output circuit and (b) parameterized output resistance as a function of the duty cycle considering the no-charge operating mode for different values of r_L/r_s.

The equivalent circuit is analyzed in order to obtain the power characteristics. The reactive input power is given by

$$Q_i = Q_o + |I_L|^2\omega_g L - |V_o|^2\omega_g C_{eq} \tag{10}$$

where Q_o is the load reactive power. Neglecting the converter losses, the input power factor is

$$\mathrm{PF}_i = \frac{P_o}{\sqrt{P_o^2 + (Q_o + |I_L|^2\omega_g L - |V_o|^2\omega_g C_{eq})^2}}. \tag{11}$$

In most parameter combinations, the reactive power related to the capacitor outweighs the inductive reactive power. Thus, for a unity power factor load, the input power factor is capacitive.

C. Output Equivalent Resistance

SCCs usually employ film capacitors. These have a low equivalent series resistance characteristic in relation to a conducting resistance of a MOSFET, which can be neglected in the following analysis. Considering that each MOSFET is modeled as a conducting resistance $R_{DS,on}$ during its ON state, the equivalent conduction resistance of a four-quadrant switch (two MOSFETs) is

$$r_s = 2R_{DS,on}. \tag{12}$$

If these and the inductor conduction resistance r_L are considered in the steady-state analysis, an equivalent output voltage

$$v_{o,ni} = v_o - R_{out} i_o \tag{13}$$

is obtained [as shown in Fig. 9(a)]. Thus, R_{out} is defined as an equivalent output conduction resistance for the no-charge operating mode [25], as follows:

$$R_{out} = \frac{r_1(1+D)^2}{D(1-D)^2} + \frac{r_2}{1-D} + \frac{r_3}{D} + \frac{r_4}{1-D} + \frac{4r_L}{(1-D)^2}. \tag{14}$$

A parameterized output resistance $\overline{R_{out}} = R_{out}/r_s$, where

$$r_1,\ r_2,\ r_3,\ r_4 = 2R_{DS,on} = r_s \tag{15}$$

is shown in Fig. 9 for different values of r_L/r_s (ratio of the inductor resistance r_L and the conducting resistance of a four-quadrant switch r_s).

This output resistance is proportional to the conduction losses, and the minimum values are obtained for duty cycles between 0.2 and 0.4. Differently from the boost converter, the equivalent

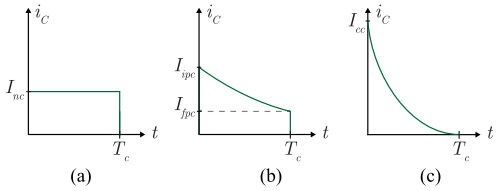

Fig. 10. Operating modes based on the current waveforms. (a) No charge. (b) Partial charge. (c) Complete charge.

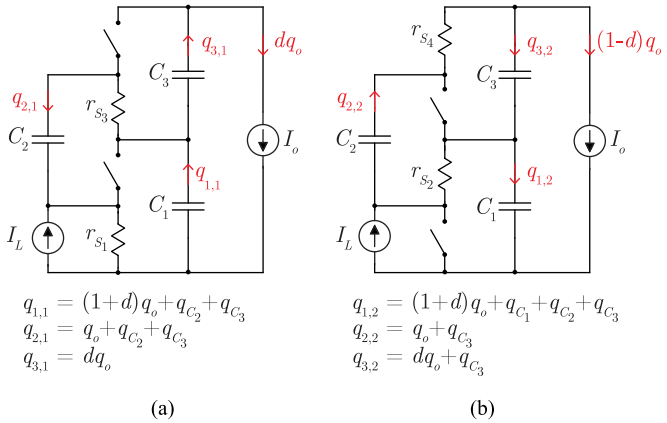

Fig. 11. Charges flowing through capacitors during (a) first and (b) second operating stages.

resistance is high for both low and high duty cycle values. Therefore, these operating points should be avoided. It can also be observed that the lowest resistance is not when the duty cycle is 0.5, as occurs in the conventional pure SC converters. Thus, the proposed integration presents its own characteristics, which are different features from ac–ac boost and ac–ac SC converters.

D. Current Analysis

SCCs are classified based on the relation between the circuit time constants and the switching period, as shown in Fig. 10 [25]. In most cases, the converters are designed in order to operate in the partial-charge mode [see Fig. 10(b)], which is the most cost-effective solution. The capacitor currents are described by exponential functions; therefore, a circuit analysis in which average values are considered is not suitable for determining effective current values.

The charge transferred to the output load during a switching period is defined as

$$q_o = \int_0^{T_s} i_o dt = \langle i_o \rangle T_s \tag{16}$$

and, considering that the voltage across a capacitor is equal to half of the output voltage, the net charge through a capacitor k during a switching period is

$$q_{C_k} = \int_0^{T_s} i_{c_k} dt = -\frac{V_{op}}{2} \omega C_k T_s \sin(\omega t). \tag{17}$$

On analyzing the operating stages, the charges flowing through the capacitors are computed and shown in Fig. 11.

Considering the no-charge mode [see Fig. 10(a)], the current in a capacitor is constant during an operating stage. Thus, for a charge q_{ch} during an interval T_{ch}, the current through a capacitor is

$$I_{nc} = \frac{q_{ch}}{T_{ch}}. \tag{18}$$

Substituting q_{ch} by the charges shown in Fig. 11 and T_{ch} with the stage duration (DT_s or $(1-D)T_s$), the currents in all capacitors can be obtained for the no-charge operating mode. For the partial-charging mode (see Fig. 10), the differential equations are obtained from Fig. 11(a) as

$$\begin{aligned} \frac{di_{C_2}}{dt} + i_{C_2}\left(\frac{C_1+C_2}{C_1C_2(r_1+r_3)}\right) &= -\langle i_o \rangle \frac{1}{C_1(r_1+r_3)} \\ i_{C_1} &= -i_{C_2} - \langle i_o \rangle \\ i_{C_3} &= -\langle i_o \rangle. \end{aligned} \tag{19}$$

The solution of the first equation of (19) results in

$$i_{C_2}(t) = I_{C_2,p_1} e^{-\frac{t}{\tau_1}} - \frac{C_2}{C_1+C_2}\langle i_o \rangle \tag{20}$$

in which the time constant τ_1 corresponds to

$$\tau_1 = (r_1+r_3)\frac{C_1C_2}{C_1+C_2} \tag{21}$$

and the value of I_{C_2,p_1} is still unknown. This value can be obtained by using the total charge variation in the capacitor C_2 during the first operating stage, which is equal to $q_o + q_{C_2} + q_{C_3}$. Thus, the following relation is valid:

$$\int_0^{DT_s} i_{c_2}(t) dt = q_o + q_{C_2} + q_{C_3}. \tag{22}$$

Solving (22) for I_{C_2,p_1} results in

$$\begin{aligned} I_{C_2,p_1} = \frac{T_s}{\tau_1\left(1-e^{-\frac{DT_s}{\tau_1}}\right)} \Bigg[\langle i_o \rangle \frac{C_1+(1-D)C_2}{C_1+C_2} + \\ -\frac{\omega V_{op}}{2}\sin(\omega t)(C_2+C_3) \Bigg]. \end{aligned} \tag{23}$$

The equation for $i_{C_2}(t)$ during the first operating stage is obtained by applying (23) in (20). Following the same steps, all currents through the capacitors can be obtained.

If the operating modes are compared for the same charge transfer, the effective current values for the no-charge mode [see Fig. 10(a)] are the smallest. Thus, the no-charge mode is considered as the ideal case. A resistance factor, defined as k_r, is introduced to compute the quadratic relation of the ratio between effective current values for partial- and no-charge modes:

$$k_r = \left(\frac{I_{ef,pc}}{I_{ef,nc}}\right)^2. \tag{24}$$

The resistance factor shows the proportion of conduction losses when comparing the partial-charge and no-charge modes. This parameter is further analyzed in the design section.

III. Design

A single-phase prototype was designed with the following specifications: input and output voltages: 55/220 V (effective values), rated apparent power = 1 kVA, minimum input power factor = 0.92, grid frequency = 60 Hz, and switching frequency = 100 kHz. The design criteria are described in the following.

A. Duty Cycle

The duty cycle can be computed using (9) and setting $\omega \to 0$ when the resonant frequency is much higher than the mains frequency

$$D = 1 - 2\frac{V_i}{V_o} = 0.5. \tag{25}$$

B. Input Inductor

The input inductance is designed to maintain a small high-frequency current ripple. From the first equation of (1), the minimum inductance value is obtained as

$$L \geq \frac{DV_i^2}{f_s P_o \overline{\Delta I_L}} \tag{26}$$

in which the parameterized current ripple $\overline{\Delta I_L}$ is a fraction of the input current.

C. Capacitors

Capacitance values must satisfy some conditions, described as follows.

1) *Input power factor:* In the hybrid converter, the capacitive reactive power usually outweighs the inductive reactive power. Therefore, from (11), there is a limit to the capacitance values that allow a minimum input power factor PF_i, given by

$$C_1 + C_2 + C_3 \leq \frac{4}{\omega V_o^2}\left[I_i^2 \omega L + Q_o - P_o \frac{\sqrt{1-\text{PF}_i^2}}{\text{PF}_i}\right]. \tag{27}$$

In this case, values of Q_o and PF_i are positive for an inductive power factor and negative otherwise.

2) *Resonant frequency:* Capacitance values also modify the resonant frequency (f_{res})—obtained when the denominator of (8) is null. Thus, the maximum capacitance values are given by

$$C_1 + C_2 + C_3 \leq \frac{(1-D)^2}{4\pi^2 f_{res}^2 L} \tag{28}$$

and the resonant frequency selected should be at least one decade above the mains frequency.

3) *Charging mode:* The conduction losses increase exponentially with low product of time constant RC and switching frequency. Therefore, the time constants should be at least half of the operating stage duration. Thus, minimum capacitance values are obtained with

$$\begin{aligned} \frac{C_1 C_2}{C_1 + C_2} &\geq \frac{D}{2(r_1 + r_3) f_s} \\ \frac{C_2 C_3}{C_2 + C_3} &\geq \frac{1-D}{2(r_2 + r_4) f_s}. \end{aligned} \tag{29}$$

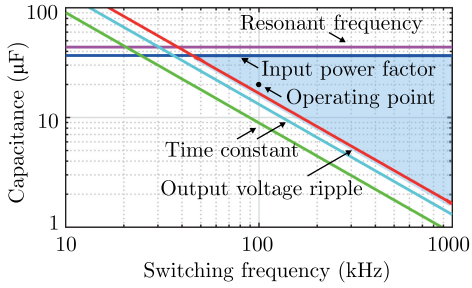

Fig. 12. Capacitance values that meet all design criteria (blue area) based on the mains (60 Hz) and switching frequencies.

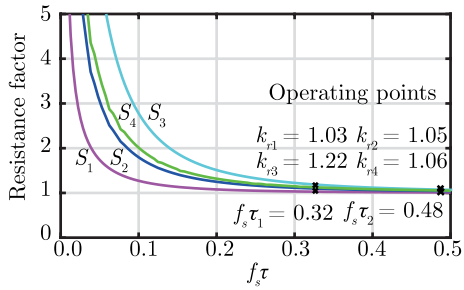

Fig. 13. Resistance factor for each switch as function of the product $f_s\tau$ for a constant duty cycle $D = 0.5$ and output current $I_o = 5$ A.

4) *Output voltage ripple:* The minimum capacitance values that satisfy a given percentage output voltage ripple $\overline{\Delta V_o}$ are computed by

$$C_1, C_3 \geq \frac{P_o(1+2D)}{\overline{\Delta V_o} f_s \text{PF}_o V_o^2} \tag{30}$$

when the output capacitance values are considered equal and PF_o is the output power factor.

Applying all of these criteria leads to the graphic shown in Fig. 12 for $f_g = 60$ Hz. The conditions of input power factor and resonant frequency are dependent on the mains frequency and are upper limits, while the conditions of time constant and output voltage ripple are related to the switching frequency and represent lower limits. The blue area shows the possible combinations of switching frequency and capacitances for these specifications, and considering the size of capacitors and increased losses at higher frequencies, the operating point was chosen as $f_s = 100$ kHz and $C = 20$ μF.

D. Resistance Factor

The values obtained from the design equations resulted in a capacitance value of 20 μF and equivalent resistances of $r_1 = 80$ mΩ and $r_2 = r_3 = r_4 = 240$ mΩ. Considering a switching frequency of 100 kHz and a duty cycle of 0.5, the equivalent resistance factors are shown in Fig. 13.

The resistance factors obtained show that the effect of the exponential shape of the currents leads to an increase of between 3.4% (switch S_1) and 21.6% (switch S_3) of the switch conduction losses.

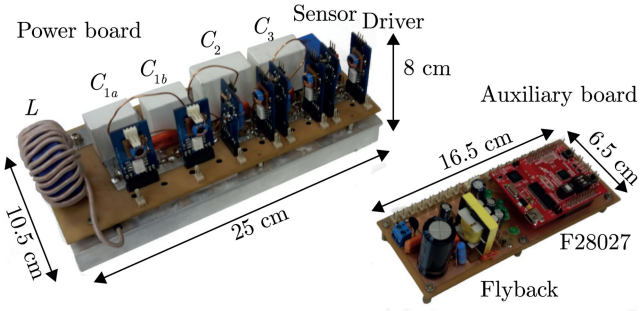

Fig. 14. Photographs of the prototype.

TABLE I
LIST OF COMPONENTS

Device	Code	Quantity
Input inductor	APH46P60 - 136 μH	1
Switches S_1	SCT3080AL - 650 V / 80 mΩ	4
Switches S_2, S_3, S_4	SCT2120AF - 650 V / 120 mΩ	6
Capacitors	600 V / 20 μF	4
Voltage sensor	LV25P	1

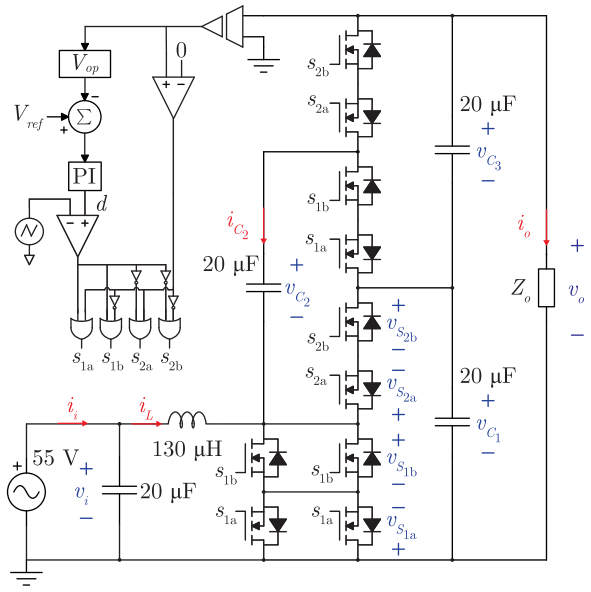

Fig. 15. Simplified electric schematic of the prototype.

IV. RESULTS

Photographs of the prototype can be seen in Fig. 14. The prototype consists of the power board and an auxiliary board, which contains the microcontroller, signal conditioning circuit, and auxiliary voltage sources. The power densities of the power stage are 1.48 kW/kg and 0.95 kW/L.

A list of the components is given in Table I. A total of ten SiC MOSFETs were employed, because switch S_1 was implemented as two parallel connected four-quadrant switches, in order to reduce the conduction losses. Dissipative voltage clamping circuits were used in all switches to prevent high voltage values during the output voltage zero crossing, when the modulation changes.

A simplified schematic of the prototype is shown in Fig. 15. The control and modulation circuits were implemented in a microcontroller TMS320F28027. The employed modulation is approached in Section II-A. The control mesh is based on output peak voltage regulation. A dead time was set as 200 ns, which corresponds to 2% of the total switching period.

The input and output voltages and currents when operating with a voltage conversion of 55/220 V at 60 Hz for 1-kVA resistive and 1-kVA inductive (PF = 0.75) output loads are shown in Fig. 16(a) and (b), respectively. The voltage gain is 4, and the output and input voltages are in phase. The input current leads the voltage for a resistive load, which represents a capacitive input power factor. For the inductive load, the input power factor is 0.90 inductive, indicating that the output inductive reactive power is partially compensated by the capacitive reactive power of the converter. Results were also obtained for a nonlinear load consisting of a full-bridge diode rectifier with a crest factor of 3 and output apparent power of 700 VA. These results can be observed in Fig. 16(c) and show that the input and output current waveforms are similar, which demonstrates that the power converter has an inner low impedance. Fig. 16(d) reports the results for the operation with two loads connected at different points (split-phase configuration). It should be noted that the voltage v_{o2} is the double of voltage v_{o1}, which corresponds to capacitors C_1 and C_3 being equalized.

The experimental results for the voltages across the capacitors are reported in Fig. 17. The switched-capacitor cell has the characteristics of voltage self-balance, and thus, the voltages across the three capacitors C_1, C_2, and C_3 are equalized each switching period without an additional control mesh. The maximum voltage stresses across the capacitors are approximately the same and equal to 155 V, which is half of the peak output voltage value.

The voltages across the switches S_{1_a} and S_{1_b} are given in Fig. 18(a), and it should be noted that each switch blocks the capacitor voltage during a grid half cycle. Fig. 18(b) compares the voltages across the switches S_{1_b} and S_{2_b}. They block the voltage across capacitor C_1 during the positive half cycle and alternate between switching periods. In both cases, the maximum voltage blocked is equal to half of the peak output voltage (155 V).

The current through the switched capacitor (i_{C_2}) is shown in Fig. 19(a) within three grid periods and Fig. 19(b) within five switching periods. Soon after the commutation, the capacitor current does not have an exponential characteristic, as expected based on the theoretical analysis (see i_{C_2} current in Fig. 3). This occurs because of the presence of parasitic inductances, which provide a resonant transition to the current. This feature helps the commutation, because it avoids high current peaks. As this inductance is small, this period is short, and once it ends, the current follows the exponential characteristic expected based on the theoretical analysis. However, when the switched capacitor operates in the partial-charging mode, the exponential characteristic is not as clearly observed after the commutation,

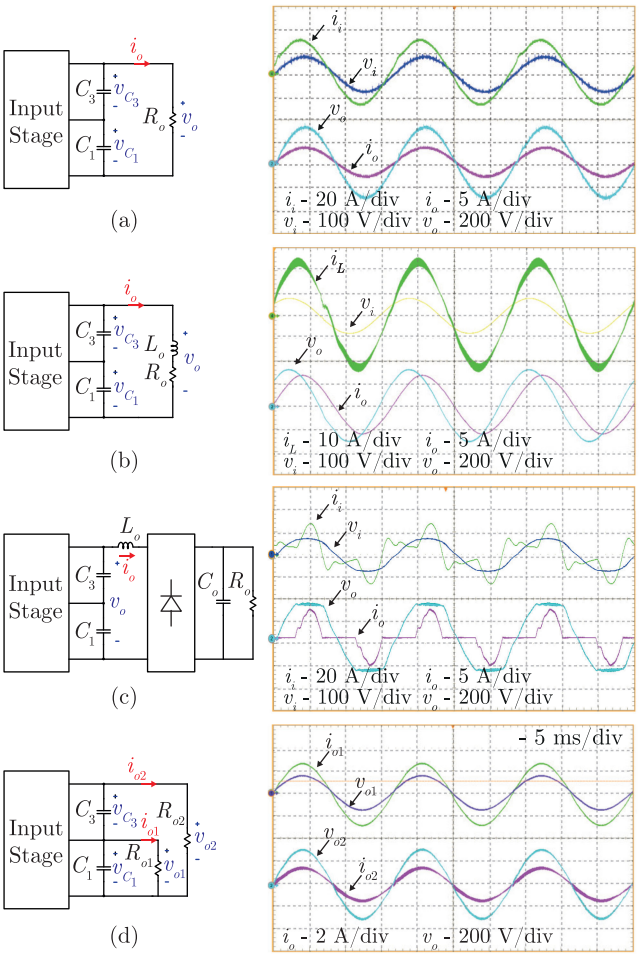

Fig. 16. Experimental results for input and output voltages and currents for a 55-V input voltage. Input and output frequencies are equal to 60 Hz (time scale: 5 ms/div). (a) Resistive load, 1 kW ($R_o = 48\ \Omega$). (b) Inductive load, 1 kVA ($L_o = 86$ mH, $R_o = 36\ \Omega$, and PF = 0.75). (c) Nonlinear load, 700 VA, ($L_o = 1$ mH, $C_o = 1.5$ mF, and $R_o = 150\ \Omega$). (d) Two resistive loads, 242 W each ($R_{o1} = 50\ \Omega$ and $R_{o2} = 200\ \Omega$).

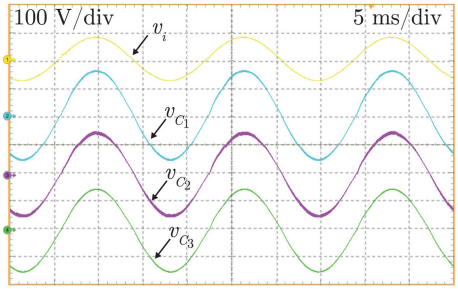

Fig. 17. Experimental results for voltages across the capacitors for a single resistive output [see Fig. 16(a)] at 60 Hz.

even in the theoretical waveforms shown in Fig. 3, because they approximate a straight line.

The experimental efficiency curve is shown in Fig. 20(a) and was obtained for 55/220-V operation and resistive loads. The measured peak efficiency is 93% at 400–500 W and 88.5% at rated power. It should be noted that the efficiency drops sharply

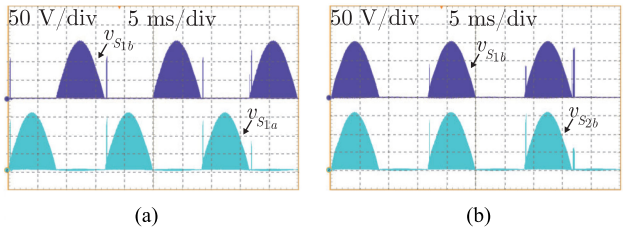

Fig. 18. (a) and (b) Experimental results for voltages across the switches during a grid period.

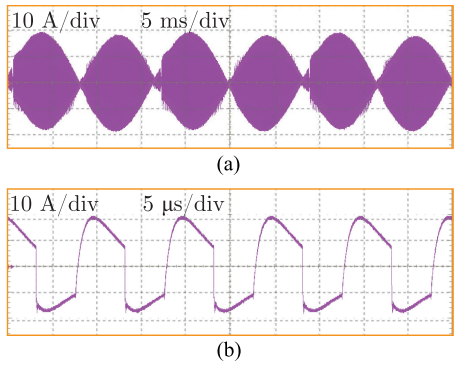

Fig. 19. Experimental results for the current through the switched capacitor C_2 during (a) three grid periods and (b) five switching periods.

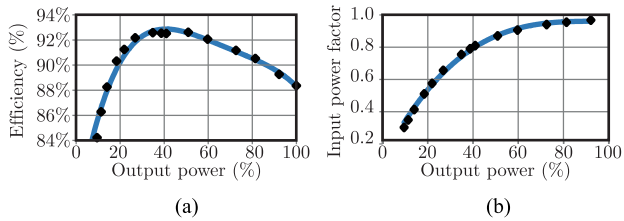

Fig. 20. Experimental (a) efficiency and (b) power factor curves for resistive loads.

TABLE II
DISTRIBUTION OF LOSSES

Device	Loss participation	Conduction/Switching(Core*)
S_1	48%	88% / 12%
S_2	14%	91% / 9%
S_3	15%	82% / 18%
S_4	13%	86% / 14%
L	8%	92% / 8*%
R_{cl}	2%	100% / -

for low power levels, because of the high-reactive-current component.

The distribution of losses was determined theoretically and is shown in Table II. The second column represents the participation of power losses of each group of devices, while the third column shows the proportions of conduction and switching losses for the semiconductor devices and of conduction and magnetic losses for the input inductor. It can be seen that almost half of the losses are in switch S_1 (element that integrates ac–ac

TABLE III
QUALITATIVE COMPARISON BETWEEN THE PROPOSED CONVERTER (HBSCC) AND OTHER NONISOLATED TOPOLOGIES

Converter	HBSCC	[11]	[13]	[19]	Boost ac-ac [26]	Back-to-Back Voltage Bus
Gain	$2/(1-D)$	4^1	4^1	4^1	$1/(1-D)$	$\leq 1^2$
Frequency	Fixed	Fixed	Fixed	Fixed	Fixed	Variable
Power Factor Control	No	No	No	No	No	Yes
Voltage Regulation	Yes	No	No	Yes	Yes	Yes
Switch count	8	16	16	16	4	8
AC Capacitor count	3	7	5	5	1	1
Bulk capacitor count	0	0	0	0	0	1
Voltage stresses	$V_h/2$	V_l	$V_h/2$, $V_h/4$	$V_h/2$, V_l	V_h	${V_{dc}}^3$
Inductor count	1	0	0	1	1	2
Complexity of Controller	Low	-	-	Medium	Low	Medium
Complexity of Modulator	Medium	Low	Low	Medium	Medium	Low
Efficiency	88.5% at 1 kW	-	94% at 600 W	95% at 300 W	-	$\sim$91% at 1kW^4

1—Step-up configuration; 2—In relation to the dc bus (V_{dc}); 3—V_{dc} is higher than V_l and V_h; 4—Estimation considering the same switches and input–output voltage levels as the proposed converter.

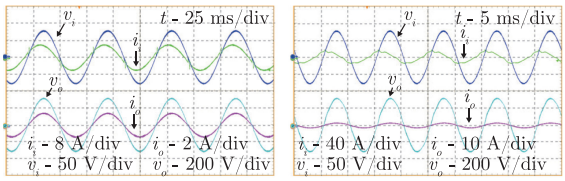

Fig. 21. Experimental results for mains frequency equal to (a) 16.67 Hz and (b) 100 Hz.

TABLE IV
SIMPLIFIED VOLTAGE GAIN FOR EACH CONNECTION

Connec.	Gain	Connec.	Gain	Connec.	Gain
(a)	$\frac{2}{1-D}$	(b)	$\frac{1}{1-D}$	(c)	$\frac{D}{1-D}$
(d)	$\frac{1+D}{1-D}$	(e)	$\frac{1}{1-D}$	(f)	2
(g)	$\frac{1}{D}$	(h)	$1+D$	(i)	1
(j)	$\frac{2}{D}$	(k)	$\frac{2}{1+D}$	(l)	2
(m)	$\frac{1+D}{D}$	(n)	$\frac{1}{D}$	(o)	$1+D$

boost and ladder switched-capacitor cell), and they correspond to conduction losses, which explains the use of parallel connections of MOSFETs.

The input power factor curves are shown in Fig. 20(b). The curves tend toward a unitary power factor as the processed power increases, and the value obtained was 0.974 for a unity power factor at rated load. In contrast, for low active output power, the reactive power of the capacitors is significant, which results in a low input power factor.

The converter can also operate with different grid frequencies. The experimental results are shown in Fig. 21 for 16.67 and 100 Hz under a 230-W unity power factor load. As expected, the reactive input current increases with the grid frequency, which results in higher losses.

A qualitative comparison between the proposed converter and other ac–ac topologies is shown in Table III, where the characteristics of voltage gain, frequency, modulation, control,

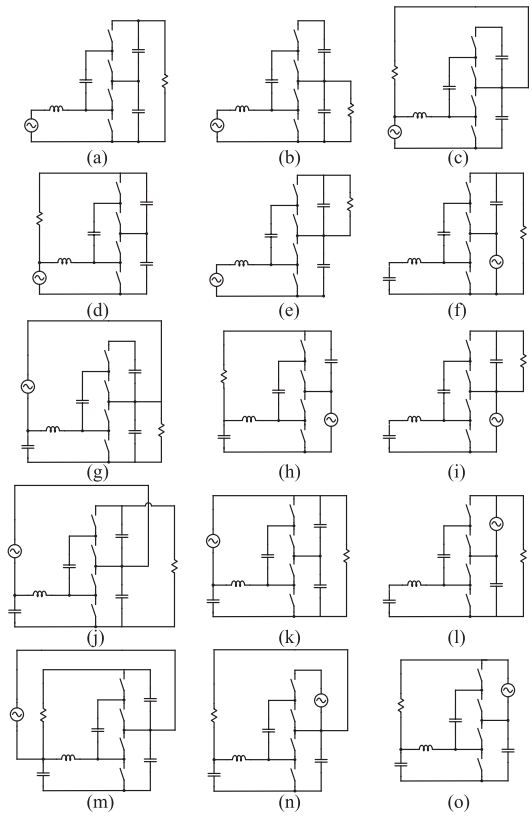

Fig. 22. (a)–(o) Different possibilities of input–output connections.

as well as the device count were considered. The parameters V_h and V_l represents the peak values in the high- and low-voltage sides, respectively.

The proposed converter is able to regulate the output voltage at the cost of an additional inductor and more complex modulator, when compared to pure switched-capacitor topologies [11], [13]. Table III also compares the HBSCC with a resonant SCC proposed in [19], which inserts a low-value inductance and is able to control the output voltage level, although the controller

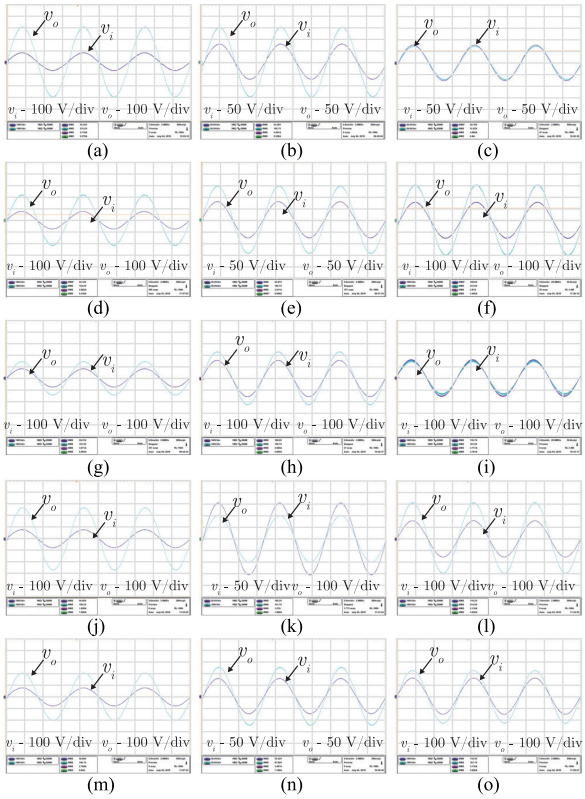

Fig. 23. (a)–(o) Experimental results for the possible connections operating in the boost mode with $P_o = 250$ W and $D = 0.5$.

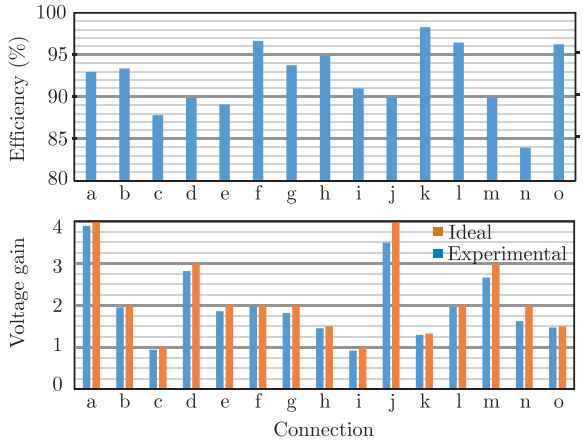

Fig. 24. Efficiency for alternative connections at $P_o = 250$ W and $D = 0.5$.

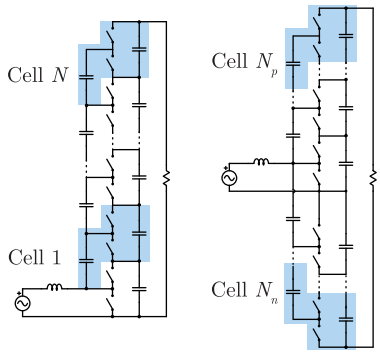

Fig. 25. Hybrid converter with more switched-capacitor ladder cells. (a) Common ground connection. (b) Differential connection.

and modulator complexities increase . Regarding the conventional ac–ac boost converter, the HBSCC has a doubled gain and reduced voltage stresses across the semiconductors, at the cost of additional capacitors. A comparison with two full-bridge converters in a back-to-back configuration is also shown as an example of indirect (ac–dc–ac) converter.

V. Proposal for Other Connections

As the converter is bidirectional in voltage and current, the input and output connection points can be changed, in order to achieve a step-down converter. Moreover, the converter presents four possible connection points; thus, a total of 15 pairs of input and output connections are allowed, as shown in Fig. 22. Note that the configuration (a) corresponds to the topology presented herein. These alternative input and output connections have different voltage gains, which are shown in Table IV.

The experimental input and output voltages waveforms are shown in Fig. 23 for all connections at 250-W output power, duty cycle 0.5, and an effective voltage of 110 V across the capacitors.

The efficiencies and voltage gains for these tests are summarized in Fig. 24. Theoretically, the connection (j) presents the same gain as the main connection (a), although the efficiency of the first is lower and there is no common connection point. Furthermore, connection (k) presented the highest efficiency; however, its voltage gain is small, around 1.3. All of these connections are bidirectional; thus, the input–output ports could be changed to obtain the step-down versions.

Higher voltage gains could be achieved by increasing the number of switched-capacitor cells, as shown in Fig. 25. The ideal voltage gain, considering low impact of the grid frequency, is

$$G = \frac{N+1}{1-D}, \tag{31}$$

where N is the number of switched-capacitor cells [$N = N_p + N_n$ in Fig. 25(b)]. Both topologies have the characteristic of voltage sharing among the capacitors, which allows the use of low-voltage semiconductor devices. Some aspects that should be observed are the potentially higher reactive current, given the increased capacitor count, and the increased number of switches, which also requires more isolated gate drivers.

VI. Conclusion

This article describes the operation of a single-phase HBSCC as a direct ac–ac topology. The main characteristics of the converter are high voltage gain, fixed frequency, and low-voltage stresses across the capacitors and switches. Moreover, the current stresses in the switches and capacitors are not only dependent on the duty cycle and output currents values, but also on the

conducting resistances of the switches, capacitances, and switching frequency. The voltage balance among the capacitors does not require an additional control mesh. Experimental results corroborated the operation with resistive, inductive, nonlinear, and multiple loads. The operation with different grid frequencies was observed, and in addition, the structure was tested in 14 variations of input–output connections. This topology is suitable for ac–ac applications, where low-voltage devices are employed and a high voltage gain is needed.

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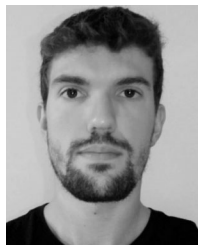

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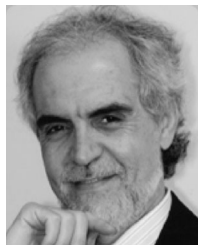

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