Letters

# Turn-OFF Delay Compensation of Series-Connected IGBTs for HVDC Applications

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***Abstract*—This letter shows a computationally inexpensive delay compensation algorithm for series-connected insulated-gate bipolar transistors (IGBTs). The algorithm adjusts the relative turn-OFF delays among series-connected IGBTs based on the measured clamp capacitor voltages. Experimental results show that the capacitor voltage differences are compensated in a few iterations, making it suitable for delay compensation of industrial series-connected IGBTs.**

***Index Terms*—High voltage direct current (HVdc), insulated-gate bipolar transistor (IGBT), turn-OFF delay, voltage source converter (VSC).**

## I. INTRODUCTION

WITH the advent of the voltage source converter (VSC) in high-voltage direct-current (HVdc) applications, newer topologies have been proposed with the aim to outperform the modular multilevel converter, which offer a reduction in converter footprint and/or losses in detriment of increased control and hardware complexity. Some examples are the alternate arm converter [1] and the series bridge converter [2]. These use a director switch (DS) device based on series-connected insulated-gate bipolar transistors (IGBTs), in order to reconfigure the topology several times per electrical cycle.

Due to voltage requirements of HVdc applications, it is not possible to construct a DS using a single semiconductor device. A practicable solution is to place smaller voltage devices in series to form a series-connected switch capable of blocking the voltage of $V_{\mathrm{DC}} = N \times V_{\mathrm{CE}}$, where $V_{\mathrm{CE}}$ is the maximum collector-to-emitter blocking voltage per device. One of the main technical challenges within series connected IGBTs of a DS is voltage balancing across all operating conditions.

Among the technical challenges of these topologies, simultaneous turn-OFF of series-connected IGBTs stands out as a critical feature to avoid steady-state voltage imbalances [3]. Should this not be guaranteed, overvoltage in one or more devices may occur, potentially damaging the power electronics equipment.

A key challenge for the DS is how to harvest power to drive each IGBT level while maintaining a voltage balance during normal operation. Providing power from ground is simply not feasible in HVdc applications due to the high insulation levels required. A solution to this problem has been found in [4] and [5] by using the energy stored in the capacitor of a clamp capacitor–diode (CD) snubber. Moreover, the power balance is ensured by using active modulation or resistive balancing techniques [4], [5]. Even though the DS is commutated under zero-voltage switching and zero-current switching, a hard switching condition might be unavoidable. Therefore, the instantaneous voltage balance across the levels poses an additional challenge. A common solution in the industry is to use an active damping circuit [6] but this relies on having a switching loop with a low parasitic inductance.

Some recent works refer to the issue of turn-OFF delay compensation of series-connected IGBT for high-voltage applications. For example, Riazmontazer *et al.* [7] assume a constant known delay in the circuit and compensate this by using an analog electronic circuit. Luo *et al.* [8] estimate the turn-OFF delay of an IGBT-based DS by measuring the voltage drop across the parasitic inductance at the IGBT emitter, although delay compensation is not investigated. In [9], a closed-loop method is derived to independently control the time derivative of both collector current and collector–emitter voltage for each IGBT, although the turn-OFF delays are not compensated for. Ji *et al.* [10] present a novel active voltage balancing control to solve the asynchronous gate delay issue with series-connected IGBTs. Such method relies on using transient voltage suppressors to allow clamping of the device. Furthermore, Ji *et al.* [10] estimate the time delay between any pair of series-connected IGBTs by measuring the clamping current through the clamping circuit. However, such time-delay compensation takes several cycles to converge due to its cascaded approach and would prove impractical for several hundreds of series-connected IGBTs. These solutions, while interesting, are too complex for high-power, high-reliability commercial applications.

The contribution of this letter is a simple and reliable solution to the problem of voltage balancing within series-connected

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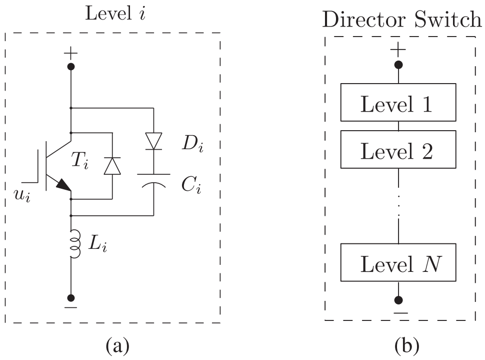


(a) (b)

Fig. 1. Schematics of a DS. (a) Single DS level. (b) $N$ series-connected levels.

IGBTs using a CD snubber circuit by varying the IGBTs turn-OFF delays. To the best of the authors' knowledge, this has not been disclosed in the literature before.

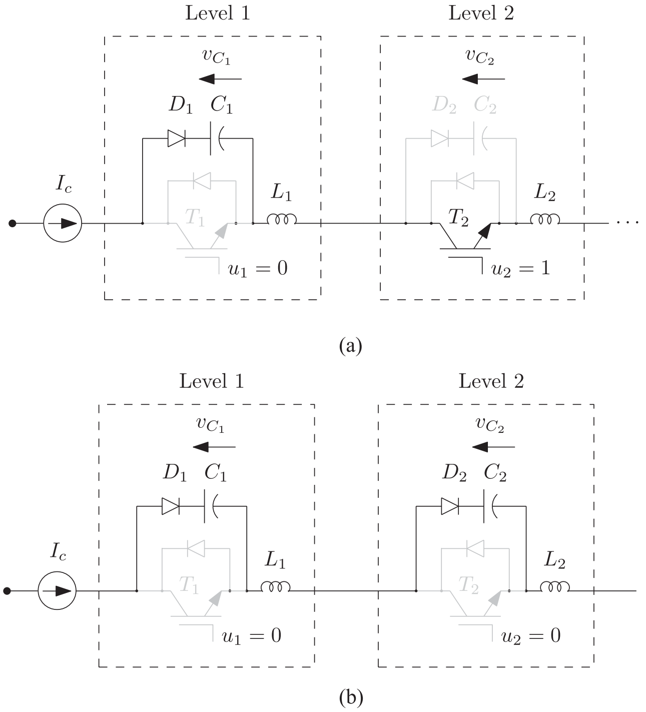
## II. DIRECTOR SWITCH

### A. System Model

Fig. 1(a) depicts the $i$th level in a DS, where $i = 1, 2, \ldots, N$ and $N$ is the number of series-connected devices in the DS. The DS current is denoted as $I_c$. Each level is composed of a IGBT, $T_i$, and gate electronics. The firing state of $T_i$ is controlled by a gate unit that drives gating logical signal $u_i$, i.e., $u_i = 1$ indicates the turn-ON of $T_i$, and $u_i = 0$ indicates its turn-OFF. Each IGBT is fitted with a built-in antiparallel diode. Additionally, a clamp snubber circuit consisting of a clamp capacitor $C_i$ and a clamp diode $D_i$ is included. Details of the gate unit and gate electronics are provided in [4]. An equivalent series inductor $L_i$ is represented at each level; typically, $L_i$ is the result of the circuit's parasitic inductance and the equivalent proportional inductance $L/N$, where $L$ is the arm inductor, typically of several tens of millihenries, fitted in each arm of the HVdc converter topology. Fig. 1(b) shows the series connection of $N$ levels in a DS, where $N$ is typically in the range of 200–300 per converter arm.

### B. Operation of the CD Snubber Under Hard Switching Conditions

The CD snubber serves the important purpose of providing sufficient storage to supply the gate electronics on a cycle-by-cycle basis. First, the clamp capacitor absorbs the inductive energy of the unclamped inductance $L_i$ during a turn-OFF event, which results in a capacitor voltage of several thousand volts by means of the energy balance $(1/2)L_i I_c^2 = (1/2)C_i v_{C_i}^2$. Also, having a CD snubber turns out beneficial to balance the voltage across IGBT levels after a turn-OFF event. Moreover, it smooths out any voltage differences, leaving the gate actuation delay and clamp capacitor tolerances as the main source of unbalance. Also, it acts as a quasi-peak detector, which reads the highest voltage achieved after a turn-OFF event. The measurement of such voltage is simple, and it does not require any complex algorithm or fast wide-bandwidth transducers and circuits. The balancing technique presented in this letter, and explained in the next section, uses the negative effect of different gate actuation delays for the benefit of forcing equal voltage sharing, regardless of the reason that created the unbalance in the first place.



(a)

(b)

Fig. 2. Current path at turn-OFF instants $t_1$ and $t_2$ between two DS levels. (a) Circuit at $t = t_1$. (b) Circuit at $t = t_2 > t_1$.

## III. TURN-OFF DELAY ESTIMATION AND COMPENSATION

Fig. 2 shows the current path of two series-connected levels. At time $t_1$, $T_1$ has completed its transition from ON-state to OFF-state, whereas $T_2$ has not yet reached OFF-state, and hence, it remains in ON-state, see Fig. 2(a). At time $t_2$, $T_1$ remains in OFF-state and $T_2$ has completed its transition from ON-state to OFF-state, see Fig. 2(b). The time delay of $(t_2 - t_1)$ s may arise due to existing delays in the application of the gate–emitter turn-OFF voltage of transistor $T_2$ with respect to that of $T_1$ due to tolerances in circuit components, or delays in the gate signals of each transistor introduced by the control platform. Without loss of generality, assuming the same clamp capacitance $C_1 = C_2 = C$ equal initial values $V_1 \triangleq v_{C_1}(t_1) = v_{C_2}(t_1) \triangleq V_2$ and constant current $I_c$ during the interval of analysis by virtue of the large value of $L$ for the short switching time, the pairwise voltage difference between the clamp capacitors in $T_1, T_2$ is

$$V_{12} = \frac{I_c}{C}\delta_{12} \tag{1}$$

where $V_{12} \triangleq V_1 - V_2 = v_{C_1} - v_{C_2}$, and $\delta_{12} \triangleq t_2 - t_1$ represents the time delay between the turn-OFF of $T_1$ at $t_1$ and the turn-OFF of $T_2$ at $t_2$, with $t_2 > t_1$. Note that the indices in the voltage difference are reversed with respect to the time differences in order to obtain positive voltage differences for positive time differences and equal initial voltages in the DS levels. Generalizing (1) to $N$ series-connected IGBTs with a

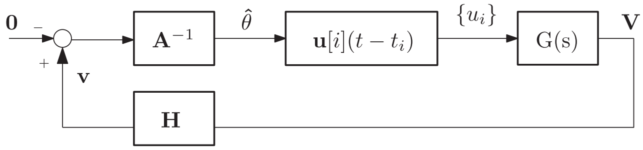


Fig. 3. Closed-loop offset estimation and turn-OFF delay compensation.

time difference in their turn-OFF instants given by

$$\delta_{ij} \triangleq t_j - t_i\,. \tag{2}$$

The voltage difference between any given pair of clamp capacitors, denoted as $V_{ij} \triangleq V_i - V_j$, arising from $\delta_{ij}$ is

$$V_{ij} = a_{ij}\delta_{ij} \tag{3}$$

where $i, j = \{1, 2, \ldots, N\}$ and $a_{ij}$ are the coefficients that linearly relate a pair of voltage and turn-OFF instant differences for a given pair of transistors $T_i$ and $T_j$. The coefficients $a_{ii} \triangleq 1$ are defined for the sake of mathematical completion, although naturally $\delta_{ii} = V_{ii} = 0$. Note that the voltage difference in (3) is independent on the state of the remaining IGBTs.

The gate unit has the ability to obtain the peak value of the clamp capacitor $V_i$ in the $i$th level, and hence, $V_{ij}$ can be computed from these measurements. In this work, an initial characterization of $a_{ij}$ in (3) has been obtained at design time. It is also possible to perform an online characterization of $a_{ij}$ by estimating the clamp capacitance, although this is out of the scope of this letter.

The objective is to synchronize all the turn-OFF events with respect to the turn-OFF instant of a reference transistor, e.g., $T_1$, without loss of generality. To this end, the proposed approach is summarized in Fig. 3. The plant $G(s)$ represents the arrangement of series-connected IGBTs; the inputs to the plant is the set of firing commands $\{u_1, u_2, \ldots, u_i, \ldots, u_N\}$ and its output is the voltage measurement vector $\mathbf{v}$. The synchronization of the turn-OFF events shall be achieved by means of a control law that attains $\mathbf{v} = \mathbf{0}$, which is obtained when no voltage difference observed between any pair of transistors $T_i, T_j$. In order to facilitate the implementation on a digital signal processor, (3) is written in a matrix form as

$$\begin{aligned}
\mathbf{A} &= \mathrm{diag}[a_{1j}] \quad j = 1, 2, \ldots, N\\
\mathbf{V} &= [V_1\, V_2 \ldots V_N]^T\\
\mathbf{v} &= [0\, V_{12}\, V_{13} \ldots V_{1\,N}]^T = \mathbf{H}\cdot\mathbf{V}\\
\theta &= [0\, \delta_{12}\, \delta_{13} \ldots \delta_{1\,N}]^T
\end{aligned} \tag{4}$$

and $\mathbf{H} = \{H_{ij}\} \in \mathbb{R}^{N\times N}$ where $H_{1j} = 0$ for all $j$, $H_{i1} = 1$ for all $i > 1$, $H_{ij} = -1$ if $(j = i \wedge j \neq 1)$, and $H_{ij} = 0$ otherwise.

The vector $\theta$ is a relative offset vector between an arbitrary transistor $T_1$ and the remaining transistors. Expanding (3), an estimate of $\theta$, denoted as $\hat{\theta}$, can be obtained as

$$\hat{\theta} = \mathbf{A}^{-1}\mathbf{v} \tag{5}$$

where $\mathbf{A}^{-1} = \mathrm{diag}(a_{1j}^{-1})$. Furthermore, in order to ensure the turn-OFF of transistor $T_1$ at nonnegative time offsets of the controller cycle scan (also known as "time zero"), its turn-OFF instant shall be determined by

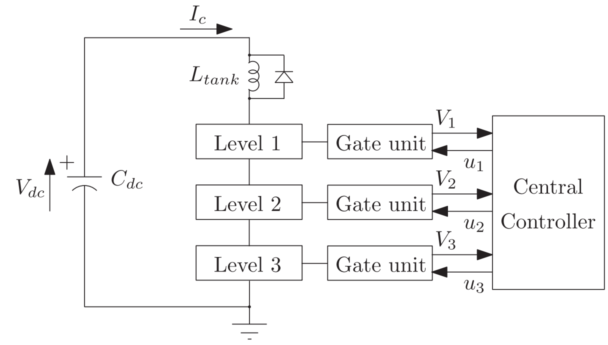


Fig. 4. Description of the experimental test setup.

$$t_1 = \begin{cases} -\min(\hat{\theta}), & \text{if } \min(\hat{\theta}) < 0\\ 0, & \text{otherwise.}\end{cases} \tag{6}$$

Therefore, using (6), the turn-OFF instants of all IGBTs are

$$t_i = t_1 + \hat{\theta}[i] \qquad i = 1, 2, \ldots, N \tag{7}$$

where $\hat{\theta}[i]$ is the $i$th element in $\hat{\theta}$. From (7), the turn-OFF command sent to the IGBTs shall be delayed as

$$u_i(t) = \mathbf{u}[i](t - t_i) \tag{8}$$

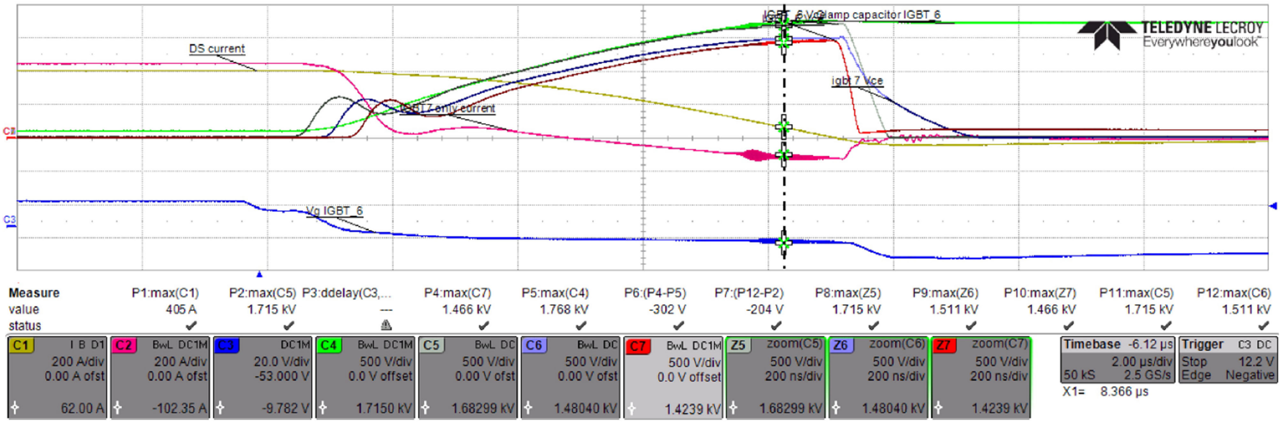
where $\mathbf{u}(t)$ is the vector containing all the turn-OFF commands without delay compensation at time $t$, $\mathbf{u}[i](t)$ is the uncompensated computer command for transistor $T_i$ at time $t$, and $u_i(t)$ is the command sent to transistor $T_i$ after the turn-OFF delay compensation has been performed.

The proposed method allows for graceful degradation of the gate driver and/or clamp capacitor, since the compensation algorithm runs in a closed-loop fashion, and hence, changes in such parameters—which would lead to further imbalance of voltage—will be continually compensated for. This makes for a rugged implementation strategy to prolong the useful life of a converter in service.

## IV. EXPERIMENTAL RESULTS

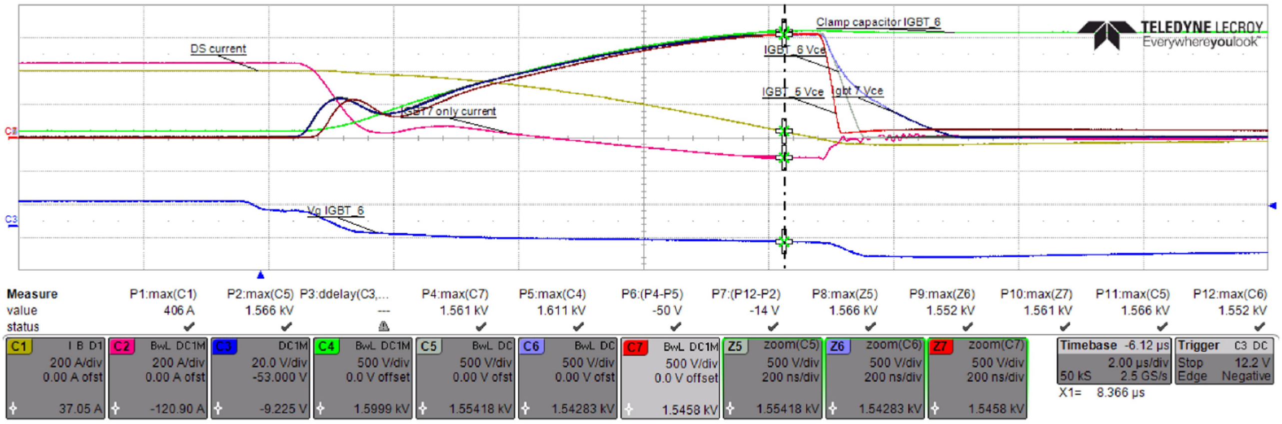
The method proposed in this letter has been experimentally demonstrated using a three-level DS configuration. As mentioned earlier, since the voltage difference between any two pairs of clamp capacitors does not depend on the number of levels, this method can be applied to several series-connected devices.

Fig. 4 shows the schematic representation of the test setup. The circuit is used in one-shot operation mode, where the turn-OFF current $I_c$ is controlled by the ON-time of the IGBTs within the DS. The current is maintained approximately constant during the turn-OFF time by virtue of the tank inductance $L_{\text{tank}}$. The IGBT control and delay compensation has been implemented in a CompactRIO 9038 central controller (CC). The characterization of (3) for each pair of clamp capacitors has been performed offline and made available to the CC. The CC receives the maximum capacitor voltages $V_i$ from the gate unit, computes the delay compensation algorithm presented in (5)–(7), and sends the firing commands $u_i$ back to the gate units. The test setup



| Measure | P1:max(C1) | P2:max(C5) | P3:ddelay(C3,... | P4:max(C7) | P5:max(C4) | P6:(P4-P5) | P7:(P12-P2) | P8:max(Z5) | P9:max(Z6) | P10:max(Z7) | P11:max(C5) | P12:max(C6) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 405 A | 1.715 kV | --- | 1.466 kV | 1.768 kV | -302 V | -204 V | 1.715 kV | 1.511 kV | 1.466 kV | 1.715 kV | 1.511 kV |
| status | ✓ | ✓ | ⚠ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

Fig. 5. Random delays in the turn-OFF signals of series-connected IGBTs results in large $V_{\mathrm{CE}}$ voltage differences among IGBTs.



| Measure | P1:max(C1) | P2:max(C5) | P3:ddelay(C3,... | P4:max(C7) | P5:max(C4) | P6:(P4-P5) | P7:(P12-P2) | P8:max(Z5) | P9:max(Z6) | P10:max(Z7) | P11:max(C5) | P12:max(C6) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| value | 406 A | 1.566 kV | --- | 1.561 kV | 1.611 kV | -50 V | -14 V | 1.566 kV | 1.552 kV | 1.561 kV | 1.566 kV | 1.552 kV |
| status | ✓ | ✓ | ⚠ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

Fig. 6. $V_{\mathrm{CE}}$ voltage difference among IGBTs is minimized after two iterations of the delay compensation algorithm.

TABLE I
EXPERIMENTAL SETUP PARAMETERS

| Parameter | Value | Unit |
|---|---|---|
| $V_{dc}$ | 300 | V |
| $C_{dc}$ | 2400 | $\mu$F |
| $I_c$ | 400 | A |
| $L_{tank}$ | 355 | $\mu$H |
| $L_i$ | 14 | $\mu$H |
| $C_i$ | 1 | $\mu$F |

parameters are summarized in Table I. A full description of the test setup can be found in [4].

In order to simulate the effect of random turn-OFF delays, the turn-OFF of each DS level is intentionally delayed as follows with respect to the beginning of the scan cycle: $t_1 = 1000$ ns, $t_2 = 162$ ns, and $t_3 = 572$ ns.

Fig. 5 shows the uncompensated voltage differences in $V_{\mathrm{CE}}$ for each IGBT in the DS, shown in gray, dark blue, and brown traces. The current $I_c$ is drawn in yellow. From this figure, a significant voltage difference of around 250 V across each DS clamp capacitor can be observed, shown in a vertical dash-dotted line. Notice that the voltage difference between levels remains constant after an IGBT turn-OFF event (i.e., zero current through the IGBTs, shown in pink). For this reason, the maximum voltage of the capacitors is measured by the gate unit at the end of switching event (i.e., zero current in the DS, see vertical dash-dotted line) and sent as an input to the algorithm.

Fig. 6 shows the compensated voltage differences in $V_{\mathrm{CE}}$ for each IGBT in the DS after two iterations of the delay compensation algorithm. Using (4) yields $\theta = [0\,\theta_{12}\,\theta_{13}]^T = [0\;838\;428]^T$ ns, and from (6), $t_1^* = -428$ ns. After two iterations of the delay compensation algorithm, the voltage difference across clamp capacitors is reduced to less than 25 V (see vertical dash-dotted line).

## V. CONCLUSION

A computationally inexpensive delay compensation algorithm for series-connected IGBTs equipped with clamp snubbers has been presented. The algorithm uses the offline device characterization to estimate the turn-OFF delays of the series-connected IGBTs in the DS, and performs a time-delay correction based on the measured voltage across the clamp capacitors. Experimental results show that the proposed algorithm compensates for the DS capacitor voltage differences in only two iterations, which makes it suitable for online delay compensation of series-connected IGBTs in VSC-HVdc applications.

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